Technical Description

The Equipment Under Test (EUT) is an AM/FM Bluetooth Radio. The Bluetooth portion is operating between 2402MHz and 2480MHz (79 channels with 1MHz channel spacing). The EUT is powered by 4.5VDC (3X1.5V “AA” batteries or 120VAC. When the EUT is switched ON in Bluetooth mode, the display with show “BT” and flashing. The corresponding device would be searched and connected the EUT before playing audio. After pairing, the “BT” will stay lit.

2.4GHz Bluetooth Module:
Antenna Type: Integral, Internal (PCB Trace)
Frequency Range: 2402MHz - 2480MHz, 1MHz channel spacing, 79 channels

Nominal field strength is 102.5dBµV/m @ 3m
Production Tolerance of field strength is +2 / - 4dB
Antenna gain is 0dBi

The functions of main ICs are mentioned below.

1. BlueTooth module IN2020 (IC3):
1) CW6633M acts as the 2.4GHz radio core of Bluetooth module
2) The 26MHz crystal provides system clock for CW6633M.

2. AM/FM Radio Portion:
1) IC1 (BK1086/88E) acts as digital AM/FM radio demodulator.
2) Z3 (32.768kHz) provides clock for the IC1.

3. MCU module:
1) IC2 (HIC168) acts as MCU core.
2) Z2 (32.768 kHz) acts as clock for the MCU core (IC2).

4. Power Management portion:
1) IC4 (LY7527) stabilize the MCU voltage is 3.0V
2) IC5(L7805) stabilize the amplifier voltage is 5.0V.

Note: The EUT is using non-adaptive frequency hopping as declared by applicant.

Bluetooth 3.0 Single Chip for A2DP/AVRCP Solution

General Description

The CONWISE CW6633M is a monolithic, single-chip, stand-alone baseband process with an integrated 2.4GHz transceiver including EDR to 3Mbits/s for Bluetooth v2.1+EDR and v3.0 applications. The CW6633M is also completely backward-compatible with Bluetooth 1.1/1.2/2.0 specification. It eliminates the need for external flash memories and active components into the device. Thus minimizing the footprint and system cost of implementing a Bluetooth system.

The CW6633M has been designed in CMOS RF technology, the most cost-performance effective silicon process today. This use of the advanced process enables the CW6633M to achieve the lowest cost total solution and maintain the possible lower current consumption in all modes of operation.

The CW6633M is the optimal solution for A2DP/AVRCP applications that requires the audio bitstream payload and remote control commands/ events via UART interface.

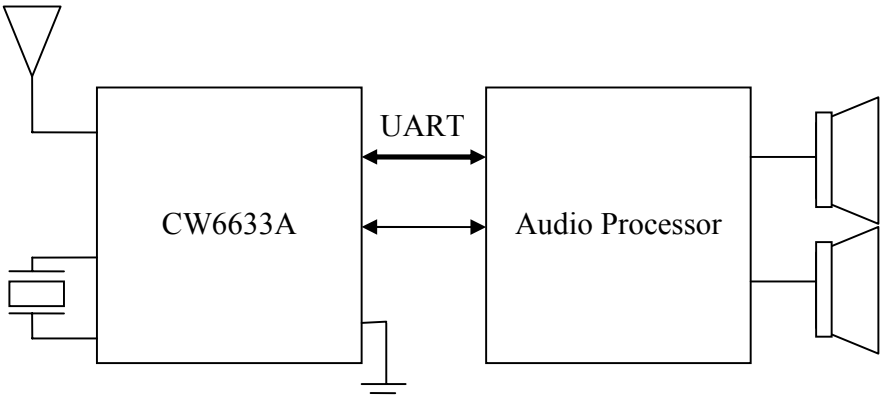
Features

- **Bluetooth specification version 3.0 compatible.**
- **Support ACL multi-slot packets for Data/Audio stream application.**
- **Support SCO/eSCO link with external PCM digital audio interface.**
- **Support high-speed UART baud rate of up to 3Mbps and USB2.0 full-speed compliant for HCI transport**
- **Support AFH for WiFi coexistence.**
- **Optimal 2-wire coexistence with WLAN.**
- **On-chip ROM eliminates dedicated flash memory chip, significantly lowering system BOM.**
- **Integrated 8-bit 8051 microprocessor core instead of ARM/MIPS such high cost processors.**
- **External Clock/Crystal 16, 26MHz system clocks are available to apply for system requirements.**
- **Optional external 32.768KHz crystal/clock for deep-low power mode using.**
- **Wide operation voltage: 2.2V~5.5V.**
- **Package types available**

  CW6633M: 48pin QFN package (6mm x 6mm)

Applications

- **Bluetooth speaker utilizing A2DP/AVRCP**
- **Audio system require audio source via Bluetooth from cellphone, PC**



1. Overview

The CW6633M is Bluetooth Core Specification version 3.0 compliant and designed for used for Bluetooth Audio application. The combination of the Radio Transceiver, BBC and the 8051-based microcontroller-BLM, BIM with on-chip ROM provide a complete lower layer Bluetooth protocol stock including the link controller (LC), link manger (LM), A2DP sink and AVRCP . The major features of CW6633M are listed in section 1.1 and the usage models- Bluetooth Audio is described in following section 1.2.

1.1. Features

Major features of the CW6633M include:

- Fully supports Bluetooth 3.0 features
- Adaptive Frequency Hopping (AFH)
- Scatter Mode
- QoS
- eSCO
- Fast Connect
- LMP improvements
- Synchronization
- Built-in regulators
- Built-in TR switch
- Maximum UART baud rates of 3 Mbps
- Support maximum Bluetooth data rates over UART interfaces
- HCI USB transport support with USB version 2.0 full-speed compliant interface
- High speed HCI UART transport support
- Channel quality driven data rate and package type selection
- Extended radio and production test mode features
- Full support for power saving modes
- Built-in LPO clock using external 32.768KHz crystal/clock

1.2. Bluetooth Audio Usage Model

The CW6633M is designed to provide direct interface to provide audio processor with audio bitstream transported via Bluetooth as show in figure 1. The CW6633M has very flexible PCM and UART interface enabling it to transparently connect with existing circuits. In addition, the low-cost crystal and external LPO (Low Power Oscillator) inputs allows to further minimizing the size, power and cost of the integration.
The CW6633M incorporates a number of unique features to accommodate the integration into audio playback platforms.

- The PCM interface provides multiple modes of operation to support both master and slave as well as interfacing to single external codec devices.
- The UART interface supports hardware flow control with tight integration to power control side band signalling to support the lowest power operation.

- The XTAL oscillation circuit provides a dedicated 26MHz to accommodate the typical reference frequency used by mobile phone.
- A programmable XTAL power-up or power-down signal allows the device to indicate when the clock supplied to the CW6633M may be disabled for added power saving during sleep mode.
- Both the XTAL and external LPO inputs are high impedance inputs that have minimal loading on the driving source.
- The highly linear design of the radio transceiver ensures that the device has the lowest output spurious emissions regardless of the stat of operation and has been fully characterized in the global cellular bands.
- The transceiver design has excellent blocking (eliminating desensitization of the Bluetooth receiver) and inter-modulation performance (distortion of the transmitted signal caused by the mixing of the cellular and Bluetooth transmissions) in the presence of a any cellular transmission (GSM, GPRS, CDMA, WCDMA or TD-SCDMA). Minimal external filtering is required for integration inside the handset.
- Minimal external components are required for integration and very compact packaging is available.

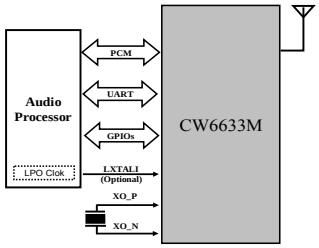


Figure 1 Bluetooth Audio Model

2. Pin Assignments

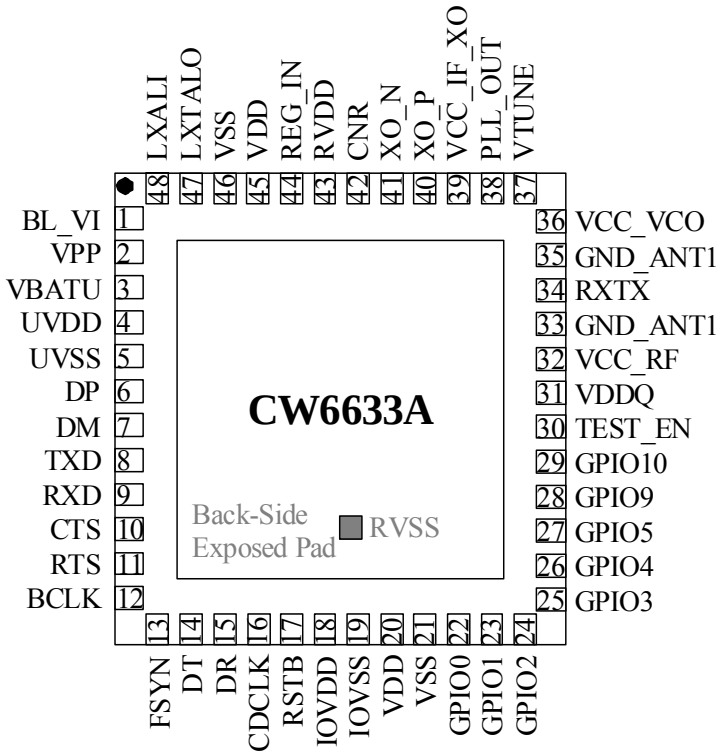


Figure 2 CW6633M 48-pin QFN6x6 Pin Diagram(Top-View)

Table 1: Pin Description

Pin Number	*Pin Name*	*I/O*	*Power Domain*	*Description*
Clock/Crystal Interface and Reset				
40	XO_P	I	RVDD	Crystal or frequency reference input
41	XO_N	O	RVDD	Crystal Oscillator output. Connect with XO_P if the reference clock is supplied

48	LXTALI	I	IOVDD	Low clock rate crystal driver input pin for *32.768KHz* crystal or external clock input. Connect to IOVSS if no low clock is applied.
47	LXTALO	O	IOVDD	Low clock rate crystal driver output pin for *32.768KHz* crystal driving. Leave unconnected if low clock is supplied.
17	RSTB	I	IOVDD	Active low system reset. This pin contains a weak pull-up.
Digital I/O and Core Power Supplies				
18	IOVDD	I	NA	Power supply for GPIOs.
19	IOGND	-	NA	Ground connection of GPIOs
44	REG_IN	I	NA	This pin serves as an input of the on-chip VDD and RVDD LDO regulators.
20, 45	VDD	-	NA	On-chip 1.8V LDO output for digital core, this pin output typical voltage is 1.8V.
21, 46	VSS	-	NA	Ground connection of on-chip 1.8 VDD LDO
2	VPP	-	VDD	Internal OTP ROM power supply. This pin should be left unconnected in field application.
RF Power Supplies				
43	RVDD	-	NA	On-chip 1.8V RVDD LDO output to supply internal RF circuits, this pin output typical voltage is 1.8V.
Exposed Pad	RVSS	-	NA	Ground connection of on-chip 1.8V RVDD LDO
31	VDDQ	I	RVDD	Digital block of RF circuit power supply. This pin must connect to RVDD.
32	VCC_RF	I	RVDD	RF circuit power supply. This pin must connect to RVDD.
36	VCC_VCO	I	RVDD	VCO circuit power supply. This pin must connect to RVDD.
39	VCC_IF_XO	I	RVDD	IF and internal Crystal Oscillator circuit power supply. This pin must connect to RVDD
42	CNR	O	RVDD	On-Chip RVDD LDO external decoupling capacitor pin.
USB Power Supplies				
3	VBATU	-	NA	This pin serves as an input of the on-chip UVDD LOD regulators. Connect to UVSS if the USB interface is not used.
4	UVDD	-	NA	On-chip 3.3V UVDD LDO output to supply USB transceiver.
5	UVSS	-	NA	Ground connection of on-chip 3.3V UVDD LDO
USB Interface				
6	DP	I/O	UVDD	USB data plus pin for the HCI USB interface. This pin should be connected to UVSS if USB is not used.
7	DM	I/O	UVDD	USB data minus pin for the HCI USB interface. This pin should be connected to UVSS if USB is not used.
UART Interface				
8	TXD	O	IOVDD	UART Serial data output port for the HCI UART interface. This pin should be left unconnected if UART is not used or can be configured to the GPIO Pin 14.
9	RXD	I	IOVDD	UART Serial data input port for the HCI UART interface. This pin should be left unconnected if UART is not used or can be configured to the GPIO Pin 15
10	CTS	I	IOVDD	UART Clear to Send-active low for HCI UART interface when the hardware flow control feature enable. This pin is used to set the system clock rate if the flow control feature is disabled.

11	RTS	O	IOVDD	UART Request to Send-active low for HCI UART interface when the hardware flow control feature enable. This pin is used to set the system clock rate if the flow control feature is disabled.
Audio PCM Interface				
12	BCLK	I/O	IOVDD	PCM serial data clock pin. In master mode, this is the clock output into the external HOST/CODEC. In clock slave mode, this is an input pin.
13	FSYN	O	IOVDD	PCM serial data synchronization pin. In master mode, this is an 8Khz sync signal to synchronize the input and output serial data streams.
14	DT	O	IOVDD	PCM serial data output pin. This data is clocked with BLCK, and first serial bit is synchronized by FSYN
15	DR	I	IOVDD	PCM serial data input pin. This data is clocked with BLCK, and first serial bit is synchronized by FSYN
16	CDCLK	O	IOVDD	External CODEC system clock. It can enable/disable to output the system clock to drive an external CODEC.
GPIO				
22, 23, 24, 25, 26, 27, 28, 29	GPIO0~GPIO 10	I/O	IOVDD	3.3V tolerant GPIO pin with programmable pull-up.
Radio				
33, 35	GND_ANT1	-	RVDD	Ground connection of RF I/O antenna. These pins must connect to RVSS.
34	RXTX	-	RVDD	RF I/O antenna pin.
37	VTUNE	I	RVDD	VCO tune input pin.
38	PLL_OUT	O	RVDD	Charge Pump output
Battery-Low Detector				
1	BL_VI	I	VDD	The input detection pin of Battery-Low Detector
Reserved Pins				
30	TEST_EN	I	IOVDD	The test mode enable pin. This pin should be left unconnected for field application.

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Table 2: Maximum Electrical Rating

Rating	*Minimum*	*Maximum*	*Unit*
Storage temperature	-40	+150	°C
Supply voltage of REG_IN	-0.4	5.5	V
Supply voltage of VBATU	-0.4	5.5	V
Supply voltage of UVDD	-0.4	4.0	V
Supply voltage of IOVDD	-0.4	4.0	V
Supply voltage of input/output Pin	IOVSS-0.4	IOVDD+0.4	V
Supply voltage of VDD	-0.4	3.0	V
Supply voltage of RVDD, VCC_RF, VCC_IF_VCO, VCC_XO	-0.4	3.0	V

3.2. Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Rating	*Minimum*	*Typical*	*Maximum*
Operation temperature	0 °C	+25°C	+70 °C
Supply voltage of REG_IN	2.2V	3.3V	5.5V
Supply voltage of VBATU	3.7V	5.0V	5.5V
Supply voltage of UVDD	2.8V	3.3V	3.6V
Supply voltage of IOVDD	1.7V	3.3V	3.6V
Supply voltage of VDD	1.7V	1.8V	2.0V
Supply voltage of RVDD, VCC_RF, VCC_IF_VCO, VCC_XO	1.7V	1.8V	2.0V

3.3. Clocks

Table 4: Signal Specification of XO_P/XO_N Pin

Crystal Oscillator	*Minimum*	*Typical*	*Maximum*
Crystal frequency	-	26MHz	-
Crystal load capacitance	8pF	10pF	12pF
Frequency tolerance			±20ppm
Digital trim range	0pF	-	3.1pF
Digital trim step	-	100fF	-
External clock of XO_P[1]	***Minimum***	***Typical***	***Maximum***
Input frequency	-	26MHz	-
Clock input level	0.8Vp-p	-	RVDD
XO_P input impedance	100KΩ	-	-
XO_P input impedance	-	-	4pF

1. Connect XO_N and XO_P together when use external reference clock instead of crystal.

Table 5: Signal Specification of LXTALI/LXTALO Pin

Crystal Oscillator	*Minimum*	*Typical*	*Maximum*

Crystal frequency	-	32.768KHz	-
Crystal load capacitance	-	20pF	-
Frequency tolerance			±200ppm
External clock of LXTALI[1]	***Minimum***	***Typical***	***Maximum***
Input frequency	-	32.768KHz	-
Clock input level	0.8 x VDD	-	-
LXTALI input impedance	100KΩ	-	-

1. Leave LXTALO unconnected when use external reference clock instead of crystal.

3.4. Linear Regulator

Table 6: UVDD LDO

UVDD Liner Regulator	***Minimum***	***Typical***	***Maximum***
Input voltage	3.7V	-	5.5V
Dropout voltage (I_{load}=70mA)	-	-	0.2V
Output voltage (I_{load}=70mA)	-	3.3V	-
Temperature coefficient	-	-	-
Output noise	-	-	-
Load regulation (I_{load}<70mA)	-	-	200mV/A
Maximum output current	-	-	70mA
Quiescent current	-	7uA	-

Table 7: VDD LDO

VDD Liner Regulator	***Minimum***	***Typical***	***Maximum***
Input voltage	2.2V	-	5.5V
Dropout voltage (I_{load}=70mA)	-	-	0.2V
Output voltage (I_{load}=70mA)	-	1.8V	-
Temperature coefficient	-	-	-
Output noise	-	-	-
Load regulation (I_{load}<70mA)	-	-	200mV/A
Maximum output current	-	-	70mA
Quiescent current	-	7uA	-

Table 8: RVDD LDO

RVDD Liner Regulator	***Minimum***	***Typical***	***Maximum***
Input voltage	2.2V	-	5.5V
Dropout voltage (I_{load}=70mA)	-	-	0.2V
Output voltage (I_{load}=70mA)	-	1.8V	-
Temperature coefficient	-	-	-
Output noise	-	-	-
Load regulation (I_{load}<70mA)	-	-	200mV/A
Maximum output current	-	-	80mA
Quiescent current	-	20uA	-

3.5. Power Consumption

Table 9 shows the current consumption for (IOVDD/REG_IN=2.8V, RVDD=1.8V, VDD=1.8V) (T_A=25°C) (XO_P=26MHz, LXTALI=GND) (UART HCI=921.6Kbps)

Table 9: Typical Current Consumption

Operational Mode	*Minimum*	*Typical*	*Maximum*
Page scan, time internal 1.28s	-	1mA	-
Inquiry	-	55mA	-
Page scan and Inquiry	-	1.6mA	-
ACL no traffic	-	26mA	-
ACL with file transfer	-	47mA	-
SCO HV3	-	52mA	-
Sleep	-	80uA	-

3.6. RF Specifications

Table 10: Receiver RF specifications

Parameter		*Minimum*	*Typical*[2]	*Maximum*
Receiver Selection				
Frequency range		2402MHz	-	2480MHz
Rx sensitivity[1]	GFSK, 0.1% BER	-88dBm	-86dBm	-84dBm
	π/4-DQPSK, 0.01% BER	-	-86dBm	-
	8-DPSK, 0.01% BER	-	-78dBm	-
Input IP3		-21dBm	-	-
Maximum input	GFSK, 0.1% BER	-	0dBm	-
	π/4-DQPSK, 0.1% BER	-	0dBm	-
	8-DPSK, 0.1% BER	-	-10dBm	-
Interference Performance				
C/I co-channel (GFSK, 0.1%BER)		11dB	10dB	-
C/I 1 MHz adjacent channel (GFSK, 0.1% BER)		-	-1dB	0dB
C/I 2 MHz adjacent channel (GFSK, 0.1% BER)		-	-36dB	-30dB
C/I >=3 MHz adjacent channel (GFSK, 0.1% BER)		-	-43dB	-40dB
C/I Image channel (GFSK, 0.1% BER)		-	-15dB	-9dB
C/I co-channel (π/4-DQPSK, 0.1% BER)		-	12dB	13dB
C/I 1 MHz adjacent channel (π/4-DQPSK, 0.1% BER)		-	-7dB	0dB
C/I 2 MHz adjacent channel (π/4-DQPSK, 0.1% BER)		-	-32dB	-30dB
C/I >=3 MHz adjacent channel (π/4-DQPSK, 0.1% BER)		-	-43dB	-40dB
C/I Image channel (π/4-DQPSK, 0.1%BER)		-	-19dB	-7dB
C/I co-channel (8-DPSK, 0.1%BER)		-	20dB	21dB
C/I 1 MHz adjacent channel (8-DPSK, 0.1% BER)		-	0dB	5dB
C/I 2 MHz adjacent channel (8-DPSK, 0.1% BER)		-	-27dB	-25dB
C/I >=3 MHz adjacent channel (8-DPSK, 0.1% BER)		-	-35dB	-33dB
C/I Image channel (8-DPSK, 0.1%BER)		-	-13dB	0dB
Intermodulation Performance				
Frequency range +3MHz~+6MHz offset (0.1% BER)		-39dBm	-	-
Out-of-Band Blocking Performance (CW)				

30 MHz - 2000 MHz, 0.1% BER	-10dBm	-3dBm	-
2000 MHz – 2399 MHz, 01% BER	-27dBm	-13dBm	-
2498 MHz – 3000 MHz, 0.1% BER	-27dBm	-14dBm	-
3000 MHz – 12.75GMz, 0.1% BER	-10dBm	-6dBm	-
Spurious Emissions			
30 MHz – 1 GHz	-	-	-
1 GHz -12.75 GHz	-	-	-

1. The receiver sensitivity is measured on the device interface.
2. Typical operating conditions are RVDD=1.8V operation voltage and 25°C ambient temperature.
3. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 3.0 specification.

Table 11: Transmitter RF specifications

Parameter	*Minimum*	*Typical*[1]	*Maximum*
Transmitter Selection			
Frequency range	2402MHz	-	2480MHz
Output power	-3dBm	+1dBm	+4dBm
Output power level control	2dB	4dB	8dB
20dB bandwidth output spectrum	-	780KHz	1000KHz
Frequency drift			
DH1 packet	-	13KHz	±25KHz
DH3 packet	-	15KHz	±40KHz
DH5 packet	-	15KHz	±40KHz
Modulation Index	0.28	0.32	0.35
Out-Band Spurious Emission			
30 MHz – 1 GHz idle mode	-	-	-57dBm
1 GHz -12.75 GHz idle mode	-	-	-47dBm
1.8 GHz - 1.9 GHz	-	-	-57dBm
5.15 GHz -5.3 GHz	-	-	-47dBm

1. Typical operating conditions are RVDD=1.8V operation voltage and 25°C ambient temperature.
2. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 3.0 specification.
3. the RF characteristics are measured at the chip interface.

4. Application Circuits

4.1. Usage Model through UART

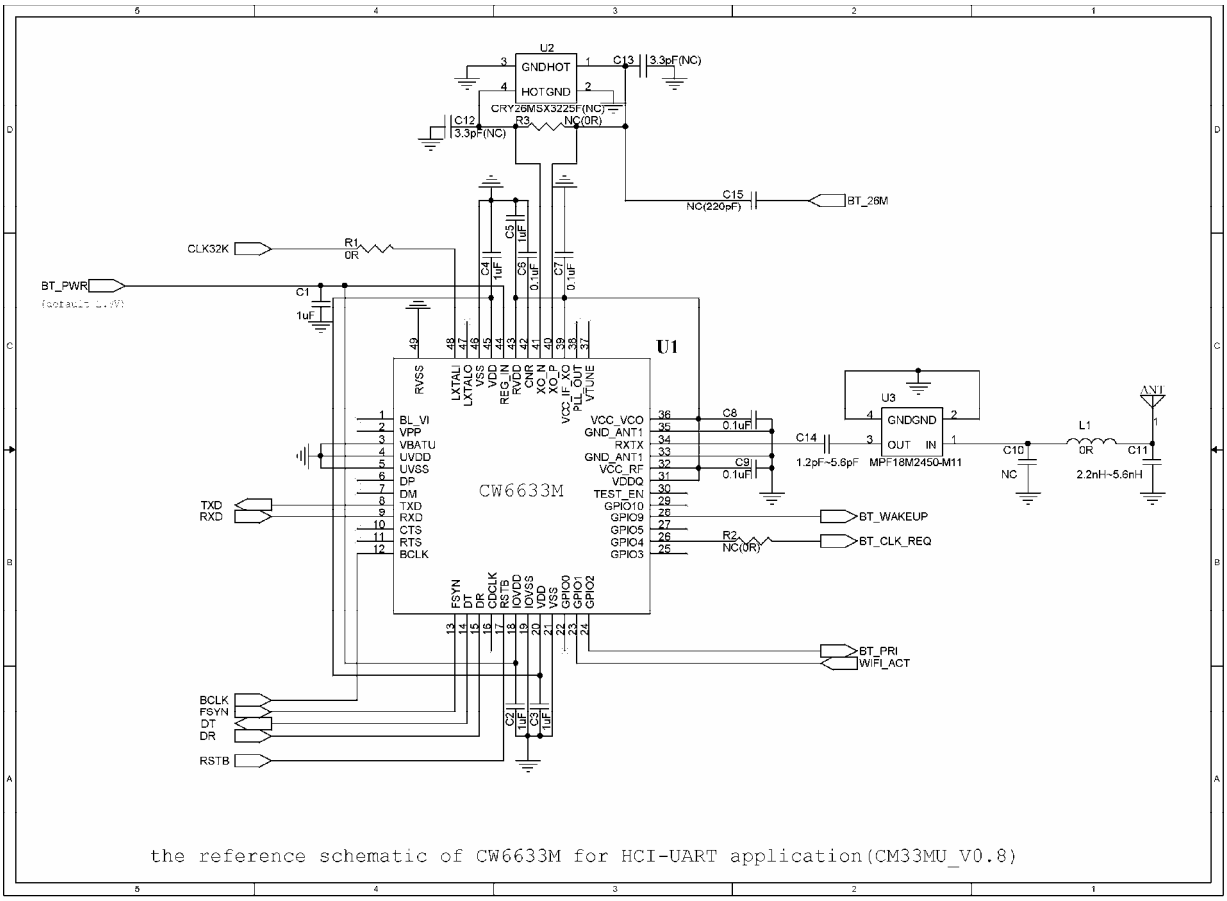
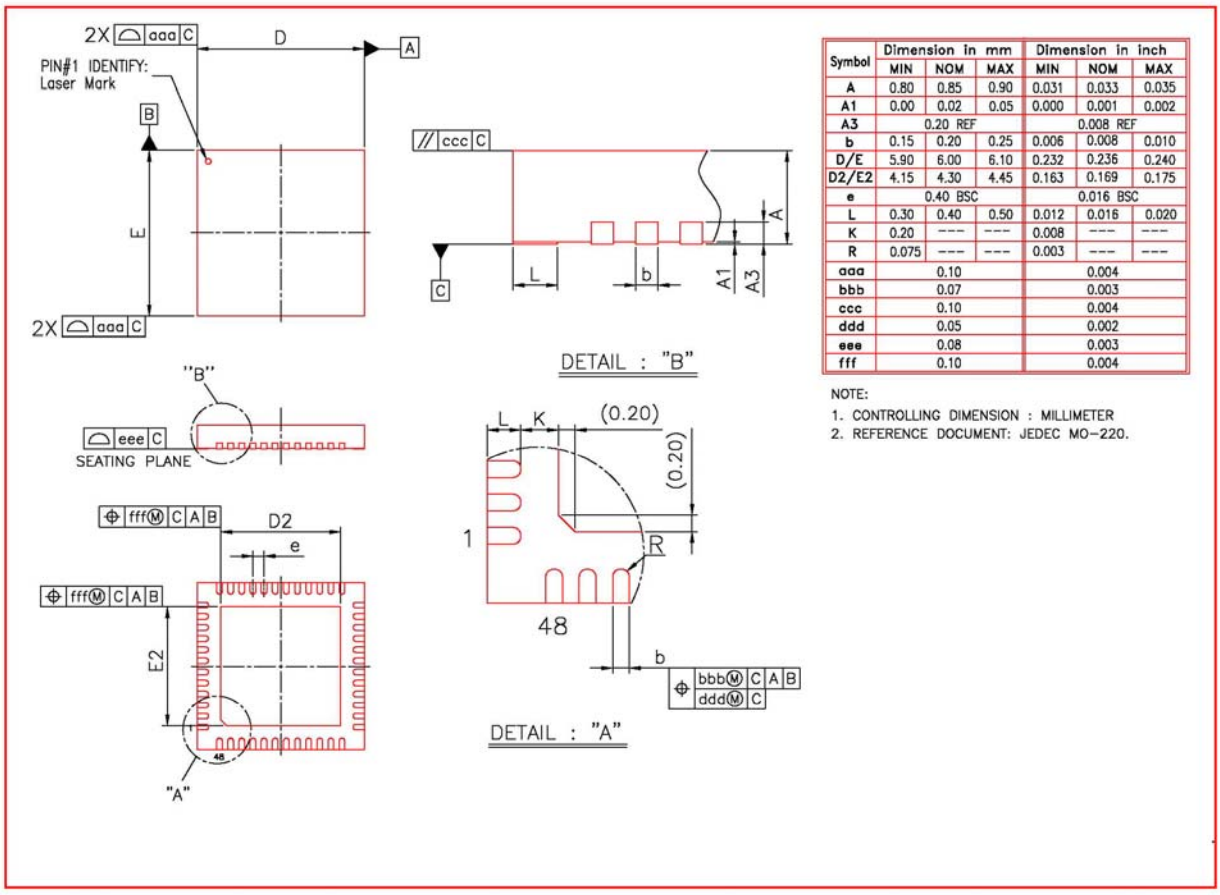


Figure 3 The Application Circuit for Usage Model-UART

5. Mechanical Information

5.1. QFN6x6 48-pin Package Information



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
D2/E2	4.15	4.30	4.45	0.163	0.169	0.175
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 4 CW6633M 48-pin, 6 x 6 x 0.85mm, 0.4mm-pitch QFN Package Dimension

Figure 5 CW6633M Product Marking

6. Ordering Information

Package			Order Number
Type	**Size**	Shipment Method	
48-Pin QFN (Pb free)	**6 x 6 x 0.85mm**	Tape&Reel	CW6633M

Minimum Order Quantity

Tape & Reel: 3Kpcs/reel

Contact Information

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