1 Introduction

This document specifies the tests and assessments that are required on the Telran TDK and it's component parts that will allow regulatory approval in Canada, US and EU.

This will allow:-

Regulatory bodies to assess if the test and assessment regime as satisfactory to allow regulatory approval before testing.

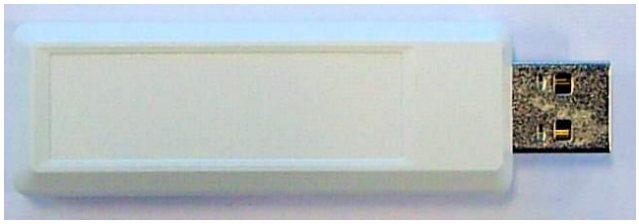
3rd Part test laboratories to provide competitive costs for the testing involved.

Toumaz to provide sufficient number and quality of test samples for the testing.

2 Product Overview

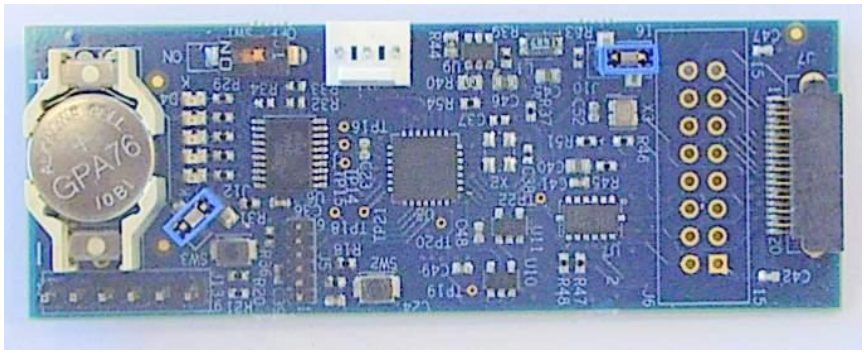
The products that require approval are:-

A USB Dongle.



A Radio Transceiver Module.

A Sensor Development Board.



A TDK (consisting of the USB Dongle and both boards).

The TDK is intended for use within an electronic engineering R&D environment. Usual laboratory ESD precautions are expected.

The RF Module is designed to be used and sold as a component of customer designed larger systems to provide low power wireless communications. It is not intended to be used as stand-alone equipment.

The Sensor Development Board is designed as a development aid for engineers. It is expected to be used and sold solely for this reason and not as stand-alone equipment.

The USB Dongle is designed for use with other Toumaz systems as well as the Telran TDK.

There are 2 versions of these products, one for the North American market and one for the European Market.

Description	Europe	North America
TDK consisting of:-	TZ1053TDK868 (Marketing)	TZ1053TDK915 (Marketing)
USB Dongle	TZ207020-ASY	TZ207021-ASY
RF Module	TZ1053RFM868 (Marketing) TZ207010-PCBA (Engineering)	TZ1053RFM915 (Marketing) TZ207011-PCBA (Engineering)
Sensor Development Board	TZ207030-PCBA	

3 Product Description

3.1 USB Dongle – TZ20702x

The USB Dongle consists of a PIC micro processor, a RF transceiver, a FTDI USB transceiver and SPI RAM on a single PCB housed in a New Age Enclosure, P1A-260906U housing. This is shown in Figure 1.

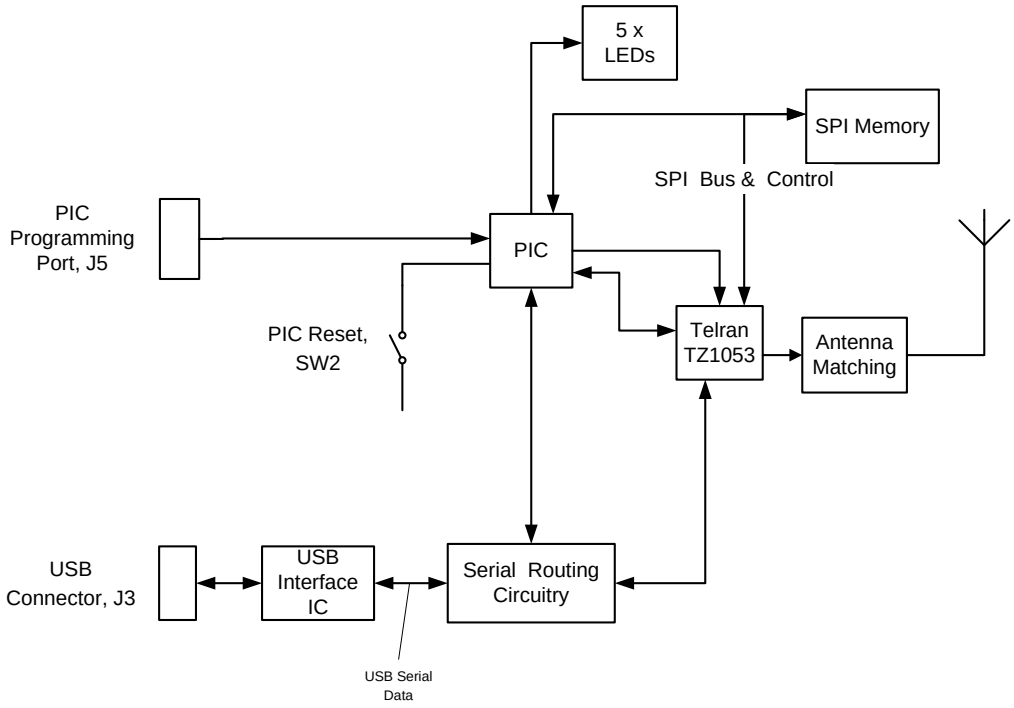


Figure 1 USB Dongle Functional Block Diagram

3.1.1 Digital

A PIC 18LF25K22 microcontroller acts as a local host controller. It has an ISP connector to allow the PIC to be programmed. The PIC uses its internal 16 MHz oscillator.

Two PIC USART connections are used to allow either the Telran, TZ1053 to communications directly with a PC via a USB interface, or the Telran to communicate via the PIC with a PC. NC7SZ157 gates are used to switch the data paths. A 256K SPI Bus Low-Power Serial SRAM (23A256) is used to allow greater storage and manipulation of data. The USB interface uses a FTDI FT232RQ. The USB port is protected by a TPD4E001 ESD diode array.

LEDs show the states of the Telran status pins. These are for R&D use only and are not visible to the end user.

3.1.2 Radio

The radio circuit is the same as the RF Module described in § 0. However the PCB layout is different.

3.1.3 Power

Power is derived from the USB bus and regulated down to 3.3V by the FTDI IC for the PIC and further to 1.25 V by a MAX8863 LDO.

3.1.4 USB Dongle information

Item	Value	Comments
Power supply sources	USB	5.0 V nominal (4.4 V to 5.25 V.)
Dimensions	65 x 23 x 15	mm (w x h x d) including USB Connector
Temperature Range	0 to + 70	°C
Connection Ports	USB A	

3.2 Radio Transceiver Module – TZ20701x

The RTM consists of a single bare PCB with a Telran RF transceiver IC and integrated antenna.

The North American version is houses the active RF circuits under a screening can.

The unit is powered by a LR44 Alkaline cell, but an external power source can be used on the EU version.

3.2.1 RF Module Summary

Item	Value	Comments
Power supply sources	Alkaline Cell	LR44 nominal 1.5 V
Operational Supply Range	1.08 to 1.50V	
Dimensions	43 x 23 x 7	mm (w x h x d) without battery holder.
	43 x 23 x 14	mm (w x h x d) with battery holder.
Temperature Range	0 to + 70	°C
Connection Ports		
Digital Interface	20 Way	2 x 10 0.05” Samtec
RF Test	U-FL	Hirose

3.2.2 Operational Frequencies

The transceiver is designed to operate in the 866 MHz SRD band in Europe and the 915 MHz ISM band in the USA. Details of the frequency ranges are in Table 1.

Table 1 Frequency Bands

Frequency Bands	From	To
Europe	863	870.0
US	902	928

3.2.3 Transceiver Description

The radio is operates in a TDMA (Time Division Multiple Access) system using the same uplink and downlink frequency.

The full RF system is contained in the Toumaz Telran TZ1053 IC along with a few additional components. The transceiver system consists of a separate Single Super-heterodyne transmit and receive chains with a common Local Oscillator System. The channel spacing is 200 kHz. This is shown in Figure 2 and described in greater detail in the following sections.

3.2.4 Transmitter

The transmit section of the Telran transceiver comprises I Q modulation from baseband up to an IF of approximately 100 MHz followed by a final up conversion by 800 MHz to a final transmit frequency of around 900 MHz. The PA stage is designed to deliver up to -3dBm into a matched antenna load. The PA output stage is open drain and requires an external inductor as a load and a series capacitor match to a 50ohm SAW filter. The transceiver uses an on-chip switch to connect to a common SAW filter and antenna path. The PA circuitry incorporates a control loop which holds

the output power at the correct level. Control of the PA output power is in approximately 1.5dB steps.

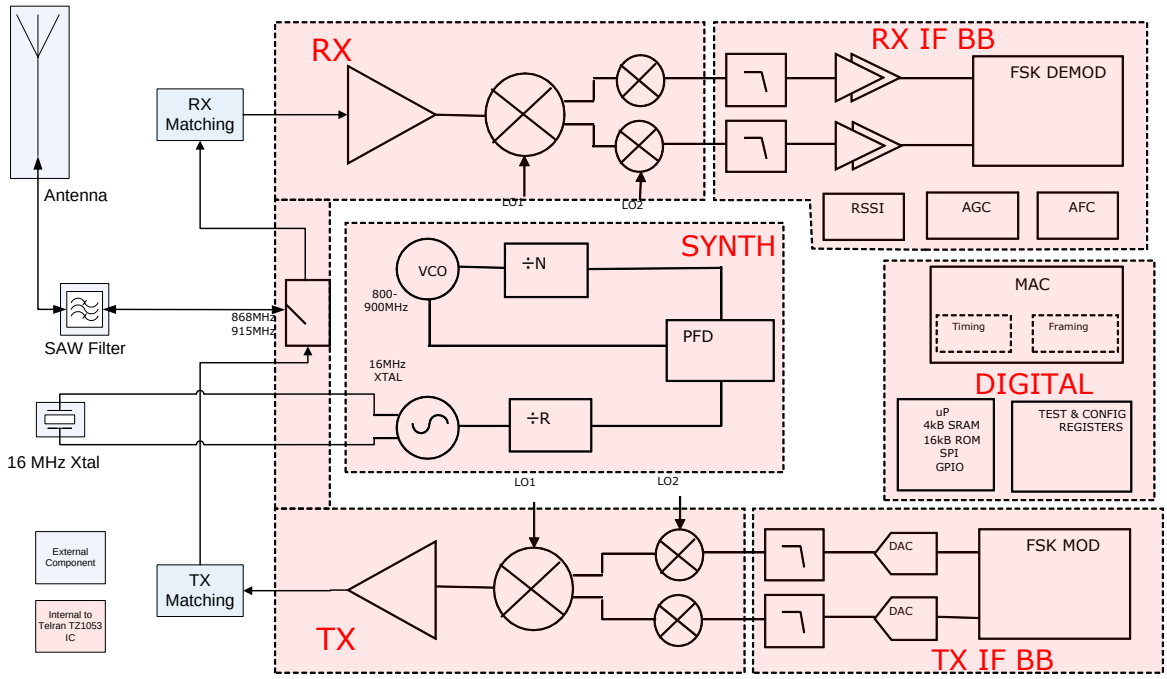


Figure 2 Transceiver Block Diagram

3.2.5 Receiver

The antenna pin of the transceiver interfaces to an on-chip symmetrical antenna switch, which is used to route either receive signals to the LNA or transmit power to the antenna. The receiver uses a sliding IF topology which provides advantages in filtering and noise profiling compared to a traditional direct conversion design. Using 900MHz as an example frequency, the first LO would be set to 800MHz resulting in a first IF of 100MHz. The second mixer is quadrature and is driven by LO2, which is one eighth of the frequency of LO1, thus producing a final IF of zero.

Overall gain of the receiver is over 100dB with an input sensitivity better than -97dBm. The baseband section contains the channel filter and limiting strip which drives the demodulator to extract the FSK/GFSK data at 50kbps. An AFC block locks the receiver's local clock to that of the basestation to within 10ppm approximately. The received signal strength indicator block allows the device to identify an empty channel.

Discrimination between positive data and negative data frequencies in the digital limiter IQ outputs is performed in the demodulator using a pulse generator circuit, majority decision circuit and data retiming DLL. An automatic frequency correction (AFC) circuit is also added to correct the local VCXO to match that of the transmitter, which is achieved within the first 10 symbols of preamble added to the data header. In doing so the DLL can sustain data lock for bursts of up to 1 second or longer by using a MAC override facility. The demodulator and AFC are controlled by timing signals from the FSB block in the MAC.

3.2.6 Synthesiser

The synthesiser is an integer-N PLL architecture as shown in comprising VCO, feedback divider, and phase-frequency detector (PFD) charge-pump with a comparison frequency at 177kHz, capable of providing 200kHz channel spacing.

The PLL can operate a fast-lock mechanism by initial condition setting of the loop filter voltage and dynamic charge-pump current during initial frequency lock. This reduction in lock time improves net power consumption. Also a lock-detect feature is provided which is sent to a configuration register. The VCO uses an internal inductor and a bank of on-chip capacitors to resonate at frequencies from 750MHz to 825MHz to cover the RF bands. The internal local oscillator clocks are derived from the VCO.

The VCO charge-pump output is fed via 2nd order low-pass loop to the variable capacitor. The VCO loop bandwidth is approximately 10 kHz.

3.2.7 Voltage Controlled Crystal Oscillator (VXO)

A crystal provides the 16.000 MHz reference for the frequency synthesiser system. In receive the crystal oscillator is tuned by the AFC loop to match the transmitter's frequency. The VCXO is the source of all demodulator and modulator clocks in the IF baseband sections.

3.2.8 Media Access Controller (MAC) Structure

The MAC block contains the protocol to send and receive data packets through the communications link in the radio section. It controls the RF channel selection and the listen before talk (LBT) compliance for EN300 220 as a class 3 device; link establishment, data transfer and sleep management. The MAC protocol follows a frame structure that comprises a preamble, sync word/start flag, error coded data words and a cycle redundancy check (CRC) word. Data is Hamming coded and also CRC checked to ensure that the system will detect and correct single and multiple (through re-transmission) errors. The control bits (preamble and Start Flag/Sync Word) are not error coded.

The frame format allows the payload size to be programmable in order to provide for the lowest power necessary for delivery of the data in a given application. The first field in the frame is a preamble word between 36 to 96 bits. The SYNC WORD / START FLAG is a 16 bit word which signifies the end of PREAMBLE and START of DATA. The message field has 16 bits wide hamming coded MAC WORDS followed by the CRC word of encoded data. Data bits are whitened before coding using a programmable MASK WORD. This provides a basic level of data encryption to the user.

A programming configuration register (CFR) with read/write registers enables the various modules to be set in their correct modes of operation. A custom implementation will need additional logic to interface to the CFRs.

3.2.9 Microprocessor and SPI

The microprocessor section contains the 8051 eWarp processor, peripherals and memories. The eWarp architecture is a state of the art 8051 microcontroller, clocking at up to 16MHz and provides an industry compatible instruction set. The microprocessor is intended purely for TELRAN configuration and not for customer use.

Key features are:

- 4kbyte on-chip RAM for data storage; a maximum of 3kbyte allocated as code RAM
- 24kbyte ROM
- SPI compatible serial interface for external serial memory or further peripherals
- UART interface with IRDA functionality

- 5 programmable General Purpose Input Output (GPIO) Ports
- Flexible clock-generation and power management unit for power saving
- Low power consumption

The internal 8051 is not generally intended for customer use as all of the operating modes are already defined in the ROM.

3.2.10 Power Supplies

The TZ1053 IC is designed to operate using an unregulated single alkaline cell.

On chip regulation is used for the VCO & PA.

3.2.11 Transceiver Parameter Summary

Table 2 Summary of Transceiver Characteristics

Parameter	EU	US / Can	Units	Comments
Clock Frequency	16.0		MHz	
Highest LO Frequency	773	822	MHz	8 / 9 of transmit frequency
Transmit Frequency	866	925	MHz	nominal
Transmit Power	-12		dBm	Maximum
Power Class (EU)	7a	n/a		5 mW max.
Channel Spacing	200		kHz	
Modulation	FSK			
Deviation	± 50		kHz	
Data rate	50		kbits/s	
Occupied Bandwidth	160		kHz	
Operating Modes	TX			As part of a TDMA system
	RX			As part of a TDMA system
	Idle			
Receive Sensitivity	-97		dBm	Typical for 80% MAR
SRD Class	2	n/a		Typical uses are Domestic Telemetry and Building Management Systems.
LBT	yes	n/a		When used as Base station

3.3 Sensor Development Board – TZ207030

The Sensor Development Board connects to the Radio Module to allow development of sensor applications. A block diagram of the SDB is shown in Figure 3.

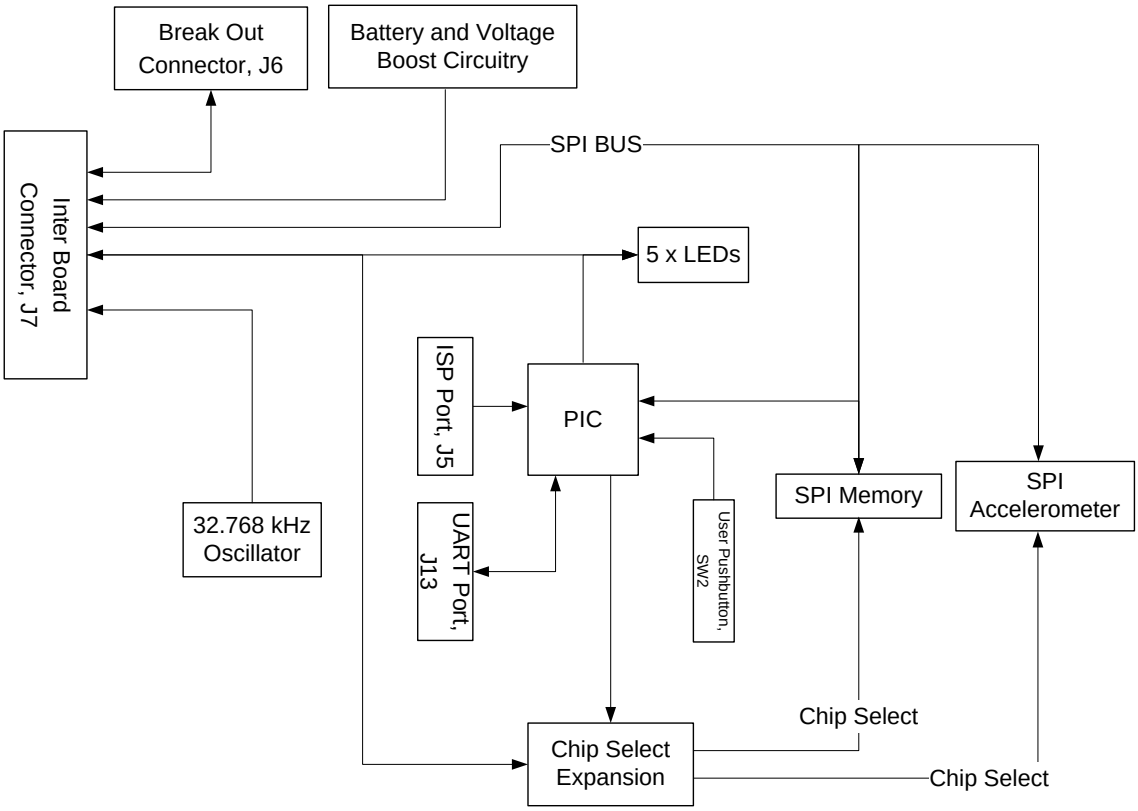


Figure 3 Telran TDK SDB Block Diagram

The Sensor Development Board has an interface connector that permits connection to an RFM. In addition to this connector will be an IDC header set out as close as possible to reflect a UMI metering connector.

3.3.1 Digital

A PIC 18LF25K22 microcontroller acts as a host controller together with a USART connector to allow communications with other devices, e.g. PCs. The PIC has an ISP connector to allow the PIC to be programmed.

LEDs show the states of the PIC & RF Module status pins.

3.3.2 Power

The board can be powered by either an on-board LR44 battery or by an external supply. This power is connected to the interface connector to power a RF module.

A MCP1640B Synchronous Boost Regulator provides a 2.5 V supply for the PIC and accelerometer.

3.3.3 Sensor

A LIS35DE 3 axis accelerometer transfers data to the PIC via the SPI bus.

A 32.768 kHz oscillator provides an accurate clock signal to the RF Module but is not used on the Sensor Development Board.

3.3.4 Sensor Development Board Summary

Item	Value	Comments
Power supply sources	Alkaline Cell	LR44 nominal 1.5 V
Operational Supply Range	1.08 to 1.50V	
Dimensions	75 x 27 x 16	mm (w x h x d)
Temperature Range	0 to + 70	°C
Digital Interface	20 Way	2 x 10 0.05” Samtec