Operational Description

Section 2. 1.033(b)(4) of the 47 CFR states:

“A brief description of the circuit functions of the device along with a statement describing how the device operates. This statement should contain a description of the ground system and antenna, if any, used with the device.”

Wireless Data Acquisition System

This data acquisition system consists of wireless data collection devices placed at the source of the data, usually within the equipment being monitored. The wireless devices join a IEEE Std. 802.15.4 based ZigBee mesh network which transfers data to a concentrator node, the network coordinator. Here the data is transferred over an USB interface to a local High Reliability Mini-Server (HMS).

GA-100-RC Operation Description

Data Acquisition Hardware with Radio Controller - The GA-100-RC block diagram shows the main functions of this printed circuit board (PCB).

Power Supply Regulator

The power conditioning circuit is a synchronous step-down switching regulator with protection and filtering. The regulator will accept input voltage from 5 to 24 VDC and provides 3.3 Volt DC regulated power to the acquisition PCB and the radio transceiver module.

Microcontroller Unit (MCU) and Peripherals

The MCU has built-in flash program memory, EEROM, timing functions, and programmable I/O which may be configured for discrete I/O, serial ports, and a JTAG programming port.

One of the serial ports may be configured as a USART to interface with either an on board USB / USART converter or a RS-232 signal voltage translator.

The MCU interfaces to the radio module, RF24A1, with another serial port configured as a SPI (Serial Peripheral Interface). This interface is managed by the Atmel ZigBee protocol stack firmware code.

Another serial port is configured as a SPI (Serial Peripheral Interface) interfaced with an external serial flash memory. This flash memory and the MCU built-in flash and EEROM memory may be used for data storage, configuration information and firmware (program) updates. Networking parameters such as the IEEE / MAC address are saved in the MCU EEROM and/or Flash.

Initial programming of the MCU is through a header on the PCB using the JTAG serial port of the MCU.

A 32.768 kHz crystal is used with a low power oscillator circuit on the MCU. This oscillator provides an accurate reference for on chip timers and oscillators.

Functional Description and Models using the GA-100-RC

Currently there are three models based on the GA-100-RC PCB with the RF24A1 radio module. These are:

1) GA-100-ASSY

   This model/assembly is used as a node in a mesh network. Event data is acquired through the various discrete and serial interfaces which is processed, tagged and sent to the network coordinator. These network nodes may also function as a network router to extend and maintain the range and capacity of the network.

2) GA-100-CASSY

   This coordinator model/assembly is interfaced to a mini-server computing device via a USB (Universal Serial Bus) interface. The coordinator is responsible for starting and maintaining the mesh network. Data and status information received from the network nodes are passed to the server data base. The server/coordinator may also send commands and information to the nodes for various purposes.

3) GA-REPEATER

   The repeater model is used as a network router. When used, the repeater is physically located to aid extending the range of the network and/or reliability of communication with other network nodes.

RF Module Circuit Description (RF24A1)

This RF module is part of equipment to wirelessly collect and remotely present real time operational informational information to owners, managers and service personnel.

The RF24A1 Module is base on an Atmel Corporation reference design, “RadioExtender231ED”, with minor non-RF changes (see schematic and block diagram). The reference design module has received FCC Part 15 Limited Module Approval (FCC ID: VNR-E31ED-X5B-00).

The RF24A1 uses an Atmel RF transceiver integrated circuit (IC) compliant to IEEE 802.15.4 communication standard and operates in the 2.4 GHz unlicensed band. The module transceiver is interfaced to an Atmel microcontroller and the microcontroller will execute the application

firmware along with the Atmel ZigBee protocol stack for 802.15.4 or other 802.15.4 based protocol(s).

Power Supply

The AT86RF231 transceiver has a band gap voltage reference and separate 1.8 volt regulators for the analog and digital logic circuits. The module also has a split ground plane, separating the digital I/O grounds from the RF grounds. These ground planes are connected centrally in one place. The power input circuit has over current and over voltage protection and RF filtering.

Frequency Control and Modulation

A 16 MHz crystal supplies the reference frequency for the on-chip Phase Locked Loop (PLL) Frequency Synthesizer that generates the RX / TX frequencies for all 16 IEEE 802.15.4 2.4 GHz channels. Fast PLL settling time supports frequency hopping operation.

The IEEE 802.15.4 is a packet data digital standard communication protocol. The modulation used for the 2.4 GHz band is Offset Quad Phase Shift Keying (O-QPSK). The Bit / Data rate is 250 kb/s, and the chipping rate is 2 k chips/s.

RF Output and Antennas

The AT86RF231 supports antenna diversity. The RF24A1 module implements dual diversity antennas (ANT0/ANT1). A digital control pin (DIG1) is used to control the external RF switch selecting one of the two antennas.

Two ceramic chip antennas, ANT0 and ANT1, are connected via an RF switch (SW1) to a balun (B1). Balun (B1) transforms the single-ended antenna port impedance of 50 ohms to the 100 ohm differential (balanced) RF port impedance at pins RFP / RFN. The RF switch enables selecting one of the two antennas located at the corners of the printed circuit board.

Conducted power output from the transceiver chip (per data sheet) is ≤ 6 dBm or 3.98 mW. Peak gain of a chip antenna is 3.0 dBi and thus the maximum radiated power ≤ 7.94 mW.

Module Interface

The module is physically connected to its controller through a 15 pin x 2 row header/connector. The data interchange is via a Serial Peripheral Interface (SPI) port which accesses the transceivers registers, frame buffer, and SRAM memory.