Fibocom
PERFECT WIRELESS EXPERIENCE

LC116-LA

Hardware Guide

V1.1

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Applicability Type

No.	Applicability Type	Description
1	LC116-LA	MCP is 2Gbit Flash+2Gbit RAM, and supports MAIN_ANT and DIV_ANT.

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Change History

V1.0 (2021-11-10)	Initial version
V1.1 (2021-12-16)	Updated the known issues.

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1 Overview

1.1 Product Introduction

The LC116-LA module is a broadband wireless terminal product based on Qualcomm 9X07 platform, applicable to multiple network systems and bands such as TDD-LTE, FDD-LTE, WCDMA and GSM. The following table lists the sub-models of the LC116-LA product.

Table 1. Sub-models of the LC116-LA product

No.	Applicability Type	Description
1	LC116-LA-00-90	MCP is 2Gbit Flash+2Gbit RAM, and supports MAIN_ANT and DIV_ANT.
2	LC116-LA-00-91	MCP is 2Gbit Flash+2Gbit RAM, and supports MAIN_ANT and DIV_ANT.
3	LC116-LA-10-90	MCP is 2Gbit Flash+2Gbit RAM, and supports MAIN_ANT.
4	LC116-LA-10-91	MCP is 2Gbit Flash+2Gbit RAM, and supports MAIN_ANT and DIV_ANT.

The following figure shows the appearance of the LC116-LA product.

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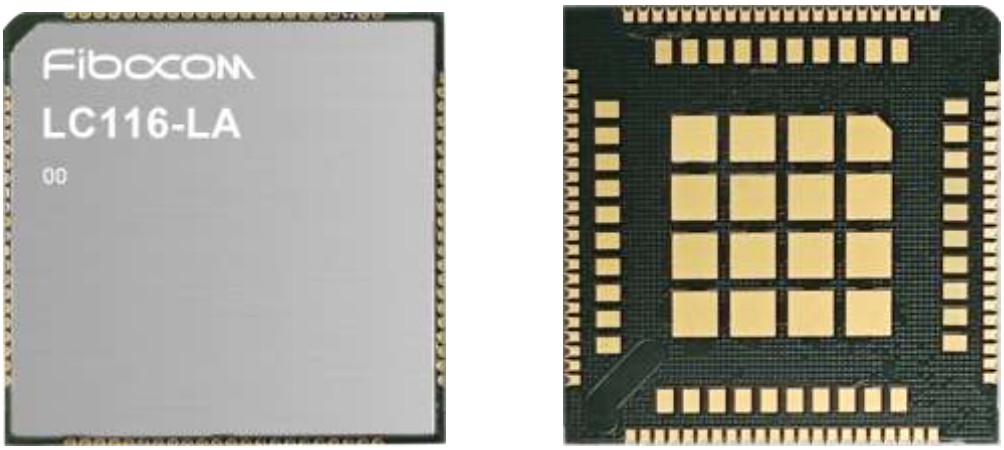

Figure 1. Product appearance

1.2 Characteristics

The product hardware has the following characteristics.

Table 2. Basic configuration

Indicator		Description
Basic Configuration	Processor	MDM9X07
	Memory	2Gbit Flash+2Gbit RAM
	Supported Operating System	LINUX

Table 3. Baseband characteristics

Category	Description
Function interface	USB × 1, support USB2.0 I^2C × 1 UART × 2 GPIOs
Peripheral interface	USIM × 1, support single card single standby mode LCD × 1 SGMII × 1

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	PCM × 1 SD × 1 ADC × 3

Table 4. RF characteristics

Category	Description
Antenna interface	Main antenna × 1 Diversity antenna × 1

1.3 System architecture

The LC116-LA product hardware consists of the following parts:

- Baseband part: PMIC, MCP, USB, (U)SIM, PCM, I^2C, UART, SGMII, SDIO, GPIOs, GSM/CDMA/EVDO/WCDMA/TD-SCDMA/LTE TDD/LTE FDD controller
- RF part: RF Transceiver, RF PA, RF filter Antenna

The following figure shows the internal structural block diagram.

1.4 Operating Mode

The module supports the following operating modes.

Table 5. Operating mode

Operating Mode	Description
Shutdown	When the VBAT pin of the module is not powered or the power voltage is lower than 3 V, the module is in a shutdown state.
Standby	The module is powered on, and it can be operated using the AT commands through the serial port. The module is registered with the network, there is no service processing in progress, and the module is ready for communication. This is the default operating mode after the

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Operating Mode	Description
	module is powered on.
Transmission	The module is powered on and successfully registered with the network for service transmission. The module can be operated using the AT commands through the serial port. The module transmits data. When data transmission is completed, the module returns to the standby or low-power mode.
Sleep	The module is in light sleep state. It is connected to a network and can receive paging messages. In this mode, the module can switch to the standby mode or PSM mode.
Flight	The wireless communication of the module is turned off.

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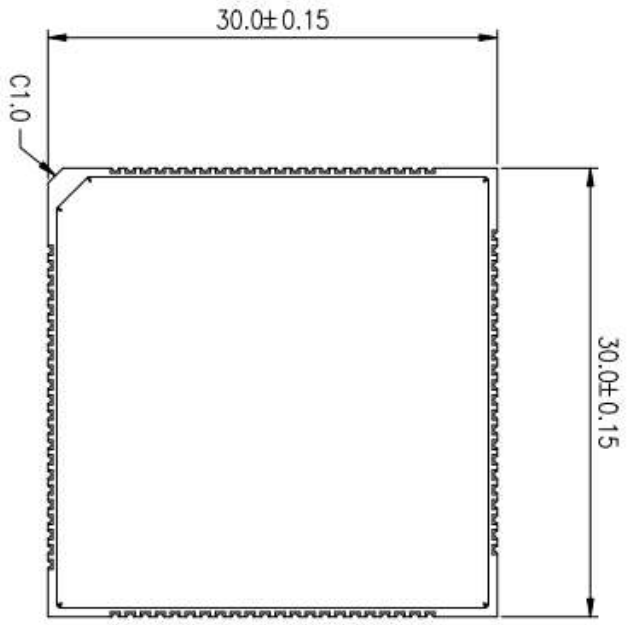
2 Technical Indicators

2.1 Physical Indicators

Table 6. LC116-LA package mode

Indicator	Description
Weight	5.2 g
Package	LCC+LGA 143 Pin
Appearance dimensions	(30.0±0.15) mm × (30.0±0.15) mm × (2.4±0.2) mm
Structural dimensions	See the figure below.

The following figure shows the structural dimensions.



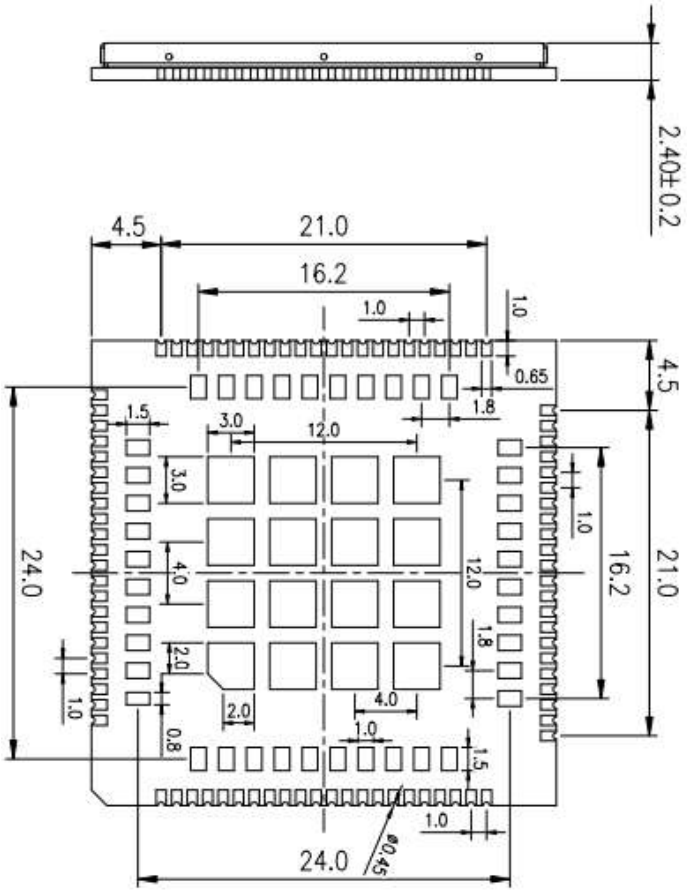


Figure 2. Structural dimensions

2.2 RF

Table 7. Operating bands

System	Band	Description	Tx (MHz)	Rx (MHz)
LTE FDD/WCDMA	Band 1	IMT 2100MHz	1920–1980	2110–2170
LTE FDD/WCDMA/GSM	Band 2	IMT 1900	1850–1910	1930–1990
LTE FDD/GSM	Band 3	DCS 1800MHz	1710–1785	1805–1880
LTE FDD	Band 4	IMT 2100	1710–1755	2110–2155
LTE FDD/WCDMA/GSM	Band 5	CLR 850MHz	824–849	869–894
LTE FDD	Band 7	IMT 2600	2500–2570	2620–2690
LTE FDD/WCDMA/GSM	Band 8	E-GSM 900MHz	880–915	925–960

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System	Band	Description	Tx (MHz)	Rx (MHz)
LTE FDD	Band 28	IMT 700	703–748	758-803
LTE TDD	Band 40	IMT 2300MHz	2300–2400	2300–2400

LC116-LA-10-90/91 does not support LTE.

Table 8. Tx power

System	Band	Tx Power (dBm)	Description
GSM	GSM850	32.5±1.5	- -
	GSM900	32.5±1.5	- -
	DCS1800	29.5±1.5	- -
	PCS1900	29.5±1.5	- -
WCDMA	Band1	23.5±1.5	- -
	Band2	23.5±1.5	- -
	Band5	23.5±1.5	- -
	Band8	23.5±1.5	- -
LTE FDD	Band1	23±2	10MHz Bandwidth, 1 RB
	Band2	23±2	10MHz Bandwidth, 1 RB
	Band3	23±2	10MHz Bandwidth, 1 RB
	Band4	23±2	10MHz Bandwidth, 1 RB
	Band5	23±2	10MHz Bandwidth, 1 RB
	Band7	23±2	10MHz Bandwidth, 1 RB
	Band8	23±2	10MHz Bandwidth, 1 RB

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System	Band	Tx Power (dBm)	Description
	Band28	23±2	10MHz Bandwidth, 1 RB
LTE TDD	Band 40	23±2	10MHz Bandwidth, 1 RB

Table 9. Sensitivity of each frequency band of the module

System	Band	Main Sensitivity (dBm)	Diversity Sensitivity (dBm)
GSM	GSM 850	-109	- -
	GSM 900	-109	- -
	DCS 1800	-108.5	- -
	PCS 1900	-108.5	- -
WCDMA	Band 1	-109	-109
	Band 2	-109.5	-109.5
	Band 5	-110	-110
	Band 8	-110	-110
LTE FDD	Band 1	-98	-98
	Band 2	-98	-98.5
	Band 3	-98	-98.5
	Band 4	-98	-98.5
	Band 5	-98	-99.5
	Band 7	-97.5	-98.5
	Band 8	-98.5	-99
	Band 28	-97.5	-99
LTE TDD	Band 40	-99	-98.5

Table 10. Main antenna indicator requirements

Indicator	Requirements

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Indicator	Requirements
Frequency range	The most suitable antenna must be used to adapt to the relevant frequency band.
Bandwidth (GSM/EDGE)	GSM850: 70 MHz GSM900: 80 MHz GSM1800 (DCS): 170 MHz GSM1900 (DCS): 140 MHz
Bandwidth (WCDMA)	WCDMA band 1 (2100): 250 MHz WCDMA band 2 (1900): 140 MHz WCDMA band 5 (800): 70 MHz WCDMA band 8 (900): 80 MHz
Bandwidth (LTE)	LTE band 1 (2100): 250 MHz LTE band 2 (1900): 140 MHz LTE Band 3 (1800): 170 MHz LTE Band 4 (2100): 440 MHz LTE Band 5 (850): 70 MHz LTE Band 7 (2600): 190 MHz LTE Band 8 (900): 80 MHz LTE Band 28 (700): 100 MHz LTE band 40 (2300): 100 MHz

2.3 GNSS Performance

Table 11. Power consumption of module

Parameter	Mode	Conditions	Average Current (mA)

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Parameter	Mode	Conditions	Average Current (mA)
I_{off}	Power-off	The module is powered on and then off.	0.02
I_{sleep}	GSM	MFRMS=5 (USB sleep)	3
	WCDMA	DRX=8 (USB sleep)	3
	LTE FDD	Paging cycle #64 frames (USB sleep)	4
		Paging cycle #128 frames (USB sleep)	3
		Paging cycle #256 frames (USB sleep)	3
	LTE TDD	Paging cycle #64 frames (USB sleep)	4
		Paging cycle #128 frames (USB sleep)	3
		Paging cycle #256 frames (USB sleep)	3
I_{idle}	GSM	MFRMS=5 (USB sleep)	20
	GSM	MFRMS=5 (USB wakeup)	30
	WCDMA	DRX=8 (USB sleep)	20
	WCDMA	DRX=8 (USB wakeup)	30
	LTE FDD	Paging cycle #64 frames (USB sleep)	20
	LTE FDD	Paging cycle #64 frames (USB wakeup)	30
	LTE TDD	Paging cycle #64 frames (USB sleep)	20
	LTE TDD	Paging cycle #64 frames (USB wakeup)	30
Radio off	- -	AT+CFUN=0,0 (USB sleep)	20
	- -	AT+CFUN=0,0 (USB wakeup)	30

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Parameter	Mode	Conditions	Average Current (mA)
$I_{GSM-RMS}$	GSM	GSM850 PCL5	260
		EGSM900 PCL5	260
		DCS1800 PCL0	200
		PCS1900 PCL0	200
$I_{GPRS-RMS}$ CS4	GPRS	GPRS Data transfer GSM850; PCL=5; 1Rx/4Tx	570
		GPRS Data transfer GSM900; PCL=5; 1Rx/4Tx	570
		GPRS Data transfer DCS1800; PCL=0; 1Rx/4Tx	430
		GPRS Data transfer PCS1900; PCL=0; 1Rx/4Tx	430
$I_{EGPRS-RMS}$ MCS9	EDGE	EDGE Data transfer GSM850; PCL=8; 1Rx/4Tx	460
		EDGE Data transfer GSM900; PCL=8; 1Rx/4Tx	470
		EDGE Data transfer DCS1800; PCL=2; 1Rx/4Tx	440
		EDGE Data transfer PCS1900; PCL=2; 1Rx/4Tx	440
$I_{WCDMA-RMS}$	WCDMA	WCDMA Data transfer Band I@+23.5dBm	650
		WCDMA Data transfer Band II@+23.5dBm	620
		WCDMA Data transfer Band V@+23.5dBm	550
		WCDMA Data transfer Band VIII@+23.5dBm	570
$I_{LTE-RMS}$	LTE FDD	LTE FDD Data transfer Band 1 @+23dBm	650
	LTE FDD	LTE FDD Data transfer Band 2 @+23dBm	650
	LTE FDD	LTE FDD Data transfer Band 3 @+23dBm	730
	LTE FDD	LTE FDD Data transfer Band 4 @+23dBm	700
	LTE FDD	LTE FDD Data transfer Band 5 @+23dBm	580
	LTE FDD	LTE FDD Data transfer Band 7 @+23dBm	750
	LTE FDD	LTE FDD Data transfer Band 8 @+23dBm	580

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Parameter	Mode	Conditions	Average Current (mA)
	LTE FDD	LTE FDD Data transfer Band 28 @+23dBm	680
	LTE FDD	LTE TDD Data transfer Band 40 @+23dBm	420

2.4 Electrical Indicators

The following figure shows the power voltage of the LC116-LA series modules as well as the maximum voltage range that the digital I/O interfaces can withstand.

Table 12. Limit voltage range of module interfaces

Interface	Description	Minimum Value (V)	Maximum Value (V)
VBAT	Power input	-0.3	4.7
USB_VBUS	USB insertion detection	-0.3	5.5
GPIO	Level power supply voltage of digital I/O	-0.3	2.0

The I/O interface level of the LC116-LA module is 1.8 V. When using the I/O interface, ensure that the level is matched. The following table describes the logic level range.

Table 13. Logical level range of the module

Parameter	Minimum Value (V)	Maximum Value (V)
V_{OH}	1.35	1.8
V_{OL}	0	0.45
V_{IH}	1.2	2.0V
V_{IL}	0.3	0.6

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2.5 Application Environment

Table 14. Environment indicators

Parameter	Minimum Value (℃)	Typical Value (℃)	Maximum Value (℃)
Operating temperature	-30	25	75
Extended temperature	-40	-	85
Storage temperature	-40	-	95

In the limited operating temperature range, some RF indexes may exceed the standard. It is suggested that the temperature control measures should be considered in the application end under the harsh environment. At the same time, it is suggested that the module application terminal should be stored at a certain temperature. Beyond this range, the module may not work properly or be damaged.

2.6 Reliability Indicators

To improve the reliability and stability of the product, the module has been tested for reliability as shown in the table below.

Table 15. Reliability test

Test Item	Test Condition
Low temperature storage test	Temperature -40℃±3℃, 24 hours in shutdown state
High temperature storage test	Temperature +85℃±3℃, 24 hours in shutdown state
Temperature shock test	In shutdown state, 0.5 hour at -40°C and +85°C ambient temperatures respectively, the temperature conversion time is less than 3 minutes, and the temperature conversion is repeated for 24 times.
High temperature and humidity test	Temperature at +85℃±3℃, humidity at 85% RH, lasting for 24 hours in shutdown state

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Test Item	Test Condition
Low temperature operating test	Temperature at -30℃±3℃, lasting for 24 hours in operating state
High-temperature operating test	Temperature at +75℃±3℃, lasting for 24 hours in operating state
Vibration test	Carry out vibration test according to the following requirements. Frequency: 5 Hz to 20 Hz; Random vibration ASD (acceleration spectral density): 0.96 m^2/s^3 Frequency: 20 Hz to 500 Hz; Random vibration ASD (acceleration spectral density): 0.96 m^2/s^3 (at 20 Hz). For other frequencies, the random vibration ASD is -3 dB/octave.
Connector lifespan test	30 times cable insertion and removal to the RF antenna interface

After the test items are tested, the module can be powered on, the function is normal, and the performance meets the standard.

2.7 ESD Indicators

The design of LC116-LA module needs to consider ESD protection. The module pins have limited anti-static ability, and the key input/output signal interfaces must be handled with ESD measures. Reasonable structural design and PCB layout design can ensure that the metal shield shell is completely grounded, so as to improve the anti-static capability of the equipment. The following table describes the ESD withstand voltage of module pins under the condition of temperature of 25℃ and humidity of 45%.

The ESD allowable discharge range of the module is as follows (temperature: 25°C, relative humidity: 40%):

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Table 16. ESD indicators

Test Location	Test Method	Contact Discharge (kV)	Air Discharge (kV)
Antenna core and antenna ground	Test the contact and non-contact discharge with an ESD simulator.	±8	±10
GND	Test the contact and non-contact discharge with an ESD simulator.	±8	±10
Other interfaces	Test the contact and non-contact discharge with an ESD simulator.	±0.5	±1

The data is tested based on the ADP-LC116-LA-00-90 development board.

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3 Pins

3.1 Pin Properties

Table 17. Pin attributes

Pin No.	Pin No.
Name	Pin name
I/O	Direction of pin signal PI: Power Input PO: Power Output DI: Digital Input DO: Digital Output DIO: Digital Input and Output AI: Analog input AO: Analog Output AIO: Analog Input and Output OD: Open Drain G: Ground
Voltage Domain	Power domain of the interface
Description	Specific meaning of the pin and processing method when it is not used

3.2 Pin Distribution

The LC116-LA module adopts LCC+LGA packaging, with a total of 143 pins, including 87 LCC pins and 56 LGA pins.

The following figure shows the pin distribution.

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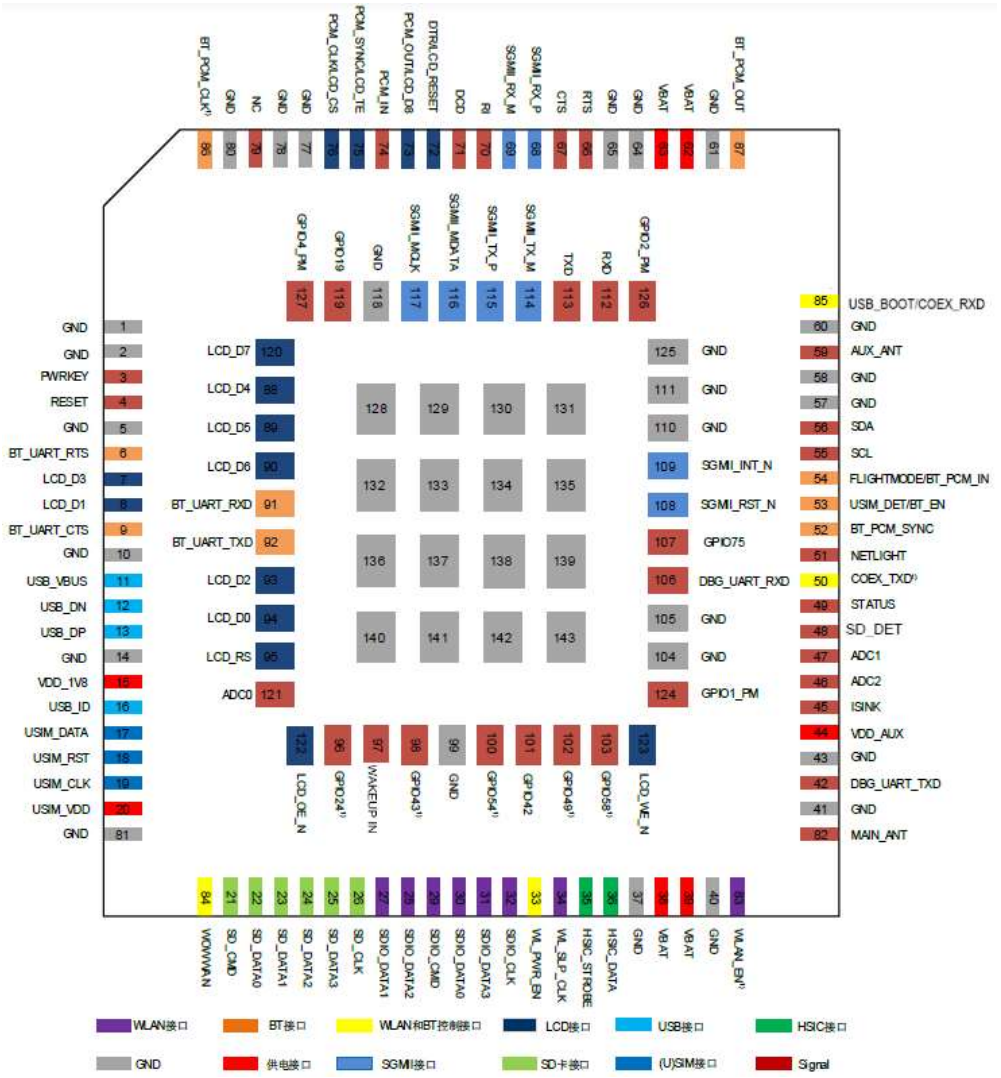

Figure 3. Pin distribution

- If the PCM_CLK, SD_CLK and SCL pins are not used, a 33pF capacitor needs to be attached near the pins to prevent interference to RF.
- Keep the reserved and other unused pins unconnected.
- Connect all GND pins to the ground network.
- Ground pins 128-143.
- It is prohibited to pull PIN50, PIN52, PIN83, PIN85, PIN86, PIN96, PIN97, PIN98, PIN100, PIN102, and PIN103 to the high level before the module is successfully powered on.

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3.3 Pin Details

3.3.1 Power Interface

Table 18. Power interface

Pin No.	Name	I/O	Voltage Domain	Description
38, 39, 62, 63	VBAT	PI	3.3–4.3 V	Baseband/RF power input (3.3–4.3 V)

3.3.2 Control Interfaces

Table 19. Control interface

Pin No.	Name	I/O	Voltage Domain	Description
4	RESET_N	I		When the module is working, pull down RESET_N for 700 ms to 1s, and then release it. The module resets.
3	PWRKEY	I		When the module is in power-off mode, pull down PWRKEY for 100 ms to 2s, and then release it. The module is powered on. When the module is in power-on mode, pull the PWRKEY for 3s to 8s, and then release it. The module is powered off.
85	USB_BOOT/COEX_RXD	I	1.8 V	When the module is in power-off mode, pull up USB_BOOT and insert the USB. The module enters the download mode.

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3.3.3 Baseband Interface

Table 20. Module interface

Pin No.	Pin Name	I/O	Power domain	Description
1, 2.5, 10, 14, 37, 40, 41, 43, 57, 58, 60, 61, 64, 65, 77, 78, 80, 81, 99, 104, 105, 110, 111, 118, 125, 128-143	GND	- -	- -	Ground
15	VDD_EXT	PO	1.8 V	Module digital level, 1.8 V output, 80 mA
45	ISINK	PI	- -	Constant current source input
79	RESERVED	- -	- -	Reserved
96	GPIO_24	IO	1.8 V	General input/output interface. It is prohibited to pull it up to the high level before the module is successfully powered on.
98	GPIO_43	IO	1.8 V	General input/output interface. It is prohibited to pull it up to the high level before the module is successfully powered on.
100	GPIO_54	IO	1.8 V	General input/output interface
101	GPIO_42	IO	1.8 V	General input/output interface
102	GPIO_49	IO	1.8 V	General input/output interface

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Pin No.	Pin Name	I/O	Power domain	Description
103	GPIO_58	IO	1.8 V	General input/output interface. It is prohibited to pull it up to the high level before the module is successfully powered on.
107	GPIO_75	IO	1.8 V	General input/output interface
119	GPIO_19	IO	1.8 V	General input/output interface
124	GPIO1_PM	IO	1.8 V	General input/output interface
126	GPIO2_PM	IO	1.8 V	General input/output interface
127	GPIO4_PM	IO	1.8 V	General input/output interface

3.3.4 RF Interface

Table 21. RF Interface

Pin No.	Pin Name	I/O	Power domain	Description
59	AUX_ANT	AI	- -	Diversity antenna, 50Ω, characteristic impedance
82	MAIN_ANT	IO	- -	Main antenna, 50Ω, characteristic impedance

3.3.5 Other interfaces

Table 22. LPG interface

Pin No.	Pin Name	I/O	Power domain	Description
49	STATUS	DO	1.8 V	Module state indicator
51	NETLIGHT	DO	1.8 V	Module network operating status

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Table 23. PCM interface

Pin No.	Pin Name	I/O	Power domain	Description
73	PCM_OUT/LCD_D8	DO	1.8 V	PCM data output/LCD bus data bit 4
74	PCM_IN	I	1.8 V	PCM data Input
75	PCM_SYNC/LCD_TE	IO	1.8 V	PCM synchronization signal/LCD bus data synchronization
76	PCM_CLK/LCD_NCS	IO	1.8 V	PCM clock signal/LCD bus chip select

Table 24. USB interface

Pin No.	Pin Name	I/O	Power domain	Description
11	USB_VBUS	AI	- -	USB insertion detection, typical value: 5 V
12	USB_DN	IO	- -	USB differential data signal (-)
13	USB_DP	IO	- -	USB differential data signal (+)
16	USB_ID	- -	- -	Primary and secondary USB bus identification, only applicable to the OTG function

Table 25. SDIO interface

Pin No.	Pin Name	I/O	Power domain	Description
27	SDIO_DATA1	IO	1.8 V	WLAN SDIO bus DATA1
28	SDIO_DATA2	IO	1.8 V	WLAN SDIO bus DATA2
29	SDIO_CMD	IO	1.8 V	WLAN SDIO bus command
30	SDIO_DATA0	IO	1.8 V	WLAN SDIO bus DATA0

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Pin No.	Pin Name	I/O	Power domain	Description
31	SDIO_DATA3	IO	1.8 V	WLAN SDIO bus DATA3
32	SDIO_CLK	DO	1.8 V	WLAN SDIO bus clock

Table 26. Bluetooth interface*

Pin No.	Pin Name	I/O	Power domain	Description
9	BT_UART_CTS	O	1.8 V	Clear to send
6	BT_UART_RTS	I	1.8 V	Request to send
91	BT_UART_RXD	DI	1.8 V	Module receives data
92	BT_UART_TXD	DO	1.8 V	Module transmits data
86	BT_PCM_CLK	IO	1.8 V	PCM clock signal. It is prohibited to pull it up to the high level before the module is successfully powered on.
87	BT_PCM_OUT	DO	1.8 V	PCM output signal
54	FLIGHTMODE/BT_PCM_IN	DI	1.8 V	Flight mode control/PCM input signal
52	BT_PCM_SYNC	DO	1.8 V	PCM synchronization signal. It is prohibited to pull it up to the high level before the module is successfully powered on.
53	USIM_DET/BT_EN	DI	1.8 V	SIM card detection/Bluetooth enable

Table 27. HSIC interface*

Pin No.	Pin Name	I/O	Power domain	Description

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Pin No.	Pin Name	I/O	Power domain	Description
35	HSIC_STROBE*	IO	- -	HSIC_STROBE wakeup
36	HSIC_DATA*	IO	- -	HSIC data

Table 28. Coexistence and control interface

Pin No.	Pin Name	I/O	Power domain	Description
50	COEX_TXD	DO	1.8 V	LTE/WLAN&BT co-existed transmission. It is prohibited to pull it up to the high level before the module is successfully powered on.
85	USB_BOOT/COEX_RXD	I	1.8 V	When the module is in power-off mode, pull up USB_BOOT and insert the USB. The module enters the download mode. It is prohibited to pull it up to the high level before the module is successfully powered on.
97	WAKEUP_IN	DI	1.8 V	External device wakeup module, active low by default, configurable by software. It is prohibited to pull it up to the high level before the module is successfully powered on.
83	WLAN_EN	DO	1.8 V	WLAN enabling. It is prohibited to pull it up to the high level before the module is successfully powered on.
84	WOWWAN	DO	1.8 V	Wake up the host
33	WL_PWR_EN	DO	1.8 V	WLAN power enabling

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Pin No.	Pin Name	I/O	Power domain	Description
34	WIFI_SLP_CLK	DO	1.8 V	WLAN sleep clock

Table 29. I²C interface

Pin No.	Pin Name	I/O	Power domain	Description
55	SCL	OD	1.8 V	I²C clock signal. It needs to be pulled up by an external 1.8 V. Disconnect it if it is not used.
56	SDA	OD	1.8 V	I²C data signal. It needs to be pulled up by an external 1.8 V. Disconnect it if it is not used.

Table 30. Debug interface

Pin No.	Pin Name	I/O	Power domain	Description
42	DBG_UART_TXD	DO	1.8 V	Debug serial port sending
106	DBG_UART_RXD	DI	1.8 V	Debug serial port receiving

Table 31. USIM interface

Pin No.	Pin Name	I/O	Power domain	Description
17	USIM_DATA	IO	1.8 V/3 V	(U)SIM data signal line. It needs to be pulled up to USIM_VDD externally.
18	USIM_RST	O	1.8 V/3 V	(U)SIM reset signal line
19	USIM_CLK	O	1.8 V/3 V	(U)SIM clock signal line
20	USIM_VDD	PO	1.8 V/3 V	(U)SIM power supply, the module

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Pin No.	Pin Name	I/O	Power domain	Description
				automatically identifies 1.8 V or 3.0 V (U)SIM card
53	USIM_DET/BT_EN	DI	1.8 V	SIM card detection/Bluetooth enabling

Table 32. SD card interface

Pin No.	Pin Name	I/O	Power domain	Description
21	SD_CMD	IO	1.8 V/3 V	SD card control signal
22	SD_DATA0	IO	1.8 V/3 V	SD card data signal 0
23	SD_DATA1	IO	1.8 V/3 V	SD card data signal 1
24	SD_DATA2	IO	1.8 V/3 V	SD card data signal 2
25	SD_DATA3	IO	1.8 V/3 V	SD card data signal 3
26	SD_CLK	O	1.8 V/3 V	SD card clock signal
48	SD_DET	IO	1.8 V	SD card insertion detection. Active low by default

Table 33. UART interface

Pin No.	Pin Name	I/O	Power domain	Description
66	RTS	O	1.8 V	Request to send
67	CTS	I	1.8 V	Clear to send
70	RI	O	1.8 V	Ring prompt
71	DCD	O	1.8 V	Carrier detection

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Pin No.	Pin Name	I/O	Power domain	Description
72	DTR/LCD_NRST	DI	1.8 V	Sleep mode control/LCD bus reset signal
112	RXD	I	1.8 V	Module receives data
113	TXD	O	1.8 V	Module transmits data

Table 34. ADC interface

Pin No.	Pin Name	I/O	Power domain	Description
46	ADC2	AI	0–1.8 V	Analog-to-digital conversion 2
47	ADC1	AI	0–1.8 V	Analog-to-digital conversion 1
121	ADC0	AI	0–1.8 V	Analog-to-digital conversion 0

Table 35. SGMII interface

Pin No.	Pin Name	I/O	Power domain	Description
68	SGMII_RX_P	AI	- -	SGMII differential data receiving positive signal
69	SGMII_RX_M	AI	- -	SGMII differential data receiving negative signal
108	SGMII_RST_N	DO	1.8/2.85 V	Ethernet reset
109	SGMII_INT_N	DI	1.8 V	Ethernet interrupt
114	SGMII_TX_M	AO	- -	SGMII differential data sending negative signal, close to PHY string 0.1 uF capacitor
115	SGMII_TX_P	AO	- -	SGMII differential data sending

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Pin No.	Pin Name	I/O	Power domain	Description
				positive signal, close to PHY string 0.1 uF capacitor
116	SGMII_MDATA	IO	1.8/2.85 V	SGMII data, 1.8/2.85 V power domain. It needs to be externally pulled up to VDD_AUX with a 1.5 kΩ pull-up resistor.
117	SGMII_MCLK	DO	1.8/2.85 V	SGMII clock
44	VDD_AUX	PO	1.8/2.85 V	SGMII_MDATA pull-up power supply, output of 1.8/2.85 V, configurable

Table 36. LCD interface

Pin No.	Pin Name	I/O	Power domain	Description
94	LCD_D0	IO	1.8 V	LCD bus data bit 0
8	LCD_D1	IO	1.8 V	LCD bus data bit 1
93	LCD_D2	IO	1.8 V	LCD bus data bit 2
7	LCD_D3	IO	1.8 V	LCD bus data bit 3
88	LCD_D4	IO	1.8 V	LCD bus data bit 4
89	LCD_D5	IO	1.8 V	LCD bus data bit 5
90	LCD_D6	IO	1.8 V	LCD bus data bit 6
120	LCD_D7	IO	1.8 V	LCD bus data bit 7
73	PCM_OUT/LCD_D8	DO	1.8 V	PCM data output/LCD bus data bit 4
72	DTR/LCD_NRST	DI	1.8 V	Sleep mode control/LCD bus reset signal

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Pin No.	Pin Name	I/O	Power domain	Description
95	LCD_RS	DO	1.8 V	LCD bus data address switching signal
122	LCD_OE_N	DO	1.8 V	LCD bus primary device read enabling
123	LCD_WE_N	DO	1.8 V	LCD bus primary device write enabling
75	PCM_SYNC/LCD_TE	IO	1.8 V	PCM synchronization signal/LCD bus data synchronization
76	PCM_CLK/LCD_NCS	IO	1.8 V	PCM clock signal/LCD bus chip select

The "*" symbol in the document indicates that the item is under development.

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4 Circuit Design

4.1 Power Interface

4.1.1 Power input

A stable power supply ensures normal operation of the LC116-LA series module. During design, ensure that the power supply ripple is lower than 300 mV (the circuit ESR is less than 100 mΩ). When the module works in GSM mode (burst transmit), the maximum working current can reach 3 A. Ensure that the power supply voltage is not lower than 3.3 V. Otherwise, the module may be powered off or restarted. When the module is operating in burst transmit state, the power limit is as shown in the following figure.

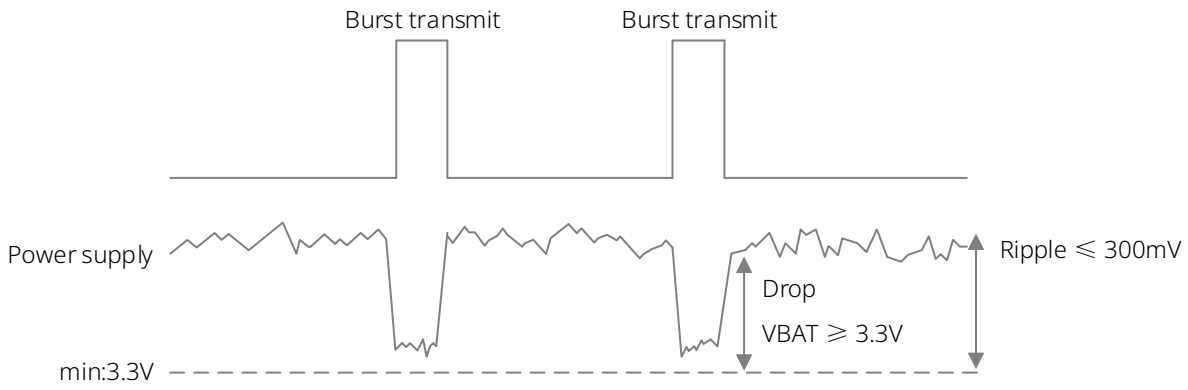

Figure 4. Power supply limit

The ripple of the power supply should be lower than 300 mV, and the line ESR (equivalent series resistance) should be <150 mΩ. When the module is working, it is necessary to ensure that the voltage of the DC power supply is not lower than the minimum voltage.

The VBAT power supply of LC116-LA module requires star wiring to the power supply pins. The following figure shows the recommended design of the power supply.

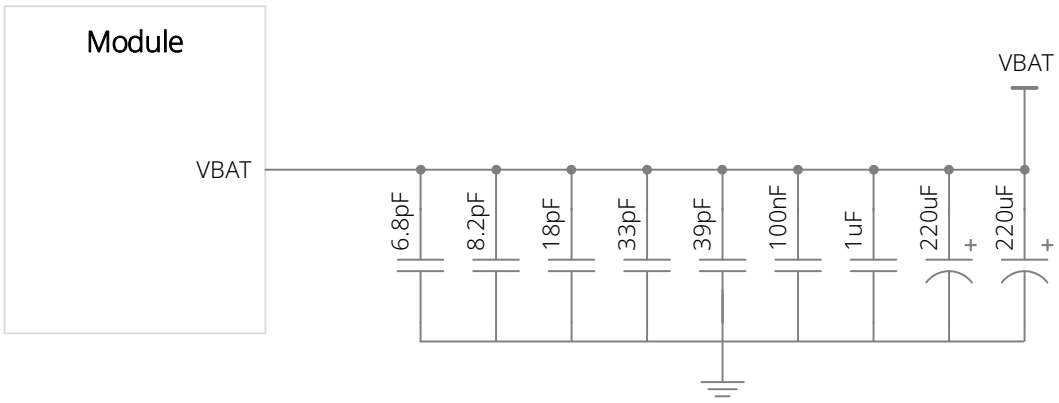

Figure 5. Reference power supply design

The following table describes the filter capacitor design of the power supply.

Table 37. Design description

Application Description	Mode	Recommended Parameter
To reduce power fluctuations during module operation	Regulating capacitor	Use a capacitor with low ESR; 220 uF x 2 or 330 uF; LDO or DC power supply requires capacitors with a capacitance of no less than 440 uF. Battery power supply requires capacitors with a capacitance of 100 uF to 220 uF.
Filter out interference caused by clock and digital signals.	Filter capacitor	1 uF, 100 nF
Eliminate low-frequency and intermediate-frequency RF interference.	Decoupling capacitor	39 pF, 33 pF
Eliminate high-frequency RF interference.	Decoupling capacitor	18 pF, 6.8 pF, 8.2 pF

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It is recommended to reserve the TVS tube position for the VBAT power supply.

PCB design:

To reduce the equivalent impedance of the VBAT cabling, the cabling from the external power supply to VBAT is required to be as short and wide as possible (it is recommended that the cabling width of VBAT should be at least 1 mm/1 A to ensure sufficient power supply capacity). The capacitors with a small capacitance should be placed close to the module, and the ground plane of the power supply part should be as complete as possible.

4.2 Control Interface

Control signals are used to power on/off, reset, and download the module.

4.2.1 Pulse startup

When the module is in power-off mode, pull down the PWRKEY for 100 ms to 2s to enable the module to start. It is recommended to use OC/OD driver circuit to control the PWRKEY pin. The following figure shows the reference circuit.

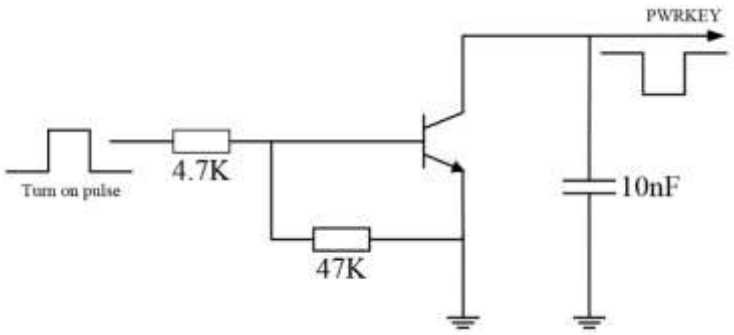

Figure 6. OC driver startup reference circuit

Another way to control the PWRKEY pin is to use a button switch. A TVS (ESD9X5VL-2/TR recommended) should be placed near the button for ESD taken. The following figure

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shows the reference circuit.

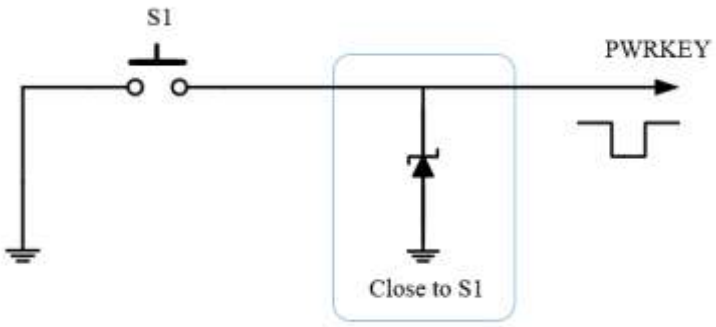

Figure 7. Button startup reference circuit

The following figure shows the startup timing sequence.

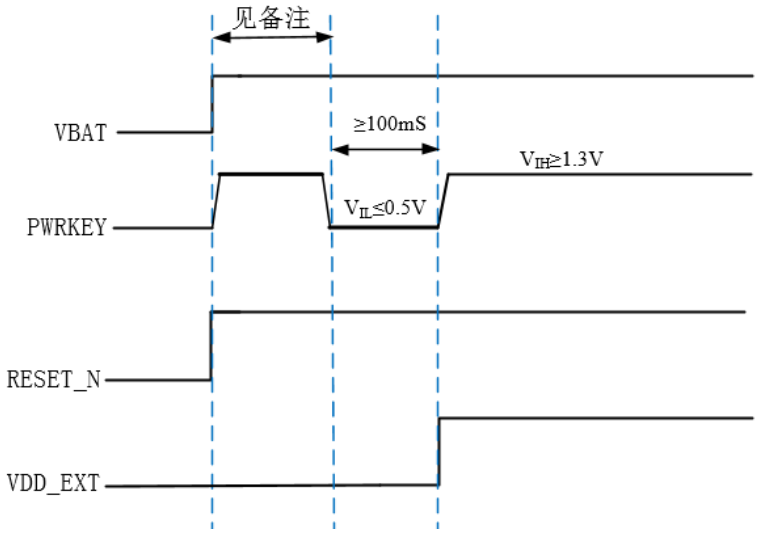

Figure 8. Startup timing sequence

Before pulling down the PWRKEY pin, make sure that the VBAT voltage is stable. It is recommended to control the interval from power-up by VBAT to PWRKEY pin pull-down no less than 30ms.

4.2.2 Auto power-on

To implement auto power-on, ground the PWRKEY pin. In this case, the module can be powered off by disconnecting the power supply.

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4.2.3 Power-off

The module supports the following three power-off modes.

Table 38. Power-off mode

Power-off Mode	Power-off Method	Applicable Scenario
Low-voltage power-off	When VBAT voltage is too low or power-down occurs, the module will be powered off.	The module does not log out from a base station.
Hardware	Pull down PWRKEY pin for 3s to 8s.	Hardware normal power-off
AT Power-off	AT+PWROFF	Software power-off

- When the module is working properly, do not cut off the power supply of the module immediately to avoid damaging the internal Flash. It is strongly recommended to power off the module by the PWRKEY pin or the module by PWRKEY or AT command before cutting AT command before cutting off the power supply.
- When using the AT command to power off the module, ensure that the PWRKEY pin is always at the high level after the power-off command is executed. Otherwise, the module will automatically power on again.

The following figure shows the power-off timing sequence.

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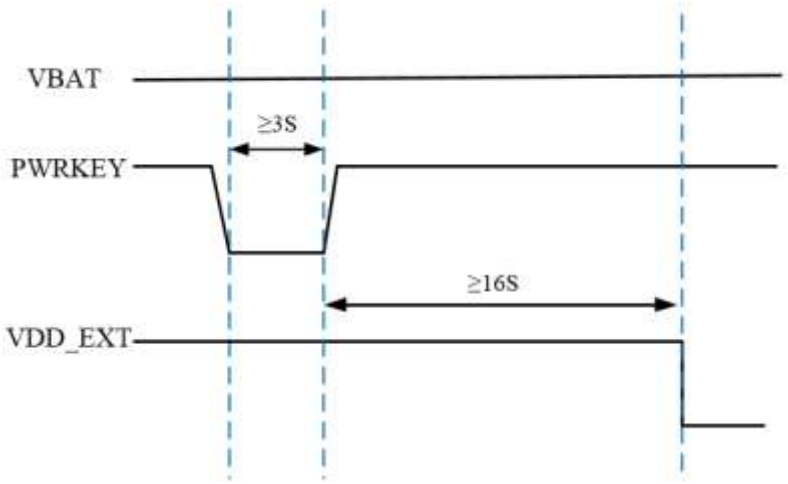

Figure 9. Power-off timing sequence

4.2.4 Reset

Module reset method: Pull down the RESET_N pin for 700 ms to 1s, and then release or send the AT command AT+RESET. Clients can control the RESET_N pin by OC/OD driver circuit and button switch. The following figure shows the reference circuits.

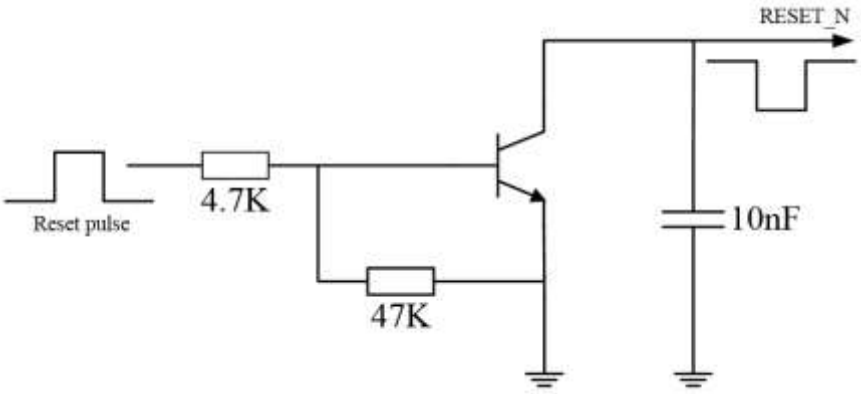

Figure 10. OC driver reset reference circuit

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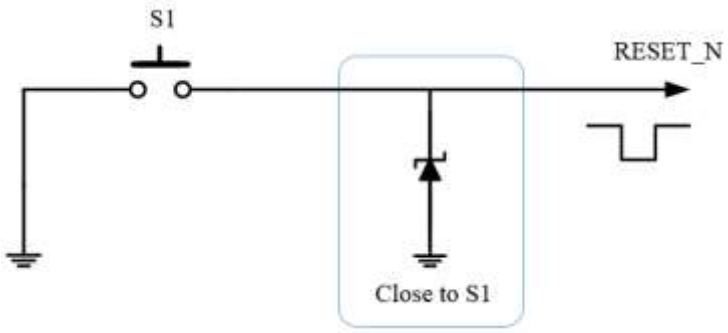

Figure 11. Button reset reference circuit

The following figure shows the RESET_N timing sequence.

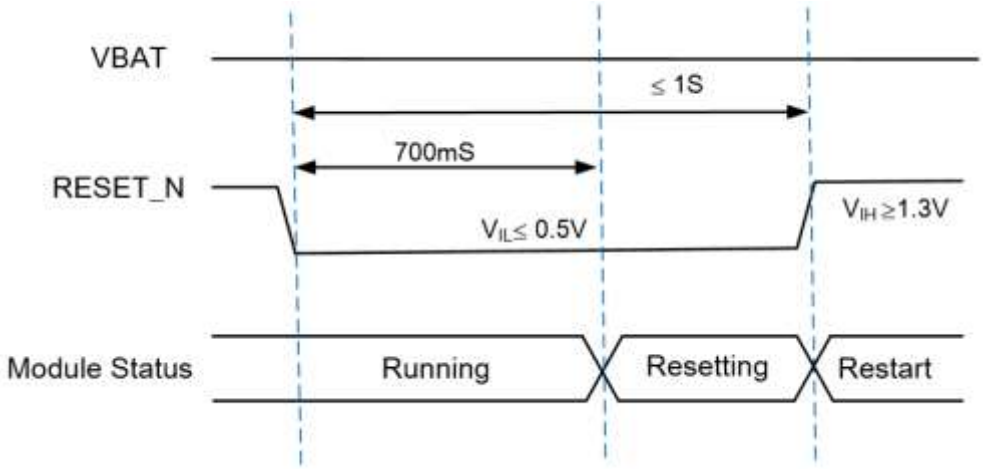

Figure 12. Reset timing sequence

PCB Design

RESET is a sensitive signal. During PCB layout, keep these signals far away from RF interference.

PCB routes must be protected using GND and kept away from edges of PCBs to avoid module reset due to ESD problems.

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4.3 Operating Mode

4.3.1 Flight mode

The following table describes the W_DISABLE# pin of the LC116-LA module.

Table 39. Flight mode interface

Pin No.	Pin Name	I/O	Power domain	Description
54	W_DISABLE#/BT_PCM_IN	DI	1.8 V	Flight mode control/PCM input signal

LC116-LA module supports two ways to enter flight mode:

Table 40. Flight mode interface

1	Hardware interface button control	Send AT+WDISABLEEN=1 to enable W_DISABLE# and pull up or disconnect the W_DISABLE# pin (pull up by default). The module enters standard mode. When this pin is pulled down, the module enters the flight mode.
2	AT command control	Run the AT+CFUN=4 command to enter flight mode Run the AT+CFUN=1 command to enter the standard mode

4.3.2 Sleep

4.3.2.1 USB Application (USB Suspend Not Supported and VBUS Supported)

If the host does not support the USB Suspend function, the module can enter the sleep mode by disconnecting USB_VBUS through the external control circuit.

Sleep mode:

Send AT+GTLPMMODE=1,X to set the effective level of the WAKEUP_IN signal that sets the module into sleep mode. Command is effective after resetting module.

(When X=0, if WAKEUP_IN pin is at high level, the module will enter sleep mode;

When X=1, if WAKEUP_IN pin is at low level, the module will enter sleep mode)

AT+CSCLK=1	Enable sleep mode function.
AT+GTUSBSLEEPEN=1,0	Set USB sleep mode.

Unplug the USB cable and turn off the USB Hub master controller. The module will enter sleep mode.

Wake mode:

Insert the USB. Turn on the USB master controller or pull down USB_VBUS. The module will wake up.

4.3.2.2 USB Application (USB Suspend Not Supported and VBUS Not Supported)

If the host does not support the USB Suspend function or VBUS detection, the module can enter the sleep mode by disconnecting USB.

Sleep mode:

Unplug the USB cable or turn off the USB Hub master controller. The module will enter sleep mode.

Wake mode:

Insert the USB or turn on the USB master controller. The module will wake up.

4.3.2.3 USB Application (USB Suspend Supported)

If the host supports USB Suspend/Resume, set the USB sleep mode in the Linux system.

Sleep mode:

The USB port of the module sets the level and control in the USB device to auto in the Linux system to suspend the USB device of the module. The module and the host are static for about 2s. Then, the module automatically enters the suspend state.

Wake mode:

The module can wake up through any USB operation.

4.3.2.4 Disabling USB

If there is no USB connection between the module and the host, you can disable the USB to enter the power saving mode. You can disable the USB inside the module to save power. For details, see the relevant software documents.

The USB ports of the module cannot contain adb ports, for example, +GTUSBMODE=17.

Power consumption of the module in idle state can be implement by the following commands and steps:

1. AT+DISK=0,0,0
2. AT+GTUSBDETECTEN=1
3. AT+SYSCMD=echo off > /sys/power/autosleep
4. Remove the USB cable.

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4.4 Baseband Interface

4.4.1 USB

The module supports USB 2.0 and is compatible with USB High-Speed (480 Mbits/s) and USB Full-Speed (12 Mbits/s). For details about the timing and electrical characteristics for the USB interface, see *Universal Serial Bus Specification 2.0*.

Schematic Diagram Design

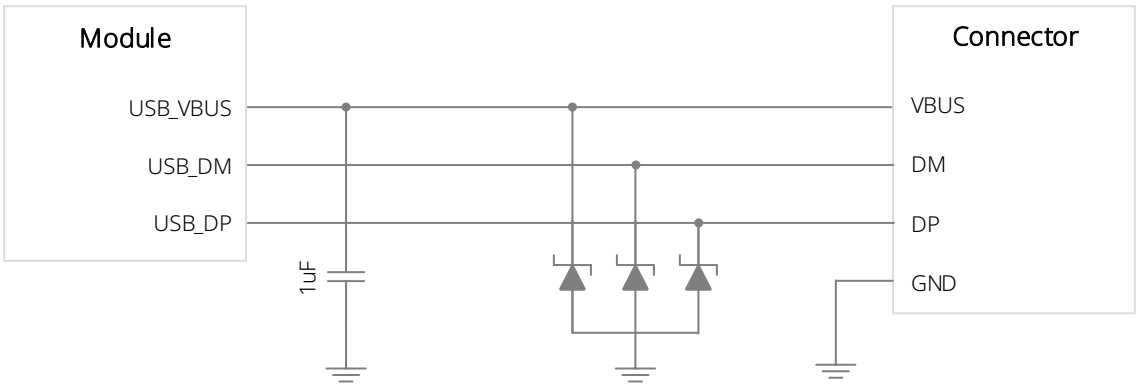

Figure 13. USB interface circuit design

Since the module supports USB 2.0 High-Speed, it is recommended to use TVS with a capacitance of 0.5 pF on the USB_DM/DP differential signal line. It is recommended to connect a 0 ohm resistor on each USB_DM/DP differential line to facilitate debugging. USB enumeration requires an additional voltage to USB_VBUS. Otherwise, USB cannot be enumerated normally. The voltage range is 3.3 V to 5.5 V.

PCB Design

USB_DP and USB_DM are high-speed differential signal lines that should be equal in length and parallel to avoid right-angle route. The difference of cabling length is controlled within ≤2 mm, and the differential impedance is controlled at 90Ω±15%.

The USB data cable cannot be routed under the crystal, oscillator, magnetic device, or RF signal. It is recommended to take an inner differential cable that is wrapped with copper connected to the ground at all directions.

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The ESD protector for the USB data cable must be placed close to the USB interface. The parasitic capacitance of the ESD protector must not exceed 1 pF.

USB 2.0 differential signal cable should be laid on the signal layer nearest to the ground.

For more information about the USB 2.0 specification, please visit http://www.usb.org/home

4.4.2 UART

The module has a main serial port, a Bluetooth serial port* for data communication and a debugging serial port.

- The main serial port supports baud rates of 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps. The default baud rate is 115200 bps, used for data transmission and AT command transmission.
- The Bluetooth serial port* supports baud rates of 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps. The default baud rate is 115200 bps, used for Bluetooth data communication.
- The debugging serial interface supports 115200 bps baud rate. It is used for Linux control and log output.

The serial port level of the LC116-LA series module is 1.8 V. If the level of the host system is 3.3 V or another value, a level converter is needed between the module and the host. Figure 15 and Figure 16 show the design of reference circuit of the serial port level conversion chip. You can design the input and output circuits of the dashed line part by referring to the solid line part in Figure 16, but pay attention to the connection direction.

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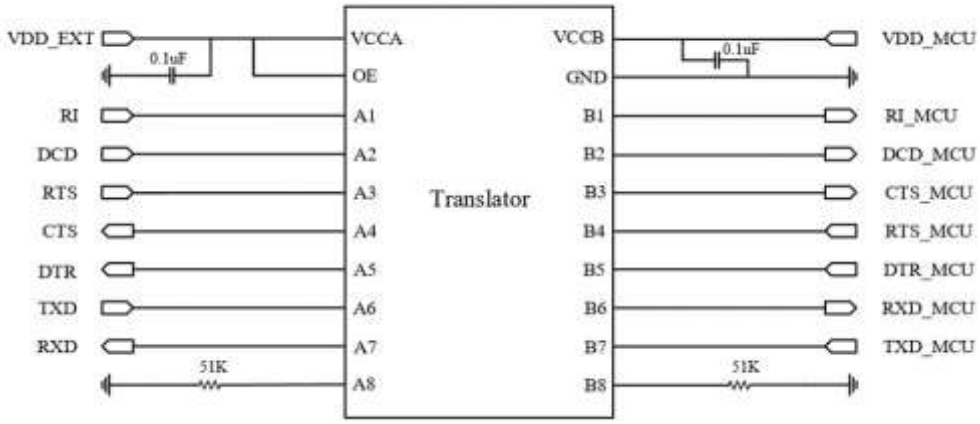

Figure 14. Reference circuit 1 for serial port level conversion

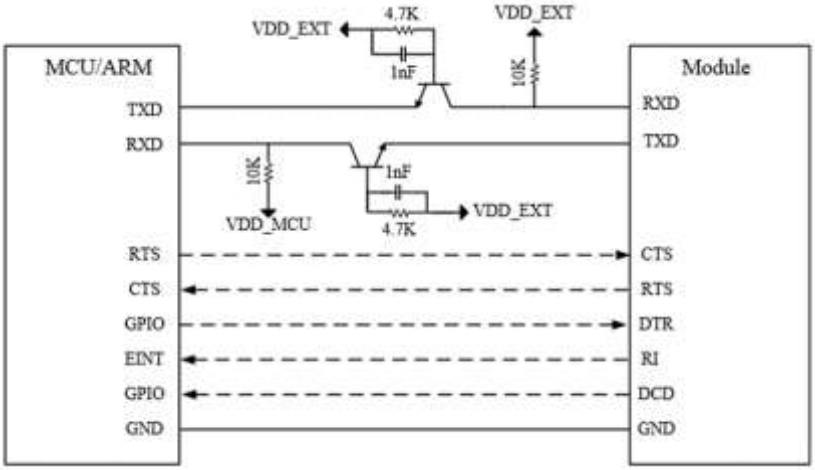

Figure 15. Reference circuit 2 for serial port level conversion

4.4.3 I²C

The module provides a set of I²C interfaces that support communication rates of 100 Kbps in standard mode, 400 Kbps in fast mode, and 3.4 Mbps in high-speed mode. The I²C bus is a simple, bidirectional two-wire synchronous serial bus. It only requires a data line and a clock line to transfer information between devices connected to the bus. It is mainly used in the communication between multiple integrated circuits in the system.

The I²C interfaces are all open-drain outputs. When using these interfaces, please pull up to 1.8 V power domain through external pull-up resistors. When I²C has more than one peripheral, please ensure the uniqueness of every peripheral address. When mounting

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peripherals with high real-time requirements, please do not share I²C with other peripherals.

4.4.4 SD card

The module supports a set of SD card interfaces that support SD 3.0 protocol. The following figure shows the SD reference circuit design.

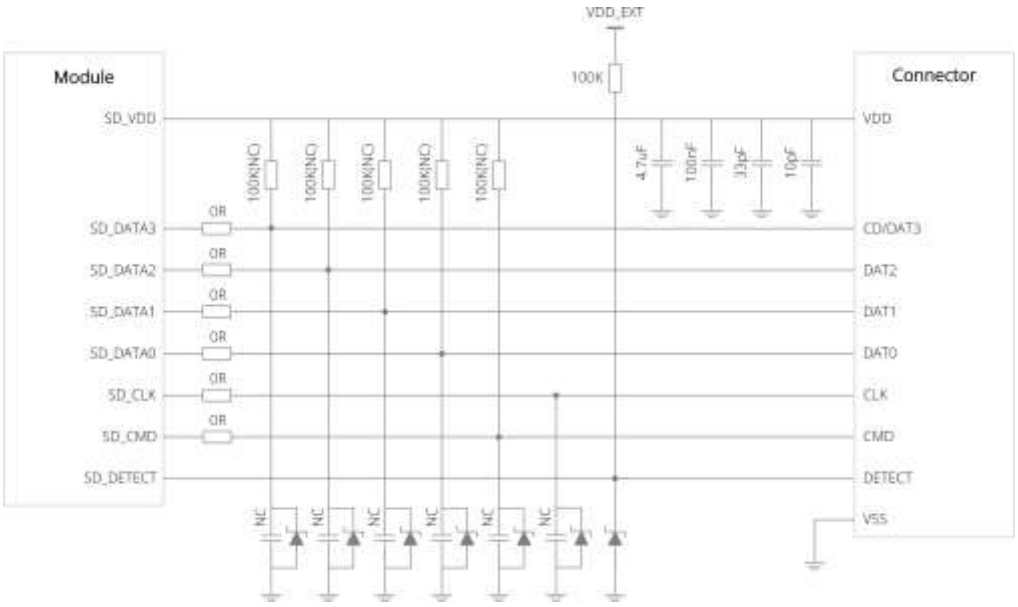

Figure 16. SD reference circuit design

PCB Design

SD circuit design must meet EMC standards and ESD requirements, and at the same time, EMS capability must be improved to ensure that the SD card can work stably. The following principles must be strictly followed in the design:

- If the cabling length of signal lines is equal to or less than 50 mm. It is recommended to place the SD card connector as close to the SD signal pins of the module as possible because the internal cabling length of the module is 40 mm. If the cabling length is equal to or less than 10 mm, the cabling length difference of the clock signal line and data signal line should be controlled equal to or less than 1 mm.

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- The SD signal line must be grounded all around and kept away from RF antenna, DCDC power supply, clock signal line and other strong interference sources.
- Reference ground must be installed for the SD signal line, and data line impedance must be controlled with 50 Ω (±10%).
- It is recommended to install resistors between the module and SD card connector in serial mode, and reserve bypass capacitors C1 to C6. In case of interference or ESD issue, you can adjust the capacitors and resistors to improve signal quality.
- The capacitance on the SD signal line must be smaller than 40 pF.

4.4.5 ADC

The module provides three analog-to-digital conversion interfaces. Run the AT+MMAD="0/1" command to read the voltage value of ADC interface. The voltage range of ADC interface is 0 V–1.8 V.

To improve the accuracy of ADC voltage measurement, it is recommended that the ADC be grounded during wiring.

4.4.6 USIM

The module has a built-in (U)SIM card interface, and supports 1.8 V and 3.0 V (U)SIM card.

4.4.6.1 (U)SIM Card Connector with Card Detection Signal

During (U)SIM design, you must select a (U)SIM card connector. A hot plugging card connector (recommended model: SIM016-8P-220P) with (U)SIM card detection function is recommended.

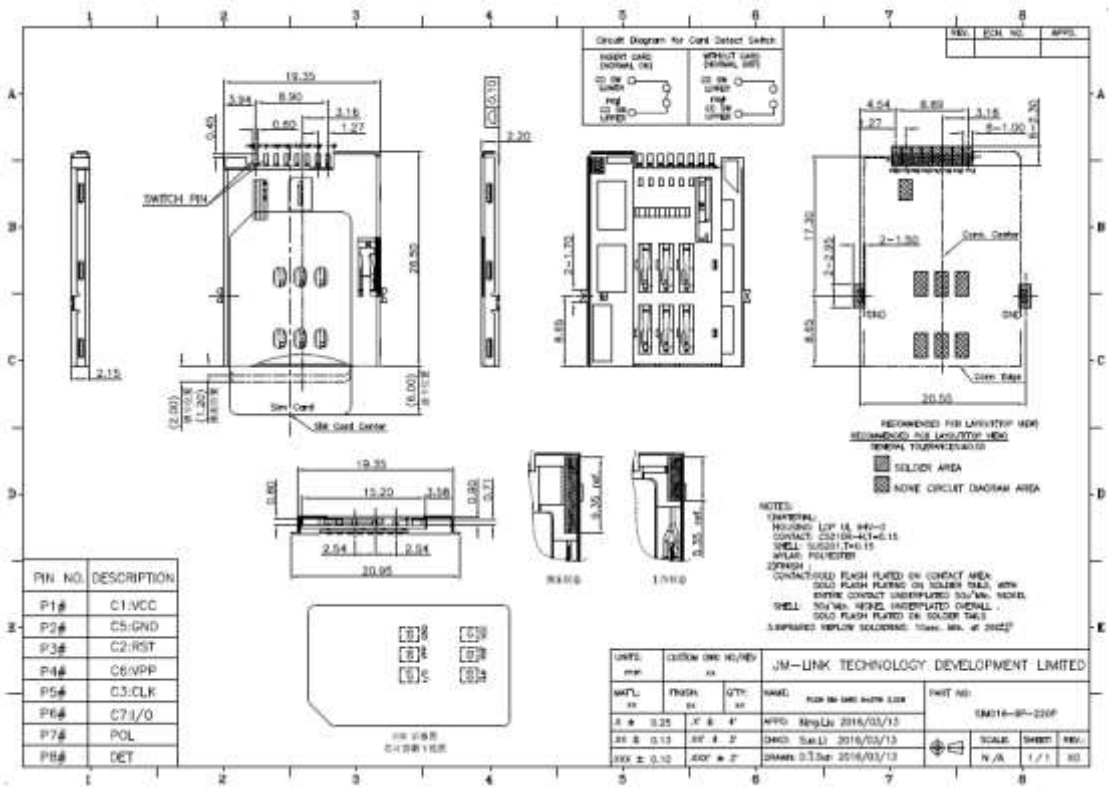

Figure 17. (U)SIM card connector (SIM016-8P-220P)

DET and POL are short connected when the card is inserted, and DET and POL are disconnected when the card is removed. The following figure shows the reference design circuits. When (U)SIM card is inserted, USIM_PRESENCE pin is at a high level. When (U)SIM card is removed, USIM_PRESENCE pin is at a low level.

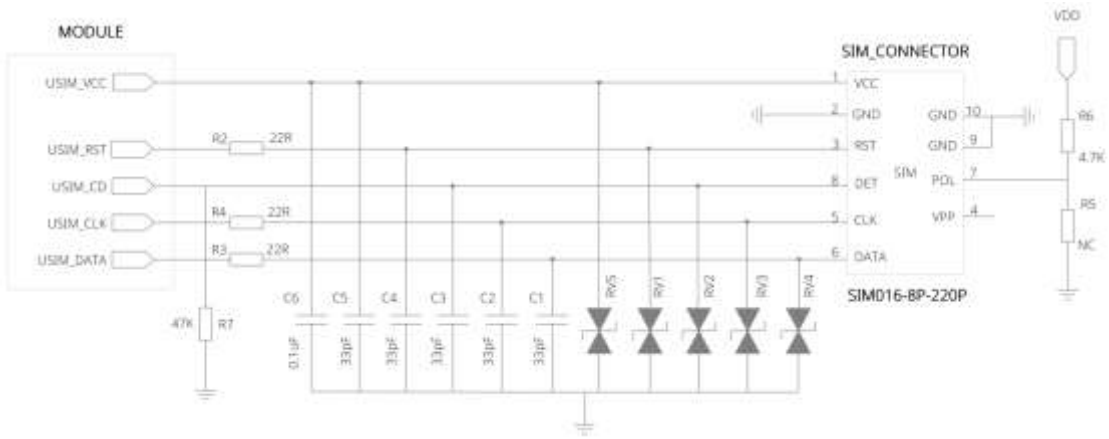

Figure 18. Reference circuit design of a (U)SIM card connector with card detection signals

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4.4.6.2 (U)SIM Card Connector Without Card Detection Signals

When you use an (U)SIM card connector without detection signals, USIM_PRESENCE pin must be disconnected. The following figure shows the reference circuit.

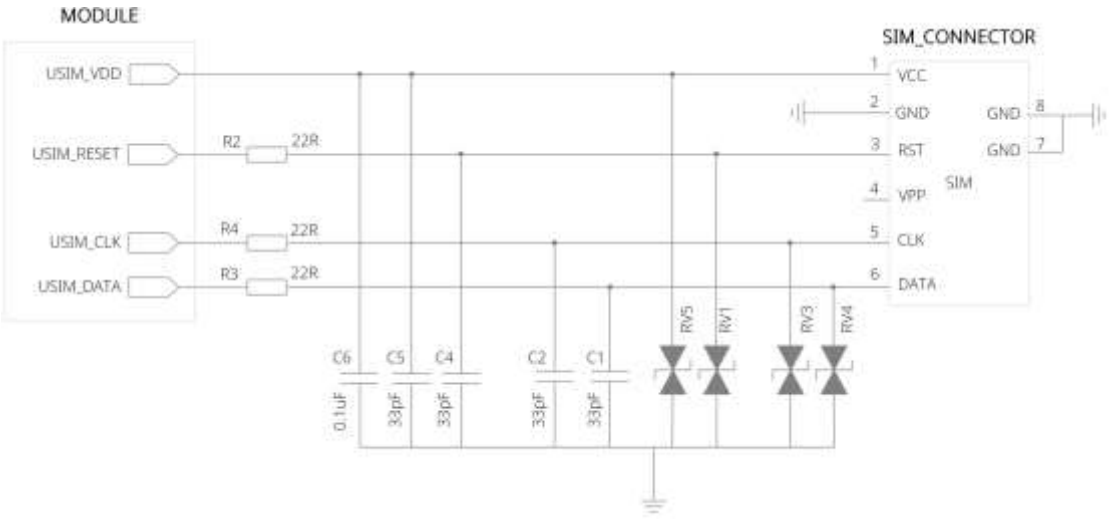

Figure 19. SIM card connector without card detection signals

The USIM_DATA module needs to be pulled up externally. The recommended model for RV1 to RV5 is EGA10402V05A2.

4.4.6.3 (U)SIM Hot Plugging

The LC116-LA module supports (U)SIM card hot plugging function. The module determines whether the (U)SIM card is in place by detecting the state of the USIM_PRESENCE pin. The (U)SIM card hot plugging function is enabled by default. When the USIM_PRESENCE is at a high level, the module initializes the (U)SIM card after detecting that the (U)SIM card is inserted, and registers the network after reading the (U)SIM card information. When the USIM_PRESENCE is at a low level, the module determines that the (U)SIM card is removed and does not read it. You can use the AT+MSMPD=0 command to disable the hot plugging function if not required.

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4.4.6.4 (U)SIM Card Design Requirements

(U)SIM circuit design must meet EMC standards and ESD requirements, and at the same time, EMS capability must be improved to ensure that the SIM can work stably. The following principles must be strictly followed in the design:

- (U)SIM card connector should be located as close to the module as possible, and kept away from the RF antenna, DCDC power, clock signal cables and other strong interference sources.
- SIM card connector is covered by metal shield shell to improve EMS.
- The cabling length from the module to the SIM card connector shall not exceed 100mm. Longer cable will reduce signal quality;
- USIM_CLK and USIM_DATA signal lines are grounded and isolated to avoid mutual interference. If it is difficult to do so, at least (U)SIM card signals must be wrapped with copper connected to the ground.
- The filter capacitor and ESD device of the (U)SIM card signal line are placed close to the (U)SIM card slot. The upper limit of the equivalent capacitance of the ESD device is 22-33 pF.
- It is recommended to make a clearance design for the PCB directly under the shrapnel of the SIM card connector to avoid the insulating green oil on the surface of the PCB being worn down when the shrapnel is pressed down, resulting in a short circuit between the SIM card signal line and the ground.
- USIM_DATA is pulled up to USIM_VDD via a 10 kΩ resistor.

4.4.7 PCM

The LC116-LA module provides a digital audio interface PCM for communication with external codec and other digital audio devices.

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4.4.7.1 PCM Interface Description

Table 41. PCM interface description

Pin Name	Frequency	Duty Ratio	Coding Format	Operating Mode
PCM_CLK	2.048MHz	50%	16bit Liner mono	Module serves as master, supporting PCM as slave
PCM_OUT	- -	- -	16bit Liner mono	Module serves as master, supporting PCM as slave
PCM_IN	- -	- -	16bit Liner mono	Module serves as master, supporting PCM as slave
PCM_SYNC	8KHz	Short pulse	16bit Liner mono	Module serves as master, supporting PCM as slave

4.4.7.2 PCM Signal Description

The main chip of the module uses PCM signals that comply with the European E1 standard. PCM_CLK works at 2.048 MHz and uses 16-bit linear coding format. PCM_SYNC is a short pulse of 8 kHz (488 nS).

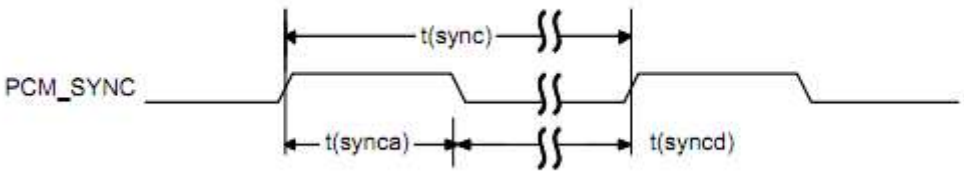

Figure 20. PCM_SYNC timing sequence

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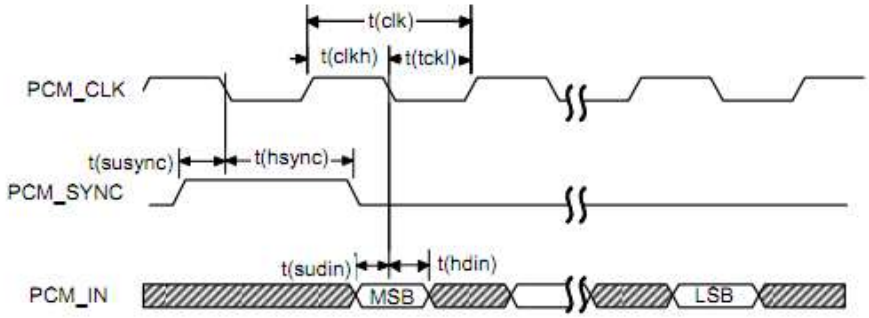

Figure 21. Timing sequence of PCM_CODEC to LC116-LA module

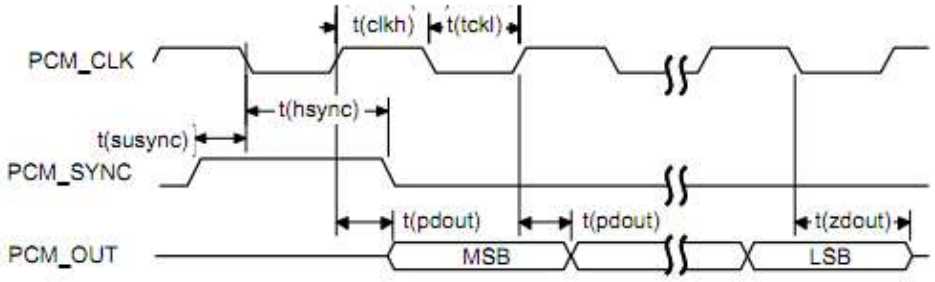

Figure 22. Timing sequence of LC116-LA module to PCM_CODEC

Table 42. Codec timing sequence parameters

Time	Parameter	Min	Typ	Max	Unit
t(sync)	PCM_SYNC cycle time	- -	125	- -	μs
t(synca)	PCM_SYNC asserted time	- -	488	- -	ns
t(syncd)	PCM_SYNC deasserted time	- -	124.5	- -	us
t(clk)	PCM_CLK cycle time	- -	488	- -	ns
t(clkh)	PCM_CLK high time	- -	244	- -	ns

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Time	Parameter	Min	Typ	Max	Unit
t(clkl)	PCM_CLK low time	- -	244	- -	ns
t(susync)	PCM_SYNC offset time to PCM_CLK falling	- -	122	- -	ns
t(sudin)	PCM_DIN setup time to PCM_CLK falling	60	- -	- -	ns
t(hdin)	PCM_DIN hold time after PCM_CLK falling	10	- -	- -	ns
t(pdout)	Delay From PCM_CLK rising to PCM_DOUT valid	- -	- -	60	ns
t(zdout)	Delay from PCM_CLK falling to PCM_DOUT high impedance	- -	160	- -	ns

4.4.8 Status Indicator

4.4.8.1 Network Status Indicator

The PIN51 of the LC116-LA module is the network status indicator signal interface. The network status indicator interface is used to drive the status indicator. The following table describes the working status of the module network indicator.

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Table 43. Working status of the network status indicator

Mode	Level Status of Network Indicator Pin	Description
1	600 ms at high level or 600 ms at low level	No SIM card SIM pin Registering with the network (T < 15s) Failed to register with the network
2	3000 ms at high level or 75 ms at low level	Standby
3	75 ms at high level or 75 ms at low level	Established a data connection
4	Low level	Voice call
5	High level	Sleep status

The following figure shows the reference circuit of network status indicator.

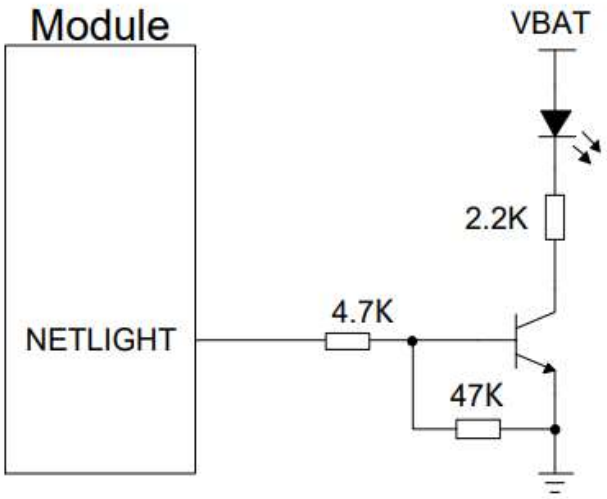

Figure 23. Reference circuit for the network status indicator

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4.4.8.2 STATES

PIN49 of the LC116-LA module is the module status indicator signal interface. The STATES indicator is used to indicate the working status of the module, and it outputs a high level after the module is powered on. The following figure shows the reference circuit of the STATES indicator.

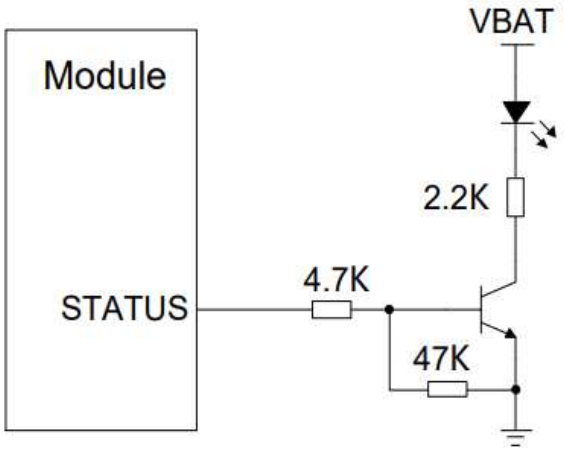

Figure 24. Reference circuit for the STATES indicator

4.4.9 HSIC Interface*

HSIC is a two-wire source-synchronous serial interface with a signal level of 1.2 V. It is suitable for low-power applications with standard LV CMOS levels.

The HSIC interface is a high-speed inter-chip interconnection bus, and supports a data transmission rate of 480 Mbps. When routing, control the routing impedance to 50Ω.

"*" indicates that the item is under development.

4.4.10 LCD Interface

The LC116-LA module provides a set of parallel LCD interfaces. The characteristics are as follows:

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- 8-bit and 9-bit parallel data interfaces: The 8-bit interface uses the lower 8 bits (D0 to D7) of the EBI2 bus, shared by the EBI2 with the Nand inside the module.
- The resolution is 320 (V) × 480 (H) pixels at a refresh rate of 30 fps.

The following figure shows the reference circuit of the LCD interface using H.028.015A01 LCD screen.

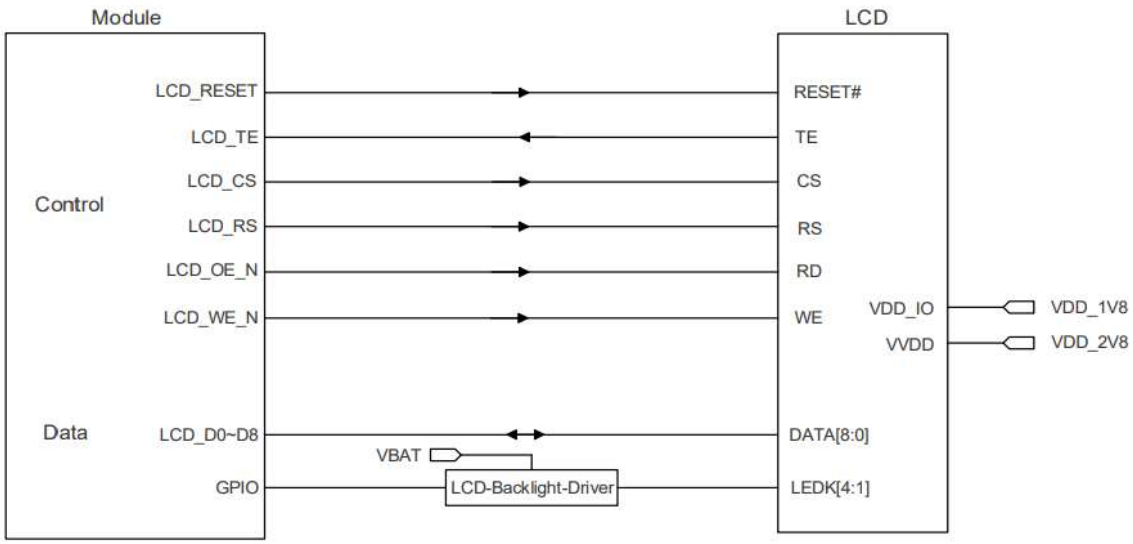

Figure 25. LCD reference circuit

4.4.11 SGMII

The LC116-LA module provides an SGMII interface with embedded Ethernet MAC. The characteristics are as follows:

- It complies with IEEE 802.3 standard.
- It supports the 10M/100M/1000M working modes.
- The maximum downlink rate is 150 Mbps, and the maximum uplink rate is 50 Mbps (on the 4G LTE network).
- It can be connected to an external Ethernet PHY chip such as AR8033, or an external switch.

The following figure shows the simple diagram of the Ethernet application scheme.

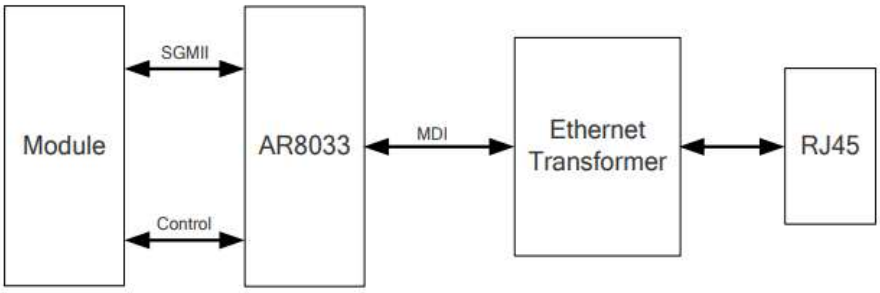

Figure 26. Simple diagram of the Ethernet application scheme

The following figure shows the reference design of the SGMII interface of the LC116-LA module connected to Ethernet PHY chip such as AR8033.

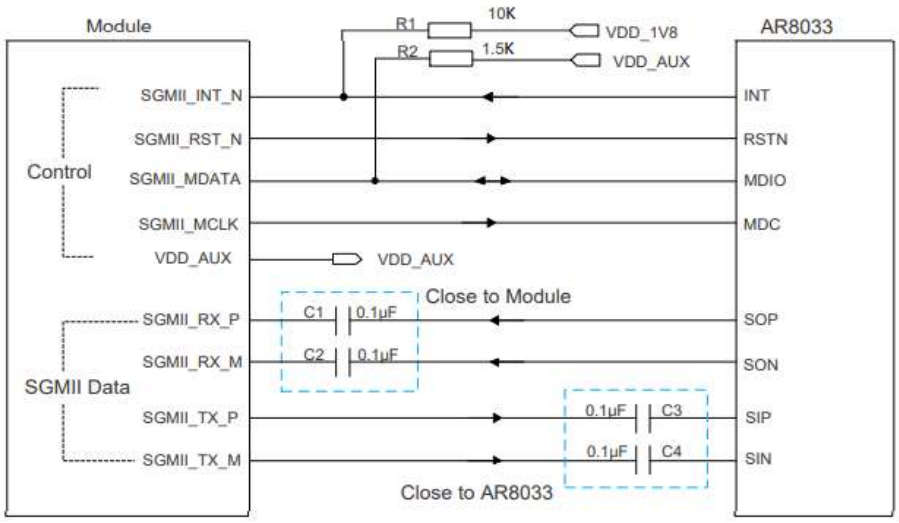

Figure 27. Reference design of the SGMII interface

4.5 RF Part

4.5.1 Antenna Design

The following table describes the major antenna performance indicators in antenna design.

Table 44. Antenna performance indicators

Indicator	Description	Recommended Value
Antenna Efficiency	Ratio of antenna radiated power to input power.	>40% (-4 dB)
S11 or VSWR	S11 shows the matching degree of 50 Ω impedance of the antenna, which affects the antenna efficiency to a certain extent. The VSWR test can be used to measure this indicator.	<-10 dB
Polarization type	Rotation direction of the electric field in the maximum radiation direction of the antenna.	Linear polarization
Radiation pattern	Intensity of electromagnetic field in all directions of far-field.	PIFA or IFA antenna is recommended.
Gain and directivity	The gain refers to the combination of antenna efficiency and antenna directivity. The directivity of antenna refers to the electromagnetic field strength of electromagnetic wave in all directions.	Gain: 2.5 dBi
Input impedance	Ratio of voltage to current at the antenna input end. The best situation is that the input impedance of the antenna is pure resistance and equal to the characteristic impedance of the feeder. At this time, there is no power reflection at the terminal of the feeder, and there is no standing wave on the feeder. The input impedance of the antenna changes smoothly with frequency.	50Ω

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Indicator	Description	Recommended Value
Input power	- -	Peak power >33 dBm (2 W) in GSM system Average power >23 dBm in WCDMA&LTE systems
VSWR	- -	≤ 2:1

4.5.2 Impedance Design

For modules that do not have a RF connector, you need to route a RF cable to connect to the antenna feeding point or connector. It is recommended to use a microstrip line. The shorter the better. The insertion loss should be controlled less than 0.2 dB, and impedance should be controlled within 50Ω.

In general, the impedance of the RF signal route is determined by the dielectric constant of the material, the route width (W), the ground clearance (S) and the height of the reference ground plane (H). The control of the characteristic impedance of the PCB usually is implemented in two ways: microstrip route and coplanar waveguide. To illustrate the design principles, the following figures show the structural designs of microstrip route and coplanar waveguide when the impedance line is at 50Ω.

- Microstrip cable complete structure

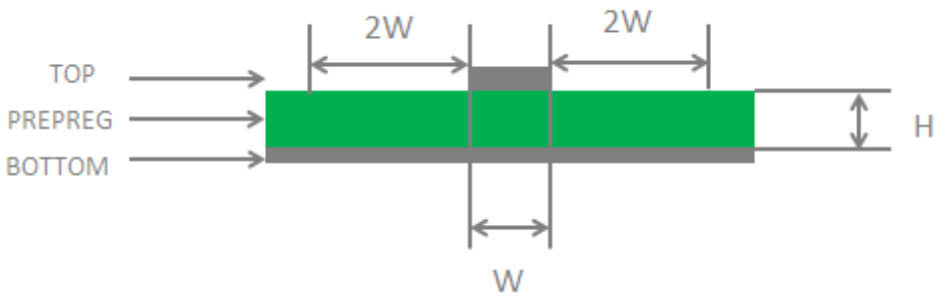

Figure 28. Two-layer PCB microstrip line structure

- Coplanar waveguide complete structure

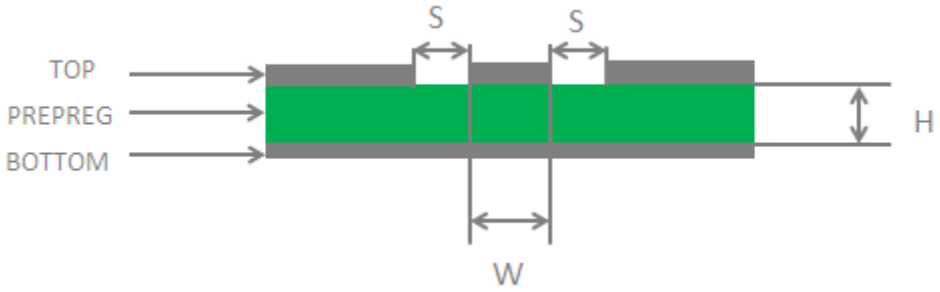

Figure 29. Two-layer PCB coplanar waveguide structure

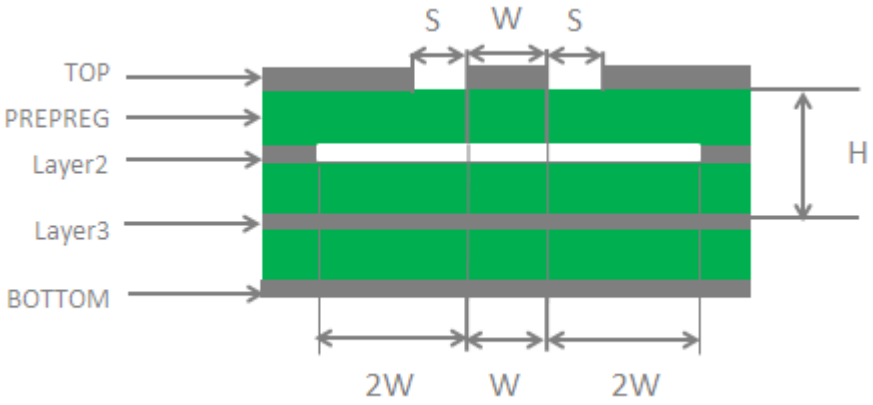

Figure 30. Four-layer PCB coplanar waveguide structure (see ground layer 3)

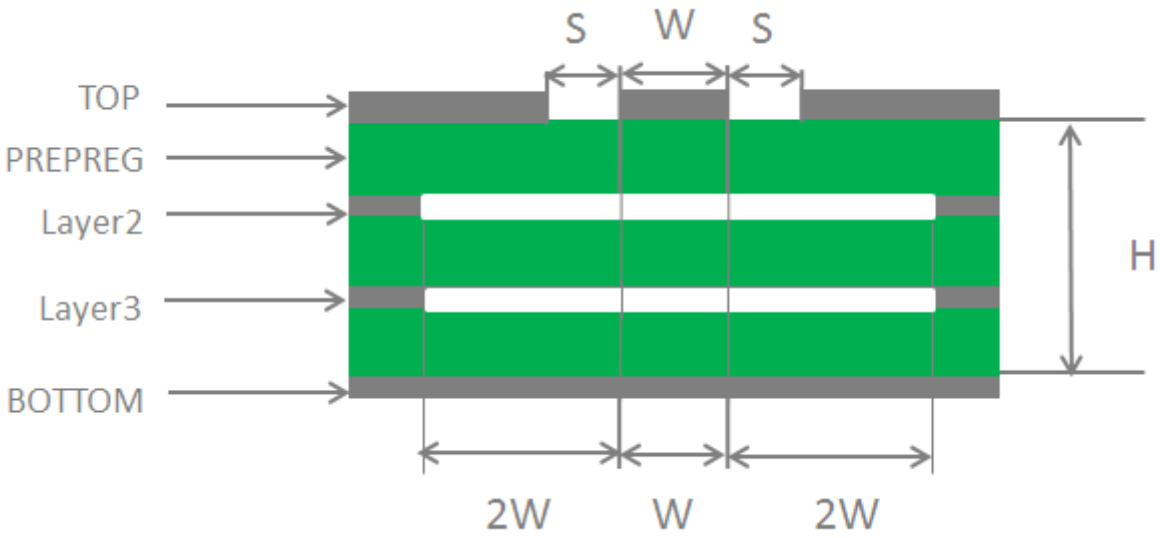

Figure 31. Four-layer PCB coplanar waveguide structure (see ground layer 4)

In the design of RF antenna interface circuit, in order to ensure good performance and reliability of the RF signal, it is recommended to observe the following principles:

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- The impedance simulation tool should be used to accurately control the RF signal cable at 50Ω impedance.
- The GND pin adjacent to the RF pin should not have thermal welding plate and should be in full contact with the ground.
- The distance between the RF pin and the RF connector should be as short as possible. At the same time, avoid the right-angle route. The recommended route angle is 135°.
- Attention should be paid to the establishment of the connection component package and the signal pin should be kept at a certain distance from the ground.
- The reference ground plane of the RF signal cable should be kept intact; adding a certain amount of ground holes around the signal and the reference ground can improve the RF performance; the distance between the ground hole and the signal cable should be at least 2 times the cable width (2*W).
- The equivalent capacitance of the TVS should be less than 0.5 pF.

Add a π-type circuit (two parallel component grounding pins are connected directly to the main GND) between the module and antenna connector (or feeding point) for antenna debugging. Two parallel components are directly connected across the RF cable, and the branch must not be pulled out.

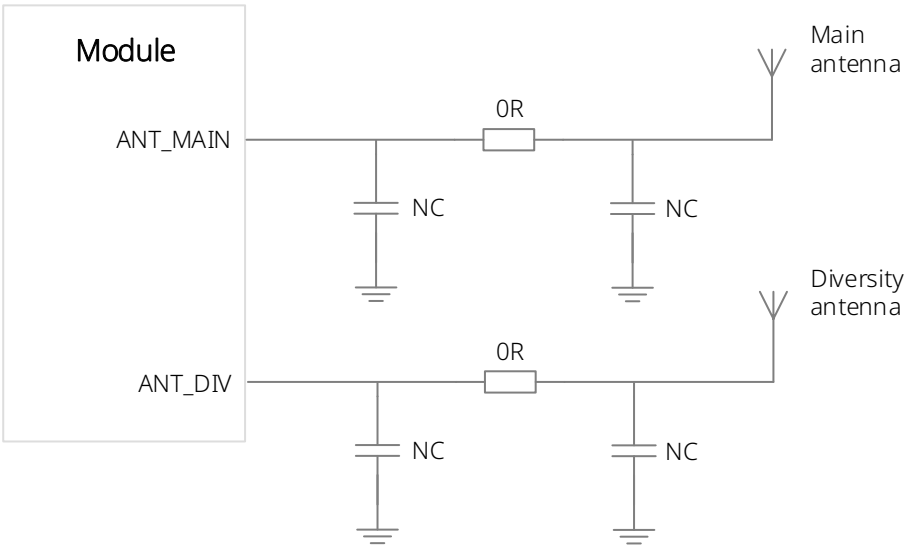

Figure 32. Antenna reference design

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5 Packaging and Storage

5.1 Packaging

For packaging and storage, please refer to *FIBOCOM LC116 Series SMT Design Guide*.

5.2 Storage

Storage conditions (recommended): The temperature is 23±5℃; the relative humidity is 35%-70%.

Storage period (sealed vacuum packaging): 12 months under the recommended storage conditions.

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6 Appendix

6.1 GPRS and EGPRS Encoding Scheme

Table 45. GPRS encoding scheme

Encoding Method	CS-1	CS-2	CS-3	CS-4
Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	- -
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	- -
Data Rate Kb/s	9.05	13.4	15.6	21.4

The GPRS standard stipulates 29 types of GPRS multi-slot modes for mobile stations. The multi-slot class defines the maximum uplink and downlink rates. The expression is 3+1 or 2+2. The first number indicates the number of downlink timeslots, and the second number indicates the number of uplink timeslots. Active timeslots indicate the total number of timeslots that the GPRS device can use for both uplink and downlink communication.

Table 46. Multislot allocation of different classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3

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Multislot Class	Downlink Slots	Uplink Slots	Active Slots
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
33	5	4	6

Table 47. EGPRS modulation and encoding methods

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	GMSK	- -	9.05kbps	18.1kbps	36.2kbps
CS-2	GMSK	- -	13.4kbps	26.8kbps	53.6kbps
CS-3	GMSK	- -	15.6kbps	31.2kbps	62.4kbps
CS-4	GMSK	- -	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.6kbps	35.2kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps

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Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps

6.2 Acronyms and Abbreviations

Table 48. Acronyms and abbreviations

Abbreviations	Definition
bps	Bits Per Second
DRX	Discontinuous Reception
EGSM	Extended GSM900 Band
FDD	Frequency Division Duplexing
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
Imax	Maximum Load Current
LTE	Long Term Evolution
CA	Carrier Aggregation
PCB	Printed Circuit Board
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency

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Abbreviations	Definition
RMS	Root Mean Square
Rx	Receive
TX	Transmit
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

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6.3 Related Documents

- FIBOCOM RF Antenna Application Design Specification
- FIBOCOM ADP-LC116 Development Board User Guide
- FIBOCOM LC116 AT Command Manual
- FIBOCOM FG101_Hardware Guide_EVB
- FIBOCOM LC116 LCC SMT Application Design Specification

6.4 Reference Standards

This product is designed with reference to the following standards:

- 3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1: Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 34.122 V10.1.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V10.6.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit(USAT)

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- 3GPP TS 36.124 V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPP TS 27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

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7. FCC regulatory information

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.

2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).

3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part

15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the
instructions, require that the host product manufacturer must notify to Fibocom Wireless Inc. that they wish to change
the antenna trace design. In this case, a Class II permissive change application is required to be filed

by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new
application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: ZMOLC116LA”

The FCC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

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Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver.

- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter
rules) listed on the grant, and that the host product manufacturer is responsible for compliance to
any other FCC rules that apply to the host not covered by the modular transmitter grant of
certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also
contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that
the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the
OEM integrator is still responsible for testing their end-product for any additional

compliance
requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

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