PERFECT WIRELESS EXPERIENCE

FIBOCOM FG621-LA Series Hardware Guide

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Applicability Type

No.	Product Model	Description
1	FG621-LA-00	LPDDR2 1Gb, SPI NAND 1Gb，support MAIN_ANT、DIV_ANT

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Change History

Version	Author	Reviewer	Approver	Update Date	Description
V0.0.1	Tan Lefan	Hu Wenkai Jin Haibo	Liu Ke	2020-09-29	Initial version
V0.0.2	Hu wenkai	Tan Lefan Jin Haibo	Liu Ke	2021-01-22	CA Combo

Contents

1 Foreword

1.1 Document Introduction

The document describes the electrical characteristics, RF performance, dimensions, and application environment, etc. of FG621-LA series wireless module. With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of FG621-LA series module and develop products.

1.2 Safety Precautions

By following the safety guidelines below, you can ensure your personal safety and help protect the product and work environment from potential damage. Product manufacturers need to communicate the following safety instructions to end users. In case of failure to comply with these safety rules, Fibocom will not be responsible for the consequences caused by the user's misuse.

Road safety first! When you drive, do not use the handheld devices even if it has a hand-free feature. Please stop and call!

Please turn off the mobile device before boarding. The wireless feature of the mobile device is not allowed on the aircraft to prevent interference with the aircraft communication system. Ignoring this note may result in flight safety issue or even violate the law.

When in a hospital or health care facility, please be aware of restrictions on the use of mobile devices. Radio frequency interference may cause medical equipment to malfunction, so it may be necessary to turn off the mobile device.

The mobile device does not guarantee that an effective connection can be made under any circumstances, for example, when there is no prepayment for the mobile device or the (U)SIM is invalid. When you encounter the above situation in an emergency, remember to use an emergency call, while keeping your device turned on and in areas where signal is strong.

Your mobile device receives and transmits RF signals when it is powered on. Radio

interference occurs when it is near televisions, radios, computers, or other electronic devices.

Keep the mobile device away from flammable gases. Turn off the mobile device when you get near to gas stations, oil depots, chemical plants or explosive workplaces. There are potential safety hazards when operating electronic equipment in any potentially explosive area.

2 Product Overview

2.1 Product Introduction

Fibocom FG621-LA series module is a CAT6 module designed based on UNISOC SL8563 platform and can support CA network architecture. FG621-LA series module integrates core devices such as Baseband, Memory, PMIC, Transceiver, and PA, and supports multi-format long-distance communication modes including FDD-LTE, TDD-LTE, and WCDMA. It supports the maximum downlink rate of 300Mbps and the maximum uplink rate of 50Mbps in CA mode. FG621-LA is designed with LGA package and is applicable for various scenarios such as CPE, VR/AR, gateway, internet TV set-top box, and intelligent monitoring.

2.2 Product Specification

Table 2-1 Product specification

Specification		
Operating frequency	FG621-LA-00	LTE FDD: Band2,4,5,7,12,13,28,66
		LTE TDD: Band40
		WCDMA/HSPA+: Band2,4,5
2xCA combination	Intra-band contiguous	CA_2C / CA_5B / CA_7C / CA_7B / CA_12B / CA_B40C CA_66B / CA_66C
	Intra-band non-contiguous	CA_2A-2A / CA_4A-4A / CA_5A-5A / CA_7A-7A / CA_12A-12A CA_B40A-B40A / CA_66A-66A
	Inter-band	CA_B2-B4/B5/B7/B12/B13/B28/B66 CA_B4-B5/B7/B12/B13/B28 CA_B5-B7/B66 CA_B7-B12/B28/B66 CA_B12-B66
Data transmission	LTE FDD	300Mbps DL, 50Mbps UL
	LTE TDD	260Mbps DL, 30Mbps UL
	WCDMA	HSPA/HSPA+: 42Mbps DL, 11Mbps UL
		UMTS: 384 kbps DL/384 kbps UL
Power	3.4V~4.3V (3.8V recommended)	

Specification	
Temperature	Normal operation: -30°C~+75°C①
	Extended operation: -40°C~+85°C②
	Storage: -40°C~+85°C③
Power consumption (TBD)	Power-off leakage current: ≤ 100uA
	Base current: ≤ 2.5mA
	Sleep mode: ≤ 4.5mA
	Idle mode: ≤ 50mA
Physical characteristics	Package: LGA 299Pin
	Size: 39.5mm×37mm×2.6 mm
	Weight: About 8.3g
Interface	
Antenna	Antenna: Main×1, DIV×1
Function interface	(U)SIM 3.0V/1.8V
	USB 2.0×1
	Status Indicator
	UART×4, PCM, I^2C, SDIO, SPI, GPIOs, RESET_N, PWRKEY
	ADC×2
Software	
Protocol stack	IPV4 and IPV6
AT command	3GPP TS 27.007 and 27.005, and proprietary FIBOCOM AT
Firmware update	USB
Voice service	VoLTE, AMR, DTMF and caller ID
SMS service	Point-to-point MO, MT, Text and PDU modes

Note:

① indicates that the module works normally within this temperature range, and the related performance meets the requirements of 3GPP standards.

② indicates that the module works normally within this temperature range, and the baseband and RF functions are normal, but some indicators may exceed the range specified in 3GPP standards. While the temperature returns to the normal operating range of the module, all the indicators of the module meet the requirements of 3GPP standards.

③ indicates the range of the temperature where the module can perform storage without being damaged or powered on.

2.3 Functional Diagram

Functional diagram shows the main hardware features of FG621-LA series module, including baseband and RF features.

Baseband includes:

- CPU
- PMIC
- LPDDR2
- NAND
- USB, (U)SIM, PCM, I^2C, SPI, UART, SDIO, GPIOs, ADCs
- WCDMA /LTE TDD/LTE FDD controller

RF includes:

- RF Transceiver
- RF PA
- RF Switch
- RF filter
- Antenna

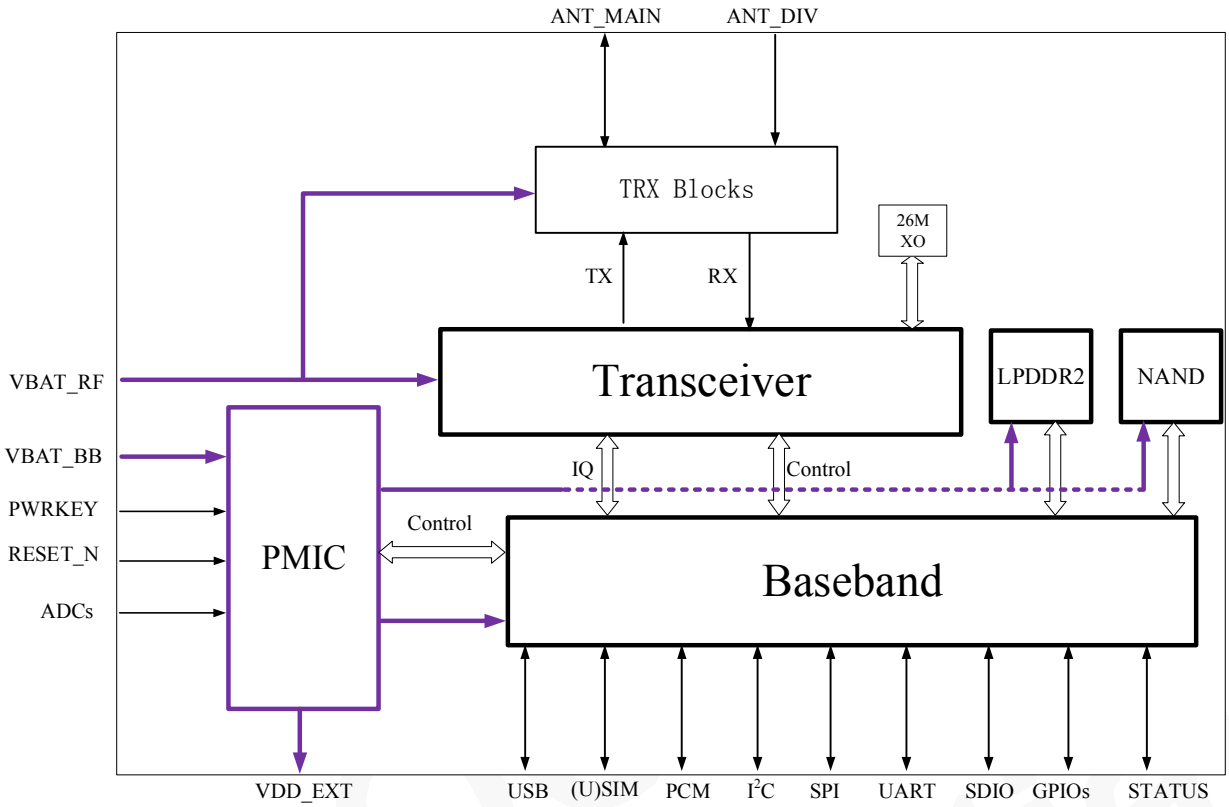

Figure 2-1 Functional diagram

2.4 Development Board

Fibocom provides EVK-FG150-00, ADP-FG621-LA-00 development board to facilitate module's debug and use.

3 Pin Description

3.1 Pin Distribution

FG621-LA series module is available with a total of 299 LGA pins. The top view of the pin distribution is shown in the figure below:

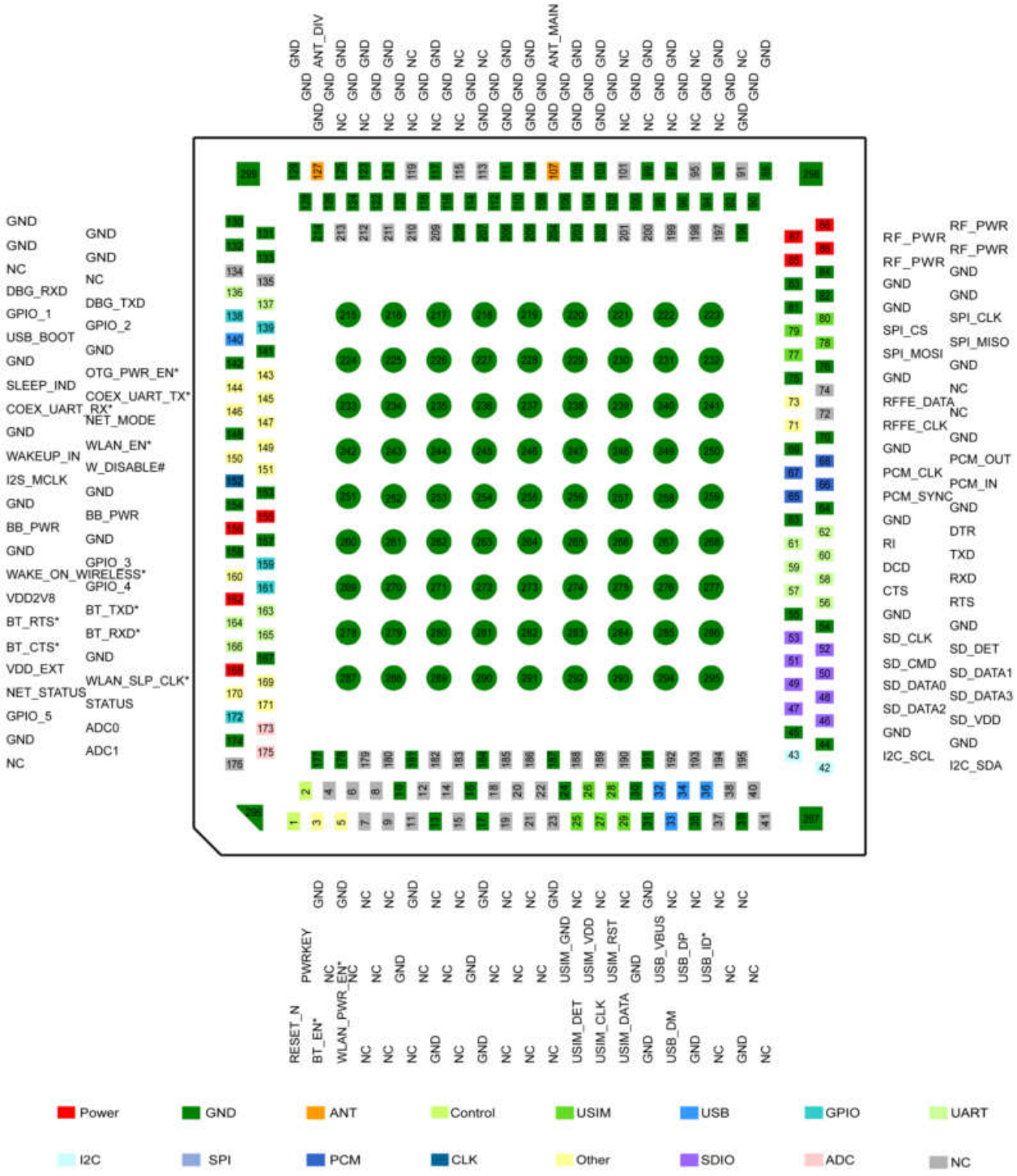

Figure 3-1 Pin distribution (top view)

3.2 Pin Function

The pin function description of FG621-LA series module is shown in the following table:

Table 3-1 Pin function description

Pin#	Pin Name	I/O	Level	Description
1	RESET_N	DI	V_{IL}min=-0.3V V_{IL}max=0.5V V_{IH}max=VBAT_BB	Module reset signal, active low, no need pull up externally
2	PWRKEY	DI	V_{IL}min=-0.3V V_{IL}max=0.5V V_{IH}max=VBAT_BB	Module power-on/off signal, active low, no need pull up externally
3	BT_EN*	DO	V_{OL}max=0.45V V_{OH}min=1.35V	BT function enabling pin, Reserved
5	WLAN_PWR_EN*	DO	V_{OH}min=1.35V V_{OL}max=0.45V	WLAN power supply enabling, Reserved
24	USIM_GND	G	-	(U)SIM ground signal, directly connected to the main ground
25	USIM_DET	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	Detect (U)SIM for hot-swap
26	USIM_VDD	PO	For 1.8V (U)SIM: Vmax=1.9V Vmin=1.7V For 3.0V (U)SIM: Vmax=2.95V Vmin=2.75V $I_O$max=50mA	(U)SIM power supply, the module automatically identifies 1.8V or 3.0V (U)SIM
27	USIM_CLK	DO	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.5V V_{IH}min=1.3V V_{IH}max=2.0V	(U)SIM clock signal line
28	USIM_RST	DO	For 1.8V (U)SIM: V_{OL}max=0.45V V_{OH}min=1.35V For 3.0V (U)SIM: V_{OL}max=0.45V V_{OH}min=2.55V	(U)SIM reset signal line
29	USIM_DATA	DIO	For 1.8V (U)SIM: V_{IL}max=0.5V V_{IH}min=1.3V V_{OL}max=0.45V	(U)SIM data signal line

Pin#	Pin Name	I/O	Level	Description
			V_{OH}min=1.35V For3.0V (U)SIM: V_{IL}max=1.0V V_{IH}min=1.95V V_{OL}max=0.45V V_{OH}min=2.55V	
32	USB_VBUS	PI	Vmax=5.25V Vmin=3.0V Vnorm=5.0V	USB plug detection
33	USB_DM	DIO	Conform to USB2.0 standard specification	USB differential data signal (-)
34	USB_DP	DIO	Conform to USB2.0 standard specification	USB differential data signal (+)
36	USB_ID*	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	OTG identification signal, Reserved
42	I2C_SDA	OD	1.8V domain	I^2C interface data signal, pulled up inside the module
43	I2C_SCL	OD	1.8V domain	I^2C interface clock signal, pulled up inside the module
46	SD_VDD	PO	For 1.8V SD: Vmax=1.9V Vmin=1.75V For 3.0V SD: Vmax=3.15V Vmin=2.75V IOmax=400mA	SD card power supply
47	SD_DATA2	DIO	For1.8V SD: V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.3V V_{IH}max=2.0V For 3.0V SD: V_{OL}max=0.35V V_{OH}min=2.15V V_{IL}min=-0.3V V_{IL}max=0.7V V_{IH}min=1.8V V_{IH}max=3.15V	SD card data signal
48	SD_DATA3	DIO		SD card data signal
49	SD_DATA0	DIO		SD card data signal
50	SD_DATA1	DIO		SD card data signal
51	SD_CMD	DO		SD card command signal
53	SD_CLK	DO		SD card clock signal

Pin#	Pin Name	I/O	Level	Description
52	SD_ DETECT	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	SD card hot-swap detection signal
56	RTS	DO	V_{OL}max=0.45V V_{OH}min=1.35V	Request to send data, Reserved
57	CTS	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	Clear to send, Reserved
58	RXD	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	Module Receive data, Reserved
59	DCD	DO	V_{OL}max=0.45V V_{OH}min=1.35V	Module output carrier detection, Reserved
60	TXD	DO	V_{OL}max=0.45V V_{OH}min=1.35V	Module Transmit data, Reserved
61	RI	DO	V_{OL}max=0.45V V_{OH}min=1.35V	Module output ring indicator
62	DTR	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	Ready, sleep mode control, Reserved
65	PCM_SYNC	DIO	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	PCM synchronization signal
66	PCM_IN	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	PCM input signal
67	PCM_CLK	DO	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	PCM clock signal
68	PCM_OUT	DO	V_{OL}max=0.45V V_{OH}min=1.35V	PCM output signal
71	RFFE_CLK	DO	V_{OL}max=0.45V V_{OH}min=1.35V	RF MIPI clock signal, Reserved
73	RFFE_DATA	DIO	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V	RF MIPI data signal, Reserved

Pin#	Pin Name	I/O	Level	Description
			V_{IH}min=1.2V V_{IH}max=2.0V	
77	SPI_MOSI	DO	V_{OL}max=0.45V V_{OH}min=1.35V	SPI output signal
78	SPI_MISO	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	SPI input signal
79	SPI_CS	DO	V_{OL}max=0.45V V_{OH}min=1.35V	SPI Chip Selection signal
80	SPI_CLK	DO	V_{OL}max=0.45V V_{OH}min=1.35V	SPI clock signal
85~88	VBAT_RF	PI	Vmax=4.3V Vmin=3.4V Vnorm=3.8V	RF power input (3.4V~4.3V)
107	ANT_MAIN	AIO	-	Main antenna
127	ANT_DIV	AI	-	Diversity antenna
136	DBG_RXD	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	DEBUG serial port receiving
137	DBG_TXD	DO	V_{OL}max=0.45V V_{OH}min=1.35V	DEBUG serial port sending
138	GPIO_1	DIO	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	GPIO
139	GPIO_2	DIO	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	GPIO
140	USB_BOOT	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	Emergency download, active low, recommended to reserve test point
143	OTG_PWR_EN*	DO	V_{OL}max=0.45V V_{OH}min=1.35V	OTG power enabling, Reserved
144	SLEEP_IND	DO	V_{OL}max=0.45V V_{OH}min=1.35V	Sleep status indicator
145	COEX_UART_TX*	DO	V_{OL}max=0.45V V_{OH}min=1.35V	LTE/WLAN shared serial port sending signal line,

Pin#	Pin Name	I/O	Level	Description
				Reserved
146	COEX_UART_RX*	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	LTE/WLAN shared serial port sending signal line, Reserved
147	NET_MODE	DO	V_{OL}max=0.45V V_{OH}min=1.35V	Module network state indicate
149	WLAN_EN*	DO	V_{OL}max=0.45V V_{OH}min=1.35V	Wake up WLAN module, Reserved
150	WAKEUP_IN	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	External device wakeup module, active low by default, configurable by software
151	W_DISABLE#	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	Module flight mode control, pull up by default, low level can make the module enter flight mode
152	I2S_MCLK	DO	V_{OL}max=0.45V V_{OH}min=1.35V	I2S output clock signal
155,156	VBAT_BB	PI	Vmax=4.3V Vmin=3.4V Vnorm=3.8V	Baseband power input (3.4V~4.3V)
159	GPIO_3	DIO	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	GPIO
160	WAKE_ON_WIRELESS*	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	WLAN chip wakeup signal for the module, Reserved
161	GPIO_4	DIO	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	GPIO
162	VDD_2V8	PO	Vnorm=2.8V $I_O$max=200mA	2.8V voltage output
163	BT_TXD*	DO	V_{OL}max=0.45V V_{OH}min=1.35V	Bluetooth serial port

Pin#	Pin Name	I/O	Level	Description
				sends data signal, Reserved
164	BT_RTS*	DO	V_{OL}max=0.45V V_{OH}min=1.35V	Bluetooth serial port requests to send data signal, Reserved
165	BT_RXD*	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	Bluetooth serial port receives data signal, Reserved
166	BT_CTS*	DI	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	Bluetooth serial port clears to send data signal, Reserved
168	VDD_EXT	PO	Vnorm=1.85V $I_O$max=50mA	1.85V power output
169	WLAN_SLP_CLK*	DO	V_{OL}max=0.45V V_{OH}min=1.35V	WLAN sleep clock signal, Reserved
170	NET_STATUS	DO	V_{OL}max=0.45V V_{OH}min=1.35V	Module network state indicate (by default).
171	STATUS	DO	V_{OL}max=0.45V V_{OH}min=1.35V	Module network state indicate
172	GPIO_5	DIO	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	GPIO
173	ADC0	AI	Input voltage ranged from 0 to 1.2V	Analog to digital converter input port 0
175	ADC1	AI	Input voltage ranged from 0 to 1.2V	Analog to digital converter input port 1
10,13,16,17,24,30,31,35,39,44,45,54,55,63,64,69,70,75,76,81~84,89,90,92~94,96~100,102~106,108~112,114,116~118,120~126,128~133,141,142,1	GND	G	-	Ground

Pin#	Pin Name	I/O	Level	Description
48,153,154,157,158,167,174,177,178,181,184,187,191,196,202~208,214~299				
4,6~9,11,12,14,15,18~23,37,38,40,41,72,74,91,95,101,113,115,119,134,135,176,179,180,182,183,185,186,188~190,192~195,197~201,209~213	NC	-	-	-

Note:

Keep the unused pins floating.

Table 3-2 I/O parameter description

Type	Description
PI	Power input
PO	Power output
DI	Digital input
DO	Digital output
DIO	Digital input/output
AI	Analog input
AO	Analog output
AIO	Analog input/output
OD	Open drain

4 Electrical Characteristics

4.1 Power

The following table shows the power interface of FG621-LA series module.

Table 4-1 Power interface

Pin Name	I/O	Pin#	Description
VBAT_RF	PI	85,86,87,88	Module power supply, 3.4V~4.3V, nominal value 3.8V
VBAT_BB	PI	155,156	Module power supply, 3.4V~4.3V, nominal value 3.8V
VDD_EXT	PO	168	Module digital level, 1.85V output, 50mA
VDD_2V8	PO	162	Level output to external circuit, 2.8V output, 200mA
GND	G	10,13,16,17,24,30,31,35,39,44,45,54,55,63,64,69,70,75,76,81~84,89,90,92~94,96~100,102~106,108~112,114,116~118,120~126,128~133,141,142,148,153,154,157,158,167,174,177,178,181,184,187,191,196,202~208,214~299	All GND pins must be grounded

Note:

In this document, VBAT includes VBAT_RF and VBAT_BB. The supply voltage of VBAT_RF and VBAT_BB must be consistent.

4.2 Power Supply

FG621-LA series module needs to be powered by the VBAT pin. The recommended power design is shown in Figure 4-1:

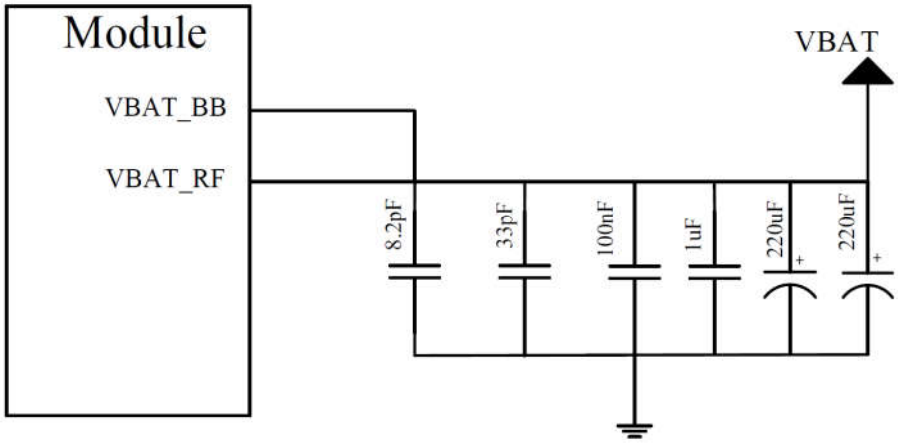

Figure 4-1 Recommended power design

Power filter capacitor design is shown in the following table:

Table 4-2 Filter capacitors design of power supply

Recommended Capacitor	Application	Description
220uF x 2	Regulating capacitor	Reduce power fluctuations during module operation, low ESR Capacitor is required, and the total capacitance should not be less than 440uF. The current driving capacity of VBAT must be not less than 2.0A.
1uF,100nF	Digital signal noise	Filter clock and digital signal interference
33pF	850MHz/900 MHz bands	Filter low band RF interference
8.2pF	1800/1900/2100/2300/2500/2600 MHz bands	Filter middle/high band RF interference

The power stability can ensure the normal operation of FG621-LA series module. Special attention requires when designing circuit that the power supply ripple limit for the module is no more than 300mV (the circuit ESR < 100mΩ). When the module is operating in maximum power consumption, the power voltage needs to be at least 3.4V. Otherwise, the module may power off or restart. When the module is operating in Burst transmit state, the power limit is shown in Figure 4-2:

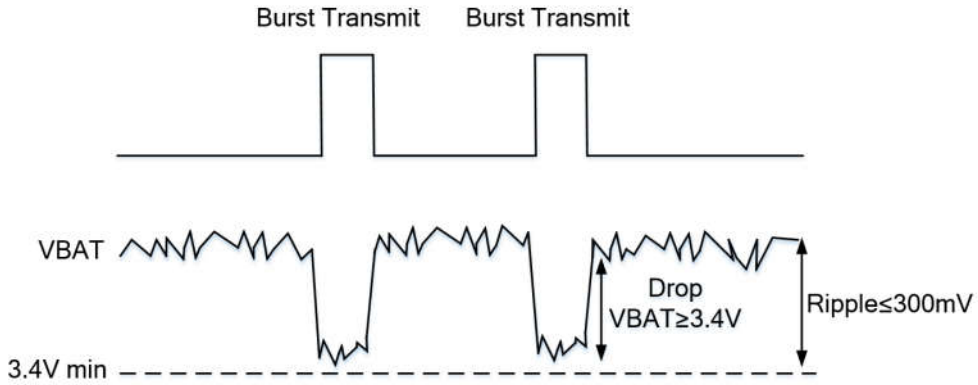

Figure 4-2 Power limit

4.3 Power Output

FG621-LA series module outputs a 1.85V voltage through the VDD_EXT for the use of the internal digital circuit of module. The voltage is the logic level of the module and can be used to indicate module power-on/off, or for external low current (< 50mA) circuits. FG621-LA series module outputs a 2.8V level through the VDD_2V8 for the use of the internal RF or other circuits, with an output current of < 200mA. Leave the signal floating if no use. The logic level of VDD_EXT and VDD_2V8 is defined as follows:

Table 4-3 VDD_EXT and VDD_2V8 logic level

Parameter	Min	Typ	Max	Unit
VDD_EXT	1.75	1.85	1.95	V
VDD_2V8	2.7	2.8	2.9	V

4.4 Power Consumption

The power consumption of FG621-LA series module measured at 3.8V power supply is shown in the following table. For AT commands used for USB sleep and wakeup, please refer to section 6.2:

Table 4-4 Power consumption

Parameter	Mode	Condition	Average Current Typ. (mA)
Ioff	Power off	Power-off	0.085
I_{sleep}	WCDMA	DRX8(USB sleep)	2.9
	FDD-LTE	Paging Cycle #64(USB sleep)	4.2
	FDD-LTE	Paging Cycle #256(USB sleep)	2.7
	TDD-LTE	Paging Cycle #64(USB sleep)	4.2

Parameter	Mode	Condition	Average Current Typ. (mA)
	TDD-LTE	Paging Cycle #256(USB sleep)	2.7
	Radio Off	AT+CFUN=0(USB sleep)	2
I_{idle}	WCDMA	DRX6(USB wakeup)	41
		DRX8(USB wakeup)	40
		DRX9(USB wakeup)	39
	FDD-LTE	Paging Cycle #32(USB wakeup)	43
		Paging Cycle #64(USB wakeup)	42
		Paging Cycle #128(USB wakeup)	41
		Paging Cycle #256(USB wakeup)	40
	TDD-LTE	Paging Cycle #32(USB wakeup)	43
		Paging Cycle #64(USB wakeup)	42
		Paging Cycle #128 USB wakeup)	41
		Paging Cycle #256(USB wakeup)	40
$I_{WCDMA-RMS}$	WCDMA	Band2 @+23.5dBm	700
		Band4 @+23.5dBm	700
		Band5 @+23.5dBm	650
$I_{LTE-RMS}$ (10MHz 1RB)	FDD-LTE	Band2 @+23dBm	800
		Band4 @+23dBm	750
		Band5 @+23dBm	700
		Band7 @+23dBm	850
		Band12 @+23dBm	800
		Band13 @+23dBm	700
		Band28 @+23dBm	750
	TDD-LTE	Band40 @+23dBm	400

In 2CA mode, The maximum power consumption combination of fg621 under the maximum bandwidth is shown in the table below.

Table 4-5 2CA power consumption

2CA Typical Combination	Condition (Tx band FRB) Data Transfer	Typical Current (mA)
2A-4A	Band 2 @+21dBm	750
4A-7A	Band 4 @+21dBm	750
5A-7A	Band 5 @+21dBm	700
7A-2A	Band 7 @+21dBm	800
12A-7A	Band 12 @+21dBm	750
13A-7A	Band 13 @+21dBm	750
28A-7A	Band 28 @+21dBm	750
40C	Band 40 @+21dBm	330

5 Functional Interface

5.1 Control Interface

Two control signals are used to open, shut down and reset the module. Pin definition is shown in the following table:

Table 5-1 Control signal

Pin Name	I/O	Pin#	Description
RESET_N	DI	1	When the module is in operating mode, pull down RESET_N for at least 2.1s (3s-8s recommended), and then release it, the module is reset. Internally pulled up.
PWRKEY	DI	2	When the module is in power-off mode, pull down PWRKEY for at least 1.6s (2s-3s recommended), and then release it, the module will power on, when the module is in operating mode, pull down PWRKEY for at least 2.1s (3s-8s recommended), and then release it, the module will power off.

5.1.1 Power-on/Off

5.1.1.1 Power-on

When FG621-LA series module is in power-off mode, pull down PWRKEY pin for at least 1.6s, the module will power on, it is recommended to use OC/OD drive circuit to control PWRKEY pin. The OC drive reference circuit is shown as follows:

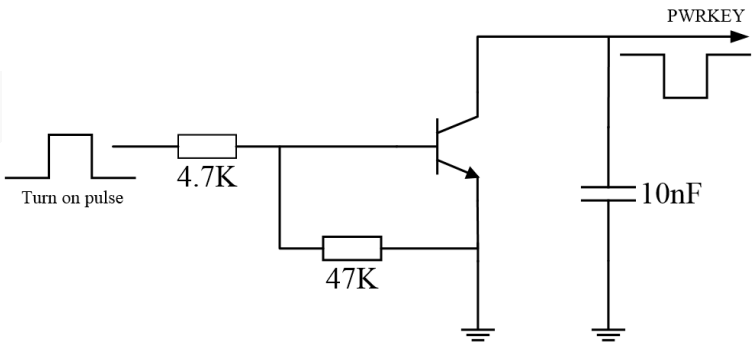

Figure 5-1 OC drive power-on reference circuit

The other way to control PWRKEY pin is to use a button switch, a TVS (ESD9X5VL-2/TR recommended) should be located close to the button for ESD protection. The reference circuit is shown in Figure 5-2:

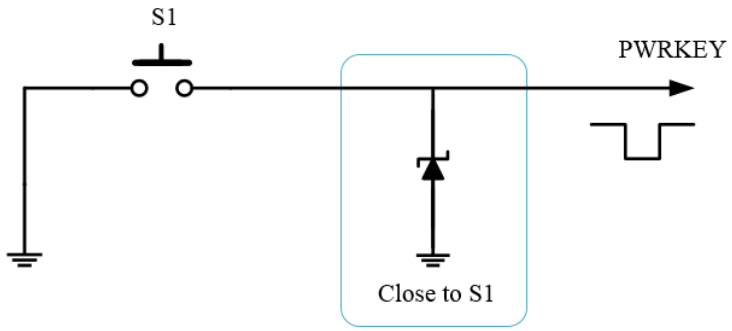

Figure 5-2 Button switch power-on reference circuit

The power-on timing is shown in the following figure:

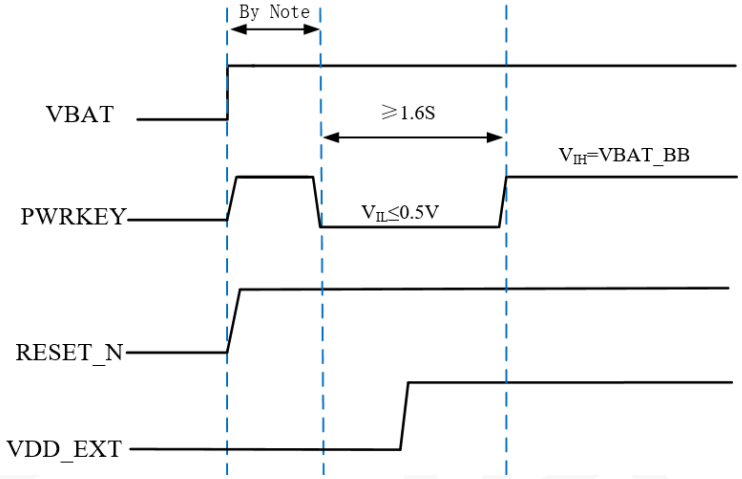

Figure 5-3 Power-on timing

Note:

Before pulling down PWRKEY pin, make sure the VBAT voltage is stable. It is recommended that the time interval between powering up VBAT and pulling down PWRKEY pin should be not less than 30ms. It takes about 30s to power-on, Other operations such as power-off, reset, etc. can be performed only after the complete power-on.

5.1.1.2 Shutdown

The module supports three shutdown modes as shown in Table 5-2.

Table 5-2 Shutdown modes

Shutdown Mode	Shutdown Method	Applicable Scenario
Low voltage shutdown	When VBAT voltage is too low or powers down, the module will shut down	The module does not shut down through normal process, i.e. does not log out from the base station

Shutdown Mode	Shutdown Method	Applicable Scenario
Hardware shutdown	Pull down PWRKEY for at least 2.1s, 3s~8s recommended	Hardware normal shutdown
AT command shutdown	AT+CPWROFF	Software normal shutdown

Note:

1. When the module is working properly, do not cut off the power of the module immediately to avoid damaging internal flash. It is strongly recommended to shut down the module by PWRKEY pin or AT command before cutting off the power supply.
2. When using the AT command to shut down the module, make sure that the PWRKEY pin is always at the high level after the shutdown command is executed, otherwise the module will automatically power on again.
3. During the shutdown process, it takes about 6 seconds from the release of PWRKEY to the complete power-off of VDD_EXT. Other operations such as power-on, reset, etc. can be performed only after the complete power-off.

   The shutdown timing is shown as follows:

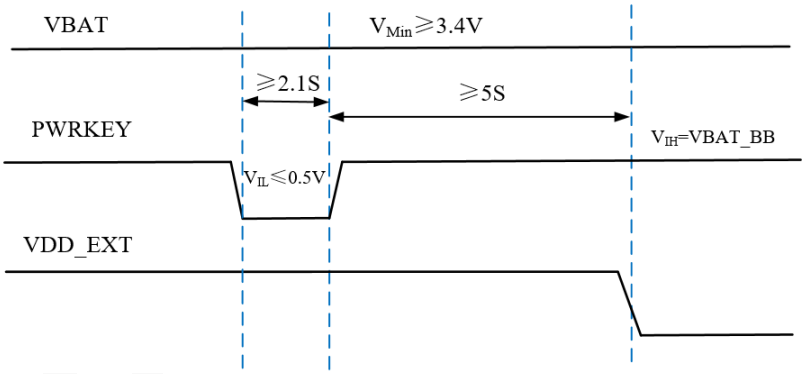

Figure 5-4 Shutdown timing

5.1.2 Reset

FG621-LA series module can be reset by hardware and software.

Table 5-3 Reset modes

Reset Mode	Reset Method
Hardware reset	Pull down RESET_N pin for more than 2s, then release it, 3s~8s recommended
Software reset	Send AT command AT+CFUN=15

Clients can control RESET_N pin by OC/OD drive circuits and button switch. The reference circuits are

shown in Figure 5-5 and Figure 5-6, respectively:

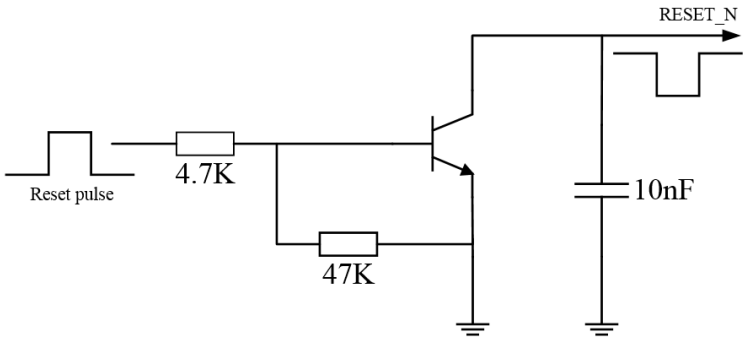

Figure 5-5 OC driven reset reference circuit

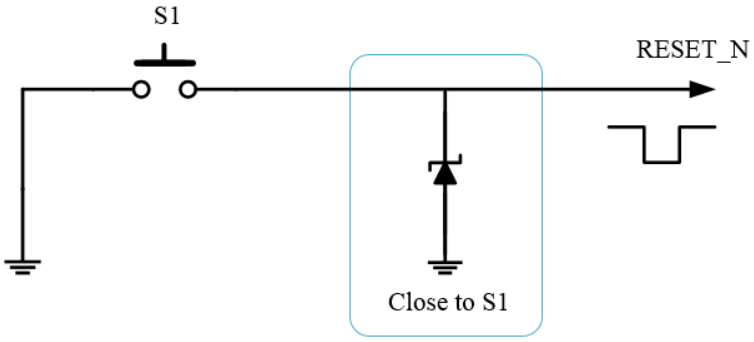

Figure 5-6 Button reset reference circuit

The reset timing is shown as follows:

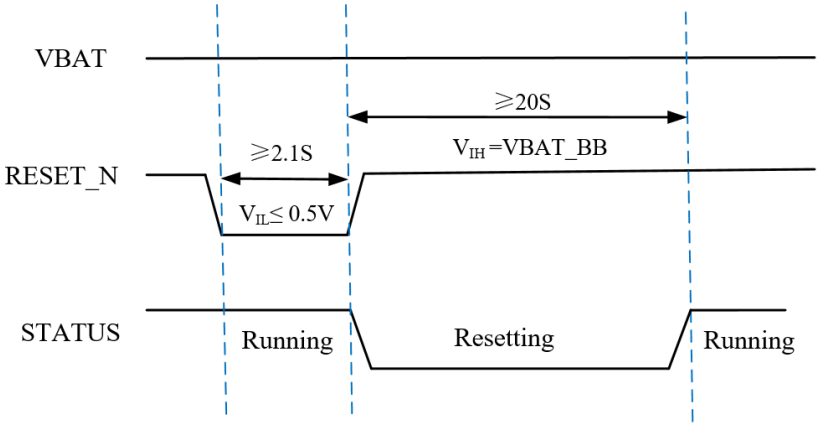

Figure 5-7 Reset timing

Note:

RESET_N is a sensitive signal, so it is recommended to add a regulator capacitor close to the module. The PCB layout should be kept away from the RF interference and protected by Ground. At the same time, avoid routing on the edge and surface of PCB (to avoid module reset caused by ESD).

5.2 Network Status Indication Interface

FG621-LA series module provides three network status indicate pins. Pin 170 is network status indicator

by default, AT commands AT+LEDCFG can switch to pin147 or pin171, table 5-4 is the pin definition.

Table 5-4 Network status indication

Pin Name	I/O	Pin#	Description
STATUS	DO	171	Network status indicator
NET_MODE	DO	147	Network status indicator(by default)
NET_STATUS	DO	170	Network status indicator

Status indicator driven by network status indicator interface is used to describe the network status of the module. FG621-LA series module network indicator is described as follow table:

Table 5-5 Network indicator light work status

Mode	Module Network Indicator Pin Level Status	Indicator Light On/Off Status	Description
1	600ms High / 600ms Low	Quick flashing 600ms on / 600ms off	No SIM card SIM PIN Registering network (T<15S) Register network failed
2	3000ms High / 75ms Low	Slow flashing 3000ms on / 75ms off	Standby
3	75ms High / 75ms Low	Speed flashing 75ms on / 75ms off	Data link established
4	Low	Off	Voice call
5	High	On	Sleep

FG621-LA series modules' network status indicator reference circuit is shown in the following figure:

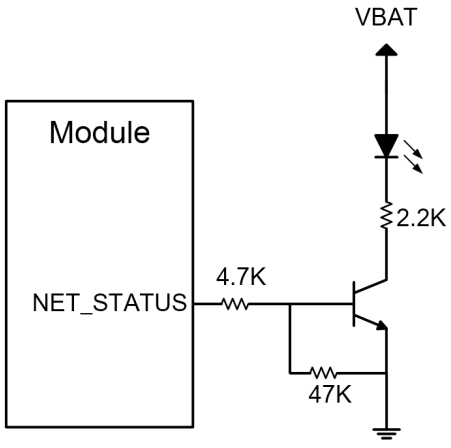

Figure 5-8 Network indication light reference circuit

5.3 (U)SIM Card Interface

FG621-LA series module has built-in (U)SIM card interface, and supports 1.8V and 3.0V (U)SIM card.

5.3.1 (U)SIM Pin Definition

(U)SIM pin definition is shown in the following table:

Table 5-6 (U)SIM pin definition

Pin Name	I/O	Pin#	Description
USIM_DET	DI	25	Detect (U)SIM card for Hot-plug
USIM_VDD	PO	26	(U)SIM Power
USIM_DATA	IO	29	(U)SIM data signal
USIM_CLK	DO	27	(U)SIM clock signal
USIM_RST	DO	28	(U)SIM reset signal

5.3.2 (U)SIM Interface Circuit

5.3.2.1 (U)SIM Card Connector with Card Detection Signal

(U)SIM card connector should be selected for (U)SIM design. It is recommended to use (U)SIM card connector with hot plug detection function (Recommended model: SIM016-8P-220P).

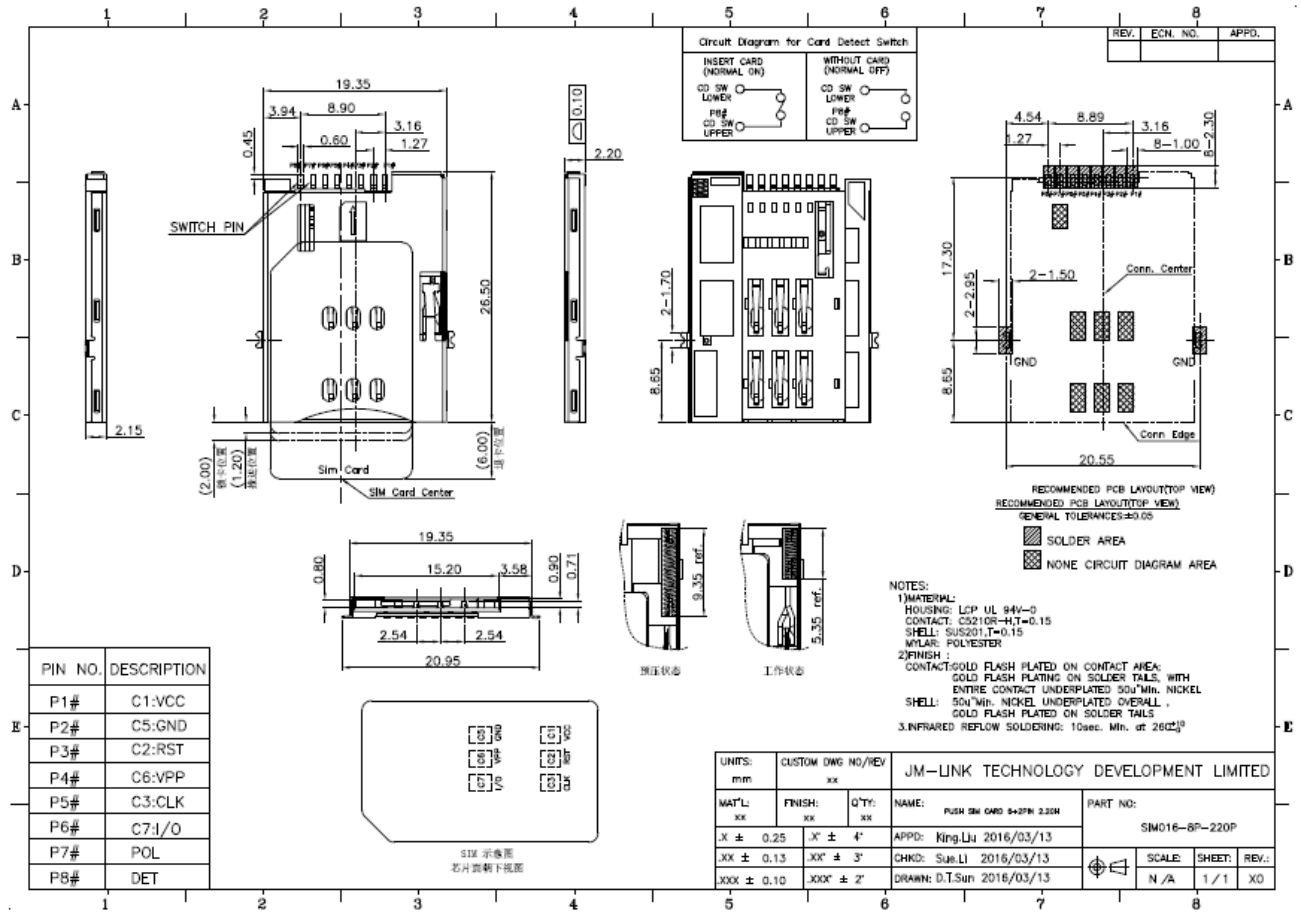

Figure 5-9 (U)SIM card connector (SIM016-8P-220P)

SIM016-8P-220P card connector, DET and POL are short connected when the card is inserted, DET and POL are disconnected when there is no card. The following is the reference design circuit. When (U)SIM card is inserted, USIM_DET pin is in high level, when (U)SIM card is removed, USIM_DET pin is in low level.

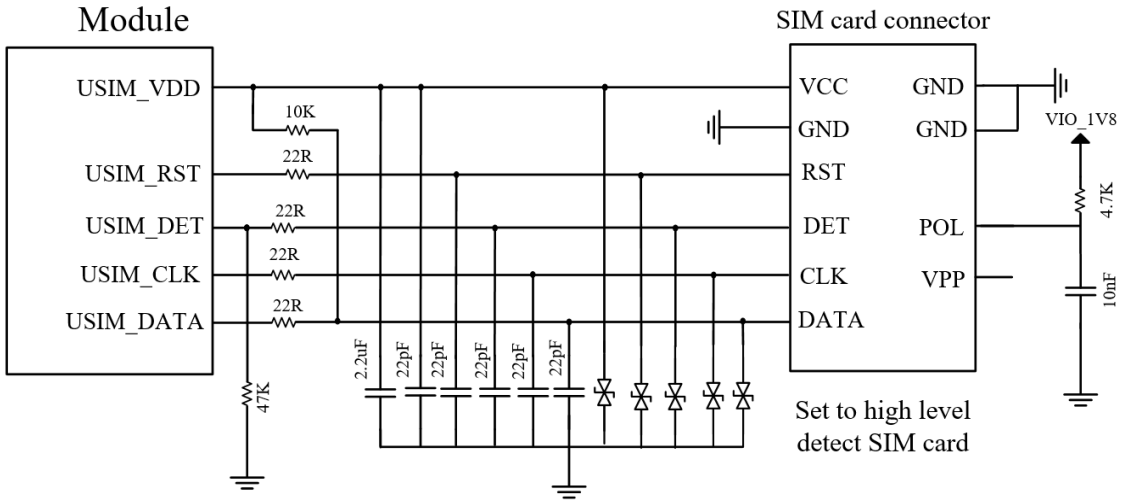

Figure 5-10 (U)SIM card connector with detection signal reference circuit

5.3.2.2 (U)SIM Card Connector without Detection Signal

When using an (U)SIM card connector without detection signal, USIM_DET pin must be left floating, and at the same time, the hot plug function should be disabled using AT command. The reference circuit is shown in the figure below.

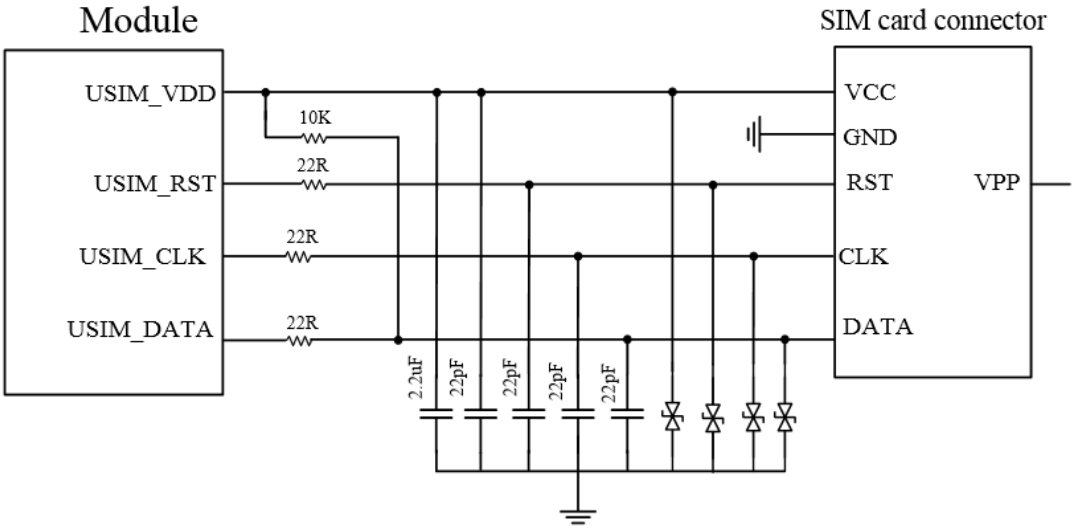

Figure 5-11 (U)SIM card connector without detection signal reference circuit

5.3.3 (U)SIM Hot Plug

FG621-LA series module supports (U)SIM hot plug function, and it determines the insertion and removal of (U)SIM card by detecting the USIM_DET pin state.

The (U)SIM hot plug function can be configured by the “AT+MSMPD” command, and the AT commands are shown in the following table:

Table 5-7 (U)SIM hot plug function configuration

AT command	(U)SIM hot plug detection	Function description
AT+MSMPD=1	Enabled	(U)SIM hot plug detection is enabled by default.
AT+MSMPD=0	Disabled	(U)SIM hot plug detection function is disabled. The module reads the (U)SIM card upon power-on, and does not detect the USIM_DET state.

After the hot plug detection function of the (U)SIM card is enabled, if USIM_DET is in high level, the module will detect the (U)SIM card insertion and execute card initialization program. After reading the (U)SIM card information, the module will register network. When the USIM_DET is in low level, the module detects (U)SIM card removal, and it will not read the (U)SIM card.

Note:

The USIM_DET pin is active high by default, and can be switched to active low by AT command.

Table 5-8 USIM_DET effective level switched

AT command	Function description
AT+GTSET="SIMPHASE",1	Default, high level detection
AT+GTSET="SIMPHASE",0	Low level detection

5.3.4 (U)SIM Design Requirements

(U)SIM card circuit design should meet EMC standards and ESD requirements, and at the same time, should improve anti-interference ability to ensure that the (U)SIM card can work stably. The design needs to strictly follow the following rules:

- (U)SIM card connector is placed as close to the module as possible, away from the RF antenna, DCDC power, clock signal lines and other strong interference sources.
- It is recommended to use (U)SIM card connector with metal shielding shell to improve anti-interference ability.
- The length of signal line from the module to the (U)SIM card connector should not exceed 100mm. Longer signal line reduces signal quality.
- USIM_CLK and USIM_DATA signals should be ground protected to avoid mutual interference. If it is difficult to do so, (U)SIM signals need to be ground protected as a set.
- The filter capacitor and ESD device of (U)SIM card signal line should be placed close to the (U)SIM card connector.
- The total capacitance of ESD equivalent capacitor and parallel capacitor should be less than 47pF.
- USIM_DATA should be pulled up to USIM_VDD with a 10K resistor.

5.4 USB Interface

FG621-LA series modules support USB2.0, and are compatible with USB High-Speed (480Mbits/s) and USB Full-Speed (12Mbits/s). Refer to the "Universal Serial Bus Specification 2.0" for USB Bus timing and electrical characteristics of modules. USB pin definition is as follow:

Table 5-9 USB pin definition

Pin Name	I/O	Pin#	Description
USB_DP	IO	34	USB differential data +
USB_DM	IO	33	USB differential data -
USB_VBUS	PI	32	USB Plug detect

For more information about the USB 2.0 specification, please visit http://www.usb.org/home.

Note:

Since the module supports USB 2.0 High-Speed, TVS equivalent capacitance on the USB_DM/DP differential signal line is required to be less than 1pF, and a 0.5pF TVS is recommended. It is recommended to connect a 0Ω resistor to USB_DM/DP differential line in series.

USB_DM and USB_DP are high-speed differential signal lines, which can achieve the maximum transmission rate of 480Mbits/s, and must follow the rules below in PCB Layout:

- The impedance of USB_DM and USB_DP signal line should be controlled in 90Ω.
- USB_DM and USB_DP signal lines shall be parallel and equal in length, and avoid the right-angle route.
- USB_DM and USB_DP signal lines are routed on the signal layer closest to the ground layer, and the lines shall be grounded.

5.5 UART Interface

FG621-LA series module provides debug serial port, which supports 115200bps baud rate for debugging and problem analysis. The following table is the description of debug serial port pins:

Table 5-10 Pin definition of debug serial port

Pin Name	I/O	Pin#	Description
DBG_RXD	DI	136	Module Receive data
DBG_TXD	DO	137	Module Transmit data

5.6 ADC Interface

FG621-LA series module supports two-channel ADC interface, 12 bit. The use of AT+MMAD command can read the value of ADC interface. The voltage range of ADC interface is 0V~1.2V.

Table 5-11 ADC pin definition

Pin Name	I/O	Pin#	Description
ADC0	AI	173	Analog to digital converter interface 0
ADC1	AI	175	Analog to digital converter interface 1

Note:

Ground isolation is recommended for ADC layout to improve ADC voltage measurement accuracy.

5.7 I2C Interface

FG621-LA series module supports one I2C interface, applying the standard I2C Specification, version 3.0. The I2C signal has been pulled up inside the chip, so there is no need to pull it up outside.

Table 5-12 I2C pin definition

Pin Name	I/O	Pin#	Description
I2C_SDA	42	DIO	I^2C interface data signal, pulled up inside the module
I2C_SCL	43	DO	I^2C interface data signal, pulled up inside the module

5.8 PCM Digital Audio Interface

FG621-LA series module provides a digital audio interface (PCM) for communication with digital audio devices such as an external Codec.

5.8.1 Support Model

Table 5-13 Support model of PCM

Product Model	Description
FG621-LA-00 series	Support

5.8.2 PCM Interface Definition

The interface signals include the transmission clock PCM_CLK, the frame synchronization signal PCM_SYNC, and the input and output PCM_DIN/PCM_DOUT.

Table 5-14 PCM interface definition

Pin Name	I/O	Pin#	Description
PCM_SYNC	IO	65	PCM data synchronization signal
PCM_IN	DI	66	PCM data input
PCM_CLK	IO	67	PCM clock
PCM_OUT	DO	68	PCM data output

5.8.3 PCM Interface Description

Table 5-15 PCM interface description

Pin Name	Frequency	Duty Cycle	Coded Format	Operating Mode	Description
PCM_CLK	2.048MHz	50%	16bit Linermono	Module serves as master, supporting PCM as slave	PCM clock
PCM_OUT	-	-			PCM data output
PCM_IN	-	-			PCM data input
PCM_SYNC	8KHz	Short pulse			PCM data synchronization signal (falling edge sampling)

FG621-LA series module adopts the above configuration by default. For any adjustment, please contact

Fibocom technical support.

5.8.4 PCM Signal Description

FG621-LA series module provides PCM signal using domestic mainstream European E1 standard. PCM_CLK is encoded by 2.048MHz clock and 16bit linear format. PCM_SYNC is an 8kHz short pulse (488ns).

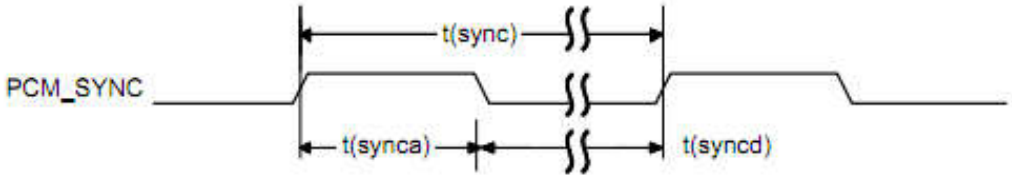

Figure 5-12 PCM_SYNC timing

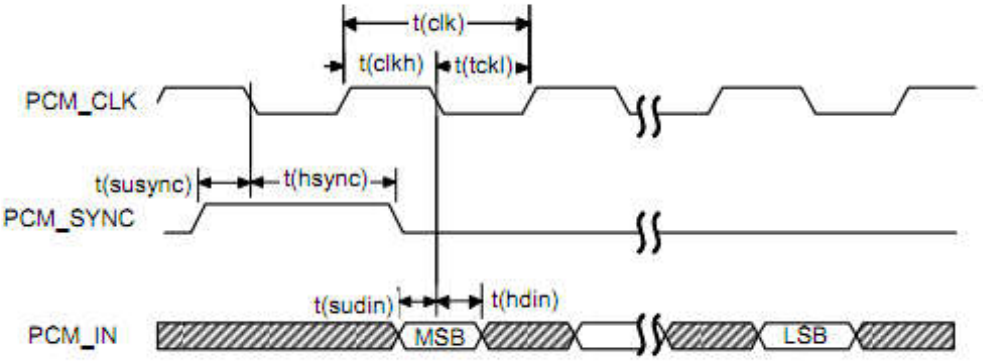

Figure 5-13 PCM_CODEC to FG621-LA timing

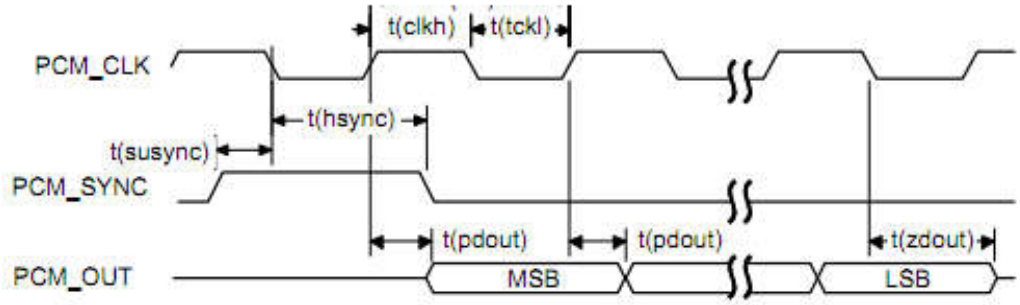

Figure 5-14 FG621-LA to PCM_CODEC timing

Table 5-16 CODEC Timing Parameters

Timing		Min	Typ	Max	Unit
t(sync)	PCM_SYNC cycle	–	125	–	μs
t(synca)	PCM_SYNC high level time	–	488	–	ns

Timing		Min	Typ	Max	Unit
t(syncd)	PCM_SYNC low level time	–	124.5	–	μs
t(clk)	PCM_CLK cycle	–	488	–	ns
t(clkh)	PCM_CLK high level time	–	244	–	ns
t(clkl)	PCM_CLK low level time	–	244	–	ns
t(susync)	PCM_SYNC setup time	–	122	–	ns
t(sudin)	PCM_DIN setup time	60	–	–	ns
t(hdin)	PCM_DIN hold time	10	–	–	ns
t(pdout)	PCM_DOUT setup start time	–	–	60	ns
t(zdout)	PCM_DOUT hold end time	–	160	–	ns

5.9 SD Interface

FG621-AE-00 module supports one-channel SD interface. The standard is as follows:

Physical Layer Specification version 3.0, SDIO Card Specification version 3.0

5.9.1 SD Pin Definition

SD pin definition is shown in the following table:

Table 5-17 SD pin definition

Pin Name	I/O	Pin#	Description
SD_VDD	PO	46	SDIO power supply, 3V by default
SD_DATA0	IO	49	SDIO data signal bit0
SD_DATA1	IO	50	SDIO data signal bit1
SD_DATA2	IO	47	SDIO data signal bit2
SD_DATA3	IO	48	SDIO data signal bit3
SD_CMD	DO	51	SDIO command signal
SD_CLK	DO	53	SDIO clock signal
SD_ DETEC	DI	52	SDIO hot plug detection signal

5.9.2 SD Interface Routing Rules

The length of signal lines should be equal to or less than 50mm, and the difference in the length of clock signal and data signal lines should be equal to or less than 2mm.

5.9.3 SD Interface Application Circuit

For SD application circuit, please refer to the following figure. SD card connector detect pin is floating when no card is inserted, and is short connected to ground when a card is inserted. Detect SD card

insertion at low level.

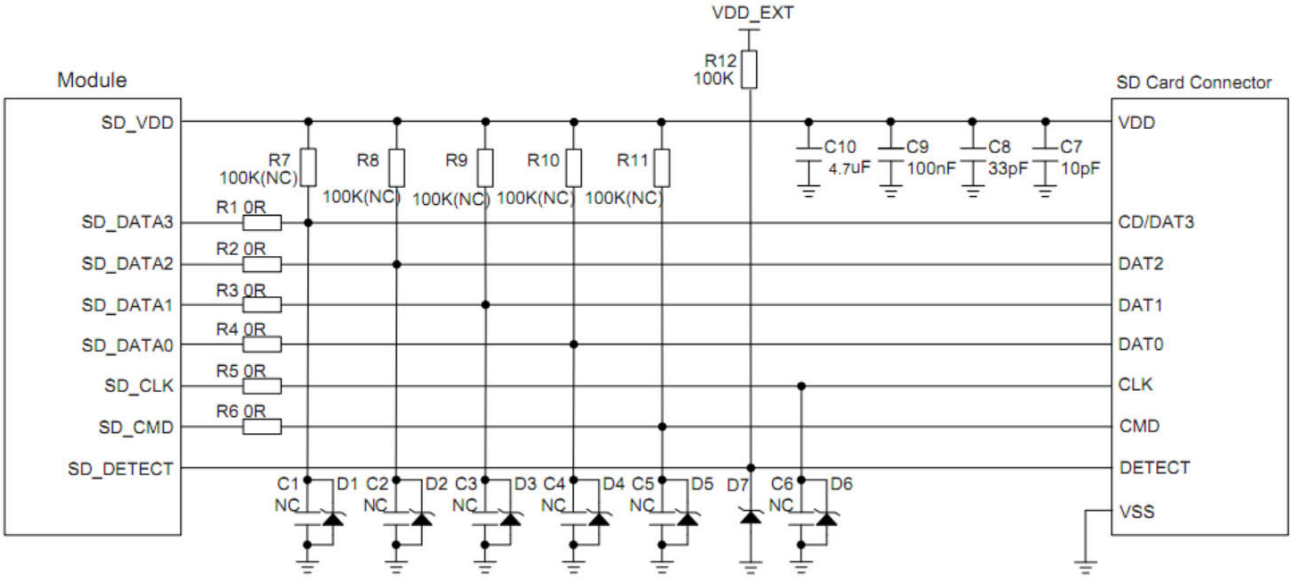

Figure 5-15 FG621-LA SD reference circuit

5.10 SPI Interface

The FG150-AE module supports 1 SPI interface, works in master mode, and the clock supports up to 50MHz.

Table 5-18 SPI interface definition

Pin Name	I/O	Pin#	Description
SPI_MOSI	77	DO	SPI output signal
SPI_MOSI	78	DI	SPI input signal
SPI_CS	79	DO	SPI Chip Selection signal
SPI_CLK	80	DO	SPI clock signal

5.11 GPIO Interface

FG621-AE-00 module reserves five GPIO interfaces for clients, with a voltage domain of 1.8V. Clients can use the interfaces as needed and simply leave them floating when not in use. GPIO pin definition is shown in the following table:

Table 5-19 GPIO pin definition

Pin Name	I/O	Pin#	Description	Instructions for Use
GPIO_1	IO	138	General-Purpose I/O Port 1	Input pull-down inside the chip by default
GPIO_2	IO	139	General-Purpose I/O	Input pull-down inside the

Pin Name	I/O	Pin#	Description	Instructions for Use
			Port 2	chip by default
GPIO_3	IO	159	General-Purpose I/O Port 3	Input pull-up inside the chip by default
GPIO_4	IO	161	General-Purpose I/O Port 4	Input pull-down inside the chip by default
GPIO_5	IO	172	General-Purpose I/O Port 5	Input pull-down inside the chip by default

6 Low Power Consumption

6.1 Flight Mode

Table 6-1 W_DISABLE# pin description

Pin Name	I/O	Pin#	Description
W_DISABLE#	DI	151	Module flight mode control (disabled and internal pulled up by default)

FG621-LA series module supports two ways to enter flight mode:

Table 6-2 Ways of entering flight mode

1	Hardware I/O interface button control	Send “AT+GTFMODE=1” to enable flight mode control function. Pull up or float W_DISABLE# pin (pull up by default), then the module enters normal mode, pull it down, then the module enters flight mode.
2	AT command control	AT+CFUN=0--module enters flight mode AT+CFUN=1--module enters normal mode

6.2 Sleep Mode

AT commands and WAKEUP_IN signal are used to set the module into sleep mode and wake up.

sleep mode:

Sent AT+GTLPMMODE=1,X Set the effective level of the WAKEUP_IN signal that sets the module into sleep mode. Command is effective after resetting module.

(X=0, when WAKEUP_IN pin is high level, module will enter sleep mode;

X=1, when WAKEUP_IN pin is low level, module will enter sleep mode)

AT+CSCLK=1 Enable sleep mode function.

Wake up:

The module will be waked up when the pin level of WAKEUP_IN is opposite to the level that set the module into sleep.

(X=1, when WAKEUP_IN pin is high level, module will be waked up;

X=0, when WAKEUP_IN pin is low level, module will be waked up)

The module will also be waked up by the incoming call or SMS.

7 RF Interface

FG621-LA series module provides two antenna interfaces, i.e., main antenna interface and diversity antenna interface. The pin definition is shown in the following table:

Table 7-1 Antenna interface

Pin Name	I/O	Pin#	Description
ANT_DIV	AI	127	Diversity antenna
ANT_MAIN	IO	107	Main antenna

7.1 Operating Bands

Table 7-2 Operating band

Band	Mode	Tx (MHz)	Rx (MHz)
Band 2	LTE FDD/WCDMA	1850- 1910	1930-1990
Band 4	LTE FDD/WCDMA	1710-1755	2110-2155
Band 5	LTE FDD/WCDMA	824-849	869-894
Band 7	LTE FDD	2500-2570	2620-2690
Band 12	LTE FDD	698-716	728-746
Band 13	LTE FDD	777-787	746-756
Band 28	LTE FDD	703-748	758-803
Band 66	LTE FDD	1710-1780	2110 - 2200
Band 40	LTE TDD	2300-2400	

7.2 Transmission Power

The RF output power of FG621-LA series module is shown as follows:

Table 7-3 Transmission power

Mode	Band	Tx Power (dBm)	Description
WCDMA	Band 2	23.5±2	-
	Band 4	23.5±2	
	Band 5	23.5±2	-
LTE FDD	Band 2	23±2	UL 10MHz Bandwidth, 1 RB
	Band 4	23±2	UL 10MHz Bandwidth, 1 RB

Mode	Band	Tx Power (dBm)	Description
	Band 5	23±2	UL 10MHz Bandwidth, 1 RB
	Band 7	23±2	UL 10MHz Bandwidth, 1 RB
	Band 12	23±2	UL 10MHz Bandwidth, 1 RB
	Band 13	23±2	UL 10MHz Bandwidth, 1 RB
	Band 28	23±2	UL 10MHz Bandwidth, 1 RB
	Band 66	23±2	UL 10MHz Bandwidth, 1 RB
LTE TDD	Band 40	23±2	UL 10MHz Bandwidth, 1 RB

7.3 Receiving Sensitivity

Table 7-4 Receiving sensitivity

Mode	Band	Typical Sensitivity Value of Main Antenna (dBm)	Typical Sensitivity Value of Diversity Antenna (dBm)	Description
WCDMA	Band 2	-110	-110	-
	Band 4	-109.5	-109	-
	Band 5	-110.5	-111	
LTE FDD	Band 2	-98	-99	UL 10MHz Bandwidth, 50RB
	Band 4	-98	-98	UL 10MHz Bandwidth, 50RB
	Band 5	-99	-100	UL 10MHz Bandwidth, 25RB,High
	Band 7	-97.5	-98	UL 10MHz Bandwidth, 50RB
	Band 12	-98	-98	UL 10MHz Bandwidth, 25RB,High
	Band 13	-98	-99	UL 10MHz Bandwidth, 20RB,Low
	Band 28	-99	-99	UL 10MHz Bandwidth, 25RB,High
	Band 66	-99	-99	UL 10MHz Bandwidth, 25RB,High
LTE TDD	Band 40	-98	-99	UL 10MHz Bandwidth, 50RB

7.4 Antenna Design

7.4.1 Antenna Indexes

- **Antenna Efficiency**

Antenna efficiency is the ratio of antenna input power to radiated power. Due to the antenna's return loss, material loss, and coupling loss, the radiated power is always lower than the input power. Antenna efficiency >40% (-4dB) is recommended.

- **S11 or VSWR**

S11 indicates that the matching degree of the antenna's 50Ω impedance, which affects the antenna efficiency to a certain extent. This indicator can be measured using VSWR test. S11<-10dB is recommended.

- **Polarization**

Polarization is the rotation direction of the electric field in the maximum radiation direction of the antenna. Linear polarization is recommended.

- **Radiation Pattern**

Radiation pattern refers to the antenna's electromagnetic field strength in the far field in all directions. Half-wave dipole antenna is the most suitable terminal antenna. For built-in antenna, PIFA antennas or IFA antennas are recommended:

Antenna area: 6mm high*10mm wide*100mm long.

Antenna radiation direction: Omni_directional (omnidirectional).

- **Gain and Directivity**

Antenna directivity refers to the electromagnetic field strength of electromagnetic wave in all directions. Gain is a collection of antenna benefits and antenna directivity.

Recommended antenna gain ≤2.5dBi.

- **Interference**

In addition to the antenna performance, other interferences on the PCB also may affect the performance of the module. In order to ensure the high performance of the module, interference must be controlled. Suggestions: For example, LCD, CP, FPC routing, audio circuit, power supply should be as far from the antenna as possible, and make the appropriate isolation and shielding, or filtering on the path.

- **Antenna Index Requirements**

Table 7-5 Main antenna requirements

FG621-LA series module Main Antenna Requirements	
Frequency range	It must use the most suitable antenna to adapt to the relevant frequency band
Bandwidth (WCDMA)	WCDMA band 2 (1900): 140 MHz WCDMA Band 4(2100): 450 MHz WCDMA band 5 (850): 70 MHz
Bandwidth (LTE)	LTE band 2(1900): 140 MHz

FG621-LA series module Main Antenna Requirements	
	LTE Band 4(2100): 450 MHz LTE Band 5(850): 70 MHz LTE Band 7(2600): 190 MHz LTE Band 12(700): 48 MHz LTE Band 13(800): 21 MHz LTE Band 28(700):100 MHz LTE Band 66(2100): 490 MHz LTE Band 40(2300): 100 MHz
Impedance	50
Input power	> 25dBm average power for WCDMA & LTE
Standing wave ratio recommended	≤ 2:1

7.4.2 Antenna Reference Design

The antenna is a sensitive device and is easily affected by the external environment. For example, the position of the antenna, the space it occupies, and the surrounding ground all may affect antenna performance. In addition, the RF cable connecting the antenna, and the position of the fixed antenna also may affect antenna performance. The three-way antenna of FG621-LA series module adopts the pad-out way. It is recommended that clients use the U.FL-R-SMT-1 antenna connector and the matching RF adapter cable. Figure 7-1 is the reference circuit design for the main and diversity antennas:

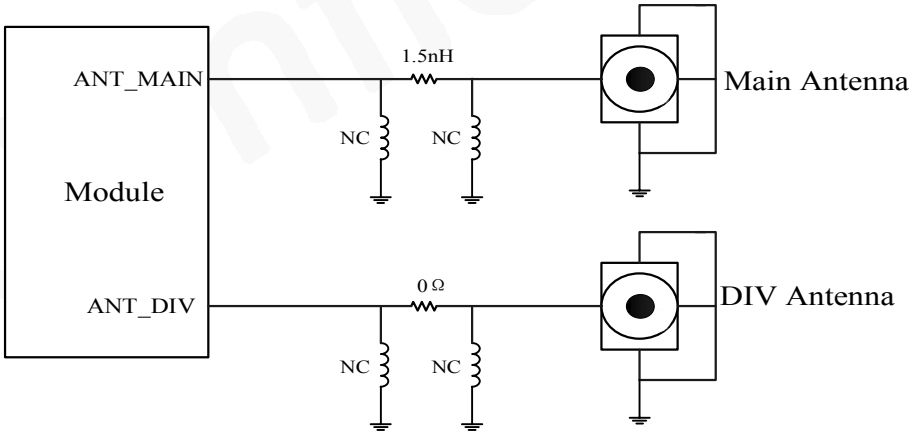

Figure 7-1 Reference circuit for main and diversity antennas

Note:

- All matches must be placed close to the antenna to make sure the characteristic impedance of transmission cable is 50Ω.

- Since the antenna cable loss should be less than 0.3dB, keep PCB routing as short as possible.
- PCB LAYOUT should be as straight as possible to avoid vias and layers, and avoid right-angle and acute-angle routing.
- PCB routing should have a good reference ground to avoid other signal line from approaching the antenna.
- A complete ground level is recommended as a reference ground.
- Strengthen the connection between the ground around the antenna and the main ground.
- The equivalent capacitance of the TVS should be less than 0.5pF.
- Refer to *FIBOCOM Design Guide_RF Antenna* for specific design details.

8 Reliability

8.1 Limiting Voltage Range

The limiting voltage includes the absolute limiting voltage and the operating limiting voltage. The absolute limiting voltage is the maximum voltage that the module can bear, beyond which the module may be damaged. The operating limiting voltage is the normal operating voltage range of the module, beyond which the module will have an abnormal performance.

8.1.1 Absolute Limiting Voltage

The absolute limiting voltage range of FG621-LA series module is shown as follow.

Table 8-1 Absolute limiting voltage range

Parameter	Description	Min	Typ	Max	Unit
VBAT	Power supply	-0.3	3.8	4.7	V
GPIO	Level power supply voltage of digital I/O	-0.3	1.85	2.05	V

8.1.2 Operating Limiting Voltage

Table 8-2 Operating limiting voltage

Signal	Logic low level		Logic high level		Unit
	Min	Max	Min	Max	
Digital input	-0.3	0.6	1.2	2.1	V
Digital output	-	0.45	1.35	-	V
Parameter	**I/O**	**Min**	**Typ**	**Max**	**Unit**
VBAT	PI	3.4	3.8	4.3	V
USIM_VDD	PO	1.7/2.75	1.8/2.85	1.9/3.05	V

8.2 Ambient Temperature Range

The FG621-LA series module is recommended to operate at -30℃~+75℃ ambient temperature. When the module is operating within the limited operating temperature range, some RF indexes may exceed the limit, so the module application terminal should consider temperature control measures. The module application terminal is recommended to be stored in certain temperature conditions. Modules may not operate or may be damaged beyond this range.

Table 8-3 Ambient temperature range

Temperature	Min	Typ	Max	Unit
Operating temperature	-30	25	75	℃
Limited operating temperature	-40	-	85	℃
Storage temperature	-40	-	85	℃

8.3 Environmental Reliability Requirements

The module is required to be able to power-on, the function is normal, and the performance meets the standard, after the following test items.

Table 8-4 Environmental reliability requirements

Test Item	Test Condition
Rapid temperature change test	85/-40℃,15℃/min,500C
Sinusoidal vibration test	5-500Hz,3g
Salt spray test	Neutral salt spray,24Hr
Temperature shock test	85/-40℃,500C
Alternating test	25-70℃,93%,24Hr,14C
Random vibration test	5-500Hz,4Grms
Mechanical shock test	100G,11ms
High temperature operating test	85℃,72H
Low temperature operating test	-40℃,72H
Connector life test	HT/HH/HV->HT/LH/HV->LT/HV->HT/HH/LV->HT/LH/LV ->LT/LV
Power offset test	Umin Oper(3min)/Umax Oper(3min), 1000 C
High temperature and humidity test	85℃,85%rh,1000H

8.4 ESD Characteristics

Although the design of FG621-LA series module has considered the ESD issues and provided ESD protection, the ESD issue may occur in the transport and secondary development, so developers should consider ESD protection for the final product. In addition to considering anti-static treatment for packaging, please refer to the recommended circuit for interface design in the document for client's application.

Refer to the following table for the ESD allowable discharge range of FG621-LA series module:

Table 8-5 ESD allowable discharge range

Part	Air Discharge	Contact Discharge
VBAT, GND	±10KV	±5KV
Antenna interface	±8KV	±4KV
Other interface	±1KV	±0.5KV

9 Structure Specification

9.1 Product Appearance

The product appearance of FG621-LA series module is shown in Figure 9-1:

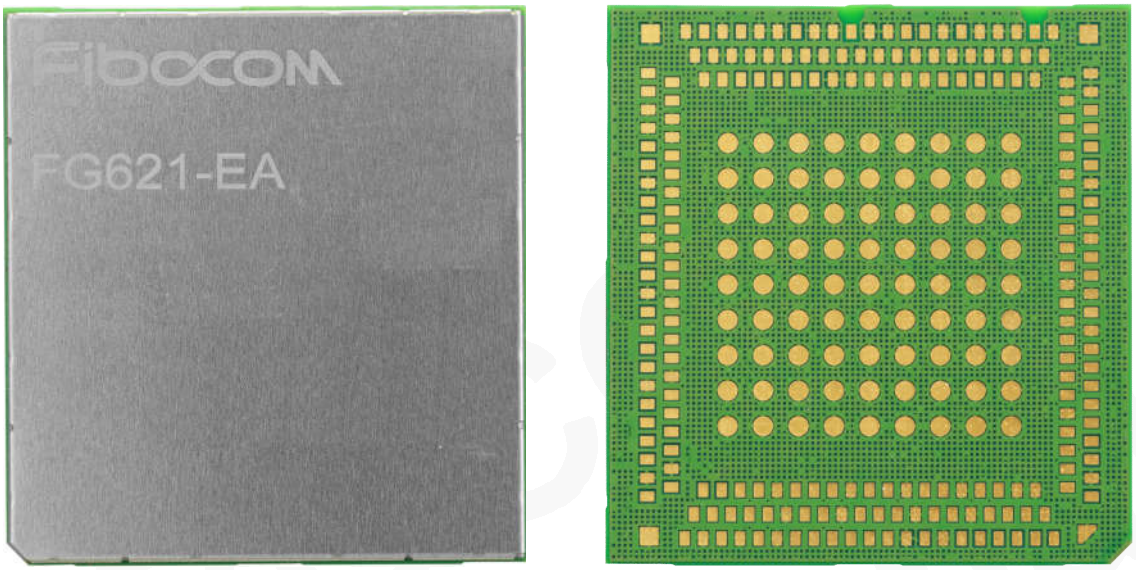

Figure 9-1 Product appearance

9.2 Structural Dimension

The structural dimension of FG621-LA series module is shown in Figure 9-2:

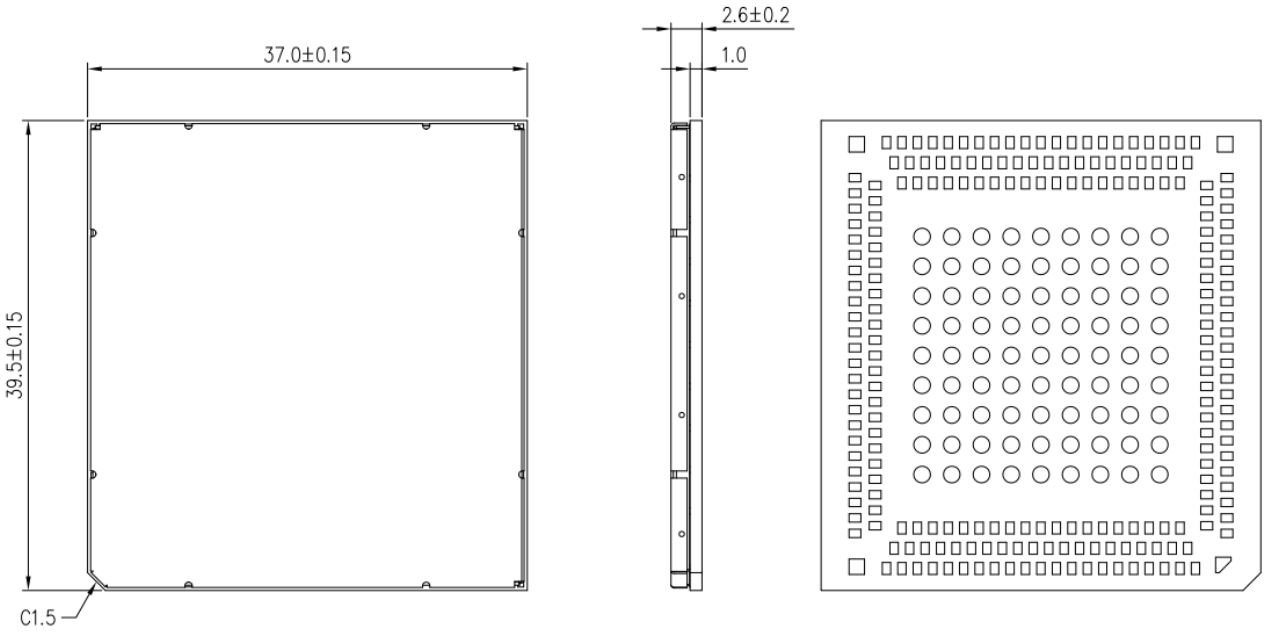

Figure 9-2 Structural dimension (in mm)

9.3 PCB Soldering Pad and Stencil Design

For PCB soldering pad and stencil design, please refer to *FIBOCOM FG621 Series SMT Design Guide*.

9.4 SMT Patch

For SMT production process parameters and related requirements, please refer to *FIBOCOM FG621 Series SMT Design Guide*.

9.5 Packaging and Storage

For packaging and storage, please refer to *FIBOCOM FG621 Series SMT Design Guide*.

10 Certification

FG621-LA series module certification is shown as follow:

Table 10-1 Certification

Certificate	FG621-LA Series Module
HF, ROHS, FCC	FG621-LA-00

For more information, please visit Fibocom website: http://www.fibocom.com/

11 OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.

2. This module is limited to installation in fixed applications, according to Part 2.1091(b).

3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Fibocom that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:

"Contains FCC ID: ZMOFG621LA"

The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna type	WCDMA B2	WCDMA B4	WCDMA B5	LTE B2	LTE B4	LTE B5	LTE B7	LTE B12	LTE B13	LTE B28	LTE B40	LTE B66
Fixed Internal	1.0 dBi	1.1 dBi	-1.0 dBi	1.0 dBi	1.1 dBi	-1.0 dBi	2.1 dBi	-1.0 dBi	-0.8 dBi	-0.9 dBi	2.9 dBi	1.1 dBi

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the

interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

12 Appendix

12.1 Terms and Abbreviations

Table 12-1 Terms and abbreviation

Abbreviation	Definition
AMR	Adaptive Multi-rate
bps	Bits Per Second
EGSM	Extended GSM900 Band
DRX	Discontinuous Reception
FDD	Frequency Division Duplexing
HSDPA	High Speed Down Link Packet Access
Imax	Maximum Load Current
LED	Light Emitting Diode
LTE	Long Term Evolution
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
RF	Radio Frequency
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TE	Terminal Equipment

Abbreviation	Definition
TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

12.2 Related Documents

- *FIBOCOM Design Guide_RF Antenna*
- *FIBOCOM ADP-FG621 User Guide*
- *FIBOCOM FG621 Series AT Commands*

- *FIBOCOM EVK-FG150-00 User Guide*
- *FIBOCOM FG621 Series SMT Design Guide*

12.3 Reference Standards

The design of this product complies with the following standards:

- *3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification, Part 1: Conformance specification*
- *3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification, Radio transmission and reception (FDD), Part 1: Conformance specification*
- *3GPP TS 34.122 V10.1.0: Technical Specification Group Radio Access Network, Radio transmission and reception (TDD)*
- *3GPP TS 36.521-1 V10.6.0: User Equipment (UE) conformance specification, Radio transmission and reception, Part 1: Conformance testing*
- *3GPP TS 21.111 V10.0.0: USIM and IC card requirements*
- *3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface*
- *3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application*
- *3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)*
- *3GPP TS 36.124 V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment*
- *3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)*
- *3GPP TS 27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)*

12.4 Contact

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