PERFECT WIRELESS EXPERIENCE

FG370-NA

Hardware Guide

V1.1

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Safety Instructions

Do not operate wireless communication products in areas where the use of radio is not recommended without proper equipment certification. These areas include environments that may generate radio interference, such as flammable and explosive environments, medical devices, aircraft or any other equipment that may be subject to any form of radio interference.

The driver or operator of any vehicle shall not operate wireless communication products while controlling the vehicle. Doing so will reduce the driver's or operator's control and operation of the vehicle, resulting in safety risks.

Wireless communication devices do not guarantee effective connection under any circumstances, such as when the (U) SIM card is invalid or the device is in arrears. In an emergency, please use the emergency call function when the device is turned on, and ensure that the device is located in an area with sufficient signal strength.

Contents

Applicable Models

No.	Product Model	Description
1	FG370-NA	North America version of the 5G communication module which forvarieties of eMBB scenarios, eight antennas.

Change History

V1.0 (2023-12-29)	Initial version
V1.1(2024-3-15)	1. Ramove 3GPP TS 34.121-1 V10.8.0: 2. Change Antenna Configuration

1 Foreword

1.1 Introduction

The document describes the electrical characteristics, RF performance, dimensions and application environment, etc. of FG370-NA (hereinafter referred to as FG370). With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of FG370 modules and develop products.

1.2 Reference Standards

The design of the product complies with the following standards:

- 3GPP TS 38.300 V16.7.0: 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; NR and NG-RAN Overall Description; Stage 2
- 3GPP TS 38.521-1 V16.7.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Range 1 Standalone;
- 3GPP TS 38.521-3 V16.7.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 3: Range 1 and Range 2 Interworking operation with other radios;
- 3GPP TS 36.521-1 V16.7.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.111 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit(USAT)
- 3GPP TS 36.124 V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPP TS 27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

1.3 Related Documents

FIBOCOM Design Guide_RF Antenna.

FIBOCOM_FG370_SMT Design Guide.

2 Overview

2.1 Introduction

The FG370 series module is a 5G module which supports NSA and SA network architectures. The FG370 integrates core devices such as Baseband, Memory, PMU, Transceiver, and PA. It supports 5G NR Sub6, FDD-LTE, TDD-LTE long-distance communication modes, supports uplink 2×2 MIMO and downlink 4×4 MIMO multi-antenna configuration in SA mode, and supports GNSS wireless positioning technology. The FG370 is designed in an LGA package and is suitable for a variety of eMBB scenarios, such as CPE, MiFi, ODU, VR/AR, gateway, TV box, and intelligent monitoring.

2.2 Specification

2.2.1 RF Characteristic

Table 1. Operating frequencies

Module	FG370-NA
NR Sub-6	n2/5/7/12/14/25/26/29/30/38/41/48/66/70/71/77/78
FDD-LTE	B2/4/5/7/12/13/14/17/25/26/29/30/66/71
TDD-LTE	B38/41/42/43/48
GNSS	GPS/GLONASS/Galileo/BDS/QZSS

Table 2. RF characteristic

Data Throughput	FG370-NA
Sub-6 SA feature	DL 7.01Gbps/UL 2.5Gbps[1]
Sub-6 NSA feature	DL 4.5Gbps/UL 836Mbps [1]
LTE feature	3GPP Release 16 100MHz 5 DLCA, 256 QAM 40MHz 2 ULCA, 256 QAM DL 1.6Gbps (CAT19), UL 211Mbps (CAT18)
Modulation Characteristic	
NR Sub6 Modulation	3GPP Release 16 300MHz 4 DLCA, 256 QAM 200MHz 2 ULCA, 256 QAM 15KHz/30KHz SCS for FDD/TDD
LTE Modulation	3GPP Release 16 100MHz 5 DLCA, 256 QAM 40MHz 2 ULCA, 256 QAM

Physical Characteristics	Dimension: 45 × 48 × 2.75 mm Package: 507 pin LGA Weight: TBD g
HPUE	N41/77/78
MIMO	NR DL 4x4 MIMO: n2/5*/7/12*/14*/25/26/29*/30/38/41/48/66/70/71/77/78
	NR UL 2x2 MIMO: n2/25/41/48/66/71/77/78
	LTE DL 4x4 MIMO: B2/4/5*/7/12*/13*/14*/17*/25/26/29*/30/38/41/42/43/48/66/71
SRS	N41/77/78
	1T4R/2T4R
Carrier Aggregation	
Sub-6 SA	DL 4CA, UL 2CA
Sub-6 NSA	DL LTE 5CA+ NR 1CA, LTE 4CA+ NR 2CA , UL LTE 2CA+ NR 1CA
LTE	DL 5CA, UL 2CA

1. NR Throughput listed here are calculated by formula defined in 3GPP TS 38.306. We assume the slot format is all Downlink slot for DL T-put and all uplink slot for UL T-put. Different UDC should be recalculated proportionally.

2.2.2 Key Features

Table 3. Key features

Performance	Function Description
Power Supply	DC: 3.3-4.4V, typical voltage: 3.8V
Temperature Characteristics	Normal operating temperature: –30 to 75℃[1] Extended operating temperature: –40 to 85℃[2] Storage temperature: –40 to 85℃
Physical Characteristics	Dimension: 45 × 48 × 2.75 mm Package: 507 pin LGA Weight: TBD g
CPU	MTK MT6990, ARM Cortex-A55, quad core, up to 2.0 GHz (boost 2.2 GHz)
Memory	2GB LPDDR4x + 4GB eMMC Flash
Interface	
USB Interface	USB2.0 high speed (HS) interface, data transmission rate up to 480Mbps USB3.2 Gen2 Super-speed (SS) interface, data transmission rate up to 10Gbps

PCIe Interface	PCIe Gen4, 2-lane x1, RC mode PCIe Gen3, 2-lane x1, RC mode
USXGMII	2 USXGMII, data transmission rate up to 10Gbps
SIM Interface	Dual SIM: 1.8V/3V SIM1: USIM SIM2: USIM
I2C	Two set of I2C interface, data transmission rate up to 400Kbit/s
ADCs	Two ADCs, Voltage Range: 0.04-1.78V
Software	
Firmware update	USB
Operating System	Linux

1. When temperature keeps in the range of –30 to 75°C, module can work normally. Module performance meets the 3GPP specifications.
2. When temperature keeps in the range of –40 to 85°C, module performance may be slightly out of 3GPP specifications.

2.3 Application Framework

The application framework below shows the main hardware functions of the FG370 module:

- Baseband
- Transceiver
- PMU
- Discrete LPDDR4x + Discrete eMMC
- Peripheral interface

2.4 Antenna Configuration

The FG370 supports eight NR/LTE antenna and one GNSS antenna. The antenna interface is defined as shown in the following table.

Pin Name	Function Description	Band Configuration (TX)	Band Configuration (RX)	Frequency Range(MHz)
ANT_1	MIMO PRX	SRS Only	LTE: B38/41 NR: n38/41	3300-4200
	MIMO PRX	SRS Only	LTE: B42/43/48 NR: n48/77	
ANT_2	MIMO PRX4		NR: n41*/77*	2496-4200
ANT_3	Second TX1	NR: n5/71		617-4200
	Main TX0/PRX	LTE: B2/4/7/25/30/38/66/41/42/43/48 NR: n2/7/25/30/38/41/48/66/70/77	LTE: B2/4/7/25/30/38/41/42/43/48/66 NR: n2/7/25/30/38/41/48/66/70/77	
	DRX	--	LTE: B52/122/132/142/172/26/292/71 NR: n52/122/142/26/292/71	
ANT_4	MIMO PRX3		NR: n41*/77*	2496-4200
ANT_5	Second TX1	LTE: 42[1]/43[1]/48[1] NR: 48[1]/77[1]	LTE: 42/43/48 NR: 48/77	617-4200
	MIMO PRX	--	LTE: B5[2]/12[2]/13[2]/14[2]/17[2]/26/29[2]/71/B2/4/7/25/30/66 NR: n5[2]/12[2]/14[2]/26/29[2]/71 n2/7/25/30/41/66/70	
ANT_6	MIMO DRX	SRS Only	LTE: B38/41/42/43/48 NR: n38/41/48/77	2496-4200
ANT_7	MIMO DRX		LTE: B5/12/13/14/17/26/29/71 NR: n5/12/14/26/29/71	617-4200
	MIMO DRX		LTE: B2/4/7/25/30/66 NR:n2/7/25/30/66/70	
	MIMO DRX3		NR: n41*/77*	

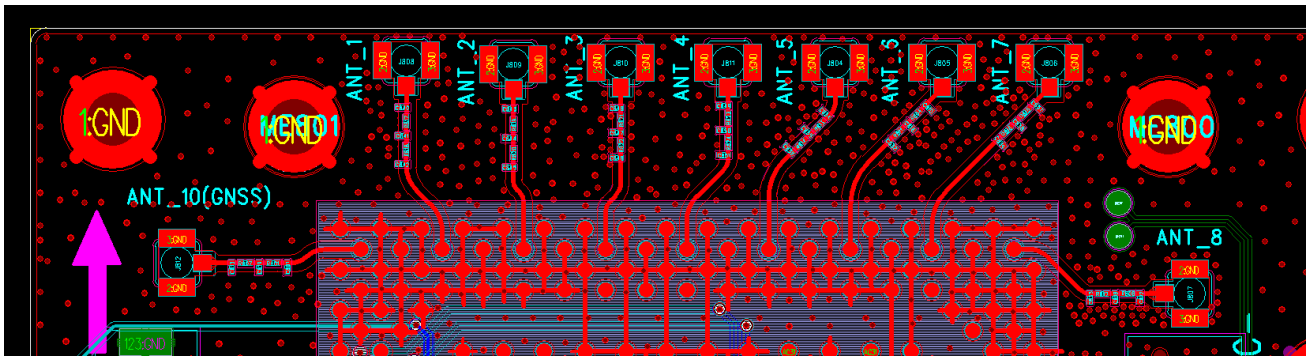
ANT_8	Main TX0/PRX	LTE: B5/12/13/14/17/26/29/71 NR: n5/12/14/26/29/71	LTE: B5/12/13/14/17/26/29/71 NR: n5/12/14/26/29/71	617-4200
	Second TX1/DRX	LTE: B2[1]/4[1]/25[1]/41[1]/66[1] NR: n2[1]/25[1]/41[1]/66[1]/70[1]	LTE: B2/4/25/41/66 NR: n2/25/41/66/70	
	DRX	--	LTE: B7/30 NR: n7/30	
	MIMO DRX4	--	NR: 77*	
ANT10_GNSS	--	--	GNSS receive L1 + L5[3]	1165-1607

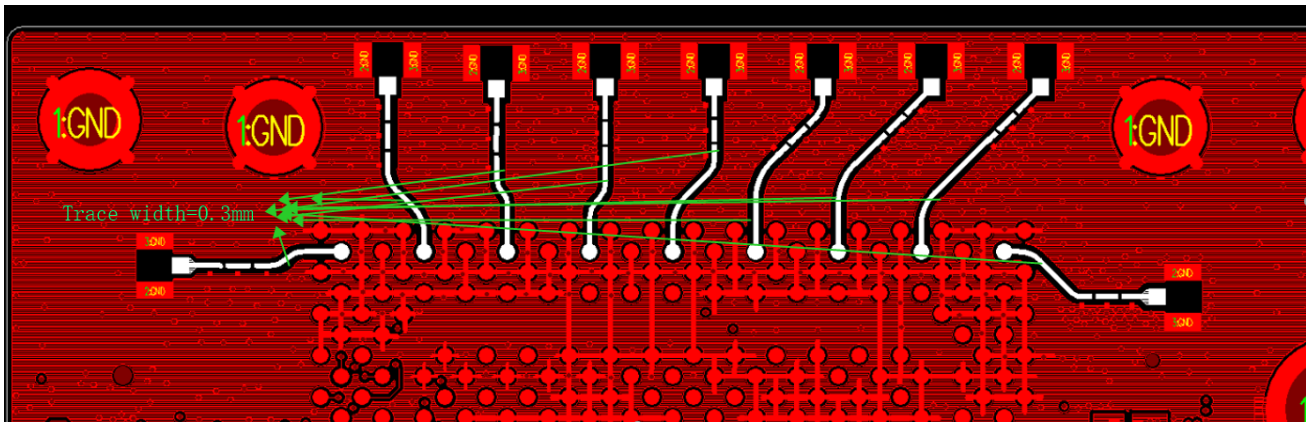
1. TX MIMO is supported in the CA combination.
2. Hardware reserved N71 ULMIMO.
3. Hardware reservation

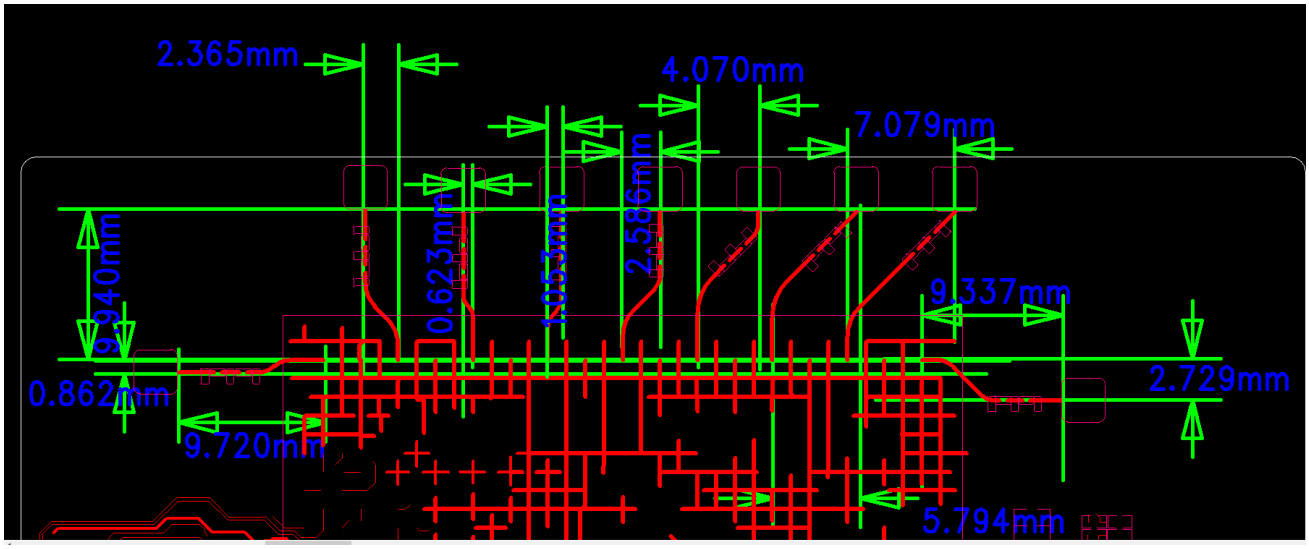
*. n41&n77 8RX

2.5 Antenna trace design

TThe FG370 trace reference design is as follows







2.6 FCC Waring

2.6.1 Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part
15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Fibocom Wireless Inc. that they wish to change
the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: ZMOFG370NA”
The FCC ID can be used only when all FCC mpliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that **20** cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.
(3)The max allowed antenna gain is 2.43 dBi for external monopole antenna.
In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the

final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Antenna Type	Bands	Peak Gain
Dipole	LTE B2	0.98
	LTE B4	2.25
	LTE B5	1.32
	LTE B7	1.06
	LTE B12	1.24
	LTE 13	1.94
	LTE 14	1.94
	LTE 17	1.58
	LTE B25	0.98
	LTE B26	1.39
	LTE B29	/
	LTE B30	0.67
	LTE B66	2.25
	LTE B71	1.39
	LTE B38	0.93
	LTE B41	1.07
	LTE B42	1.52
	LTE B43	1.52
	LTE B48	1.52

Antenna Type	Bands	Peak Gain
Dipole	5G NR n2	0.98
	5G NR n4	2.25
	5G NR n5	1.32
	5G NR n7	1.06
	5G NR n12	1.24
	5G NR n14	1.94
	5G NR n25	0.98
	5G NR n26	1.29
	5G NR n29	/
	5G NR n30	0.67
	5G NR n66	2.25
	5G NR n70	1.16
	5G NR n71	1.39
	5G NR n38	0.93
	5G NR n41	1.07
	5G NR n48	1.52
	5G NR n77	2.43
	5G NR n78	2.43

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

2.6.2 FCC Statement

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

This device is intended only for OEM integrators under the following conditions: (For

module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance **20** cm between the radiator & your body.

3 Pin Definition

The FG370 module applies LGA interface with 507 pins.

3.1 Pin Assignment

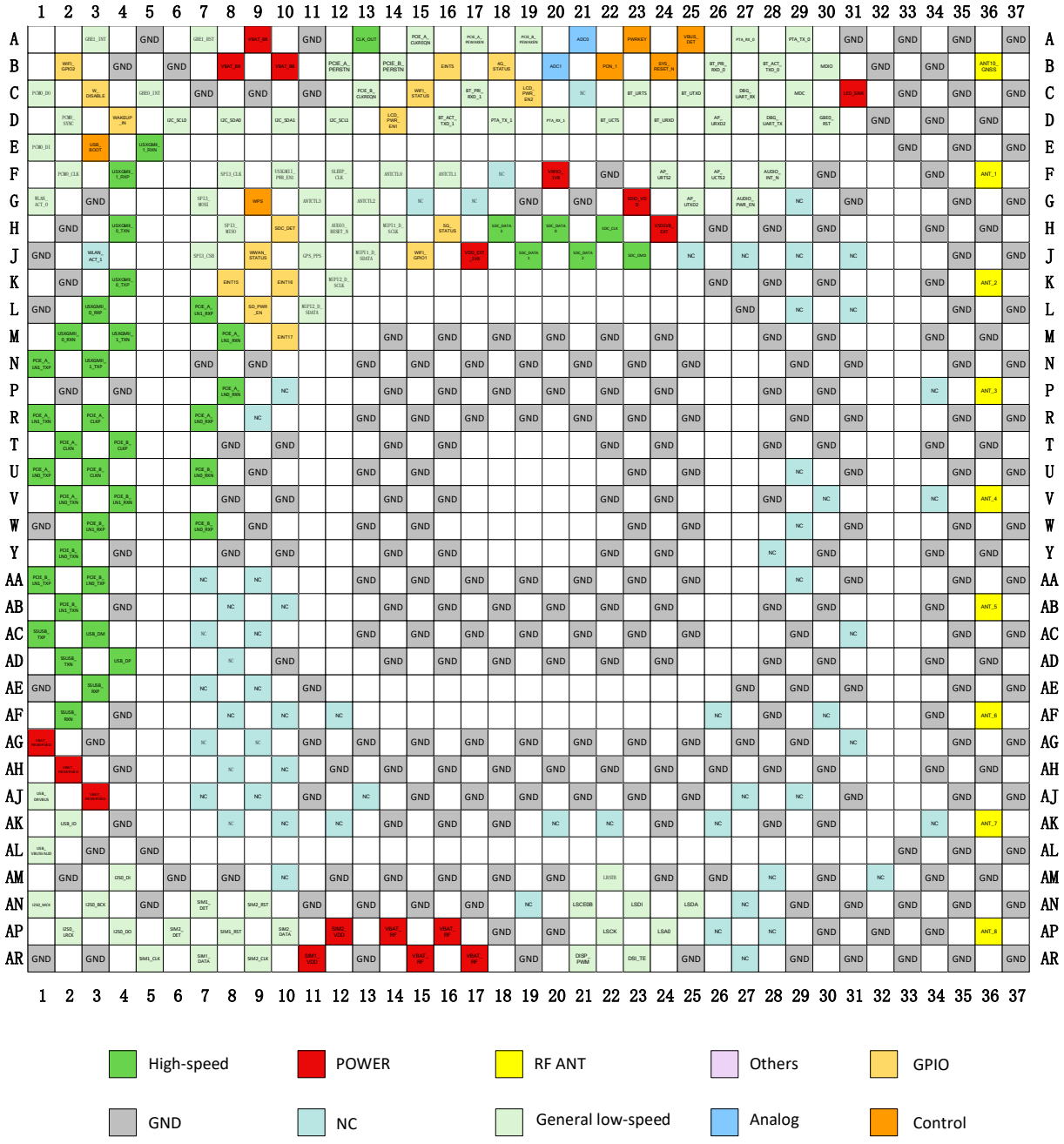


Figure 1. Pin assignment

The pin "RESERVED" means that the position pin is reserved and does not need to be connected.

3.2 Pin Definition

Table 4. IO parameter definition

Type	Description
PI	Power Input
PO	Power Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
OD	Open Drain
PU	Internal pull up
PD	Internal pull down
Hi-Z	High impedance

Table 5. LGA pin description

Pin No.	Pin Name	I/O	Reset Level	Pin Description	Pin DC Feature
Power					
A9, B8, B10	VBAT_BB	PI	--	Baseband power input	3.3V - 4.4V
AG1, AH2, AJ3	VBAT_BB_RESERVED	NC	NC	NC	NC
AP14, AP16, AR17, AR15	VBAT_RF	PI	--	RF power input	3.3V - 4.4V
J17	VDD_EXT_1V8	PO	1.8V	1.8V power output, 50mA	1.8V
F20	VRFIO_1V8	PO	1.8V	1.8V power output for ANT tuner, 50mA	1.8V
USB					
AD2	SSUSB_TXN	AO	--	USB super speed transmit data minus	--
AC1	SSUSB_TXP	AO	--	USB super speed transmit data plus	--

Pin No.	Pin Name	I/O	Reset Level	Pin Description	Pin DC Feature
AF2	SSUSB_RXN	AI	--	USB super speed receive data minus	--
AE3	SSUSB_RXP	AI	--	USB super speed receive data plus	--
AC3	USB_DM	AIO	--	USB high speed data minus	--
AD4	USB_DP	AIO	--	USB high speed data plus	--
A25	VBUS_DET	DI	--	USB VBUS detection	0 – 21V
AJ1	USB_DRVBUS	DO	PD	USB OTG power enable	1.8V
AL1	USB_ VBUSVALID	DO	PD	USB power valid	1.8V
AK2	USB_ID	DI	PD	USB ID	1.8V
USIM					
AR11	SIM1_VDD	PO	--	SIM1 power supply	3V/1.8V
AR7	SIM1_DATA	DIO	PD	SIM1 data input/output	3V/1.8V
AR5	SIM1_CLK	DO	PD	SIM1 clock signal	3V/1.8V
AP8	SIM1_RST	DO	PD	SIM1 reset signal	3V/1.8V
AN7	SIM1_DET	DI	PD	SIM1 detect signal	1.8V
AP12	SIM2_VDD	PO	--	SIM2 power supply	3V/1.8V
AP10	SIM2_DATA	DIO	PD	SIM2 data input/output	3V/1.8V
AR9	SIM2_CLK	DO	PD	SIM2 clock signal	3V/1.8V
AN9	SIM2_RST	DO	PD	SIM2 reset signal	3V/1.8V
AP6	SIM2_DET	DI	PD	SIM2 detect signal	1.8V
GPIO					
C3	W_DISABLE	DI	PD	Module flight mode control signal, Reserved	1.8V
D4	WAKEUP_IN	DI	PD	Module wake up input from host	1.8V
H16	5G_STATUS	DO	PD	5G status indicator	1.8V
B18	4G_STATUS	DO	PD	4G status indicator	1.8V
C15	WIFI_STATUS	DO	PD	Module output to wake up host, can use as GPIO	1.8V
J9	WWAN_STATUS	DO	PD	Module status indicator	1.8V
K8	EINT15	DO	PD	B code output, can use as GPIO	1.8V
J11	GPS_PPS	DO	PD	PPS signal output	1.8V
K10	EINT16	DO	PD	Can use as GPIO	1.8V

Pin No.	Pin Name	I/O	Reset Level	Pin Description	Pin DC Feature
H10	SDC_DET	DI	PD	Use GPIO	1.8V
L9	SD_PWR_EN	DO	PD	Use GPIO	1.8V
C31	ISINK1	AI	Hi-Z	LED negative drive signal	--
ANT					
F36	ANT_1	AIO	--	RF antenna interface, ANT_1	50 Ω
K36	ANT_2	AIO	--	RF antenna interface, ANT_2	50 Ω
P36	ANT_3	AIO	--	RF antenna interface, ANT_3	50 Ω
V36	ANT_4	AIO	--	RF antenna interface, ANT_4	50 Ω
AB36	ANT_5	AIO	--	RF antenna interface, ANT_5	50 Ω
AF36	ANT_6	AIO	--	RF antenna interface, ANT_6	50 Ω
AK36	ANT_7	AIO	--	RF antenna interface, ANT_7	50 Ω
AP36	ANT_8	AIO	--	RF antenna interface, ANT_8	50 Ω
B36	ANT10_GNSS	AI	--	GNSS antenna	50 Ω
ANT Tuner Control					
J13	MIPI1_D_SDATA	DIO	PD	External Tuner MIPI Control Data Pin	1.8V
H14	MIPI1_D_SCLK	DO	PD	External Tuner MIPI Control Clock Pin	1.8V
L11	MIPI2_D_SDATA	DIO	PD	External Tuner MIPI Control Data Pin	1.8V
K12	MIPI2_D_SCLK	DO	PD	External Tuner MIPI Control Clock Pin	1.8V
F14	ANTCTL0	DO	PD	Antenna control signal 0	1.8V
F16	ANTCTL1	DO	PD	Antenna control signal 1	1.8V
G13	ANTCTL2	DO	PD	Antenna control signal 2	1.8V
G11	ANTCTL3	DO	PD	Antenna control signal 3	1.8V
Module Control					
A23	PWRKEY	DI	PU	Module power-key control signal	1.8V
B24	RESET_N	DI	PU	Module reset control signal	1.8V
B22	PON_1	DI	PD	Module power on signal	--
G9	WPS	DI	PD	Interrupt input signal, used for WPS key input signal	1.8V
E3	USB_BOOT	DI	PU	Force into USB download boot	1.8V

Pin No.	Pin Name	I/O	Reset Level	Pin Description	Pin DC Feature
				mode	
SD					
H20	SDC_DATA0	DIO	PD	SDC interface DATA0 signal, reserved	1.8V
J19	SDC_DATA1	DIO	PD	SDC interface DATA1 signal, reserved	1.8V
J21	SDC_DATA2	DIO	PD	SDC interface DATA2 signal, reserved	1.8V
H18	SDC_DATA3	DIO	PD	SDC interface DATA3 signal, reserved	1.8V
J23	SDC_CMD	DIO	PD	SDC interface command signal, Reserved	1.8V
H22	SDC_CLK	DO	PD	SDC interface clock signal, reserved	1.8V
H24	VSD1V8_EXT	PI	--	Digital power for FG370 SD interface, reserved	1.8V
G23	SDIO_VDD	PO	--	SD card IO interface Power, reserved	1.8V
USXGMII					
E5	USXGMII_1_RXN	AIO	--	USXGMII 1 receive data minus	--
F4	USXGMII_1_RXP	AIO	--	USXGMII 1 receive data plus	--
M4	USXGMII_1_TXN	AIO	--	USXGMII 1 transmit data minus	--
N3	USXGMII_1_TXP	AIO	--	USXGMII 1 transmit data plus	--
A3	GBE1_INT	DI	PD	USXGMII 1 interrupt input signal	1.8V
A7	GBE1_RST	DO	PD	USXGMII 1 reset signal	1.8V
M2	USXGMII_0_RXN	AIO	--	USXGMII 0 receive data minus	--
L3	USXGMII_0_RXP	AIO	--	USXGMII 0 receive data plus	--
H4	USXGMII_0_TXN	AIO	--	USXGMII 0 transmit data minus	--
K4	USXGMII_0_TXP	AIO	--	USXGMII 0 transmit data plus	--
C5	GBE0_INT	DI	PD	USXGMII 0 interrupt input signal	1.8V
D30	GBE0_RST	DO	PD	USXGMII 0 reset signal	1.8V
F10	USXGMII_PWR_EN1	DO	PD	USXGMII power supply enable 1	1.8V
B30	MDIO	DIO	PD	USXGMII MDIO signal	1.8V
C29	MDC	DO	PD	USXGMII MDC signal	1.8V
PCIE					

Pin No.	Pin Name	I/O	Reset Level	Pin Description	Pin DC Feature
T2	PCIE_A_CLKN	AIO	--	PCIe A reference clock minus	--
R3	PCIE_A_CLKP	AIO	--	PCIe A reference clock plus	--
V2	PCIE_A_LN0_TXN	AIO	--	PCIe A Tx0 minus	--
U1	PCIE_A_LN0_TXP	AIO	--	PCIe A Tx0 plus	--
P8	PCIE_A_LN0_RXN	AIO	--	PCIe A Rx0 minus	--
R7	PCIE_A_LN0_RXP	AIO	--	PCIe A Rx0 plus	--
R1	PCIE_A_LN1_TXN	AIO	--	PCIe A Tx1 minus	--
N1	PCIE_A_LN1_TXP	AIO	--	PCIe A Tx1 plus	--
M8	PCIE_A_LN1_RXN	AIO	--	PCIe A Rx1 minus	--
L7	PCIE_A_LN1_RXP	AIO	--	PCIe A Rx1 plus	--
A17	PCIE_A_PEWAKEN	DI	PU	PCIe A wake-up signal	1.8V
B12	PCIE_A_PERSTN	DO	PU	PCIe A reset signal	1.8V
A15	PCIE_A_CLKREQN	DIO	PD	PCIe A clock request signal	1.8V
U3	PCIE_B_CLKN	AIO	--	PCIe B reference clock minus	--
T4	PCIE_B_CLKP	AIO	--	PCIe B reference clock plus	--
Y2	PCIE_B_LN0_TXN	AIO	--	PCIe B Tx0 minus	--
AA3	PCIE_B_LN0_TXP	AIO	--	PCIe B Tx0 plus	--
U7	PCIE_B_LN0_RXN	AIO	--	PCIe B Rx0 minus	--
W7	PCIE_B_LN0_RXP	AIO	--	PCIe B Rx0 plus	--
AB2	PCIE_B_LN1_TXN	AIO	--	PCIe B Tx1 minus	--
AA1	PCIE_B_LN1_TXP	AIO	--	PCIe B Tx1 plus	--
V4	PCIE_B_LN1_RXN	AIO	--	PCIe B Rx1 minus	--
W3	PCIE_B_LN1_RXP	AIO	--	PCIe B Rx1 plus	--
A19	PCIE_B_PEWAKEN	DI	PD	PCIe B wake-up signal	1.8V
B14	PCIE_B_PERSTN	DO	PD	PCIe B reset signal	1.8V
C13	PCIE_B_CLKREQN	DIO	PD	PCIe B clock request signal	1.8V
I2C					
D8	I2C_SDA0	DIO	PU	I2C0 data	1.8V
D6	I2C_SCL0	DO	PU	I2C0 clock	1.8V
D10	I2C_SDA1	DIO	PU	I2C1 data	1.8V
D12	I2C_SCL1	DO	PU	I2C1 clock	1.8V
I2S					

Pin No.	Pin Name	I/O	Reset Level	Pin Description	Pin DC Feature
AP4	I2S0_DO	DO	PD	I2S data output signal	1.8V
AN1	I2S0_MCK	DO	PD	I2S clock output signal	1.8V
AM4	I2S0_DI	DI	PD	I2S data input signal	1.8V
AN3	I2S0_BCK	DO	PD	I2S data bit clock signal	1.8V
AP2	I2S0_LRCK	DO	PD	I2S frame clock signal	1.8V
ADC					
A21	ADC0	AI	--	A/D conversion channel 0	--
B20	ADC1	AI	--	A/D conversion channel 1	--
Debug UART					
D28	DBG_UART_TX	DO	PU	Debug UART transmit signal	1.8V
C27	DBG_UART_RX	DI	PU	Debug UART receive signal	1.8V
UART					
F26	AP_UCTS2	DI	PD	UART receive ready signal	1.8V
F24	AP_URTS2	DO	PD	UART transmit request signal	1.8V
G25	AP_UTXD2	DO	PD	UART transmit signal	1.8V
D26	AP_URXD2	DI	PD	UART receive signal	1.8V
SPI					
H8	SPI3_MISO	DI	PD	SPI interface input signal	1.8V
G7	SPI3_MOSI	DO	PD	SPI interface output signal	1.8V
J7	SPI3_CSB	DO	PD	SPI interface chip select signal	1.8V
F8	SPI3_CLK	DO	PD	SPI interface clock signal	1.8V
AUDIO CODEC					
H12	AUDIO_RESET_N	DO	PD	External CODEC reset signal, can use GPIO	1.8V
F28	AUDIO_INT_N	DI	PD	External CODEC interrupt signal, can use GPIO	1.8V
G27	AUDIO_PWR_EN	DO	PD	External CODEC power enable, can use GPIO	1.8V
CLK OUT					
F12	SLEEP_CLK	DO	--	32KHz clock output, reserved	1.8V
A13	CLK_OUT	DO	--	26MHz clock output, reserved	1.8V
LCD					
AP22	LSCK	DO	PD	CLK signal for DBI-C serial 3/4 wire	1.8V

Pin No.	Pin Name	I/O	Reset Level	Pin Description	Pin DC Feature
				SPI LCD, connect to LCD CLK signal	
AN25	LSDA	DO/DI	PD	Data signal for DBI-C serial 3/4 wire SPI LCD. For type interface I LCD, is data input/output signal. For type interface II LCD, is data output signal from FG370 module and connect to LCD data in signal	1.8V
AP24	LSA0	DO	PD	RS signal for DBI-C serial 4 wire SPI LCD, DBI-C serial 3 wire SPI LCD not has this signal	1.8V
AN21	LSCE0B	DO	PD	CS signal for DBI-C serial 3/4 wire SPI LCD, connect to LCD CS signal	1.8V
AN23	LSDI	DI	PD	Data signal for DBI-C serial 3/4 wire SPI LCD. For type interface II LCD, is data input signal from FG370 module and connect to LCD data output signal. For type interface I LCD, not has this signal	1.8V
AM22	LRSTB	DO	PD	Reset signal for DBI-C serial 3/4 wire SPI LCD, connect to LCD RST signal	1.8V
AR23	DSI_TE	DI	PD	LCD frame synchronization signal	1.8V
AR21	DISP_PWM	DO	PD	LCD Backlight control PWM signal	1.8V
D14	LCD_PWR_EN1	DO	PD	LCD power supply enable 1	1.8V
C19	LCD_PWR_EN2	DO	PD	LCD power supply enable 2	1.8V
AP22	LSCK	DO	PD	CLK signal for DBI-C serial 3/4 wire SPI LCD, connect to LCD CLK signal	1.8V
AN25	LSDA	DO/DI	PD	Data signal for DBI-C serial 3/4 wire SPI LCD. For type interface I LCD, is data input/output signal. For type interface II LCD, is data output signal from FG370 module and connect to LCD data in signal	1.8V
AP24	LSA0	DO	PD	RS signal for DBI-C serial 4 wire SPI LCD, DBI-C serial 3 wire SPI LCD not has this signal	1.8V
AN21	LSCE0B	DO	PD	CS signal for DBI-C serial 3/4 wire SPI LCD, connect to LCD CS signal	1.8V
AN23	LSDI	DI	PD	Data signal for DBI-C serial 3/4 wire SPI LCD. For type interface II LCD, is data input signal from FG370 module and connect to LCD data output signal. For type interface I	1.8V

Pin No.	Pin Name	I/O	Reset Level	Pin Description	Pin DC Feature
				LCD, not has this signal	
AM22	LRSTB	DO	PD	Reset signal for DBI-C serial 3/4 wire SPI LCD, connect to LCD RST signal	1.8V
AR23	DSI_TE	DI	PD	LCD frame synchronization signal	1.8V
AR21	DISP_PWM	DO	PD	LCD Backlight control PWM signal	1.8V
D14	LCD_PWR_EN1	DO	PD	LCD power supply enable 1	1.8V
C19	LCD_PWR_EN2	DO	PD	LCD power supply enable 2	1.8V
WIFI/BT					
C25	BT_UTXD	DO	PD	UART TX signal	1.8V
D24	BT_URXD	DI	PD	UART RX signal	1.8V
C23	BT_URTS	DO	PD	UART RTS signal	1.8V
D22	BT_UCTS	DI	PD	UART CTS signal	1.8V
C1	PCM0_DO	DO	PD	PCM data output	1.8V
E1	PCM0_DI	DI	PD	PCM data input	1.8V
F2	PCM0_CLK	DO	PD	PCM clock output	1.8V
D2	PCM0_SYNC	DO	PD	PCM synchronization signal	1.8V
M10	EINT17	DIO	PD	GPIO	1.8V
B16	EINT5	DIO	PD	GPIO, used for control WIFI RESET signal	1.8V
B26	BT_PRI_RXD_0	DI	PD	WIFI/BT and RF coexistence control signals	1.8V
B28	BT_ACT_TXD_0	DO	PD	WIFI/BT and RF coexistence control signals	1.8V
G1	WLAN_ACT_0	DI	PD	WIFI/BT and RF coexistence control signals	1.8V
A27	PTA_RX_0	DI	PD	WIFI/BT and RF coexistence control signals	1.8V
A29	PTA_TX_0	DO	PD	WIFI/BT and RF coexistence control signals	1.8V
C17	BT_PRI_RXD_1	DI	PD	WIFI/BT and RF coexistence control signals	1.8V
D16	BT_ACT_TXD_1	DO	PD	WIFI/BT and RF coexistence control signals	1.8V
J3	WLAN_ACT_1	DI	PD	WIFI/BT and RF coexistence control signals	1.8V

Pin No.	Pin Name	I/O	Reset Level	Pin Description	Pin DC Feature
D20	PTA_RX_1	DI	PD	WIFI/BT and RF coexistence control signals	1.8V
D18	PTA_TX_1	DO	PD	WIFI/BT and RF coexistence control signals	1.8V
J15	WIFI_GPIO1	DIO	PD	WIFI control signal 1, Reserved use GPIO	1.8V
B2	WIFI_GPIO2	DIO	PD	WIFI control signal 2, Reserved use GPIO	1.8V

Pin NO.	Pin Name
NC	
AP26, AR27, AP28, AN19, AJ7, AF12, P10, AC9, AK26, R9, J29, AC31, AK22, AE9, AF10, J25, AG31, AK20, V34, AN27, AJ29, AK12, AM28, AK10, AJ9, AH10, AA7, AB8, AF8, AE7, AA9, AB10, AA29, AK34, U29, J27, AF30, W29, AF26, L31, Y28, AJ13, V30, L29, G29, J31, P34, AM32, AJ27, AM10, AK8, G15, C21, AC7, AD8, AG7, G17, AH8, F18, AG9	NC
GND	
AP20, AR19, AP18, D32, A11, A31, G3, M14, K2, AN5, B4, AD18, M20, G19, G21, N25, B32, M24, AK16, AH18, AH4, K28, M16, AM12, T30, AG25, AJ21, AJ19, A33, A35, A37, N13, AG3, AR25, C9, V8, M18, K30, AM30, AH16, AH28, AH26, AK4, C11, T28, C35, C37, AG13, AM8, AJ25, AJ11, AK18, A5, AK24, B34, D36, E35, E37, G35, G37, H36, J35, J37, L35, L37, M36, N35, N37, U37, W13, W15, U35, W25, W23, P2, W35, W37, N19, AM18, G31, N7, T22, V10, Y8, AD36, AE35, AE37, AG35, AG37, R37, AJ35, AJ37, AL35, AL37, AM36,AN35, AN37, AA13, AA15, AA17, AA19, AA21, AA23, AA25, R13, R15, AA35, AA37, R35, N9, AM16, B6, AB14, AB16, AB18, AB20, AB22, AB24, R17, R21, AB34, AJ17, R23, AC13, AC15, AC17, AC21, AC23, AC25, R25, U15,AC35,AC37,Y30,AL3, AD14, AD16, AD22, AD24, AD28, AD30, AD34, N15, AF28, AG17, AC19, AM14, AN29, AJ31, AM26, N29, M30, E33, AM34, AM24, AE31, H28, AM6, N23, U25, AG23, AG21, AJ23, P30, AN31, AN33, Y4, P24, AJ15, F34, T34, H30, U13, C7, P22, M34, P20, AK28, H2, AP30, AP32, AP34, N31, AM20, AR3, P28, D34, T8, T36, N17, AN11, M28, AR29, AL33, AG19, AR31, AR33, AR35, AR37, AR13, AL5, AE27, M22, AE11, K26, L27, J1, AN15, AN17, AN13, AH30, AH14, AF4, N21, W1, AG15, H34, AH20, AH22, AR1, K34, C33, P4, H26, W9, Y10, AM2, Y34, AE1, F22, U23, T10, Y14, Y16, AB4, AD20, V14, AF34, U9, AG27, AG29, AG11, T14, L1, V16, V22, V24, T24, T16, U31, AK30, P14, Y22, Y24, AB28, Y36, AD10, AH12, P16, P18, AB30, AE29, AH24, AA31, W31, F30, AH34, AH36, AC29, AK14, R29, V28, R31, R19	GND

The PWRKEY and RESET_N pins have internal pull-up, and the pull-up power supply is in exclusive mode; no external pull-up is required; PON_1 pin module with weak pull-down, maximum input voltage must not exceed VBAT_BB.

4 Electrical Characteristics

4.1 Recommended Operating Conditions

Table 6. Recommended operating voltage

Pin Name	Type	Min (V)	Typ (V)	Max (V)	Current Limit Max(mA)
VBAT_BB, VBAT_RF	PI	3.3[1]	3.8	4.4[1]	4000
VDD_EXT_1V8	PO	1.7	1.8	1.9	50
VRFIO_1V8	PO	1.7	1.8	1.9	50
SIM1_VDD, SIM2_VDD	PO	1.7	1.86	1.9	200
		2.75	2.95	3.0	200
PON_1	DI	0	--	VBAT_BB	--
VBUS_DET[2]	DI	0	--	21	--
ADC0	AI	0.04	--	1.78	--
ADC1	AI	0.04	--	1.78	--

1. Directly measured at Module. Voltage must stay within the min/max values, including voltage drop, ripple and spikes.
2. When VBUS_DET input voltage ⩾4.2V, USB detection trigger.

4.2 I/O Logic Characteristics

Table 7. I/O port logic characteristics

Parameters	Min	Typical	Max	Unit
1.8V logic level				
V_{IH}	1.3	1.8	1.98	V
V_{IL}	-0.3	0	0.6	V

Parameters	Min	Typical	Max	Unit
V_{OH}@2mA	1.35	1.8	1.98	V
V_{OL}	-0.3	0	0.45	V
3.0V logic level				
V_{IH}	2.6	3	3.3	V
V_{IL}	-0.3	0	0.4	V
V_{OH}	2.6	3	3.1	V
V_{OL}	-0.3	0	0.4	V
PON_1				
V_{IH}	1.4	3.8	VBAT_BB	V
V_{IL}	-0.3	0	0.7	V

4.3 Radio Frequency

4.3.1 Operating Band

Table 8. Operating band

Band	Mode	Tx (MHz)	Rx (MHz)
Band 2	LTE/NR FDD	1850–1910	1930–1990
Band 4	LTE FDD	1710–1755	2110–2155
Band 5	LTE/NR FDD	824–849	869–894
Band 7	LTE/NR FDD	2500-2570	2620-2690
Band 12	LTE/NR FDD	699–716	729–746
Band 13	LTE FDD	777-787	746-756
Band 14	LTE/NR FDD	788-798	758-768

Band	Mode	Tx (MHz)	Rx (MHz)
Band 17	LTE FDD	704-716	734-746
Band 25	LTE/NR FDD	1850–1915	1930–1995
Band 26	LTE/NR FDD	814-849	859-894
Band 29	LTE/NR FDD	--	717-728
Band 30	LTE/NR FDD	2305-2315	2350-2360
Band 38	LTE/NR TDD	2570-2620	2570-2620
Band 41	LTE/NR TDD	2496–2690	2496–2690
Band 42	LTE TDD	3400-3600	3400-3600
Band 43	LTE TDD	3600-3800	3600-3800
Band 48	LTE/NR TDD	3550–3700	3550–3700
Band 66	LTE/NR FDD	1710–1780	2110–2200
Band 70	NR FDD	1695-1710	1995-2020
Band 71	LTE/NR FDD	663-698	617-652
Band 77	NR TDD	3300–4200	3300–4200
Band 78	NR TDD	3300–3800	3300–3800
GPS L1	--	--	1575.42±1.023
GLONASS G1	--	--	1602.5625±4
Galileo E1	--	--	1575.42±2.046
BDS B1	--	--	1561.098±2.046
QZSS	--	--	1575.42±1.023

4.3.2 Antenna Requirements

Table 9. Module antenna requirements

FG370 module antenna requirements	
LTE/NR	VSWR: ≤ 2:1 Input power (W): > 28dBm average power LTE & NR Input impedance (Ω): 50 Antenna isolation (dB): > 25
GNSS	Frequency range: 1559MHz–1607MHz VSWR: < 2: 1

5 Interface Introduction

5.1 Power

The DC power input range of FG370 module is 3.3V–4.4V, and the recommended value is 3.8V. DC power output ability requires more than 4A. The performance of the power supply, such as load capacity and ripple size, will directly affect the performance and stability of the module.

5.1.1 Power Supply

FG370 module provides power supply via VBAT_BB and VBAT_RF.
The power supply design is shown in Figure 3:

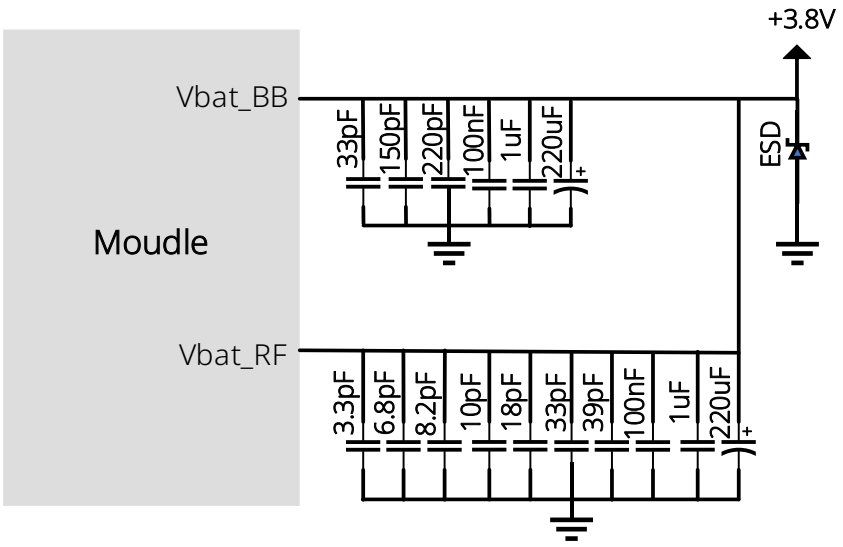


Figure 2. Power supply design

The filter capacitor design for power supply as shown in the following table:

Table 10. Power supply filter capacitor design

Recommended Capacitance	Description
220uF × 2	Reduce power fluctuations of the module in operation, requiring capacitors with low ESR. LDO or DC/DC power supply requires the capacitor no less than 440uF. The capacitor for battery power supply can be reduced to 100-200uF.
1uF × 2,100nF × 2	Filter out the interference generated from the clock and digital signals
33pF	Filter out 600/700/850/900MHz frequency band RF interference(low band)
3.3pF,6.8pF,8pF, 10pF	Filter out 1700/1800/1900/2100/2300/2500/2600/3500/3700MHz,5GHz frequency band RF interference(high band)

The stable power supply can ensure the normal operation of FG370 module, and the ripple of the power supply should be less than 300mV in design. Because module support 5G NR Sub-6 download, when module operates with the maximum data transfer throughput, the peak current can reach to upper 4000 mA. It requests the power source voltage should not be lower than 3.3V, otherwise module may shut down or restart. The power supply requirement is shown in Figure 4:

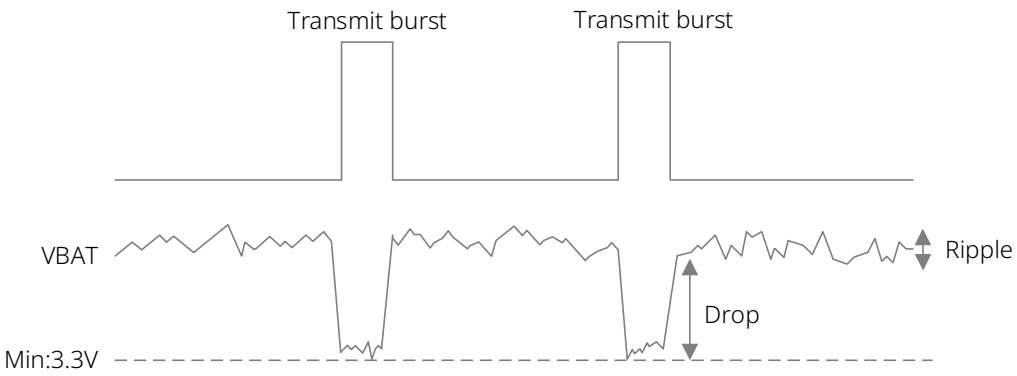


Figure 3. Power supply voltage drop diagram

The filter capacitor is located near the pin of the power supply and arranged in order of capacity size. It is recommended that the PCB traces of the power supply be as short as possible. It is wide enough power supply traces to ensure that no large voltage drops occur in maximum transmit power status.

5.2 Control Interface

Control signals are used to power on/off and reset the module. The pin definitions are as follows:

Table 11. Control signal

Pin name	Pin No	I/O	Description
PON_1	B22	DI	Module power on/off input, internal pull down (51KΩ) Power on: High Power off: Low/Floating
PWRKEY	A23	DI	Module power on/off input, internal pull up Pull down PWRKEY with pulse, module will power on from power off status. Pull down PWRKEY with pulse, module will power off from power on status.
RESET_N	B24	DI	Pull down RESET_N with pulse, module will reset

5.2.1 Module Start-up and Shutdown

FG370 provides two modes to control power on and power off. One mode is voltage level control with PON_1, another is pulse control with PWRKEY.

5.2.1.1 Module Start-up

- Mode 1

The PON_1 pin needs an external pull up for power on. The recommended design is shown in Figure 5:

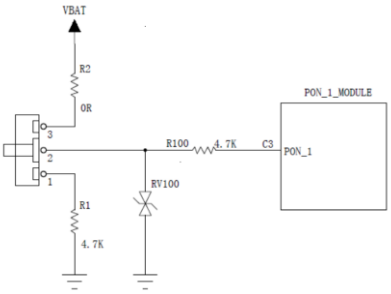


Figure 4. Start-up circuit 1

When power supply is ready, the PMU of module will power on and start initialization process by pulling high PON_1 signal. After about 30s, module will complete initialization process. The start-up timing is shown in Figure 6.

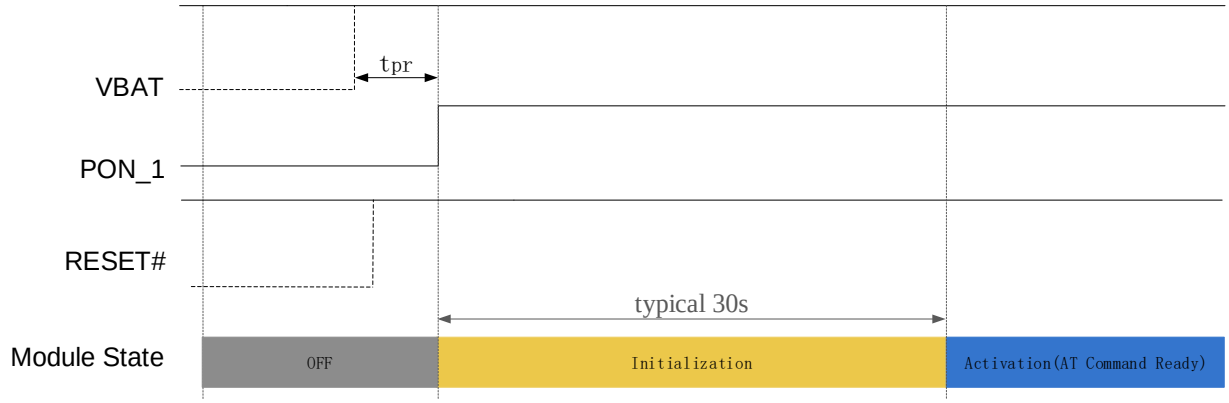


Figure 5. Timing control for start-up mode 1

Index	Min.	Recommended	Max.	Comments
t_{pr}	0ms	--	--	The delay time of power supply rising from 0V up to 3.3V. If power supply always ready, it can be ignored

- Mode 2

When the module is in shutdown mode, pull down PWRKEY with pulse to enable the module to start.

The way to control the PWRKEY pin is directly through a push button switch. A TVS (EGA10402V05AH-A recommended) should be placed near the button for ESD protection. The reference circuit is shown below:

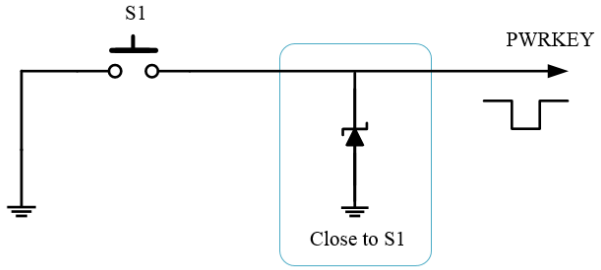


Figure 6. Start-up circuit 2

The start-up timing sequence is shown in Figure 8:

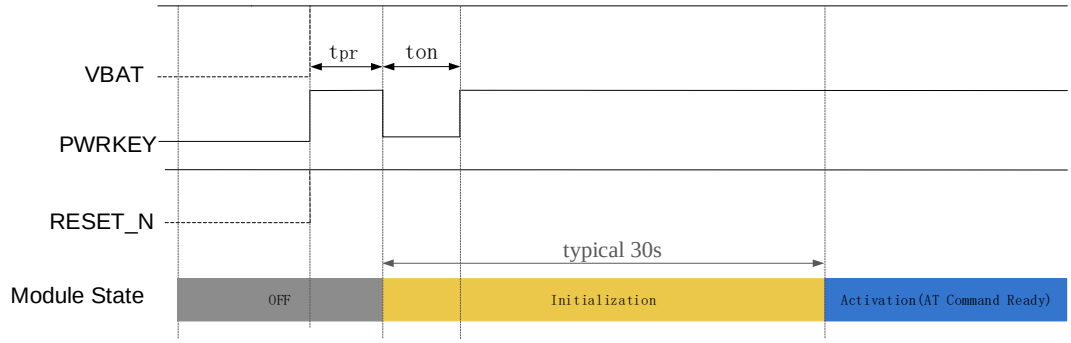


Figure 7. Timing control for start-up mode 2

Index	Min.	Recommended	Max.	Comments
t_{pr}	0ms	--	--	The delay time of power supply rising from 0V up to 3.3V. If

Index	Min.	Recommended	Max.	Comments
				power supply always ready, it can be ignored
t_{on}	1.2s	2s	3s	Pull down PWRKEY with pulse

Before pulling down the PWRKEY pin, ensure that the VBAT voltage is more than 3.3V.

5.2.1.2 Module Shutdown

The module supports the following two shutdown mode:

Table 12. Shutdown mode

Shutdown Type	Shutdown Method	Remark
Hardware shutdown	Pull down PON_1	Shutdown mode 1
	Pull down PWRKEY with pulse, then release	Shutdown mode 2

The shutdown mode 1 timing sequence is shown in Figure 9.

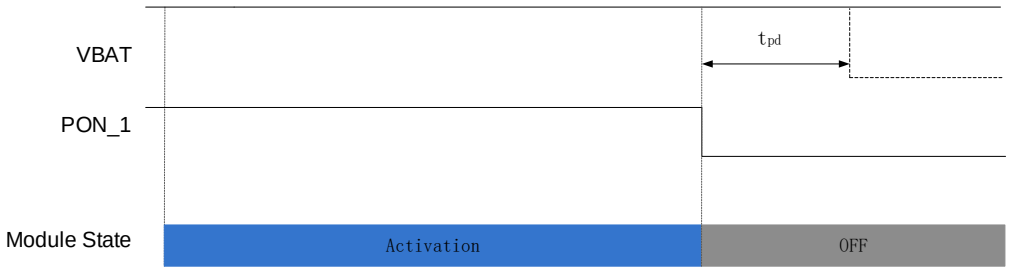


Figure 8. Timing control for shutdown

Index	Min.	Recommended	Max.	Comments
T_{pd}	0	--	--	Pull down PON_1 to shutdown module

The shutdown mode 2 timing sequence is shown in Figure 10.

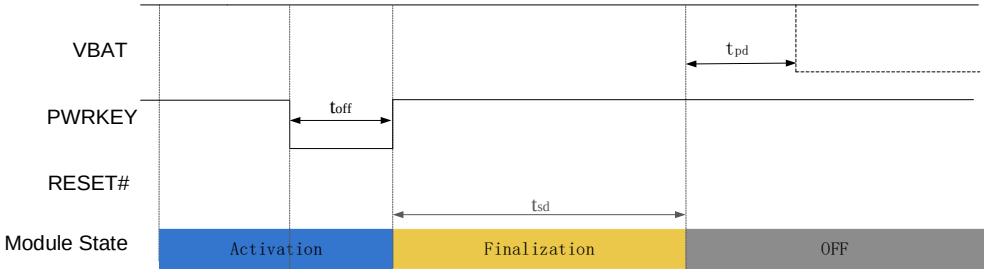


Figure 9. Shutdown timing

Index	Min.	Recommended	Max.	Comments
T_{off}	3s	--	5s	Pull down PWRKEY with pulse
T_{pd}	10ms	100ms		VBAT power supply goes down time. If power supply is always on, it can be ignored

After the PWRKEY signal is released, the next power-on trigger can be performed at least 2 seconds later. This interval is reserved for the module shutdown process and the power release of the peripheral circuit connecting with module interface.

5.2.2 Module Reset

There is a type of module reset: hardware reset

Table 13. Reset method

Reset type	Reset method
Hardware reset	Pull down the RESET_N pin with pulse, then release

The reference circuits are shown in the figure:

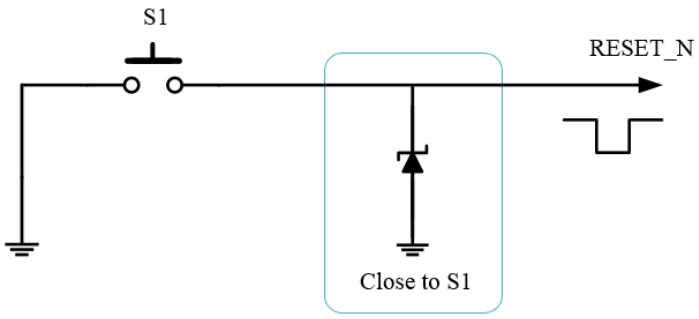


Figure 10. Reset circuit

Reset timing sequence is shown in the figure：

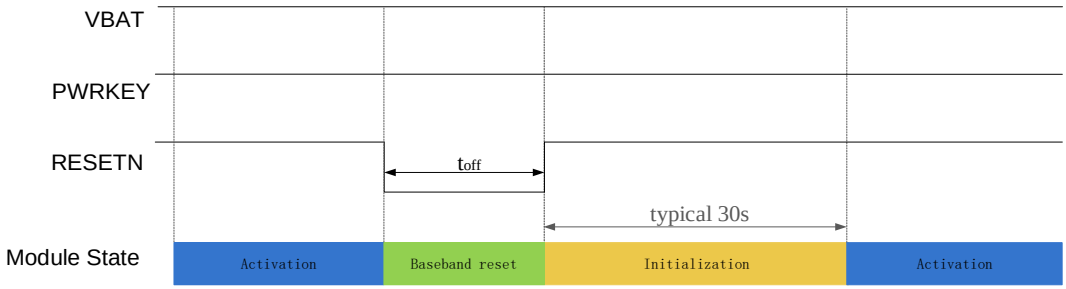


Figure 11. Reset timing

Index	Min.	Recommended	Max.	Comments
t_{off}	0.5s	1s	--	Pull down the RESET_N pin with pulse, then release

30 seconds minimum before next reset operation. The RESET_N pin of module has internal pull-up, no need external pull-up.

5.3 Network Status Indicator Interface

The module provides four status indicator signal interfaces. The pin definition is shown in following Table.

Table 14. Status indicator pin

Pin Name	Pin No	I/O	Description
5G_STATUS	H16	DO	5G status indicator
4G_STATUS	B18	DO	4G status indicator
STATUS	J9	DO	Module status indicator Module power on: high level Module power off: low level

5.3.1 Interface Status Description (Reserved)

The network status indicator interface is used to drive the status indicator, which is used to indicate the network status of the module as following table.

Table 15. Status indicator output mode

Mode	Module Network Status	Indicator Pin status	LED Status
1	Data T-put transfer	75ms high level / 75ms low level	Flash, 75ms on / 75ms off
2	Network ready	High level	on
3	Network not ready	Low level	off

The network status indicator reference circuit is as follows:

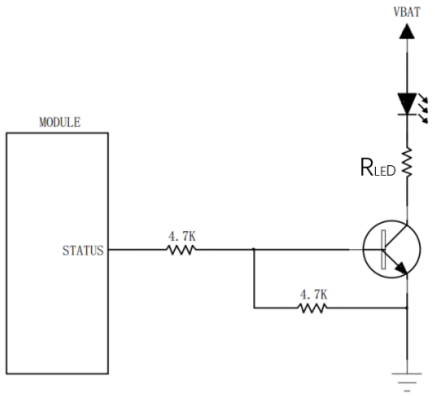


Figure 12. Indicator drive circuit diagram

The LED brightness depends on resistance of R_{LED}.

5.4 SIM Card Interface

The FG370 module have two SIM card interface and can supports 1.8V and 3.0V SIM cards, but only support dual sim cards, single standby.

5.4.1 SIM Card Interface Definition

SIM pin definition is shown in the following table:

Table 16. SIM pin definition

Pin name	Pin No	I/O	Description
SIM1_VDD	AR11	PO	SIM1 power output, 3V/1.8V
SIM1_DATA	AR7	DIO	SIM1 data signal
SIM1_CLK	AR5	DO	SIM1 clock signal
SIM1_RST	AP8	DO	SIM1 reset signal
SIM1_DET	AN7	DI	SIM1 insert detection signal, internal 390K pull-up. Active high, high level indicates SIM card inserted and low level indicates SIM card plugged out.
SIM2_VDD	AP12	PO	SIM2 power output, 3V/1.8V
SIM2_DATA	AP10	DIO	SIM2 data signal
SIM2_CLK	AR9	DO	SIM2 clock signal
SIM2_RST	AN9	DO	SIM2 reset signal
SIM2_DET	AP6	DI	SIM2 insert detection signal, internal 390K pull-up. Active high, high level indicates SIM card inserted and low level indicates SIM card plugged out.

5.4.2 SIM Card Interface Circuit

SIM card interface reference circuit is shown in Figure 14.

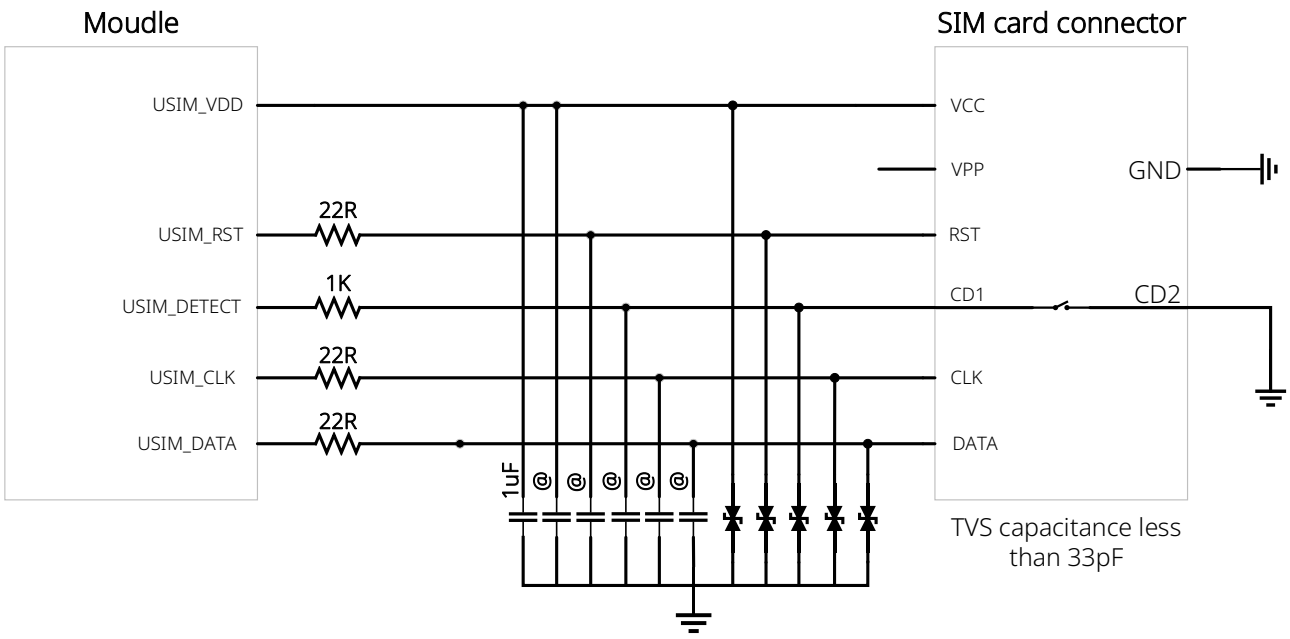


Figure 13. SIM interface reference circuit

The SIM card slot of Figure 14 is normally closed, when the SIM card is detached, CD pin is connected to GND pins, so the CD pin is low. When the SIM card is inserted, CD pin is not connected to GND pins, and pulled high by FG370 module.

5.5 USB Interface

FG370 module supports USB3.2, USB2.0, compatible with USB1.1.

5.5.1 USB Interface Definition

Table 17. USB interface pin definition

Pin Name	Pin No	I/O	Description
SSUSB_TXN	AD2	AO	USB super speed transmit data minus
SSUSB_TXP	AC1	AO	USB super speed transmit data plus
SSUSB_RXN	AF2	AI	USB super speed receive data minus
SSUSB_RXP	AE3	AI	USB super speed receive data plus
USB_DM	AC3	AIO	USB high speed data minus
USB_DP	AD4	AIO	USB high speed data plus
VBUS_DET	A25	DI	USB VBUS detection
USB_DRVBUS	AJ1	DO	USB OTG power enable
USB_ID	AK2	DI	USB ID

5.5.2 USB Interface Circuit

USB interface reference circuit is shown below:

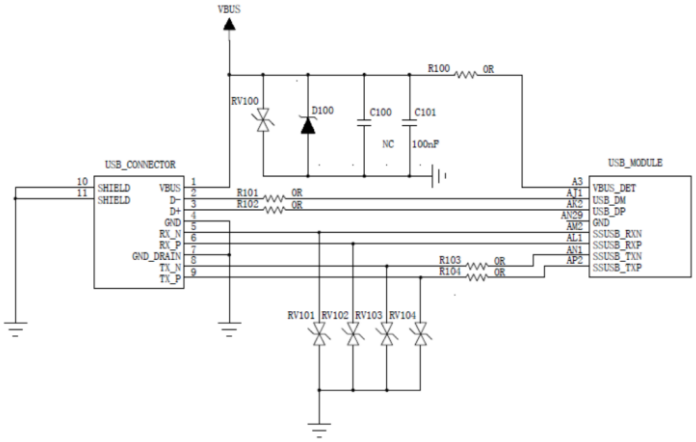


Figure 14. USB interface reference design

5.5.3 USB Routing Rules

5.5.3.1 USB2.0 Routing Rules

- The USB_DM / USB_DP trace length mismatch is controlled within ≤ 50mil, and the differential impedance is controlled as 90Ω ± 10%.
- USB_D- and USB_D+ signal lines should be routed on the layer that is adjacent to the ground layer, and wrapped with GND vertically and horizontally.

5.5.3.2 USB3.2 Routing Rules

- SSUSB _RXP/N and SSUSB_TXP/N are two sets of differential signals, with differential impedance controlled as 90Ω ± 10%; the length match of the intra differential pair ≤ 5mil.
- The two pairs of differential signal lines should be routed on the layer that is adjacent to the ground layer, and wrapped with GND vertically and horizontally.

5.6 ADC Interface

The FG370 module provides two analog-to-digital conversion interfaces.

5.6.1 ADC Interface Definition

Table 18. ADC interface definition

Pin Name	Pin No	I/O	Description
ADC0	A21	AI	A/D conversion channel 0
ADC1	B20	AI	A/D conversion channel 1

5.6.2 ADC Electrical Characteristics

Table 19. ADC electrical characteristics

Pin Name	Input Voltage Range (V)	ADC Resolution (uV)
ADC0	0.04-1.78	450
ADC1	0.04-1.78	450

Please keep ADC signals connect to ground if not used.

5.7 Forced-download Interface

The FG370 module has a forced-download signal shown in the following table.

Table 20. Forced-download interface

Pin Name	Pin No	I/O	Description
USB_BOOT	E3	DI	Forced into USB download boot mode Default high, low active.

5.7.1 Configuration Signal Interface Circuit

Reference circuit is shown in Figure 16.

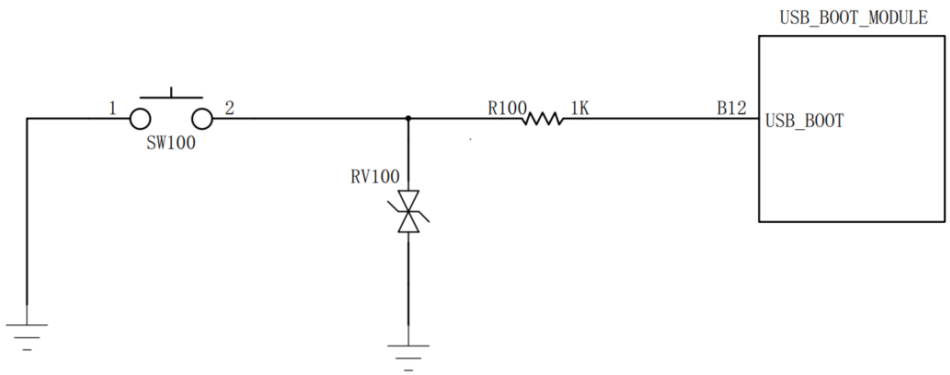


Figure 15. Configuration signal circuit

5.8 Flight Mode Control Interface (Reserved)

Pull down the W_DISABLE pin to enter flight mode

Table 21. Flight mode control pin

Pin Name	Pin No.	I/O	Description
W_DISABLE	C3	DI	Module flight mode control signal, reserved

5.9 GPIO Interface

Table 22. GPIO table

Pin Name	Pin No	Level	Pull Type	EINT	GPIO No
W_DISABLE	C3	1.8V	PD	Y	GPIO0
WAKEUP_IN	D4	1.8V	PD	Y	GPIO4
5G_STATUS	H16	1.8V	PD	Y	GPIO18
4G_STATUS	B18	1.8V	PD	Y	GPIO6
WIFI_STATUS	C15	1.8V	PD	Y	GPIO7
WWAN_STATUS	J9	1.8V	PD	Y	GPIO8
EINT15	K8	1.8V	PD	Y	GPIO15
GPS_PPS	J11	1.8V	PD	Y	GPIO145
EINT16	K10	1.8V	PD	Y	GPIO16
USB_VBUSVALID	AL1	1.8V	PD	Y	GPIO47

All GPIO in the table above can be used as interrupt ports and can be configured according to the requirements.

5.10 PCIE Interface

FG370 module supports 2 group, PCIE_A can support Gen4, 2-lane, RC mode. PCIE_B and can support Gen3, 2-lane, RC mode.

5.10.1 PCIe Interface Definition

Table 23. PCIe signal list

Pin Name	Pin No	I/O	Pin Description
PCIE_A_CLKN	T2	AIO	PCIe A reference clock minus
PCIE_A_CLKP	R3	AIO	PCIe A reference clock plus
PCIE_A_LN0_TXN	V2	AIO	PCIe A Tx0 minus
PCIE_A_LN0_TXP	U1	AIO	PCIe A Tx0 plus
PCIE_A_LN0_RXN	P8	AIO	PCIe A Rx0 minus
PCIE_A_LN0_RXP	R7	AIO	PCIe A Rx0 plus
PCIE_A_LN1_TXN	R1	AIO	PCIe A Tx1 minus

Pin Name	Pin No	I/O	Pin Description
PCIE_A_LN1_TXP	N1	AIO	PCIe A Tx1 plus
PCIE_A_LN1_RXN	M8	AIO	PCIe A Rx1 minus
PCIE_A_LN1_RXP	L7	AIO	PCIe A Rx1 plus
PCIE_A_PEWAKEN	A17	DI	PCIe A wake-up signal
PCIE_A_PERSTN	B12	DO	PCIe A reset signal
PCIE_A_CLKREQN	A15	DIO	PCIe A clock request signal
PCIE_B_CLKN	U3	AIO	PCIe B reference clock minus
PCIE_B_CLKP	T4	AIO	PCIe B reference clock plus
PCIE_B_LN0_TXN	Y2	AIO	PCIe B Tx0 minus
PCIE_B_LN0_TXP	AA3	AIO	PCIe B Tx0 plus
PCIE_B_LN0_RXN	U7	AIO	PCIe B Rx0 minus
PCIE_B_LN0_RXP	W7	AIO	PCIe B Rx0 plus
PCIE_B_LN1_TXN	AB2	AIO	PCIe B Tx1 minus
PCIE_B_LN1_TXP	AA1	AIO	PCIe B Tx1 plus
PCIE_B_LN1_RXN	V4	AIO	PCIe B Rx1 minus
PCIE_B_LN1_RXP	W3	AIO	PCIe B Rx1 plus
PCIE_B_PEWAKEN	A19	DI	PCIe B wake-up signal
PCIE_B_PERSTN	B14	DO	PCIe B reset signal
PCIE_B_CLKREQN	C13	DIO	PCIe B clock request signal

5.10.2 PCIE Routing Rules

The FG370 module supports one PCIe Gen4 group and one PCIe Gen3 groups, each group including five difference pairs: transmit pair TXP/N, receiving pair RXP/N and clock pair CLKP/N.
The PCIe Gen4 bus can up to 16 GT/s speed and PCIe Gen3 bus can up to 8 GT/s speed. The following rules should be followed strictly in PCB layout:

- The impedance of differential pair lines is recommended to be 85Ω ± 10%. The length match of the intra differential pair ≤ 5mil, The lane to lane skew ≤ 100mil.
- The differential signal pair lines shall be short if possible and be controlled within 8.5 inch (215.9 mm).

5.10.3 PCIE Application Circuit

TBD

5.11 USXGMII Interface

The FG370 module supports two groups USXGMII interface and data transmission rate up to 10G bps, and is matched with PHY IC.

5.11.1 USXGMII Interface Definition

Table 24. USXGMII signal list

Pin Name	Pin No	I/O	Pin Description
USXGMII_1_RXN	E5	AIO	USXGMII 1 receive data minus
USXGMII_1_RXP	F4	AIO	USXGMII 1 receive data plus
USXGMII_1_TXN	M4	AIO	USXGMII 1 transmit data minus
USXGMII_1_TXP	N3	AIO	USXGMII 1 transmit data plus
GBE1_INT	A3	DI	USXGMII 1 interrupt input signal
GBE1_RST	A7	DO	USXGMII 1 reset signal
USXGMII_0_RXN	M2	AIO	USXGMII 0 receive data minus
USXGMII_0_RXP	L3	AIO	USXGMII 0 receive data plus
USXGMII_0_TXN	H4	AIO	USXGMII 0 transmit data minus
USXGMII_0_TXP	K4	AIO	USXGMII 0 transmit data plus
GBE0_INT	C5	DI	USXGMII 0 interrupt input signal
GBE0_RST	D30	DO	USXGMII 0 reset signal
USXGMII_PWR_EN1	F10	DO	USXGMII power supply enable 1
MDIO	B30	DIO	USXGMII MDIO signal
MDC	C29	DO	USXGMII MDC signal

5.11.2 USXGMII Routing Rules

USXGMII can up to the maximum transmission rate of 10G bps. The following rules should be followed strictly in PCB layout:

- The impedance of differential pair lines is recommended to be 100Ω ± 10%. The length match of the intra differential pair ≤5mil;
- The differential signal pair lines shall be short if possible and be controlled within 8 inch (203.2 mm).

5.11.3 USXGMII Application Circuit

TBD

5.12 SD Interface

FG370 module supports SD interface, the standard is as follows:
Physical Layer Specification version 3.0, SDIO Card Specification version 3.0

5.12.1 SD Interface Definition

Table 25. SD signal list

Pin Name	Pin No	I/O	Pin Description
SDC_DATA0	H20	DIO	SDC interface DATA0 signal, reserved
SDC_DATA1	J19	DIO	SDC interface DATA1 signal, reserved
SDC_DATA2	J21	DIO	SDC interface DATA2 signal, reserved
SDC_DATA3	H18	DIO	SDC interface DATA3 signal, reserved
SDC_CMD	J23	DIO	SDC interface command signal, Reserved
SDC_CLK	H22	DO	SDC interface clock signal, reserved
VSD1V8_EXT	H24	PI	Digital power for FG370 SD interface, reserved
SDIO_VDD	G23	PO	SD card IO interface Power, reserved

5.12.2 SD Interface Routing Rules

The length of the signal line is controlled to ≤ 3000mil, and the difference between the length of the clock signal and the data signal is controlled to ≤ 200mil.

5.12.3 SD Interface Application Design

TBD

5.13 I2C Interface

The FG370 module supports one I2C interface, applying the standard *I2C Specification, version 3.0*

Table 26. I2C Interface Definition

Pin Name	Pin No	I/O	Pin Description
I2C_SDA0	D8	DIO	I2C0 data
I2C_SCL0	D6	DO	I2C0 clock
I2C_SDA1	D10	DIO	I2C1 data
I2C_SCL1	D12	DO	I2C1 clock

5.14 I2S Interface

The FG370 module supports one I2S interface. The default is I2S, which can be configured as a PCM interface.

The default sampling rate is 48KHz. Applied Standards *Philips I2S Bus Specifications revised June 5, 1996.*

Table 27. I2S interface definition

Pin Name	Pin No	I/O	Pin Description
I2S0_DO	AP4	DO	I2S data output signal, can be defined as PCM_OUT
I2S0_DI	AN1	DI	I2S data input signal, can be defined as PCM_IN
I2S0_BCK	AM4	DO	I2S data bit clock signal, can be defined as PCM_CLK
I2S0_LRCK	AN3	DO	I2S frame clock signal, can be defined as PCM_SYNC
I2S0_MCK	AP2	DO	I2S main clock, used for external audio codec

5.15 UART Interface

The FG370 module supports three UART interfaces which defined in the following tables.

Table 28. UART interface 1

Pin Name	Pin No	I/O	Pin Description
DBG_UART_TX	D28	DO	UART transmit signal
DBG_UART_RX	C27	DI	UART receive signal

Table 29. UART interface 2

Pin Name	Pin No	I/O	Pin Description
AP_UCTS2	F26	DI	UART receive ready signal
AP_URTS2	F24	DO	UART transmit request signal
AP_UTXD2	G25	DO	UART transmit signal
AP_URXD2	D26	DI	UART receive signal

Table 30. UART interface 3

Pin Name	Pin No	I/O	Pin Description
BT_UTXD	C25	DO	UART transmit signal
BT_URXD	D24	DI	UART receive signal
BT_URTS	C23	DO	UART transmit request signal
BT_UCTS	D22	DI	UART receive ready signal

UART interface 1 is debug UART port, used to access the main chip kernel and print log information, and baud rate is 921600.
UART interface 2 is general UART port used to send transmission of information

UART interface 3 is BT UART port, used to transmission of BT information

5.16 SPI Interface

The FG370 module supports 1 SPI interface, works in master mode, and the clock supports up to 52MHz.

Table 31. SPI interface definition

Pin Name	Pin No	I/O	Pin Description
SPI3_MISO	H8	DI	SPI interface input signal
SPI3_MOSI	G7	DO	SPI interface output signal
SPI3_CSB	J7	DO	SPI interface chip select signal
SPI3_CLK	F8	DO	SPI interface clock signal

5.17 Other Interfaces

For the application of other interfaces, please refer to the recommended design. If the application scenario and the recommended design are not consistent, please contact our technicians for confirmation.

6 Electrostatic Protection

In the application of the module, due to static electricity generated by human body and charged friction between micro-electronics, etc. discharging to the module through various channels that may cause damage, so ESD protection should be taken seriously attention. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken. For example, anti-static protection should be added at the designed circuit interface and the points susceptible to electrostatic discharge or impact. Anti-static gloves should be worn during production.
ESD performance parameters are as follows (temperature: 25 ° C, humidity: 45%)

Table 32. ESD performance

Test Point	Contact Discharge	Air Discharge	Unit
GND	±8	±15	KV
RF Antenna Interface	±8	NA	KV
Other pins	±1	NA	KV

The data is based on the test of FIBOCOM ADP-FG370-NA development board.
ESD performance is related to PCB design. Pay special attention to the protection of important control signals such as reset signals and the preservation of the complete ground plane.

7 Thermal Design

FG370 is designed to work on an extreme temperature range, to make sure the module can work properly for a long time and achieve a better performance on conditions like maximum power or high data transmission.

8 Structural Specification

8.1 Product Appearance

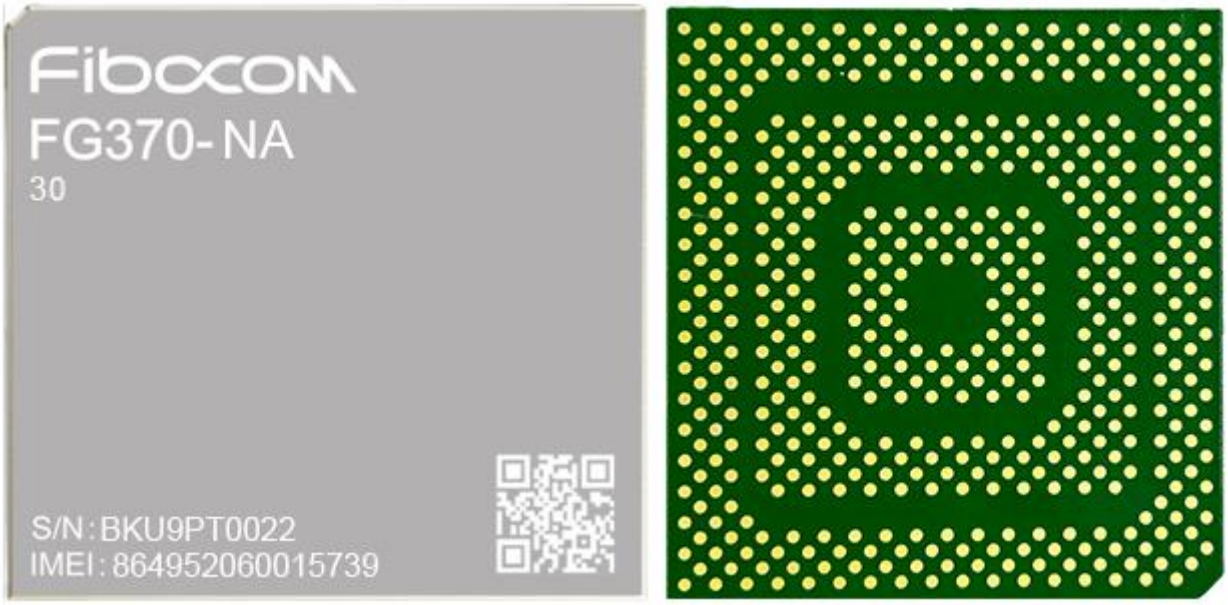


Figure 16. Module product appearance

8.2 Dimension of Structure

The structural dimensions of the FG370 module are shown in the figure:

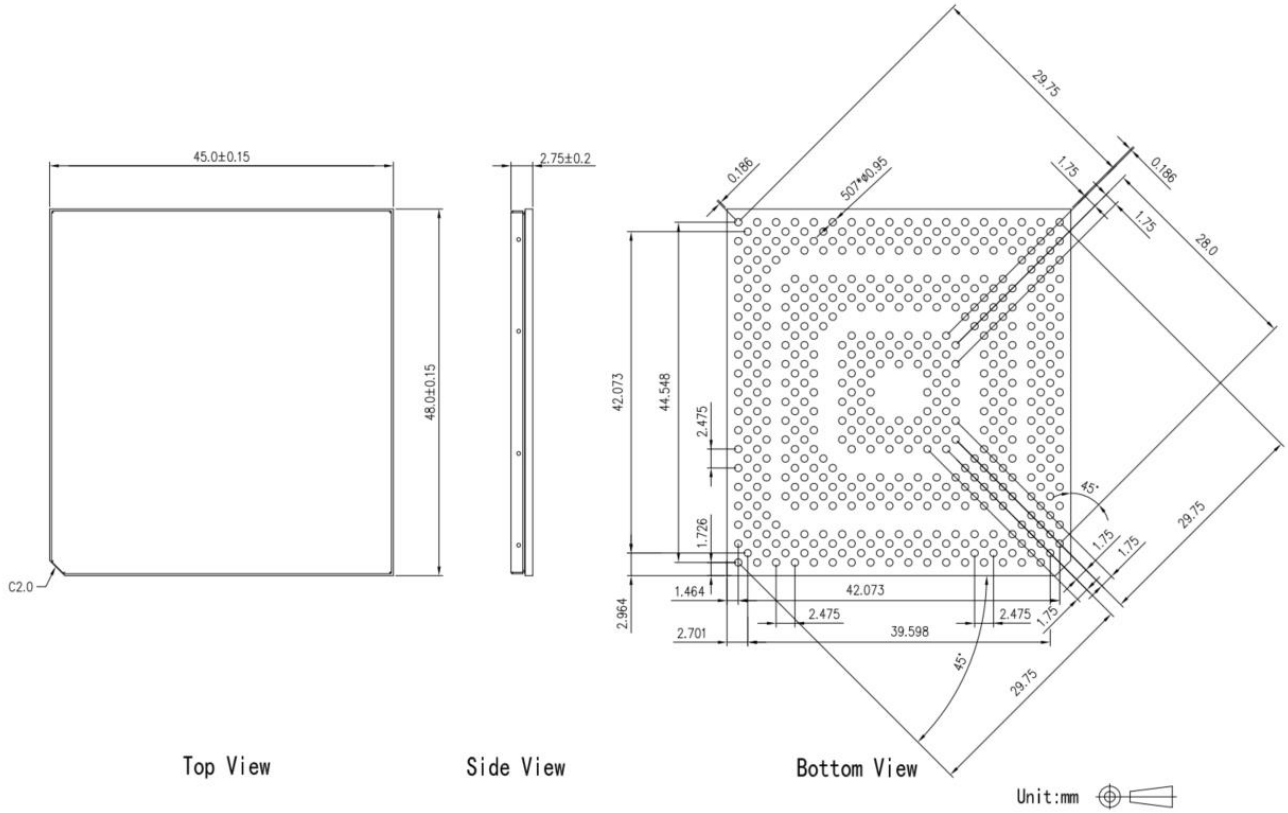


Figure 17. Structure size chart

Unmarked dimensional tolerances are 0.1 mm.

8.3 Storage

Refer to *Fibocom_FG370_SMT Design Guide.*

8.4 Packing

Refer to *FIBOCOM _FG370_SMT Design Guide.*