5.3. WIRELESS SPECIFICATIONS

The WM-BN-BM-01 module complies with the following features and standards;

Features	Description
WLAN Standards	IEEE 802 Part 11b/g/n (802.11b/g/n[a])
Antenna Port	Support Single Antenna for WiFi
Frequency Band	2.400 GHz – 2.484 GHz

◆ a: 802.11n in this module only support HT20

5.4. RADIO SPECIFICATIONS 802.11B/G/N

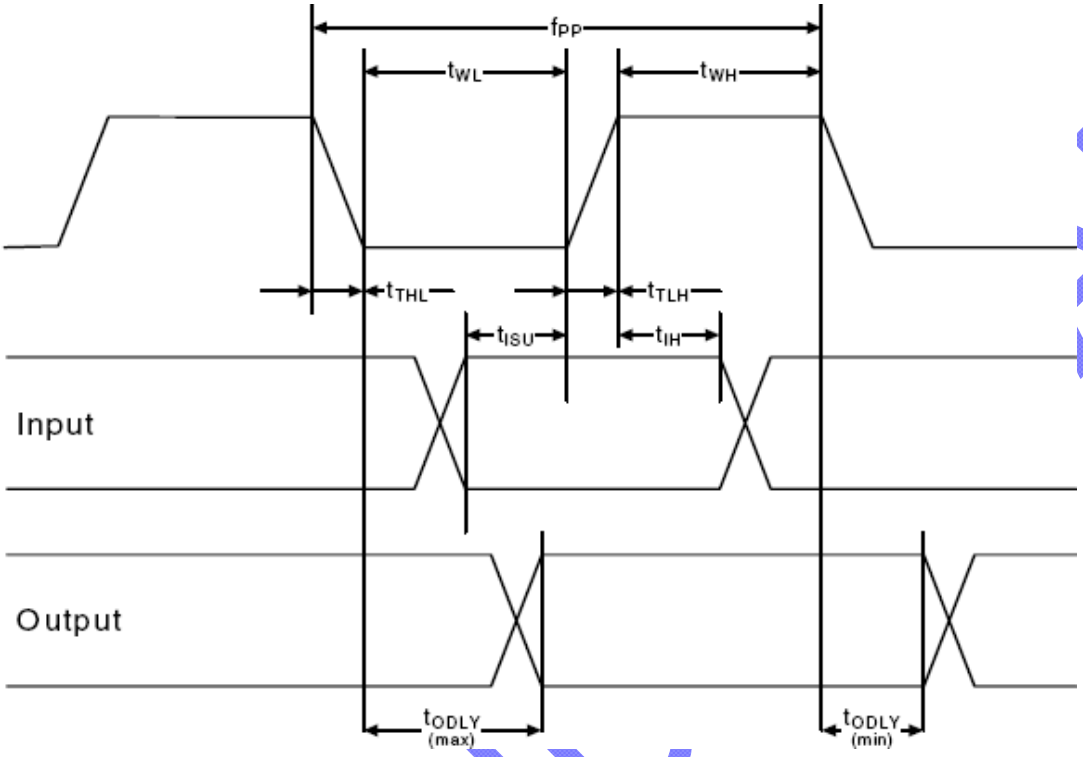
Features	Description
Frequency Band	2.4000 GHz – 2.497 GHz (2.4 GHz ISM Band)
Number of selectable Sub channels	14 channels
Modulation	OFDM, DSSS (Direct S equence Spread Spectrum), DBPSK, DQPSK, CCK , 16QAM, 64QAM
Supported rates	1,2, 5.5,11,6,9,12,24,36,48,54 Mbps
Maximum receive level	-10dBm (with PER < 8%)
Output Power	17 dBm +2.0/-2.0 dBm for 802.11b 15 dBm +2.0/-2.0 dBm for 802.11g 15 dBm +2.0/-2.0 dBm for 802.11n
Wide-Band Noise	-160 dBm/Hz (max.)@869 MHz~960 MHz -160 dBm/Hz (max.)@1800 MHz~1990 MHz -152 dBm/Hz (max.)@2110 MHz~2170MHz

EVM:

Characteristic		Typical	Maximum	Unit
RF Average Output EVM (11b)	@11 Mbps	-13	-10	dB
	@1 Mbps	-13	-10	dB
RF Average Output EVM (11g)	@54 Mbps	-30	-25	dB
	@6 Mbps	-30	-25	dB
RF Average Output EVM (11n)	@ MCS7	-30	-28	dB
	@ MCS0	-30	-25	dB

SDIO TIMING

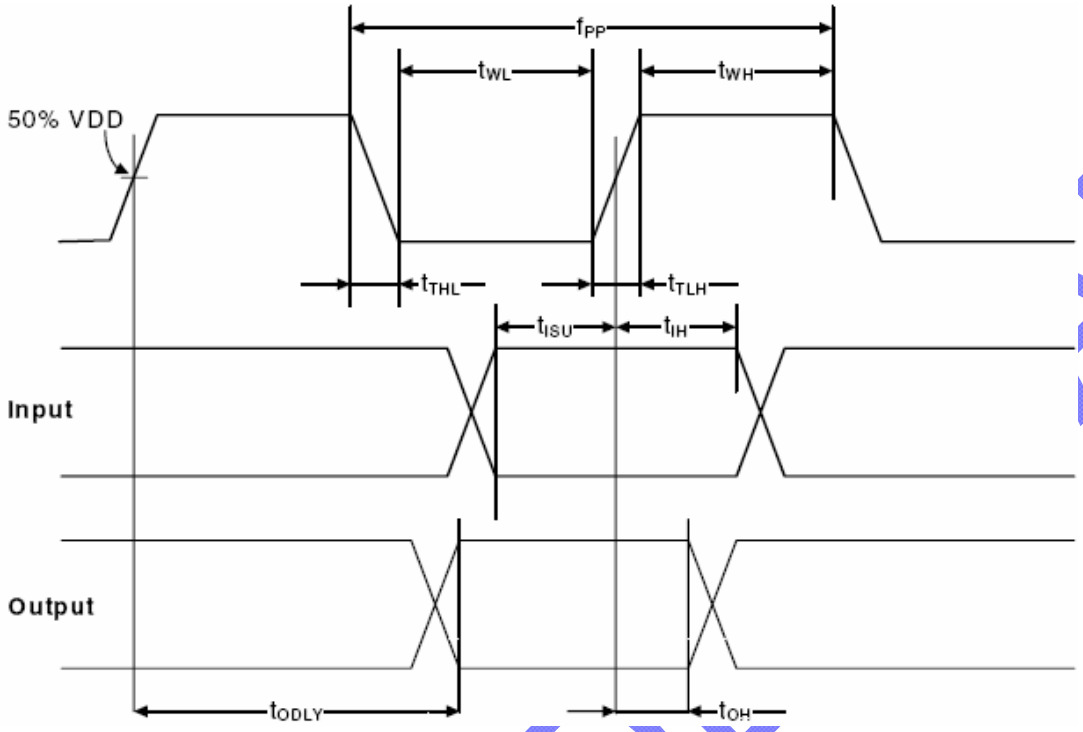
SDIO timing in default mode



SDIO Bus Timing Parameters (Default Mode)

Parameter	Symbol	Min	Typical	Max	Unit
Clock CLK (All values are referred to min. VIH and max. VIL)					
Frequency--Data Transfer Mode	fPP	0	-	25	MHz
Frequency--Identification Mode	fOD	0	-	400	kHz
Clock Low Time	tWL	10	-	-	ns
Clock High Time	tWH	10	-	-	ns
Clock Rise time	tTLH	-	-	10	ns
Clock Low Time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input Setup Time	tISU	5	-	-	ns
Input Hold Time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output Delay time--Data Transfer Mode	tODLY	0	-	14	ns
Output Delay time--Identification Mode	tODLY	0	-	50	ns

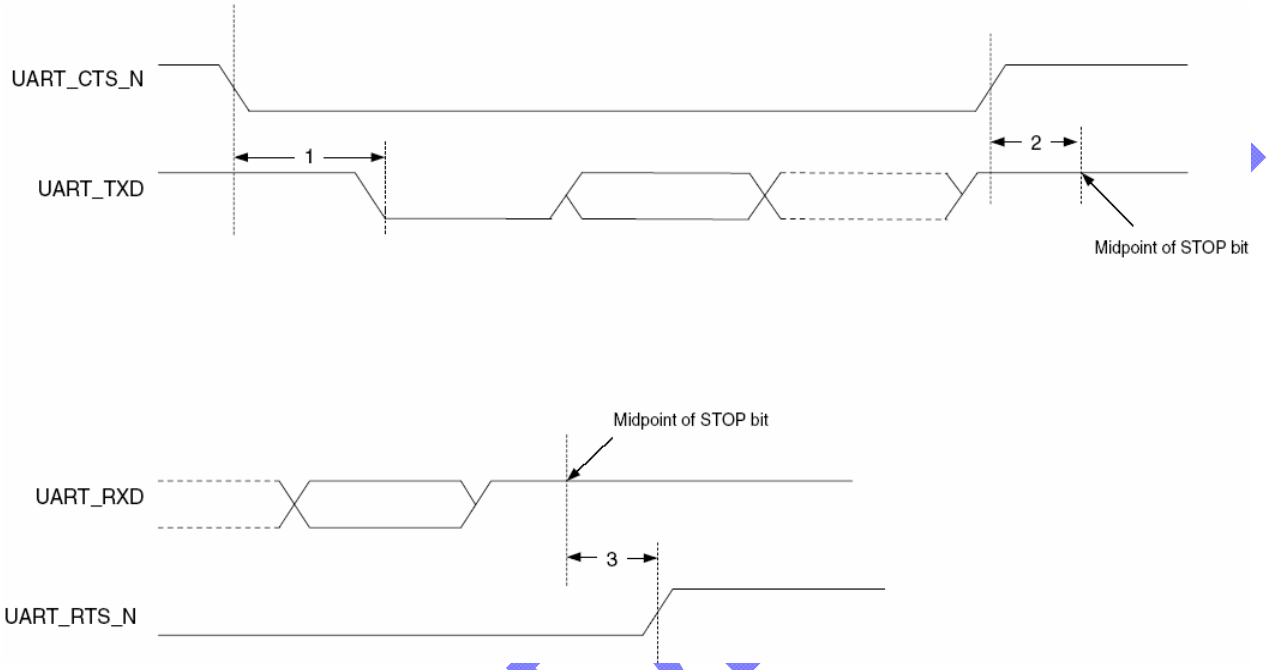
SDIO timing in High-Speed Mode



SDIO Bus Timing Parameters (High-Speed Mode)

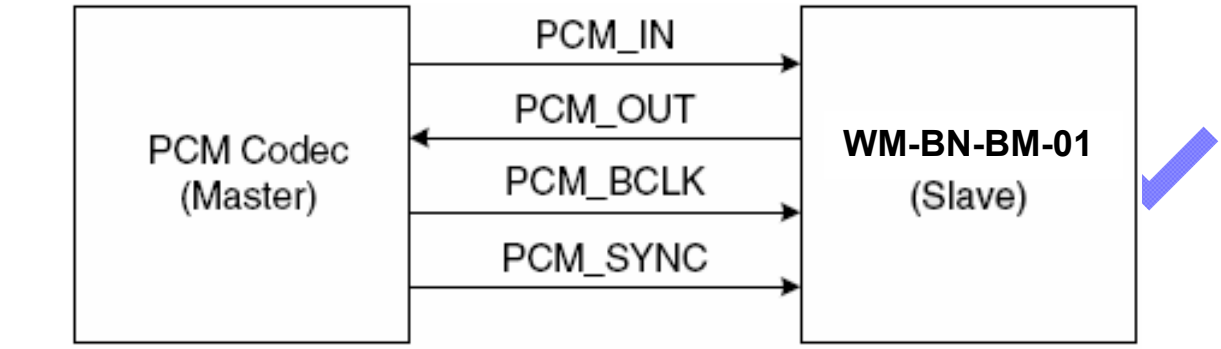
Parameter	Symbol	Min	Typical	Max	Unit
Clock CLK (all values are referred to min. VIH and max. VIL)					
Frequency--Data Transfer Mode	fPP	0	-	50	MHz
Frequency--Identification Mode	fOD	0	-	400	kHz
Clock Low Time	tWL	7	-	-	ns
Clock High Time	tWH	7	-	-	ns
Clock Rise time	tTLH	-	-	3	ns
Clock Low Time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input Setup Time	tISU	6	-	-	ns
Input Hold Time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output Delay time--Data Transfer Mode	tODLY	-	-	14	ns
Output Hold time	tOH	2.5	-	-	ns
Total System Capacitance (each line)	CL	-	-	40	pF

UART Timing

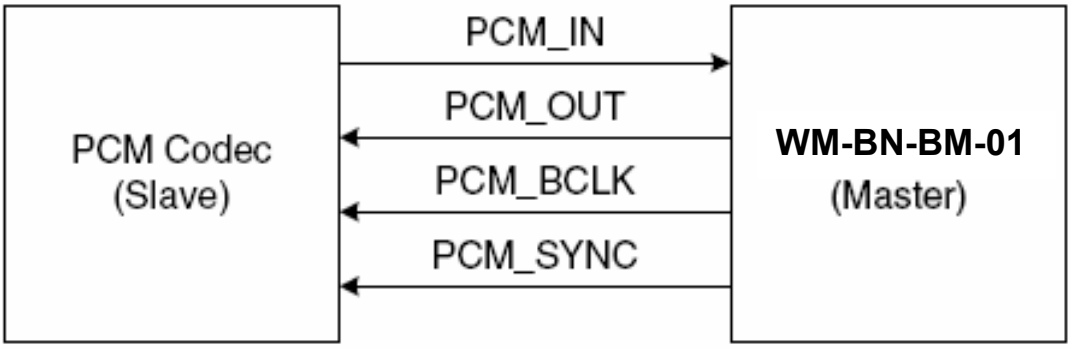


Reference	Description	Min	Typ	Max	Unit
1	Delay time, BT_UART_CTS_N low to UART_TXD valid	-	-	24	Baudout cycles
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	-	-	10	ns
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	-	-	2	Baudout cycles

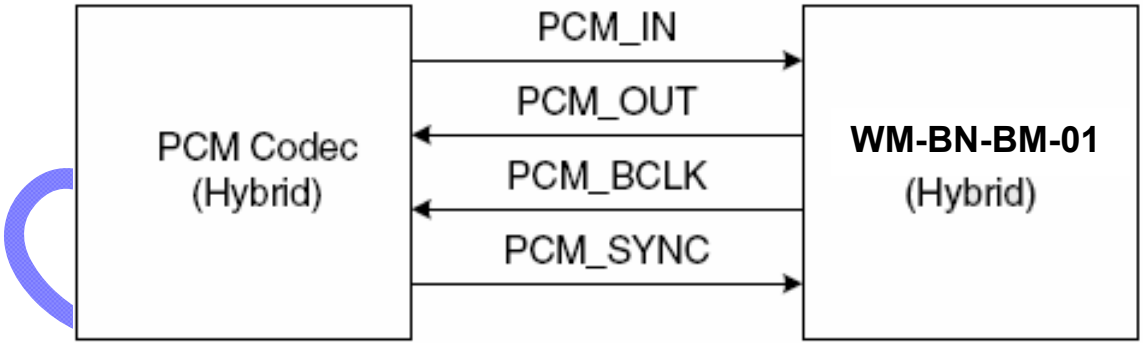
PCM INTERFACE TIMING



PCM Interface Slave Mode



PCM Interface Master Mode



.

Pin-Nmnber	Pin-Define	Type	Description
1	GND	I	Ground
2	GND	I	Ground
3	SW_RX2	O	Control signal for Antenna Diversity RF2
4	SW_RX1	O	Control signal for Antenna Diversity RF1
5	TDO	I	For debug only
6	TAG_TRST_N	I	For debug only
7	WL_RST_N	I	Low asserting reset for WLAN core
8	TCK	I	For debug only
9	TMS	I	For debug only
10	WL_GPIO_1	O	HOST_WAKE Host wake up: Signal from the module to the host indicating that the module requires attention. • Asserted: Host device must wake-up or remain awake. • Deasserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
11	WL_GPIO_0	I	WLAN_WAKE WLAN device wake-up: Signal from the host to the module indicating that the host requires attention. • Asserted: WLAN device must wake-up or remain awake. • Deasserted: WLAN device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
12	TDI	I	For debug only
13	VDDIO	I	Digital I/O supply (1.8V ~ 3.3V)
14	XTAL_PU	O	Crystal circuit/reference clock enable (programmable polarity, default is active high)
15	SDIO_CLK	I/O	SDIO clock. This pin has an internal weak pull-up resistor.
16	VDDIO_SD	I	SDIO/SPI I/O supply (1.8V ~ 3.3V)
17	SDIO_D0	I/O	SDIO data 0. This pin has an internal weak pull-up resistor.
18	SDIO_D2	I/O	SDIO data 2. This pin has an internal weak pull-up resistor.
19	SDIO_CMD	I/O	SDIO command. This pin has an internal weak pull-up resistor.