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JULY 2011

BTM160

Bluetooth QD ID : B018233 (End Product Listing)
FCC ID : ZDSBTM160
IC : 9583A-BTM160

Class 2 BC04-ext Mini Module

Wireless Modules

User's Manual

Hardware Description
Revision 1.3

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1. General Device Overview

1.1 Features

General

- The module is a Max.4dBm(Class2) module.
- Low current consumption : Hold,Sniff,Park,Deep sleep Mode
- 3.0V or 1.8V operation
- Interface: USB,UART&PCM(for voice CODEC)
- Support for 802.11 Co-Exsitence
- RoHS compliant
- Small outline. 14 x 12 x 2.2 mm

Interfaces

- USB v2.0
- Standard RS232 UART for communicating with other devices : 1200 baud to 3Mbaud
- Serial Peripheral Interface (SPI)

RF

- Transmit power typ. 2.0 dBm
- Receiver sensitivity typ. -83 dBm
- Integrated channel filters
- Supports pi/4 DQPSK (2Mbps) and 8DPSK (3Mbps) modulation

Bluetooth

- Bluetooth standard Ver. 2.1 + EDR compliant.
- Support for up to seven slaves : SCO links<3>,ACL links,Piconet<7>
- HCI or SPP,HSP/HFP,HID,DUN firmware is available

1.2 Block Diagram

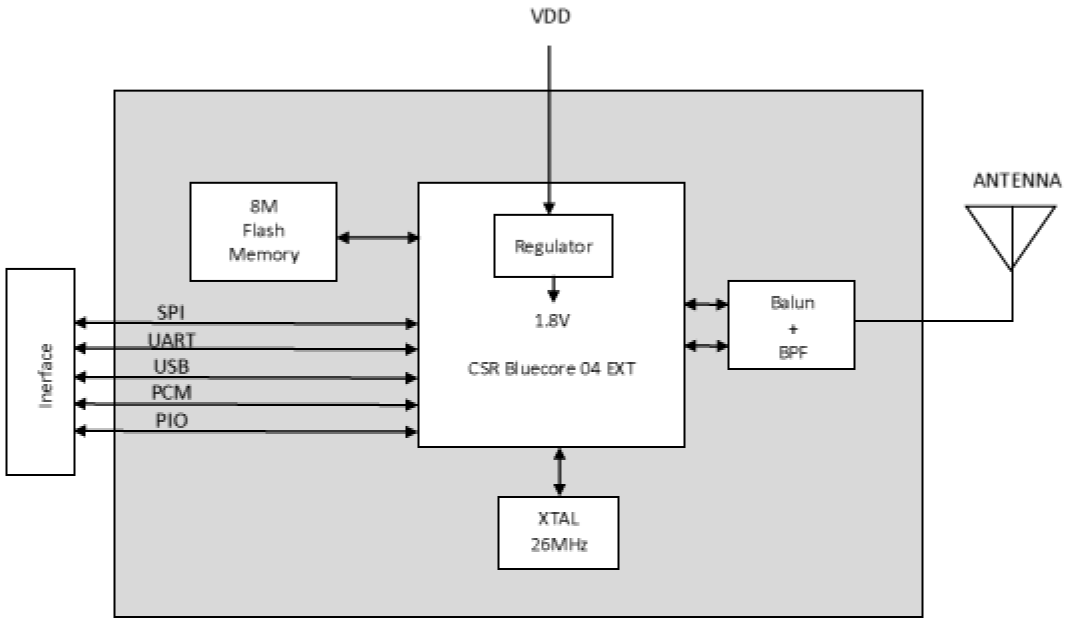


Figure 1 Simplified Block Diagram of BTM160

1.3 Pin Configuration

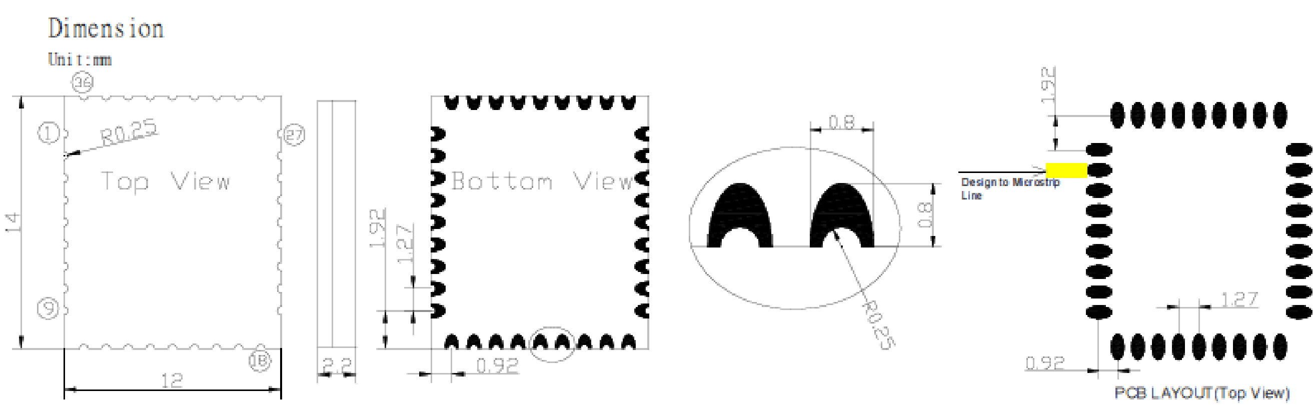


Figure 2 Pin Configuration for the BTM160 and PCB Layout

1.4 Pin Description

PIN	NAME	TYPE	FUNCTION
1	GND	GND	Ground
2	RF_IO	Analogue	Antenna Interface
3	GND	GND	Ground
4	PIO(11)	Bi-directional	Programmable Input/Output line
5	PIO(10)	Bi-directional	Programmable Input/Output line
6	PIO(9)	Bi-directional	Programmable Input/Output line
7	PIO(8)	Bi-directional	Programmable Input/Output line
8	PIO(2)	Bi-directional	Programmable Input/Output line
9	AIO(1)	Bi-directional	Programmable Input/Output Line
10	GND	GND	Ground
11	VDD	Power	3.3V or 1.8V Power Supply Input
12	AIO(0)	Bi-directional	Programmable Input/Output Line , 32KHz sleep clock input
13	UART_TX	CMOS Input	UART Data Output
14	UART_RTS	CMOS Output	UART Request To Send (Active Low)
15	UART_RX	CMOS Output	UART Data Input
16	UART_CTS	CMOS Input	UART Clear To Send (Active Low)
17	USB_DP	Bi-directional	USB Data Plus
18	USB_DN	Bi-directional	USB Data Minus
19	PCM_CLK	Bi-directional	Synchronous Data Clock
20	PCM_IN	CMOS Input	Synchronous Data Input
21	PCM_OUT	CMOS Output	Synchronous Data Output
22	PCM_SYNC	Bi-directional	Synchronous Data Sync
23	VDD_USB	Power	3.3V Power Supply Input
24	PIO(7)	Bi-directional	Programmable Input/Output line
25	PIO(6)	Bi-directional	Programmable Input/Output line , CLK_REQ , WLAN_Ative/Ch_Data input
26	PIO(5)	Bi-directional	Programmable Input/Output line , USB_DETACH, BT_Ative output
27	PIO(4)	Bi-directional	Programmable Input / Output Line , USB_ON, BT_Priority/Ch_Clk Output
28	GND	GND	Ground
29	RESETB	CMOS input	Reset if low. Input debounced so must be low for >5ms to cause a reset
30	SPI_CSB	CMOS Input	Chip Select For Synchronous Serial Interface active low
31	SPI_MOSI	CMOS Input	Serial Peripheral Interface Data Input
32	SPI_MISO	CMOS Output	Serial Peripheral Interface Data Output
33	SPI_CLK	CMOS Input	Serial Peripheral Interface Clock
34	PIO(3)	Bi-directional	Programmable Input/Output Line , USB_WAKE_UP, CLK_REQ_IN
35	PIO(1)	Bi-directional	Programmable Input/Output Line , TX Enable
36	PIO(0)	Bi-directional	Programmable Input / Output Line , RX Enable

Table 1 Pin Description

1.5 Firmware

The BlueCore4 chip is supplied with Bluetooth v2.1 + EDR compliant stack firmware, which runs on the internal RISC microcontroller.
The BlueCore4 chip software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any). The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

2 Basic Operating Information

2.1 Power Supply

The BTM160 is supplied from a single supply voltage VDD. This supply voltage must always be present.
The CSR Bluecore 4 chip utilizes an internally generated 1.8 V supply voltage. This voltage can be accessed from the 1.8v pin. This voltage may not be used for supplying other components in the host system.

All digital I/O pins on the CSR chip are supplied internally by the1.8 V supply, except for VDD_PADS, which supplies the digital I/O ports other than PIO.

2.2 Clocking

BTM160 contains a 26MHz crystal from which the internal system clock for the Bluecore4 chip is generated.

3 Physical Description

3.1 RF Receiver

The receiver features a near-zero IF architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input allows the radio to be used in close proximity to GSM and WCDMA cellular phone transmitters without being desensitized. The use of a digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore4 chip to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.
For EDR, an ADC is used to digitize the IF received signal.

3.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1 Bluetooth operation; differential mode is used for Class 2 operation.

3.1.2 Analog to Digital Converter

The ADC is used to implement fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

3.2 RF Transmitter

3.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimize the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

3.2.2 Power Amplifier

The internal PA has a maximum output power of 6dBm. This allows BlueCore4 chip to be used in Class 2 and Class 3 radios without an external RF PA.
Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

3.3 RF Synthesizer

The radio synthesizer is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesizer is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.1 + EDR specification.

3.4 Clock Input and Generation

The reference clock for the system is generated from a crystal input of 26MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

3.5 Baseband and Logic

3.5.1 Memory Management Unit

The MMU provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimize the overheads on the processor during data/voice transfers.

3.5.2 Burst Mode Controller

During radio transmission the BMC constructs a packet from header information previously loaded into memory mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimizes the intervention required by the processor during transmission and reception.

3.5.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/µ-law/linear voice data (from host)
- A-law/µ-law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatch correction

The hardware supports all optional and mandatory features of Bluetooth v2.1 + EDR including AFH and eSCO.

3.5.4 System RAM

48KB of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

3.5.5 External Memory Driver

The External Memory Driver interface can be used to connect to the external Flash memory and also to the optional external RAM for memory intensive applications.

3.5.6 USB

This is a full-speed USB interface for communicating with other compatible digital devices. BlueCore4 chip acts as a USB peripheral, responding to requests from a master host controller such as a PC.

3.5.7 Synchronous Serial Interface

3.5.8 UART

This is a standard UART interface for communicating with other serial devices.

3.6 Microcontroller

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit RISC microcontroller is used for low power consumption and efficient use of memory.

3.6.1 Programmable I/O

BlueCore4 chip has a total of 15 (12 digital and 3 analog) programmable I/O terminals. These are controlled by firmware running on the device.

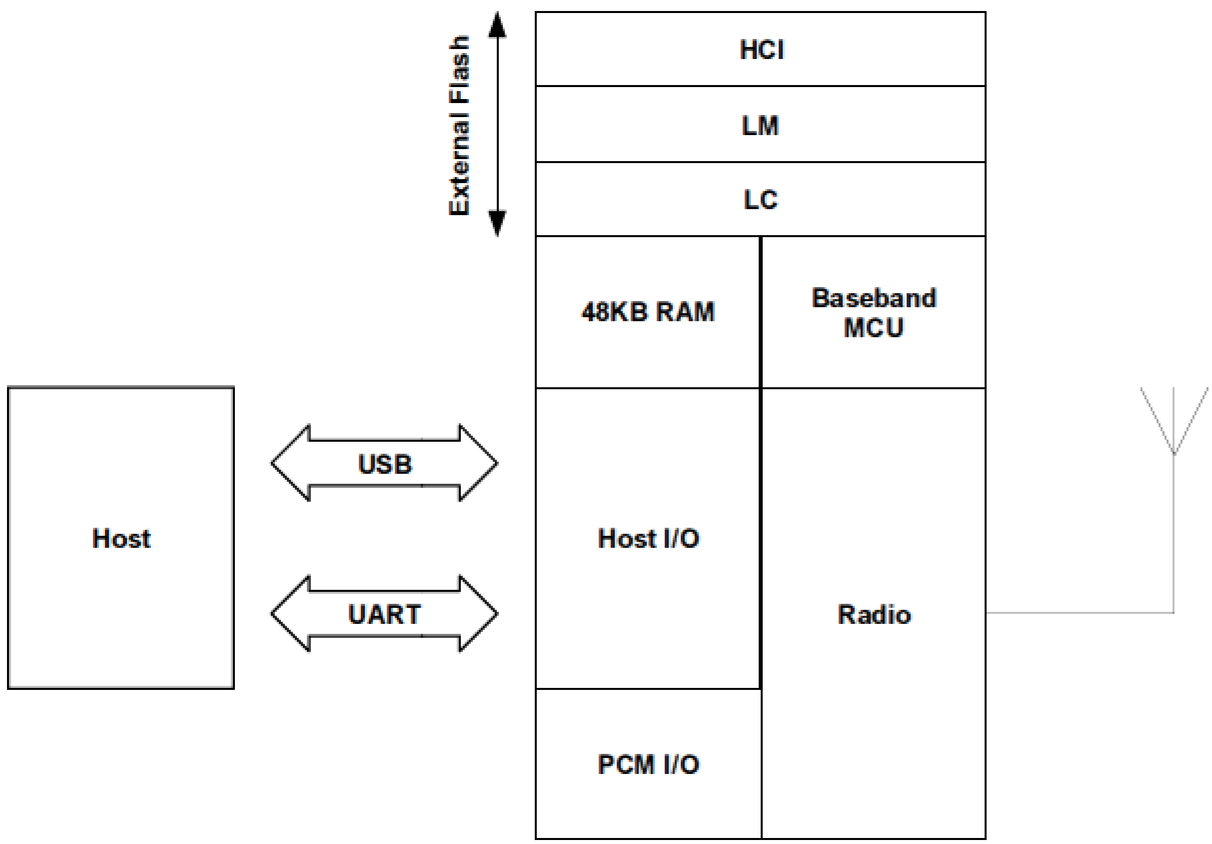
3.6.2 802.11 Coexistence Interface

Dedicated hardware is provided to implement a variety of 802.11 (Wi-Fi) coexistence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware. The details of some methods are proprietary. Contact CSR for details.

4 Bluetooth Software Stacks

The BlueCore4 chip is supplied with Bluetooth v2.1 + EDR compliant stack firmware, which runs on the internal RISC microcontroller.

The BlueCore4 chip software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any). The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.



4.1 BlueCore HCI Stack

Figure 3 BlueCore HCI Stack

In the implementation shown in Figure 3 the internal processor runs the Bluetooth stack up to the HCI. The Host processor must provide all upper layers including the application.

4.1.1 Key Features of the HCI Stack: Standard Bluetooth Functionality

Bluetooth v2.1 + EDR mandatory functionality:

- AFH, including classifier
- Faster connection - enhanced inquiry scan (immediate FHS response)
- LMP improvements
- Parameter ranges

Optional Bluetooth v2.1 + EDR functionality supported:

- AFH as Master and Automatic Channel Classification
- Fast Connect: Interlaced Inquiry and Page Scan plus RSSI during Inquiry
- eSCO, eV3 +CRC, eV4, eV5
- SCO handle
- Synchronization

The firmware was written against the Bluetooth v2.1 + EDR specification.

- Bluetooth components:
  - Baseband (including LC)
  - LM
  - HCI
- Standard USB v2.0 and UART HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps
- Operation with up to seven active slaves[1]
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7
- Maximum number of simultaneous active SCO connections: 3[2]
- Operation with up to three SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers' transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes
- A block of radio test or BIST commands allows direct control of the chip's radio. This aids the development
- of modules' radio designs, and can be used to support Bluetooth qualification.
- VM. The firmware provides the VM environment in which to run application-specific code. Although the is mainly used with BlueLab and RFCOMM builds (alternative firmware builds providing L2CAP, SDP and
- RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LEDs via the chip's
- PIO port.
- Hardware low power modes: Shallow Sleep and Deep Sleep. The chip drops into modes that significantly
- reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed
- over the chip's single PCM port (at the same time as routing any remaining SCO channels over HCI).

1
This is the maximum allowed by Bluetooth v2.1 + EDR specification.
2
BlueCore4 chip supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth v2.1 + EDR specification.

The firmware's supported Bluetooth features are detailed in the standard PICS documents, available from www.csr.com.

4.2 BCHS Software

BlueCore Embedded Host Software is designed to enable CSR customers to implement Bluetooth functionality into embedded products quickly, cheaply and with low risk.
BCHS is developed to work with CSR's family of BlueCore s. BCHS is intended for embedded products that have a host processor for running BCHS and the Bluetooth application, e.g., a mobile phone or a PDA. BCHS together with the BlueCore IC with embedded Bluetooth core stack (L2CAP, RFCOMM and SDP) is a complete Bluetooth system solution from RF to profiles.
BCHS includes most of the Bluetooth intelligence and gives the user a simple API. This makes it possible to develop a Bluetooth product without in-depth Bluetooth knowledge.
The BlueCore Embedded Host Software contains three elements:

- Example Drivers (BCSP and proxies)
- Bluetooth Profile Managers
- Example Applications

The profiles are qualified which makes the qualification of the final product very easy. BCHS is delivered with source code (ANSI C). BCHS also comes with example applications in ANSI C, which makes the process of writing the application easier.

4.3 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore4 chip, a UART software driver is supplied that presents the L2CAP, RFCOMM and SDP APIs to higher Bluetooth stack layers running on the host. The code is provided as C source or object code.

4.4 CSR Development Systems

CSR’s BlueLab Multimedia and Casira development kits are available to allow the evaluation of the BlueCore4-External hardware and software, and as toolkits for developing on-chip and host software.

5 Interfaces

5.1 UART Interface

This is a standard UART interface for communicating with other serial devices.
BlueCore4 chip UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

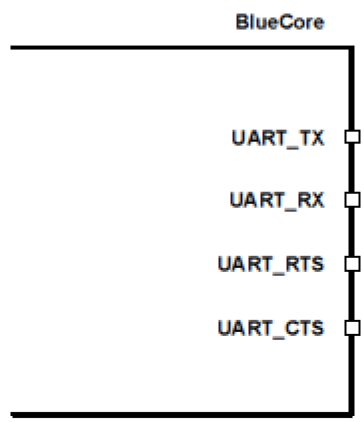


Figure 4 Universal Asynchronous Receiver/Transmitter

Four signals are used to implement the UART function, as shown in Figure 4. When BlueCore4 chip is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD_USB.
UART configuration parameters, such as data rate and packet format, are set using BlueCore4 chip software.
Note:
In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter	Possible Values	
Data Rate	Minimum	1200 bits/s (2%Error)
		9600 bits/s (1%Error)
	Maximum	3M bit/s (1%Error)
Flow Control	RTS/CTS or None	
Parity	None, Odd or Even	
Number of Stop Bits	1 or 2	
Bits per Channel	8	

Table 2 UART Settings

The UART interface is capable of resetting BlueCore4 chip upon reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 5. If t BRK is longer than the value, defined by PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialize the system to a known state. Also, BlueCore4 chip can emit a break character that may be used to wake the host.

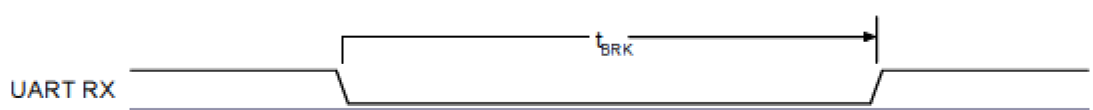


Figure 5 Break Signal

Note:
The DFU boot loader must be loaded into the Flash device before the UART or USB interfaces can be used.
This initial flash programming can be done via the SPI.
Table 3 shows a list of commonly used data rates and their associated values for PSKEY_UART_BAUD_RATE (0x204).
There is no requirement to use these standard values. Any data rate within the supported range can be set in the PS Key according to the formula

Data Rate = PSKEY_UART_BAUDRATE/0.004096

Data Rate (bits/s)	Persistent Store Value	Error	Dec
	Hex		
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%

Table 3 Standard Data Rates

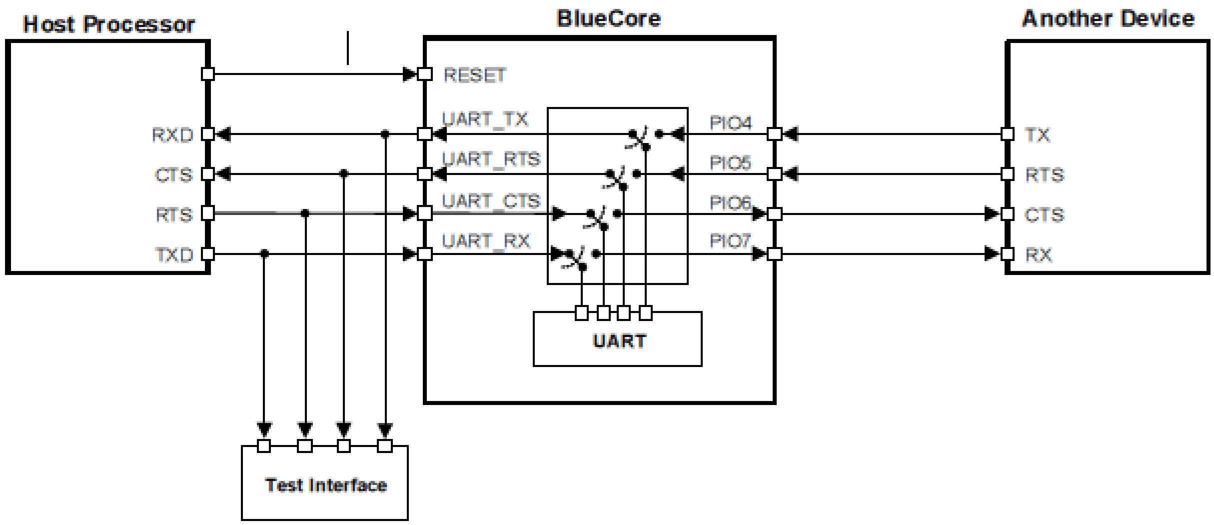


Figure 6 UART Bypass Architecture

5.1.1 UART Configuration While RESET is Active

The UART interface for BlueCore4 chip while the chip is being held in reset is tristate. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tristate when BlueCore4 chip reset is de-asserted and the firmware begins to run.

5.1.2 UART Bypass Mode

Alternatively, for devices that do not tristate the UART bus, the UART bypass mode on BlueCore4 chip can be used. The default state of BlueCore4 chip after reset is de-asserted; this is for the host UART bus to be connected to the BlueCore4 chip UART, thereby allowing communication to BlueCore4 chip via the UART.
All UART bypass mode connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS.
In order to apply the UART bypass mode, a BCCMD command will be issued to BlueCore4 chip. Upon this issue, it will switch the bypass to PIO[7:4] as Figure 7 indicates. Once the bypass mode has been invoked, BlueCore4 chip will enter the Deep Sleep state indefinitely.
In order to re-establish communication with BlueCore4 chip, the chip must be reset so that the default configuration takes effect.
It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore, it is not possible to have active Bluetooth links while operating the bypass mode.

5.1.3 Current Consumption in UART Bypass Mode

The current consumption for a device in UART bypass mode is equal to the values quoted for a device in standby mode.

5.2 USB Interface

This is a full speed (12Mbits/s) USB interface for communicating with other compatible digital devices. BlueCore4-External acts as a USB peripheral, responding to requests from a master host controller such as a PC.
The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth v2.1 + EDR specification or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.
As USB is a master/slave oriented system (in common with other USB peripherals), BlueCore4 chip only supports USB Slave operation.

5.2.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the BlueCore4 chip, therefore, have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP/USB_DN and the cable.

5.2.2 USB Pull-Up Resistor

BlueCore4 chip features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when BlueCore4 chip is ready to enumerate. It signals to the PC that it is a full speed (12Mbits/s) USB device.
The USB internal pull-up is implemented as a current source, and is compliant with section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15k 5% pull-down resistor (in the hub/host) when VDD_PADS = 3.1V. This presents a Thevenin resistance to the host of at least 900.
Alternatively, an external 1.5k pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

5.2.3 USB Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

5.2.4 Self-Powered Mode

In self-powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BlueCore4 chip via a resistor network (R vb1 and R vb2), so BlueCore4 chip can detect when VBUS is powered up. BlueCore4 chip will not pull USB_DP high when VBUS is off.
Self-powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pullup purposes. A 1.5k 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self-powered mode. The internal pull-up in BlueCore is only suitable for bus-powered USB devices, e.g., dongles.

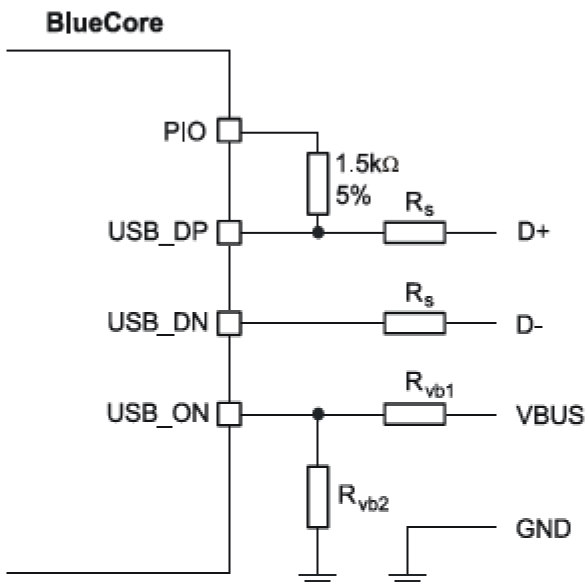


Figure 7 USB Connections for Self-Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.
Note:
USB_ON is shared with BlueCore4 chip PIO terminals.

Identifier	Value	Function
R_s	27 nominal	Impedance matching to USB cable
R_{vb1}	22k 5%	VBUS ON sense divider
R_{vb2}	47k 5%	VBUS ON sense divider

Table 3 USB Interface Component Values

5.2.5 Bus-Powered Mode

In bus-powered mode, the application circuit draws its current from the 5V VBUS supply on the USB cable. BlueCore4 chip negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.
For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus-powered mode, BlueCore4 chip requests 100mA during enumeration.
For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is accomplished by setting PSKEY_USB_MAX_POWER (0x2c6). This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA.
When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification. See the USB Specification . Some applications may require soft start circuitry to limit inrush current if more than 10F is present between VBUS and GND.
The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analog supply pins of BlueCore4 chip will result in reduced receive sensitivity and a distorted RF transmit signal.

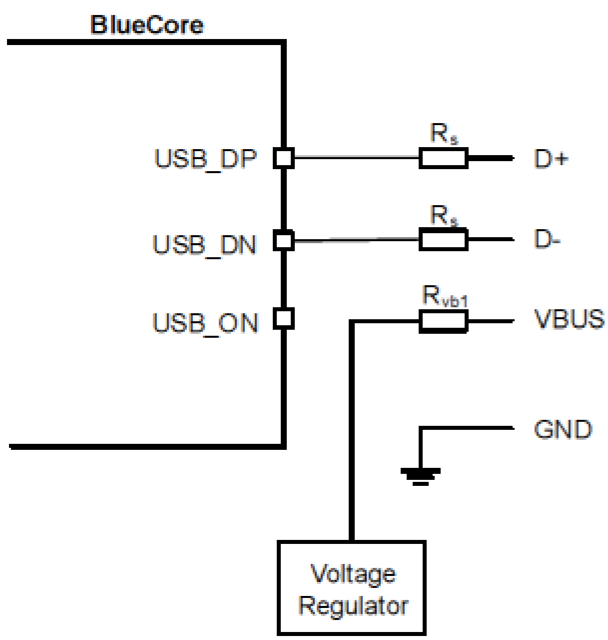


Figure 8 USB Connections for Bus-Powered Mode

5.2.6 Suspend Current

All USB devices must permit the USB controller to place them in a USB suspend mode. While in USB Suspend, bus-powered devices must not draw more than 0.5mA from USB VBUS (self-powered devices may draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus-powered devices during USB Suspend.
The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100A) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by BlueCore4 chip. The entire circuit must be able to enter the suspend mode. Refer to separate CSR documentation for more details on USB Suspend.

5.2.7 Detach and Wake_Up Signaling

BlueCore4 chip can provide out-of-band signaling to a host controller by using the control lines called USB_DETACH and USB_WAKE_UP. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore4 chip into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.
USB_DETACH is an input which, when asserted high, causes BlueCore4 chip to put USB_DN and USB_DP in a high impedance state and turns off the pull-up resistor on DP. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore4 chip will connect back to USB and await enumeration by the USB host.
USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable) and cannot be sent while BlueCore4 chip is effectively disconnected from the bus.

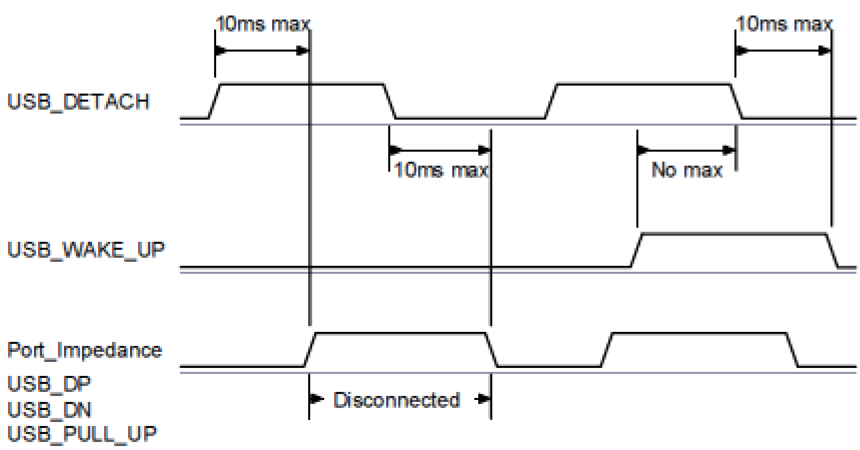


Figure 9 USB_DETACH and USB_WAKE_UP Signals

5.2.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore4 chip and Bluetooth software running on the host computer. Suitable drivers are available from http://www.csrsupport.com.

5.2.9 USB v2.0 Compliance

BlueCore4 chip is qualified to USB Specification v2.1, details of which are available from http://www.usb.org.
The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labeling.
Although BlueCore4 chip meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7.
Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.
Terminals USB_DP and USB_DN adhere to the USB Specification v2.0 (Chapter 7) electrical requirements.

5.2.10 USB 2.0 Compatibility

BlueCore4 chip is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

5.3 Serial Peripheral Interface

BlueCore4 chip uses 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped. This section details the considerations required when interfacing to BlueCore4 chip via the four dedicated serial peripheral interface terminals. Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

5.3.1 Instruction Cycle

The BlueCore4 chip is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 4 shows the instruction cycle for an SPI transaction.

1	Reset the SPI interface	Hold SPI_CSB high for two SPI_CLK cycles
2	Write the command word	Take SPI_CSB low and clock in the 8 bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CSB high

Table 4 Instruction Cycle for an SPI Transaction

With the exception of reset,SPI_CSB must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore4 chip on the rising edge of the clock line SPI_CLK. When reading, BlueCore4 chip will reply to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CSB high.
Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore4 chip offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CSB is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

5.3.2 Writing to the Device

To write to BlueCore4 chip, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are
written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CSB is taken high.

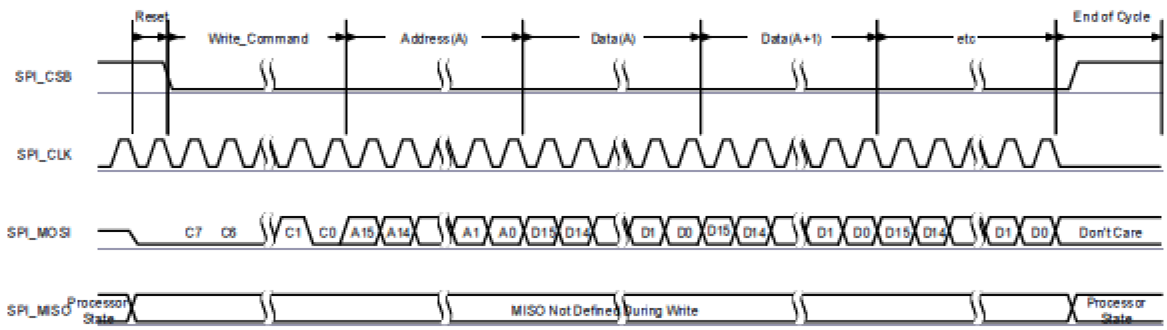


Figure 10 SPI Write Operation

5.3.3 Reading from the Device

Reading from BlueCore4 chip is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]).BlueCore4 chip then outputs
on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].
The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.
If SPI_CSB is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CSB is taken high.

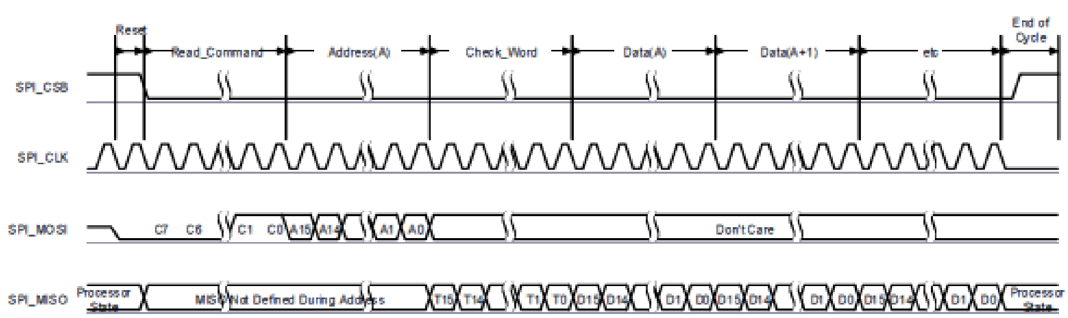


Figure 11 SPI Read Operation

5.3.4 Multi-Slave Operation

BlueCore4 chip should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueCore4 chip is deselected (SPI_CSB = 1), the SPI_MISO line does not float. Instead, BlueCore4 chip outputs 0 if the processor is running or 1 if it is stopped.

5.4 PCM Codec Interface

PCM is a standard method used to digitize audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, BlueCore4 chip has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore4 chip offers a bidirectional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.
Hardware on BlueCore4 chip allows the data to be sent to and received from a SCO connection.
Up to three SCO connections can be supported by the PCM interface at any one time.
BlueCore4 chip can operate as the PCM interface master generating an output clock of 128, 256 or 512kHz.
When configured as PCM interface slave, it can operate with an input clock up to 2048kHz. BlueCore4 chip is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.
It supports 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting PSKEY_PCM_CONFIG32.
BlueCore4 chip interfaces directly to PCM audio devices.

5.4.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, BlueCore4 chip generates PCM_CLK and PCM_SYNC.

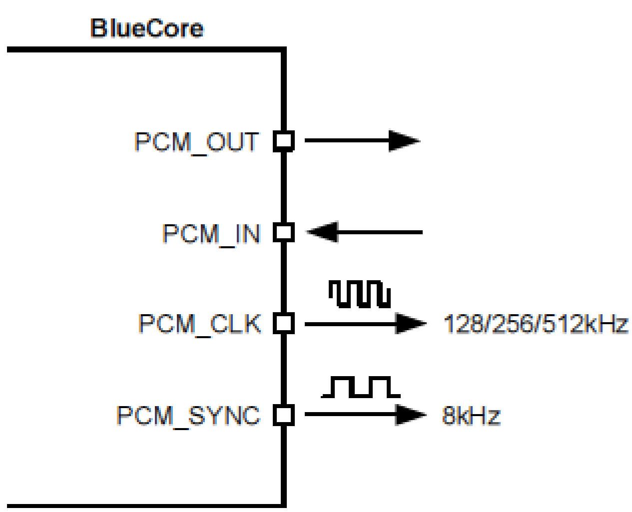


Figure 12 PCM Configured as a Master

When configured as the Slave of the PCM interface, BlueCore4 chip accepts PCM_CLK rates up to 2048kHz.

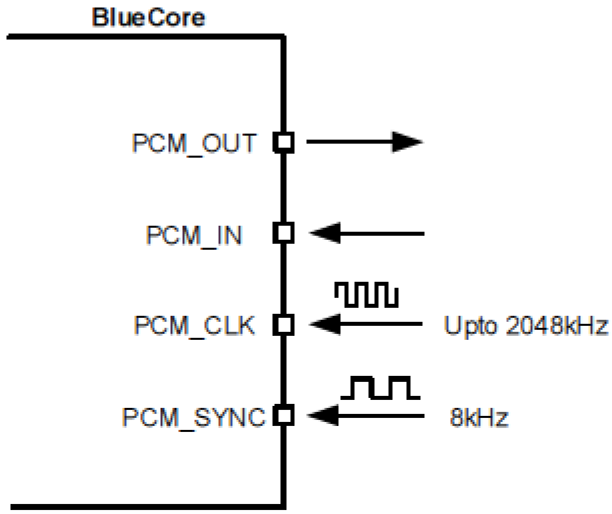


Figure 13 PCM Configured as a Slave

5.4.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore4 chip is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore4 chip is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5s long.

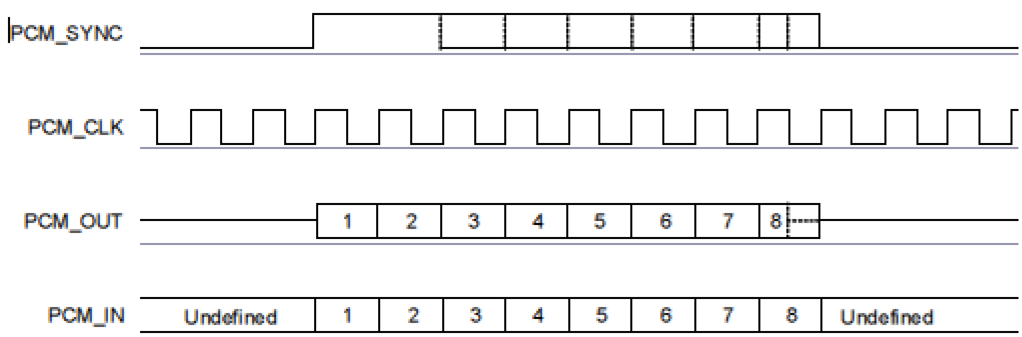


Figure 14 Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore4 chip samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

5.4.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

When configured as the Slave of the PCM interface, BlueCore4 chip accepts PCM_CLK rates up to 2048kHz.

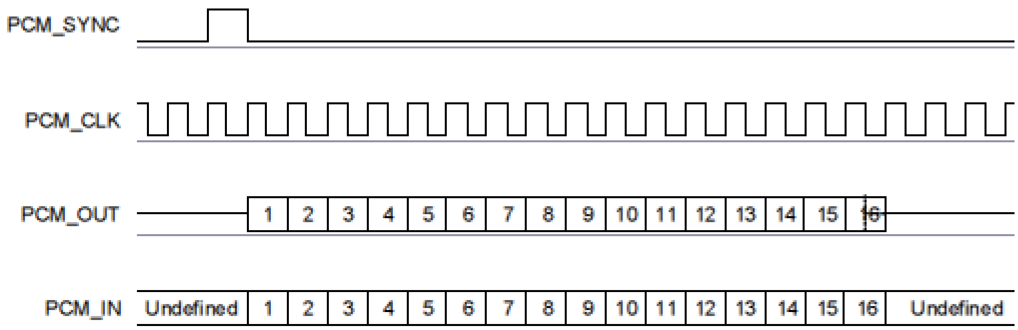


Figure 15 Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore4 chip samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

5.4.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

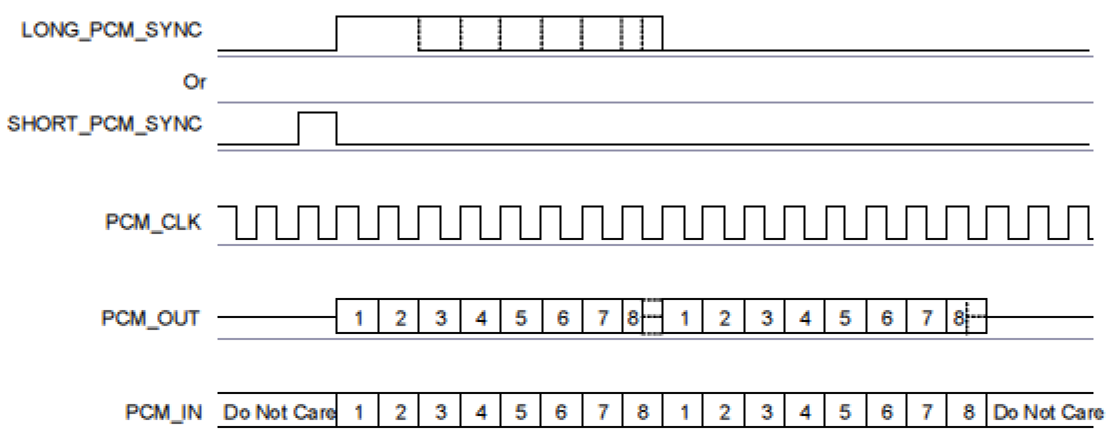


Figure 16 Multi-slot Operation with Two Slots and 8-bit Companded Samples

5.4.5 GCI Interface

BlueCore4 chip is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The two 64kbits/s B channels can be accessed when this mode is configured.

Figure 18 GCI Interface

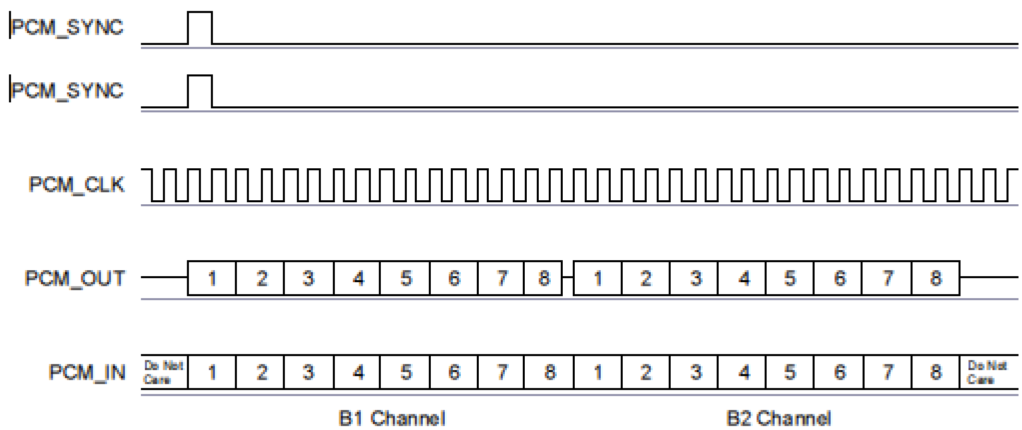


Figure 17 GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore4 chip in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

5.4.6 Slots and Sample Formats

BlueCore4 chip can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats.

BlueCore4 chip supports 13-bit linear, 16-bit linear and 8-bit -law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola codecs.

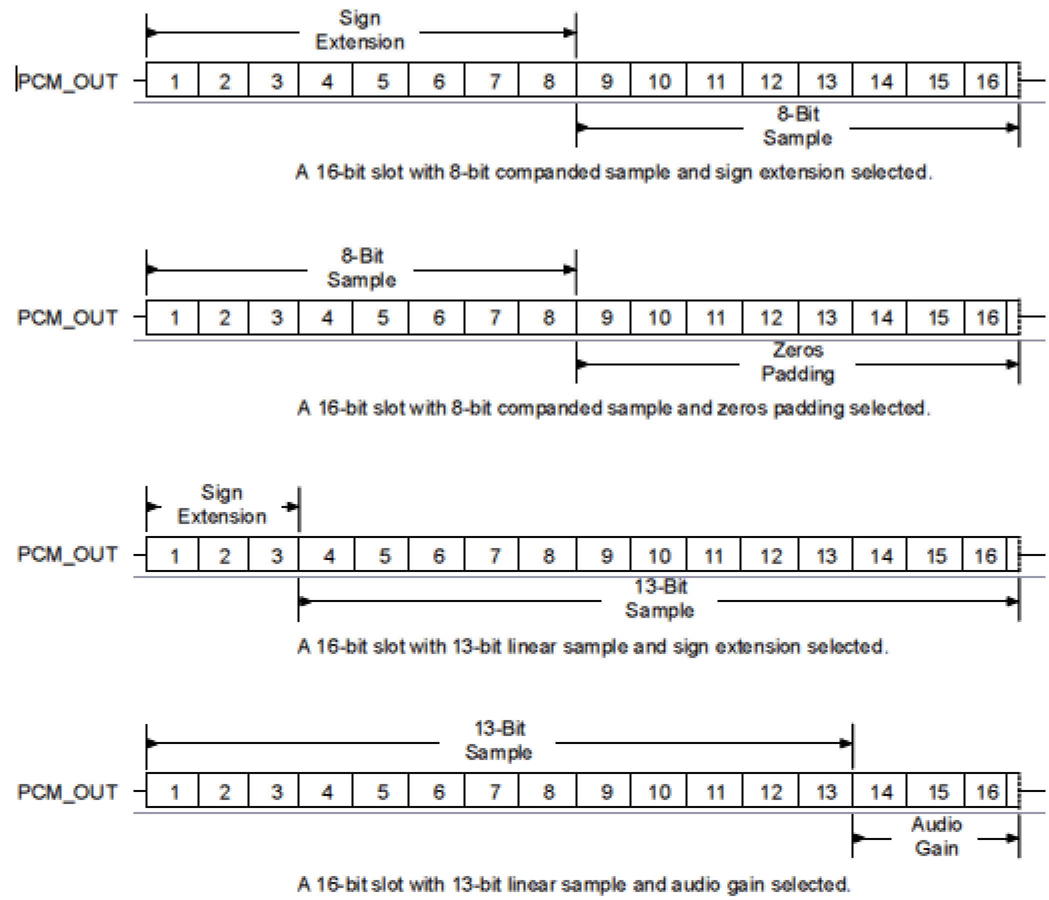


Figure 18 16-bit Slot Length and Sample Format

5.4.7 Additional Features

BlueCore4 chip has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some codecs use to control power down.

5.4.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Table 7.16.	-	128	-	kHz
				256		
				512		
	PCM_CLK frequency	48MHz DDS generation. Selection of frequency is programmable. See Table 7.17 and Section 7.8.9.	2.9	-	-	kHz
	PCM_SYNC frequency	-	8	-	-	kHz
t_{mclkh} [a]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} [a]	PCM_CLK low	4MHz DDS generation	730	-	-	ns
	PCM_CLK jitter	48MHz DDS generation	-	-	21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 5 PCM Master Timing

(a) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

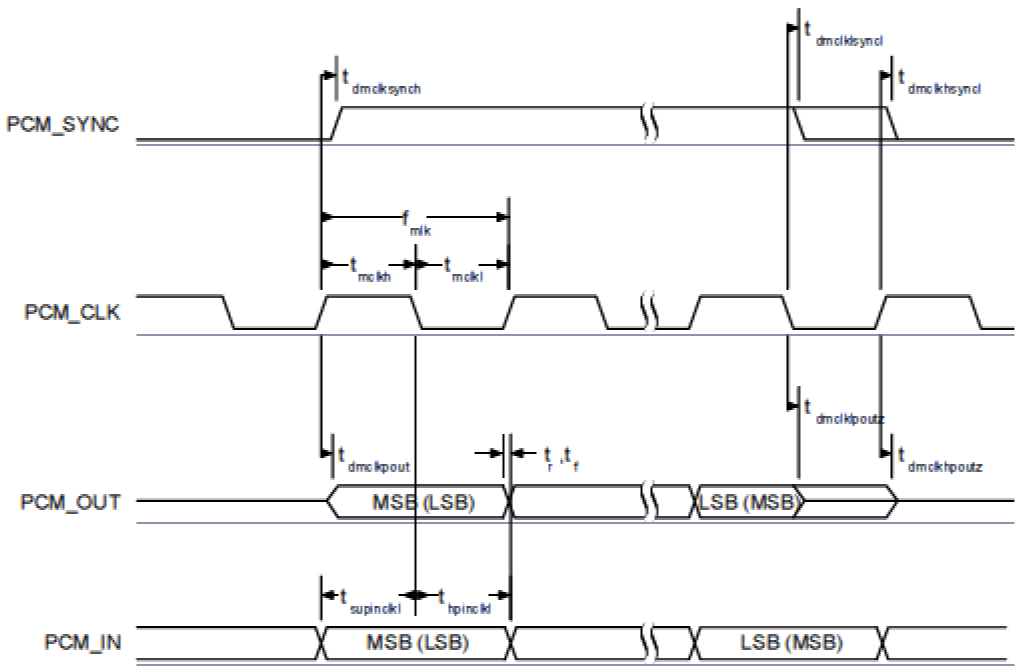


Figure 19 PCM Master Timing Long Frame Sync

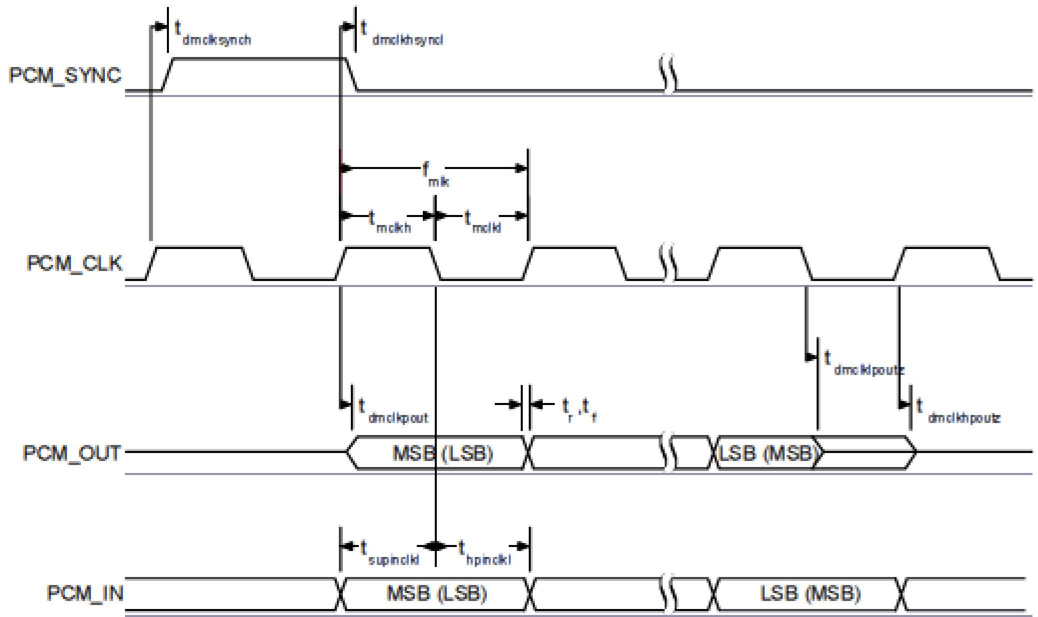


Figure 20 PM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 6 PCM Slave Timing

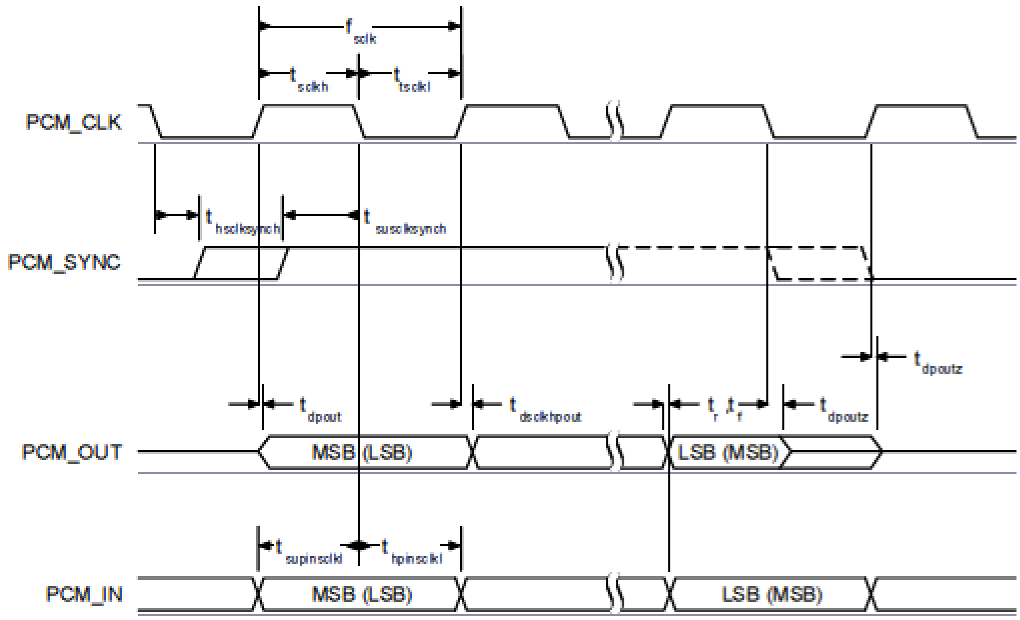


Figure 21 PCM Slave Timing Long Frame Sync

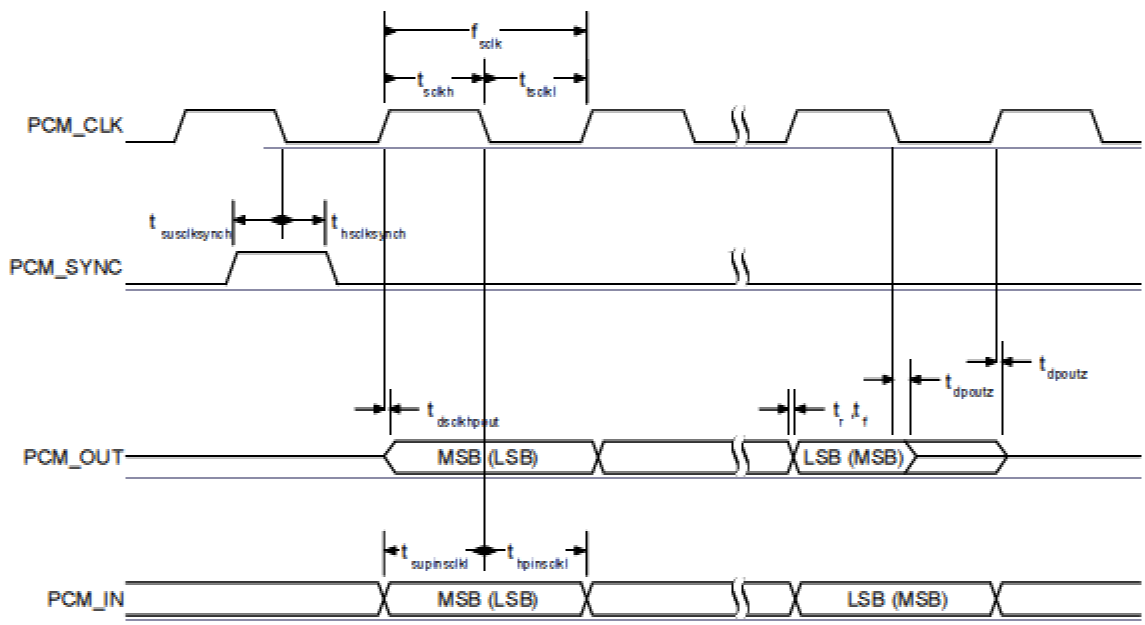


Figure 22 PCM Slave Timing Short Frame Sync

5.4.9 PCM_CLK and PCM_SYNC Generation

BlueCore4 chip has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by DDS from BlueCore4 chip internal 4MHz clock (which is used in BlueCore2-External). Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock (which allows a greater range of frequencies to be generated with low jitter but consumes more power). This second method is selected by setting bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

This equation describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = (CNT\_RATE/CNT\_LIMIT) \times 24MHz$$

The frequency of PCM_SYNC relative to PCM_CLK can be set using :

$$f = PCM\_CLK/SYNC\_LIMIT \times 8$$

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

5.4.10 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 detailed in Table 7.16 and PSKEY_PCM_LOW_JITTER_CONFIG in Table 7.17. The default for PSKEY_PCM_CONFIG32 is 0x00800000
, i.e., first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tristate of PCM_OUT.

Name	Bit Position	Description
-	0	Set to 0
SLAVE_MODE_EN	1	0 = master mode with internal generation of PCM_CLK and PCM_SYNC. 1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 = long frame sync (rising edge indicates start of frame). 1 = short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = sign-extension.

Table 7 PSKEY_PCM_CONFIG32 Description

LSB_FIRST_EN	5	0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples.
TX_TRISTATE_EN	6	0 = drive PCM_OUT continuously. 1 = tristate PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 = tristate PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active. 1 = tristate PCM_OUT after rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC whilst keeping PCM_CLK running. Some codecs utilise this to enter a low power state.
GCI_MODE_EN	9	1 = enable GCI mode
MUTE_EN	10	1 = force PCM_OUT to 0
48M_PCM_CLK_GEN_EN	11	0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48MHz clock.
LONG_LENGTH_SYNC_EN	12	0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is 0001. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration.

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit
CNT_RATE	[23:16]	Sets PCM_CLK count rate
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK

Table 8 PSKEY_PCM_LOW_JITTER_CONFIG Description

5.5 I/O Parallel Ports

Fifteen lines of programmable bidirectional input/outputs (I/O) are provided. PIO[11:8] and PIO[3:0] are powered from VDD_PIO. PIO[7:4] are powered from VDD_PADS. AIO [2:0] are powered from VDD_MEM.
PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.
PIO[0] and PIO[1] are normally dedicated to RXEN and TXEN respectively, but they are available for general use.
Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO[2] can be configured as a request line for an external clock source. This is useful when the clock to BlueCore4-External is provided from a system ASIC. Using PSKEY_CLOCK_REQUEST_ENABLE (0x246), this terminal can be configured to be low when BlueCore4 chip is in Deep Sleep and high when a clock is required. The clock must be supplied within 4ms of the rising edge of PIO[6] or PIO[2] to avoid losing timing accuracy in certain Bluetooth operating modes.
BlueCore4 chip has three general purpose analog interface pins, AIO[0], AIO[1] and AIO[2]. These are used to access internal circuitry and control signals. One pin is allocated to decoupling for the on-chip band gap reference voltage, the other two may be configured to provide additional functionality.
Auxiliary functions available via these pins include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the band gap reference voltage and a variety of clock signals: 48, 24, 16, 8MHz and the XTAL clock frequency. When used with analog signals, the voltage range is constrained by the analog supply voltage (1.8V). When configured to drive out digital level signals (e.g., clocks), the output voltage level is determined by VDD_MEM (1.8V).

5.5.1 PIO Defaults

CSR, maker of the BlueCore4 chip, cannot guarantee that these terminal functions remain the same. Refer to the software release note for the implementation of these PIO lines, as they are firmware build-specific.

5.6 I2C Interface

PIO[8:6] can be used to form a master I2C interface. The interface is formed using software to drive these lines. Therefore, it is suited only to relatively slow functions such as driving a dot matrix LCD, keyboard scanner or EEPROM.
Any three PIOs can be used as a master I2C interface by configuring the hardware bit serializer with suitable firmware. The strong pull-ups in the PIO pads eliminate the need for external pull-up resistors.
Note:
PIO lines need to be pulled-up through 2.2k resistors.
PIO[7:6] dual functions, UART bypass and EEPROM support, therefore, devices using an EEPROM cannot support UART bypass mode.

5.7 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore4 chip where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the host clock enables input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore4 chip.

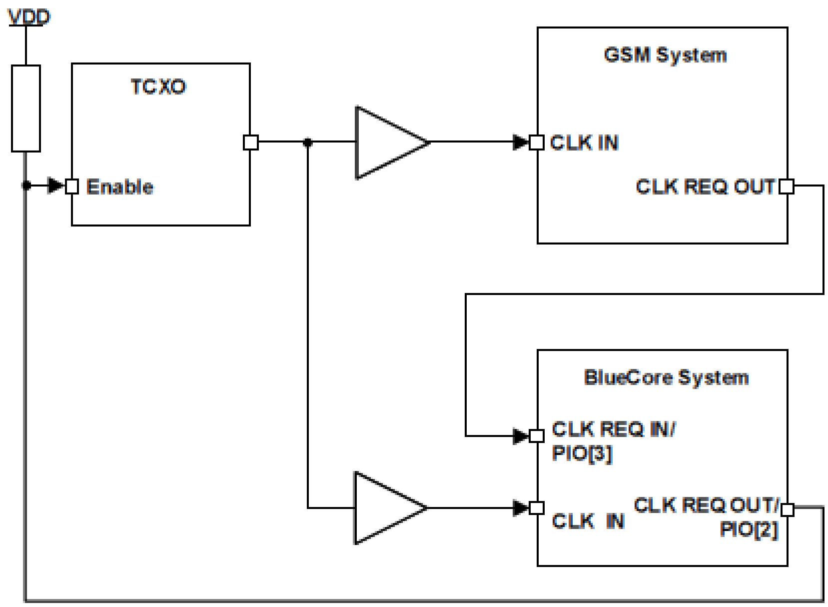


Figure 23 Example of OR Function

On reset and up to the time the PIO has been configured, PIO[2] will be tristate. Ensure that the circuitry connected to this pin is pulled via a 470k resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

5.8 Reset

BlueCore4 chip may be reset from several sources: RESETB pin, power on reset, a UART break character or via a software configured watchdog timer.
The RESETB pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESETB be applied for a period greater than 5ms.
The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V. At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are tristate. The PIOs have weak pull-downs. Following a reset, BlueCore4 chip assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore4 chip is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore4 chip free runs, again at a safe frequency.

5.8.1 Pin States on Reset

Pin Name	State
PIO[11:0]	Input with weak pull-down
PCM_OUT	Tristated with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	Input with weak pull-down
UART_TX	Output tristated with weak pull-up
UART_RX	Input with weak pull-down
UART_CTS	Input with weak pull-down
USB_DP	Input with weak pull-down
USB_DN	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Output tristated with weak pull-down
AIO[2:0]	Output, driving low
RESETB	Input with weak pull-up
TEST_EN	Input with strong pull-down
RF_A	High impedance
RF_B	High impedance
RF_IN	High impedance
XTAL_IN	High impedance, 250k to XTAL_OUT
XTAL_OUT	High impedance, 250k to XTAL_IN

Table 9 Pin States on Reset

5.8.2 Status after Reset

The chip status after a reset is as follows:

- Warm Reset: Data rate and RAM data remain available
- Cold Reset: Data rate and RAM data not available

5.9 Power Supply

5.9.1 Voltage Regulator

The BTM160 module is powered from a single regulated 3.3V supply connected to pin 11 (VDD) and pin 23 (VDD_USB).

5.9.2 Sensitivity to Disturbances

CSR recommends if supplying BlueCore4 chip from an external voltage source with less than 10mV rms noise levels between 0 to 10MHz. In addition, avoid single tone frequencies.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Absolute Maximum Ratings		
Ratings	**Min.**	**Max.**
Storage Temperature	-40 ℃	+150 ℃
Supply Voltage VDD (3.3V version, BTM-160)	-0.4 V	3.7 V
Supply Voltage VDD (1.8V version, BTM-170)	-0.4 V	2.2 V
Recommended Operating Condition		
Operating Condition	**Min.**	**Max.**
Operating Temperature range	-20 ℃	+75 ℃
Supply Voltage VDD (3.3V version, BTM-160)	3.0 V	3.6 V
Supply Voltage VDD (1.8V version, BTM-170)	1.7 V	1.9 V

Table 10 Absolute Maximum Ratings

6.2 DC Characteristics

Parameter	Description	Min.	Typ.	Max.	Units
RF Output Power	Measured in 50 ohm	0	2	4	dBm
RX Sensitivity			-83	-80	dBm
Input Low Voltage	RESET,UART,GPIO,PCM	-0.30	-	0.80	V
Input High Voltage	RESET,UART,GPIO,PCM	0.70VDD	-	VDD+0.30	V
Output Low Voltage	UART,GPIO,PCM	-	-	0.40	V
Output High Voltage	UART,GPIO,PCM	VDD-0.40	-	-	V
Average Current Consumption	Deep sleep		40		uA
	ACL 40ms sniff		2.4		mA
	SCO connection HV1		39	-	mA
Peak Current	Tx burst +4dBm		-	58	mA

Table 11 Typical DC Characteristics

6.3 Radio Characteristics - Basic Data Rate

Radio Characteristics, VDD = 3.3V Temperature =+20°C						
	Freauency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-83	-82	≤ - 70	dBm
	2.441	-	-83	-82		dBm
	2.480	-	-83	-82		dBm
Maximum received signal at 0.1% BER	2.402	-	-6	0	≥ - 20	dBm
	2.441	-	-6	0		dBm
	2.480	-	-6	0		dBm
RF transmit power(1)	2.402	-	+2	-	-6 to +4(2)	dBm
	2.441	-	+2	-		dBm
	2.480	-	+2	-		dBm
Initial carrier frequency tolerance	2.402	-	12	20	±75	kHz
	2.441	-	10	20		kHz
	2.480	-	9	20		kHz
20dB bandwidth for modulated carrier	2.402	-	879	1000	≤ 1000	kHz
	2.441	-	816	1000		kHz
	2.480	-	819	1000		kHz
Drift (single slot packet)	2.402	-	-	20	≤25	kHz
	2.441	-	-	20		kHz
	2.480	-	-	20		kHz
Drift (five slot packet)	2.402	-	-	20	≤40	kHz
	2.441	-	-	20		kHz
	2.480	-	-	20		kHz
Drift Rate	2.402	-	-	15	20	kHz/50µs
	2.441	-	-	15		kHz/50µs
	2.480	-	-	15		kHz/50µs
RF power control range		16	35	-	≥16	dB
RF power range control resolution		-	1.8	-	-	dB
$\triangle f1^{avg}$ "Maximum Moudulation"	2.402	145	165	175	$140<\triangle f1^{avg}<175$	kHz
	2.441	145	165	175		kHz

	2.480	145	165	175		kHz
△f2^{max} "Minimum Modulation"	2.402	115	150	-	115	kHz
	2.441	115	150	-		kHz
	2.480	115	150	-		kHz
C/I co-channel		-	10	11	<= 11	dB
Adjacent channel selectivity C/I F=F_0 +1 MHz[(3)(5)]		-	-4	0	<= 0	dB
Adjacent channel selectivity C/I F=F_0 - 1MHz[(3)(5)]		-	-4	0	<= 0	dB
Adjacent channel selectivity C/I F=F_0 +2 MHz[(3)(5)]		-	-35	-30	<= - 30	dB
Adjacent channel selectivity C/I F=F_0 - 2MHz[(3)(5)]		-	-21	-20	<= - 20	dB
Adjacent channel selectivity C/I F>=F_0 +3 MHz[(3)(5)]		-	-45	-	<= - 40	dB
Adjacent channel selectivity C/I F<=F_0 -5 MHz[(3)(5)]		-	-45	-	<= - 40	dB
Adjacent channel selectivity C/I F=F_{image} [(3)(5)]		-	-18	-9	<= - 9	dB
Adjacent channel transmit power F=F_0±2MHz[(4)(5)]		-	-35	-20	<= - 20	dBc
Adjacent channel transmit power F=F_0±3MHz[(4)(5)]		-	-55	-40	<= - 40	dBc

Notes:

(1) BlueCore-External firmware maintains the transmit power to be within the Bluetooth specification v2.0 limits.
(2) Class 2 RF transmit power range, Bluetooth specification v2.0
(3) Up to five exceptions are allowed in v2.0 of the Bluetooth specification
(4) Up to three exceptions are allowed in v2.0 of the Bluetooth specification
(5) Measured at F_0 = 2441MHz

Table 12 Radio Characteristics - Basic Data Rate

6.4 Radio Characteristics - Enhanced Data Rate

Transmitter , VDD = 3.3V Temperature =+20°C

	Frequency (GHz)	Min.	Typ.	Max.	Bluetooth Specification	Unit
Maximum RF transmit power	2.402	-6	0	+2	-6 to +20	dBm
	2.441	-6	0	+2		dBm
	2.480	-6	0	+2		dBm
Relative transmit power		-	-1.5	-	-4 to +1	dB
π/4 DQPSK Maximum carrier frequency stability w_0		-	2	-	$\leq \pm 10$ for all blocks	kHz
π/4 DQPSK Maximum carrier frequency stability w_i		-	6	-	$\leq \pm 75$ for all packets	kHz
π/4 DQPSK Maximum carrier frequency stability $\lvert w_0 + w_i \rvert$		-	8	-	$\leq \pm 75$ for all blocks	kHz
8 DPSK Maximum carrier frequency stability w_0		-	2	-	$\leq \pm 10$ for all blocks	kHz
8 DPSK Maximum carrier frequency stability w_i		-	6	-	$\leq \pm 75$ for all packets	kHz
8 DPSK Maximum carrier frequency stability $\lvert w_0 + w_i \rvert$		-	8	-	$\leq \pm 75$ for all blocks	kHz
π/4 DQPSK Modulation Accuracy	RMS DVEM	-	7	-	$\leq$ 20	%
	99% DEVM	-	13	-	$\leq$ 30	%
	Peak DEVM	-	19	-	$\leq$ 35	%
8 DPSK Modulation Accuracy	RMS DVEM	-	7	-	$\leq$ 13	%
	99% DEVM	-	13	-	$\leq$ 20	%
	Peak DEVM	-	17	-	$\leq$ 25	%
In-band spurious emissions	$F>F_0$ +3 MHz	-	<-50	-	$\leq$ -40	dBm
	$F<F_0$ -3 MHz	-	<-50	-	$\leq$ -40	dBm
	$F=F_0$ -3 MHz	-	-46	-	$\leq$ -40	dBm
	$F=F_0$ -2 MHz	-	-34	-	$\leq$ -20	dBm
	$F=F_0$ -1 MHz	-	-35	-	$\leq$ -26	dBm
	$F=F_0$ +1 MHz	-	-35	-	$\leq$ -26	dBm
	$F=F_0$ +2 MHz	-	-31	-	$\leq$ -20	dBm
	$F=F_0$ +3 MHz	-	-33	-	$\leq$ -40	dBm
EDR Differential Phase Encoding			No Errors		$\geq$ 99	%

Receiver , VDD = 3.3V Temperature =+20°C						
	Modulation	**Min.**	**Typ.**	**Max.**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	π/4 DQPSK	-	-82	-	$\leq$ -70	dBm
	8 DPSK	-	-76	-	$\leq$ -70	dBm
Maximum received signal level at 0.1% BER	π/4 DQPSK	-	-8	-	$\geq$ -20	dBm
	8 DPSK	-	-10	-	$\geq$ -20	dBm
C/I co-channel at 0.1% BER	π/4 DQPSK	-	10	-	$\leq$ +13	dB
	8 DPSK	-	19	-	$\leq$ +21	dB
Adjacent channel selectivity C/I $F=F_0$ +1 MHz	π/4 DQPSK	-	-10	-	$\leq$ 0	dB
	8 DPSK	-	-5	-	$\leq$ +5	dB
Adjacent channel selectivity C/I $F=F_0$ -1 MHz	π/4 DQPSK	-	-11	-	$\leq$ 0	dB
	8 DPSK	-	-5	-	$\leq$ +5	dB
Adjacent channel selectivity C/I $F=F_0$ +2 MHz	π/4 DQPSK	-	-40	-	$\leq$ -30	dB
	8 DPSK	-	-40	-	$\leq$ -25	dB
Adjacent channel selectivity C/I $F=F_0$ -2 MHz	π/4 DQPSK	-	-23	-	$\leq$ -20	dB
	8 DPSK	-	-20	-	$\leq$ -13	dB
Adjacent channel selectivity C/I $F=F_0$ +3 MHz	π/4 DQPSK	-	-45	-	$\leq$ -40	dB
	8 DPSK	-	-45	-	$\leq$ -33	dB
Adjacent channel selectivity C/I $F=F_0$ -5 MHz	π/4 DQPSK	-	-45	-	$\leq$ -40	dB
	8 DPSK	-	-45	-	$\leq$ -33	dB
F_0 = 2405, 2441, 2477 MHz						
Adjacent channel selectivity C/I $F=F_{image}$	π/4 DQPSK		-20		$\leq$ -7	dB
	8 DPSK		-15		$\leq$ 0	dB

Figure 13 Radio Characteristics - Enhanced Data Rate

7 Package Information

7.1 Package Marking

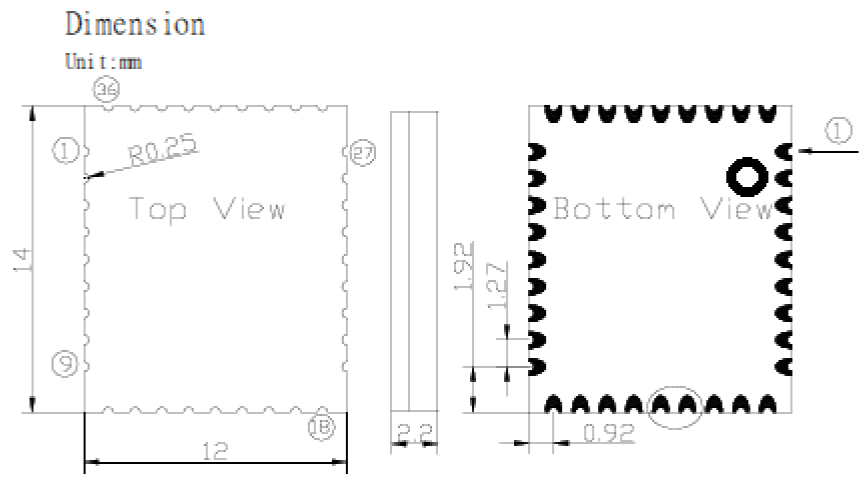


Figure 24 Package Dimensions and Pin 1 Marking

8 Important Application Information

8.1 Antenna Trace and Connector Information

The BTM160 has been tested and certified for use with a small UMCC RF connector place right next to the module. The module should be installed on a multi-layer PCB with a ground plane placed directly beneath it and the connector

PCBs designed for use with this module shall use the design layout shown below which represents the included Gerber files.

PCB Layout – Using a 4 layer PCB, a trace with a total length of less than 1mm is used to connect the RF output pad of the BTM160 module (pad 2) to a surface mount UMCC RF connector (Tyco 1566230-1). Vias alongside the UMCC connector connect to the underlying ground plane.

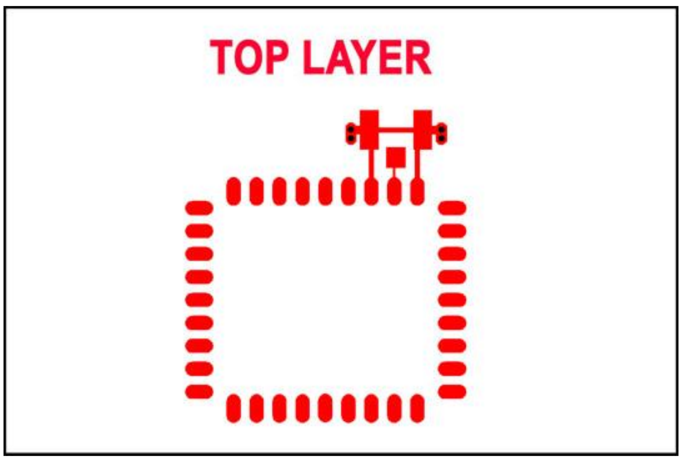


Figure 25 PCB Layout

Design Verification

The UMCC RF connector must be placed adjacent to the BTM160 as shown with a trace length between the two limited to less than 1mm. The connector must be connected to the underlying ground plane with vias placed next to each ground pad as shown.

8.2 Antenna Information

The BTM160 is intended to be installed inside end user equipment. The BTM160 is Bluetoooth-qualified and also FCC-certified and Industry Canada approved, and conforms to R&TTE requirements and directives.
FCC certification is with the following antennas:

Manufacturer	Model	Type	Peak antenna gain	Impedance
Bohua	BH051	sma mini whip	2dBi	50ohm
Pulse	W1010	sma mini whip	2dBi	50ohm
Pulse	W1038	sma whip 6.6”	4.9dBi	50ohm

Table 13 Antennas

Antennas must be permanently attached or inaccessible to the end user or, if detachable, must use a unique connector such as a reverse polarity SMA connector.

8.3 FCC Class B Digital Devices Regulatory Notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by 1 or more of the following measures:

- Reorient or relocate the antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio or television technician for help

8.4 FCC Wireless Notice

This product emits radio frequency energy, but the radiated output power of this device is far below the FCC radio frequency exposure limits. Nevertheless, the device should be used in such a manner that the potential for human contact with the antenna during normal operation is minimized.

- To meet the FCC's RF exposure rules and regulations:
- The system antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
- The system antenna used for this module must not exceed 4.9 dBi.
- Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

Installer is advised to clarify any regulatory questions and to have their complete product tested and approved for FCC compliance.

8.5 FCC Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
1. This device may not cause harmful interference
2. This device must accept any interference received, including interference that may cause undesired operation.

8.6 FCC Identifier

FCC ID: ZDSBTM160

8.7 European R&TTE Declaration of Conformity

Hereby, Gibson Corporation, declares that the Bluetooth module BTM160
is in compliance with the essential requirements and other relevant provisions of Directive 1999/5/EC.
As a result of the conformity assessment procedure described in Annex III of the Directive 1999/5/EC, the end customer equipment is labeled as shown in section 8.10.

The BTM160 can be used in the following countries:

Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

8.8 Unauthorized Changes to Equipment Statement

Changes or modifications not expressly approved by Gibson could void the user's authority to operate the equipment.

Declaration of Conformity (DoC)
1999/5/EC

We, Gibson Corporation
309 Plus Park Blvd.
Nashville, TN 37217

declare under our sole responsibility that the product:

Type of equipment: Bluetooth 2.1+EDR Module

Manufacturer: Rayson Technology Company, LTD

Model name: BTM160

to which this declaration relates, is in compliance with all the applicable essential requirements, and other provisions of the European Council Directive:

1999/5/EC	Radio and Telecommunications Terminal Equipment Directive (R&TTE)

The conformity assessment procedure used for this declaration is Annex IV of this Directive. Product compliance has been demonstrated on the basis of:

- IEC 60950-1 (2006)	For article 3.1 (a) : Health and Safety of the User
- EN 301 489-1 V1.8.1 - EN 301 489-17 V2.1.1	For article 3.1 (b) : Electromagnetic Compatibility
- EN 300 328 V1.6.1 (2004-11) - EN 300 328 V1.7.1 (2006-10)	For article 3.2 : Effective use of spectrum allocated

The technical construction file is kept available at:
Gibson Corporation, 309 Plus Park Blvd., Nashville TN 37217, USA

Issued on:

Signed by the manufacturer:
(Company name) Gibson Corporation
(Signature)
(Printed name)
(Title)

Figure 26 Declaration of Conformity

8.8 Bluetooth Qualified Design ID

Gibson has submitted End Product Listing (EPL) for BTM160 under Bluetooth QD ID B013295. Manufacturers of Bluetooth devices incorporating BTM160 can reference the same QD ID number.

8.9 Industry Canada Certification

BTM160 complies with the regulatory requirements of Industry Canada (IC), certification: IC: 9583A-BTM160

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from **www.ic.gc.ca.**

This device has been designed to operate with the antennas listed in Table 13 above, having a maximum gain of 4.9 dBi. Antennas not included in this list or having a gain greater than 4.9 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.	Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

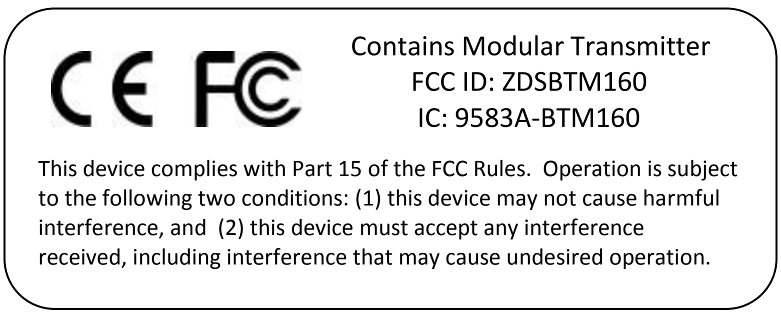
Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.	Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

This radio transmitter IC: 9583A-BTM160 *has been approved by Industry Canada to operate with the*	*Le présent émetteur radio* IC: 9583A-BTM160 *a été approuvé par Industrie Canada pour fonctionner*

antenna types listed in Table 13 with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.	*avec les types d'antenne énumérés en Table 13 et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.*

8.10 Label Design of the Host Product

The following information is required either on a label attached to the host product or silkscreened onto the product itself:



If the device is less than 4” x 4” the lower text may be omitted.

Figure 27 Equipment Label

8.11 End User Product Manual Requirements

The printed or electronic manual provided to the end user needs to contain the following:

This device complies with Part 15 of the FCC Rules and RSS-210 of Industry Canada. Operation is subject to the following two conditions:
1. This device may not cause harmful interference
2. This device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :
(1) l'appareil ne doit pas produire de brouillage
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by 1 or more of the following measures:

- Reorient or relocate the antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio or television technician for help

Caution: Changes or modifications not expressly approved by Gibson could void the user's authority to operate this equipment.