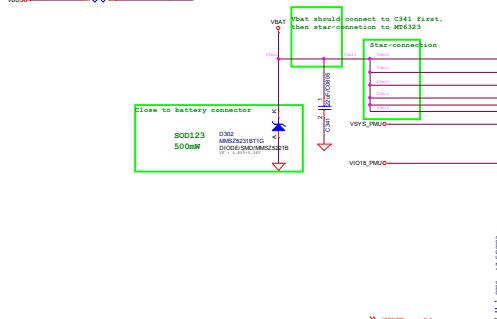
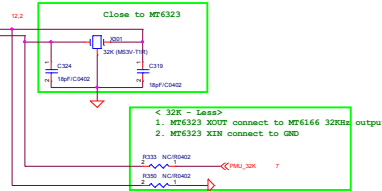
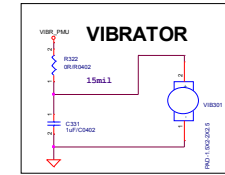
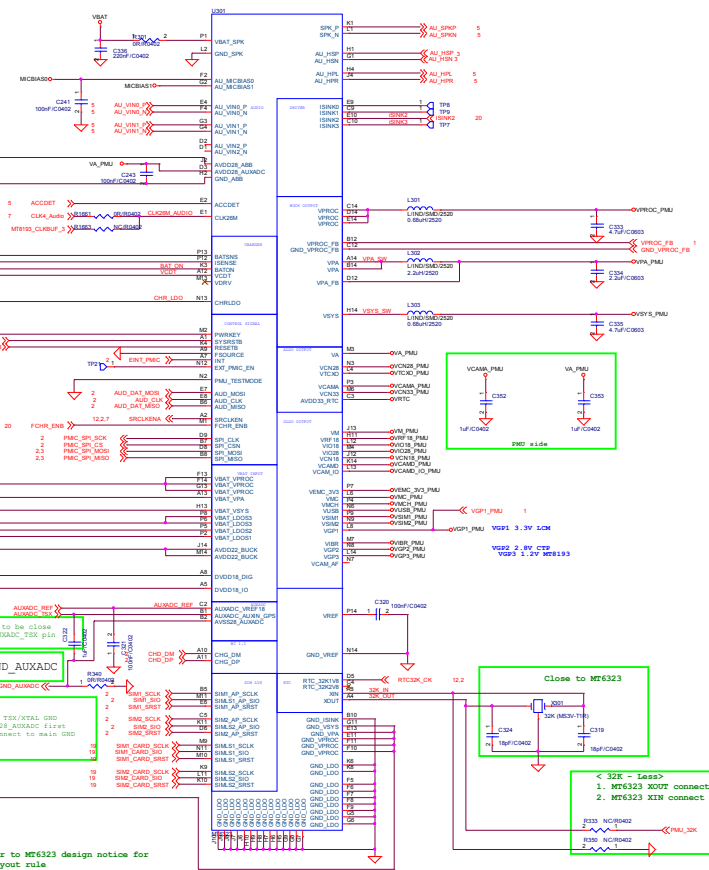




[illegible]

- (1) MT6323 Buck GND (GND_VPROC/GND_VPA/GND_VSYS) is connected together first, and then single trace connect to GND layer
- (2) Use single trace >40mil or GND plan to connect buck input bypass cap and MT6323 GND pins of buck in the same layer, and then isolate this GND plan



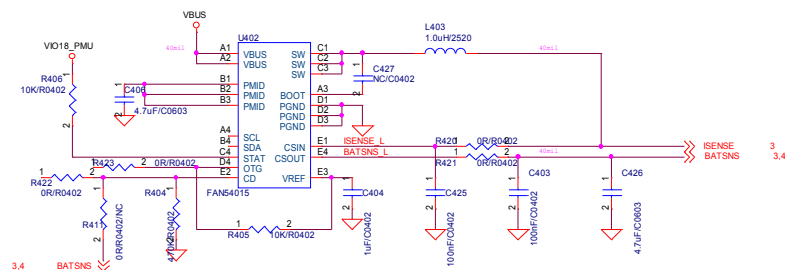
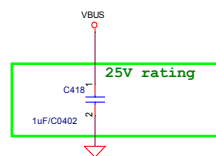
LA	LDO	Output Voltage(V)	Output Current(mA)	Bypass cap	cap range	Notes
VA	2.8	1.8	150	1uF	-20%~+20%	Far-end bypass cap
VCN28	2.8	1.8	30	1uF	-20%~+20%	Far-end bypass cap
VTXCO	2.8	1.8	40	1uF	-20%~+20%	Far-end bypass cap
VCAMA	2.8	1.8	150	3.2uF	-20%~+20%	1uF near-end 2.2uF Far-end bypass cap
VCN33	3.3/3.4/3.5/3.6	240	4.7uF	-20%~+20%	Far-end bypass cap	
VRTC	2	2	0.1uF or 1000uF	-20%~+20%	Far-end bypass cap	
VTA	1.24/1.39/1.54/1.84	700	10uF	-20%~+20%	Far-end bypass cap	
VRF18	1.8/25	200	4.7uF	-20%~+200%	Far-end bypass cap	
VIO18	1.8	300	4.7uF	-20%~+200%	Far-end bypass cap	
VCIO28	2.8	200	2.2uF	-20%~+200%	Far-end bypass cap	
VCN18	1.8	120	1uF	-20%~+20%	Far-end bypass cap	
VCAMD	1.2/1.3/1.5/1.8	150	1uF	-20%~+20%	Far-end bypass cap	
VCAM_J0	1.8	100	1uF	-20%~+20%	Far-end bypass cap	
VFSB_V3/3	3.0/3.3	400	4.7uF	-20%~+20%	Far-end bypass cap	
VMC	1.8/3.3	100	1uF	-20%~+20%	Far-end bypass cap	
VMCH	3.0/3.3	400	2.2uF	-20%~+20%	Far-end bypass cap	
VUSB	3.3	20	1uF	-20%~+20%	Far-end bypass cap	
VSM1	1.8/3.0	50	1uF	-20%~+20%	Far-end bypass cap	
VSM2	1.8/3.0	50	1uF	-20%~+20%	Far-end bypass cap	
VGP1	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	100	1uF	-20%~+20%	Far-end bypass cap	
VGP2	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	100	1uF	-20%~+20%	Far-end bypass cap	
VGP3	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	100	1uF	-20%~+20%	Far-end bypass cap	
VCAM_AF	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	100	1uF	-20%~+20%	Far-end bypass cap	
VDIG18	1.8	20	1uF	-20%~+20%	Far-end bypass cap	

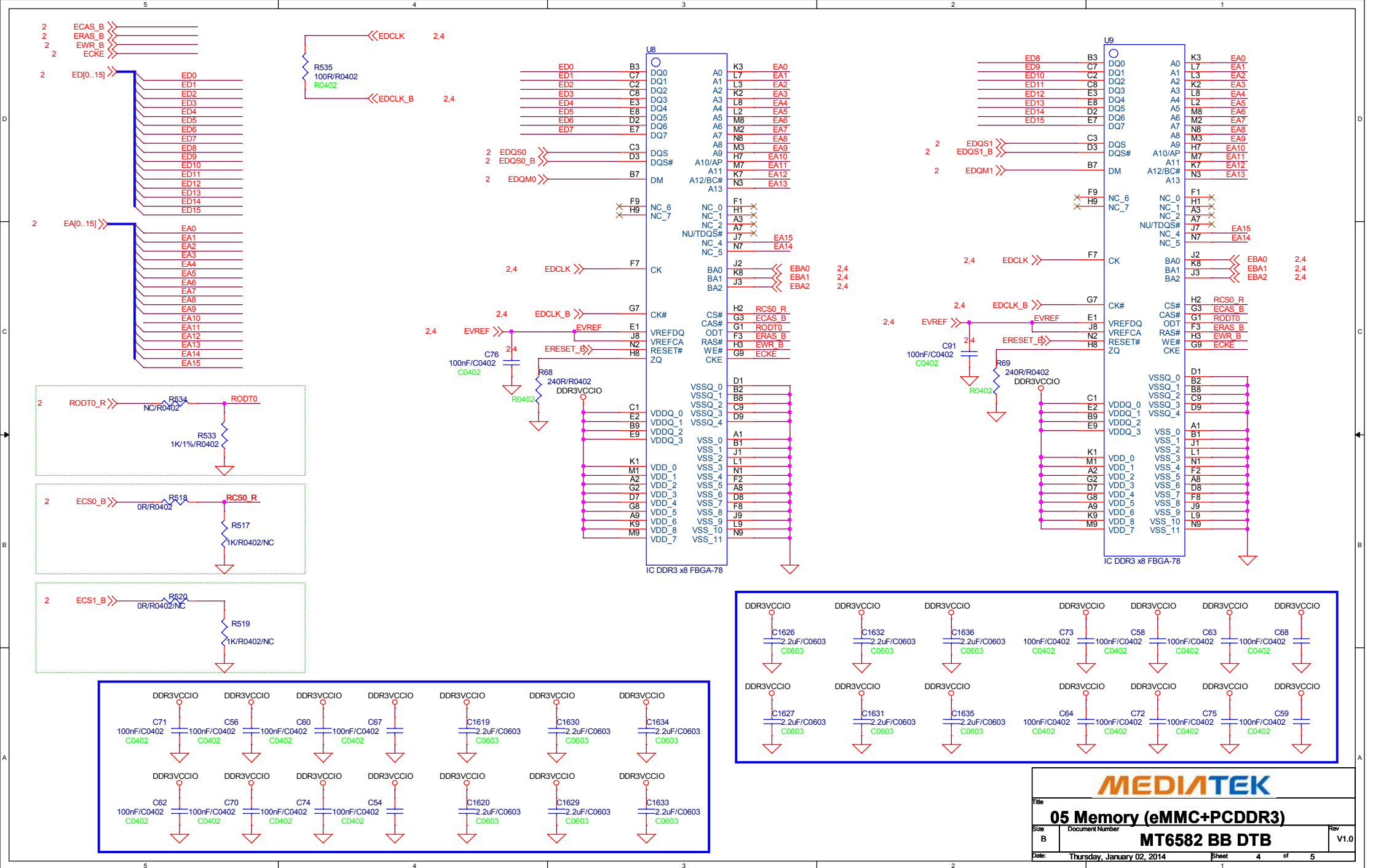
A



MODE \ Logic	DCXO = 32K_EN	XMODE	VXODIG
DCXO + 32K XO	0 (GND)	1 (VIO18)	1 (VIO18)
DCXO + 32K-Less	1 (VFXCO28)	1 (VFXCO28)	1 (VFXCO28)

Switching Charger



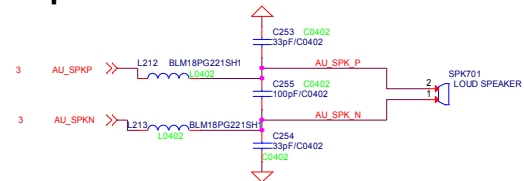
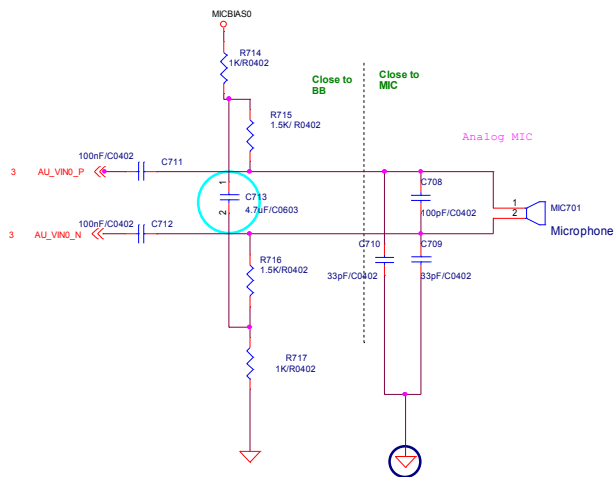


Speaker

3 AU_SPKP >> L212 BLM18PG221SH C253 C0402 33pF/C0402 AU_SPK_P

3 AU_SPKN >> L213 BLM18PG221SH C254 C0402 33pF/C0402 AU_SPK_N

2 1 SPK701 LOUD SPEAKER

[illegible]

close to IC

close to connector

3 AU_HSP

3 AU_HSN

C706
33pF/C0402

C705
100pF/C0402

C704
33pF/C0402

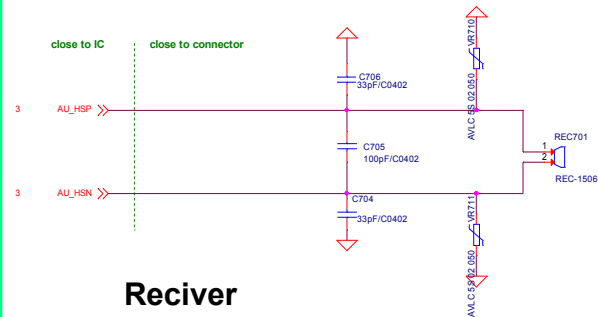
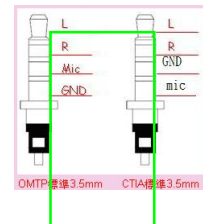
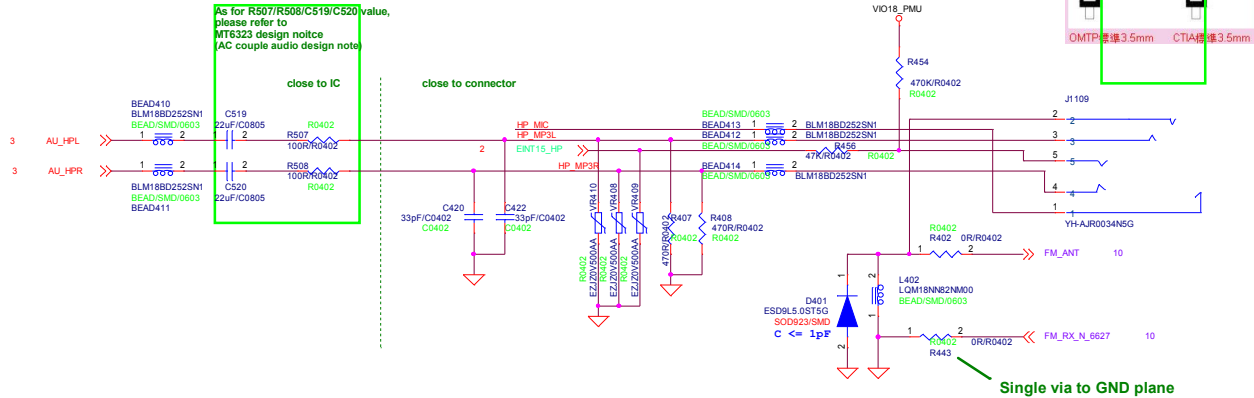
AVX C-85 02 500

AVX C-85 02 100

REC701

REC-1506

Reciver

[illegible]

Earphone MICPHONE

Earphone MICPHONE

Close to BB

Close to MIC

3 AU_VIN1_N >> C525 2 || 100nF/C0402

3 AU_VIN1_P >> C535 2 || 100nF/C0402

3 ACCDET <<< R516 1 2 1K/R0402

1 MICBIAS1

1K/R0402

R1011

C532 1 2 10uF/C0803

GND_EARMIC

Close to EarJack

tie together and single via to GND plane

HP_MIC

33pF/C0402

100pF/C0402

C534 1 2

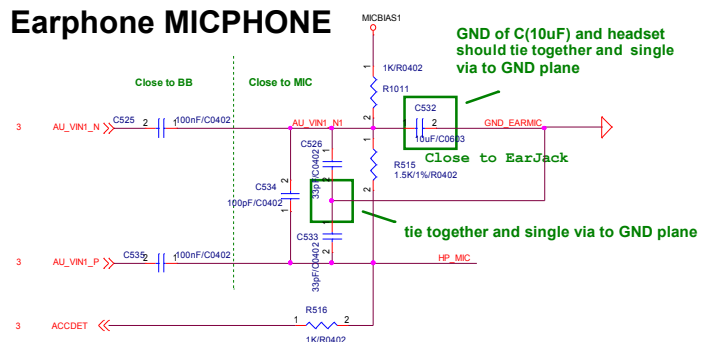
C533 1 2

33pF/C0402

100pF/C0402

1.5K/R0402

R515



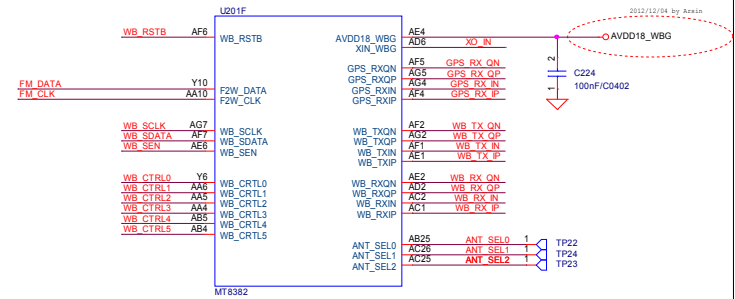
GND of C(10uF) and headset should tie together and single via to GND plane

Close to EarJack

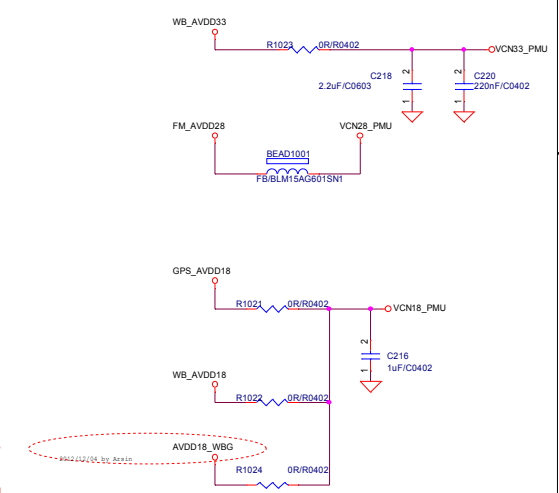
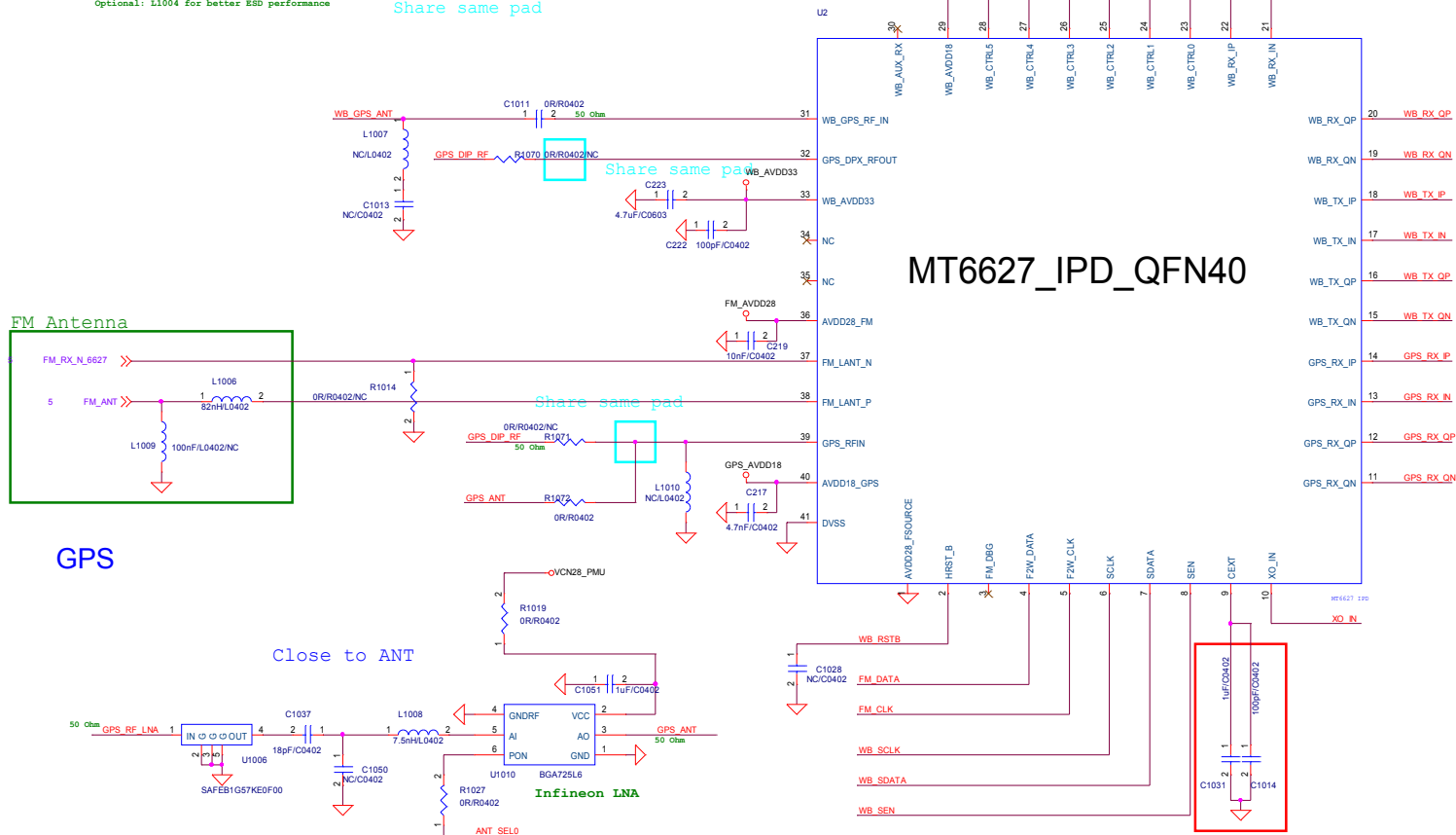
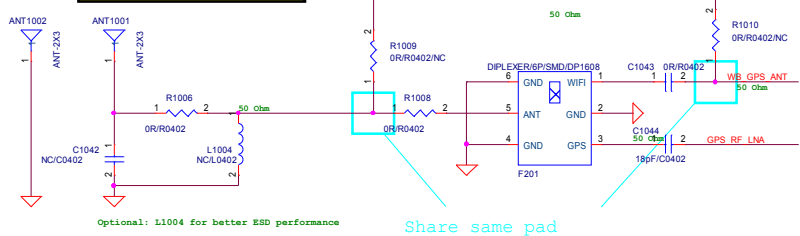
tie together and single via to GND plane

The schematic diagram illustrates the SDIO interface between the SDINCS2-16GBALLS and the U504 controller. The U504 controller is shown with its pins connected to the SDINCS2-16GBALLS pins. The connections are as follows:

- U504 Pin 1 (T10):** Connected to VEMC_3V3_PMU.
- U504 Pin 2 (U8):** Connected to VEMC_3V3_PMU.
- U504 Pin 3 (U9):** Connected to VEMC_3V3_PMU.
- U504 Pin 4 (U6):** Connected to VEMC_3V3_PMU.
- U504 Pin 5 (U7):** Connected to VEMC_3V3_PMU.
- U504 Pin 6 (U5):** Connected to VEMC_3V3_PMU.
- U504 Pin 7 (U4):** Connected to VEMC_3V3_PMU.
- U504 Pin 8 (U3):** Connected to VEMC_3V3_PMU.
- U504 Pin 9 (U2):** Connected to VEMC_3V3_PMU.
- U504 Pin 10 (U1):** Connected to VEMC_3V3_PMU.
- U504 Pin 11 (U0):** Connected to VEMC_3V3_PMU.
- U504 Pin 12 (U10):** Connected to VEMC_3V3_PMU.
- U504 Pin 13 (U9):** Connected to VEMC_3V3_PMU.
- U504 Pin 14 (U8):** Connected to VEMC_3V3_PMU.
- U504 Pin 15 (U7):** Connected to VEMC_3V3_PMU.
- U504 Pin 16 (U6):** Connected to VEMC_3V3_PMU.
- U504 Pin 17 (U5):** Connected to VEMC_3V3_PMU.
- U504 Pin 18 (U4):** Connected to VEMC_3V3_PMU.
- U504 Pin 19 (U3):** Connected to VEMC_3V3_PMU.
- U504 Pin 20 (U2):** Connected to VEMC_3V3_PMU.
- U504 Pin 21 (U1):** Connected to VEMC_3V3_PMU.
- U504 Pin 22 (U0):** Connected to VEMC_3V3_PMU.
- U504 Pin 23 (U10):** Connected to VEMC_3V3_PMU.
- U504 Pin 24 (U9):** Connected to VEMC_3V3_PMU.
- U504 Pin 25 (U8):** Connected to VEMC_3V3_PMU.
- U504 Pin 26 (U7):** Connected to VEMC_3V3_PMU.
- U504 Pin 27 (U6):** Connected to VEMC_3V3_PMU.
- U504 Pin 28 (U5):** Connected to VEMC_3V3_PMU.
- U504 Pin 29 (U4):** Connected to VEMC_3V3_PMU.
- U504 Pin 30 (U3):** Connected to VEMC_3V3_PMU.
- U504 Pin 31 (U2):** Connected to VEMC_3V3_PMU.
- U504 Pin 32 (U1):** Connected to VEMC_3V3_PMU.
- U504 Pin 33 (U0):** Connected to VEMC_3V3_PMU.
- U504 Pin 34 (U10):** Connected to VEMC_3V3_PMU.
- U504 Pin 35 (U9):** Connected to VEMC_3V3_PMU.
- U504 Pin 36 (U8):** Connected to VEMC_3V3_PMU.
- U504 Pin 37 (U7):** Connected to VEMC_3V3_PMU.
- U504 Pin 38 (U6):** Connected to VEMC_3V3_PMU.
- U504 Pin 39 (U5):** Connected to VEMC_3V3_PMU.
- U504 Pin 40 (U4):** Connected to VEMC_3V3_PMU.
- U504 Pin 41 (U3):** Connected to VEMC_3V3_PMU.
- U504 Pin 42 (U2):** Connected to VEMC_3V3_PMU.
- U504 Pin 43 (U1):** Connected to VEMC_3V3_PMU.
- U504 Pin 44 (U0):** Connected to VEMC_3V3_PMU.
- U504 Pin 45 (U10):** Connected to VEMC_3V3_PMU.
- U504 Pin 46 (U9):** Connected to VEMC_3V3_PMU.
- U504 Pin 47 (U8):** Connected to VEMC_3V3_PMU.
- U504 Pin 48 (U7):** Connected to VEMC_3V3_PMU.
- U504 Pin 49 (U6):** Connected to VEMC_3V3_PMU.
- U504 Pin 50 (U5):** Connected to VEMC_3V3_PMU.
- U504 Pin 51 (U4):** Connected to VEMC_3V3_PMU.
- U504 Pin 52 (U3):** Connected to VEMC_3V3_PMU.
- U504 Pin 53 (U2):** Connected to VEMC_3V3_PMU.
- U504 Pin 54 (U1):** Connected to VEMC_3V3_PMU.
- U504 Pin 55 (U0):** Connected to VEMC_3V3_PMU.
- U504 Pin 56 (U10):** Connected to VEMC_3V3_PMU.
- U504 Pin 57 (U9):** Connected to VEMC_3V3_PMU.
- U504 Pin 58 (U8):** Connected to VEMC_3V3_PMU.
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- U504 Pin 61 (U5):** Connected to VEMC_3V3_PMU.
- U504 Pin 62 (U4):** Connected to VEMC_3V3_PMU.
- U504 Pin 63 (U3):** Connected to VEMC_3V3_PMU.
- U504 Pin 64 (U2):** Connected to VEMC_3V3_PMU.
- U504 Pin 65 (U1):** Connected to VEMC_3V3_PMU.
- U504 Pin 66 (U0):** Connected to VEMC_3V3_PMU.
- U504 Pin 67 (U10):** Connected to VEMC_3V3_PMU.
- U504 Pin 68 (U9):** Connected to VEMC_3V3_PMU.
- U504 Pin 69 (U8):** Connected to VEMC_3V3_PMU.
- U504 Pin 70 (U7):** Connected to VEMC_3V3_PMU.
- U504 Pin 71 (U6):** Connected to VEMC_3V3_PMU.
- U504 Pin 72 (U5):** Connected to VEMC_3V3_PMU.
- U504 Pin 73 (U4):** Connected to VEMC_3V3_PMU.
- U504 Pin 74 (U3):** Connected to VEMC_3V3_PMU.
- U504 Pin 75 (U2):** Connected to VEMC_3V3_PMU.
- U504 Pin 76 (U1):** Connected to VEMC_3V3_PMU.
- U504 Pin 77 (U0):** Connected to VEMC_3V3_PMU.
- U504 Pin 78 (U10):** Connected to VEMC_3V3_PMU.
- U504 Pin 79 (U9):** Connected to VEMC_3V3_PMU.
- U504 Pin 80 (U8):** Connected to VEMC_3V3_PMU.
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- U504 Pin 84 (U4):** Connected to VEMC_3V3_PMU.
- U504 Pin 85 (U3):** Connected to VEMC_3V3_PMU.
- U504 Pin 86 (U2):** Connected to VEMC_3V3_PMU.
- U504 Pin 87 (U1):** Connected to VEMC_3V3_PMU.
- U504 Pin 88 (U0):** Connected to VEMC_3V3_PMU.
- U504 Pin 89 (U10):** Connected to VEMC_3V3_PMU.
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- U504 Pin 99 (U0):** Connected to VEMC_3V3_PMU.
- U504 Pin 100 (U10):** Connected to VEMC_3V3_PMU.
- U504 Pin 101 (U9):** Connected to VEMC_3V3_PMU.
- U504 Pin 102 (U8):** Connected to VEMC_3V3_PMU.
- U504 Pin 103 (U7):** Connected to VEMC_3V3_PMU.
- U504 Pin 104 (U6):** Connected to VEMC_3V3_PMU.
- U504 Pin 105 (U5):** Connected to VEMC_3V3_PMU.
- U504 Pin 106 (U4):** Connected to VEMC_3V3_PMU.
- U504 Pin 107 (U3):** Connected to VEMC_3V3_PMU.
- U504 Pin 108 (U2):** Connected to VEMC_3V3_PMU.
- U504 Pin 109 (U1):** Connected to VEMC_3V3_PMU.
- U504 Pin 110 (U0):** Connected to VEMC_3V3_PMU.
- U504 Pin 111 (U10):** Connected to VEMC_3V3_PMU.
- U504 Pin 112 (U9):** Connected to VEMC_3V3_PMU.
- U504 Pin 113 (U8):** Connected to VEMC_3V3_PMU.
- U504 Pin 114 (U7):** Connected to VEMC_3V3_PMU.
- U504 Pin 115 (U6):** Connected to VEMC_3V



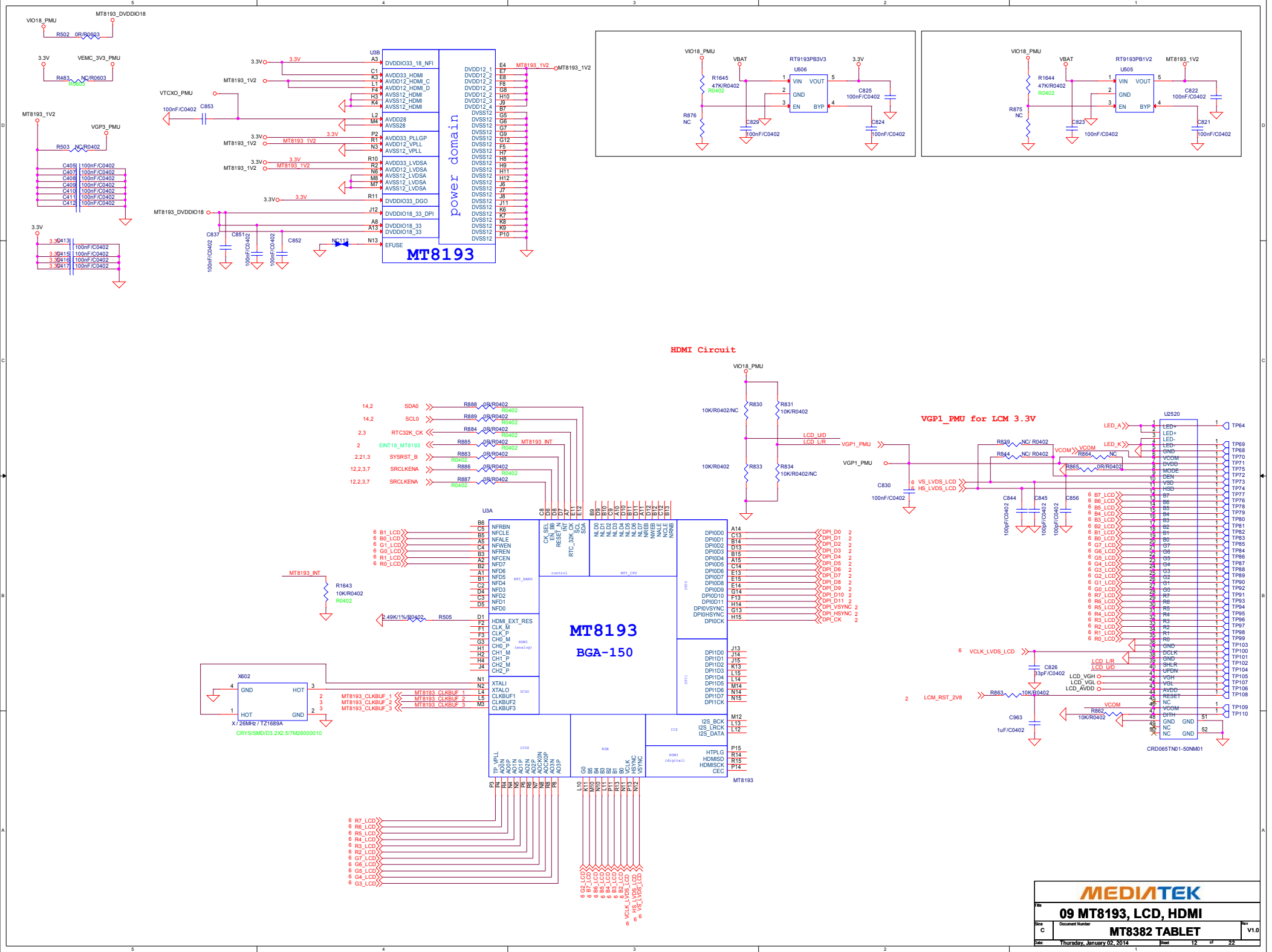
wifi 2412-2462MHz
BT: 2402-2480MHz

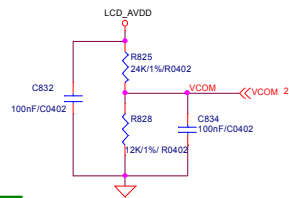
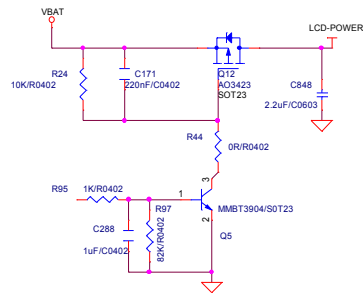


MT6627_IPD_QFN40

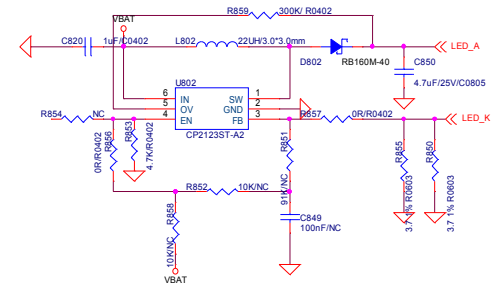
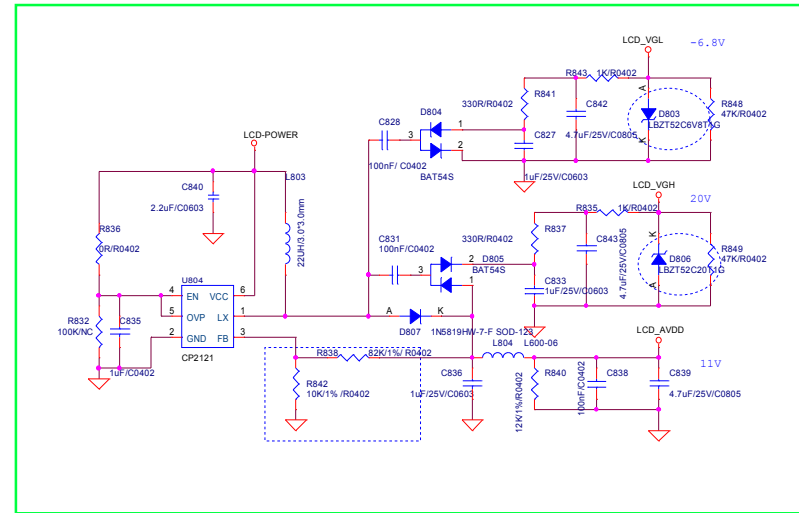
GPS

Close to ANT



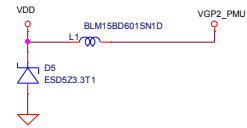


DVDD	3.0 ~ 3.6v (typ. 3.3v)
AVDD	10.8 ~ 11.2v (typ. 11.0v)
VGH	19.7 ~ 20.3v (typ. 20.0v)
VGL	-7.1 ~ -6.5v (typ. -6.8v)
VCOM	3.46 ~ 3.86v (typ. 3.66v)

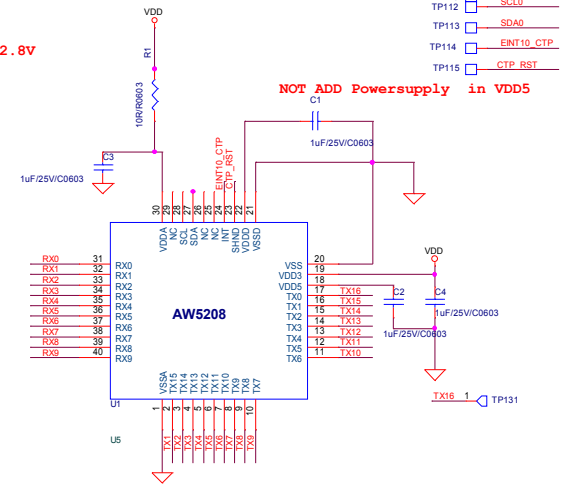


LED Backlight Driver

VGP2_PMU for CTP 2.8V

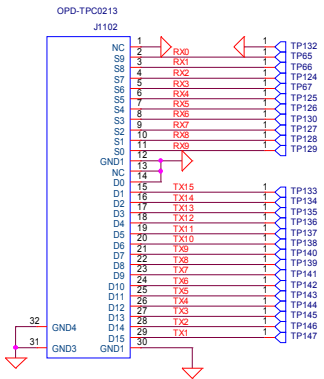


NOT ADD Powersupply in VDD5

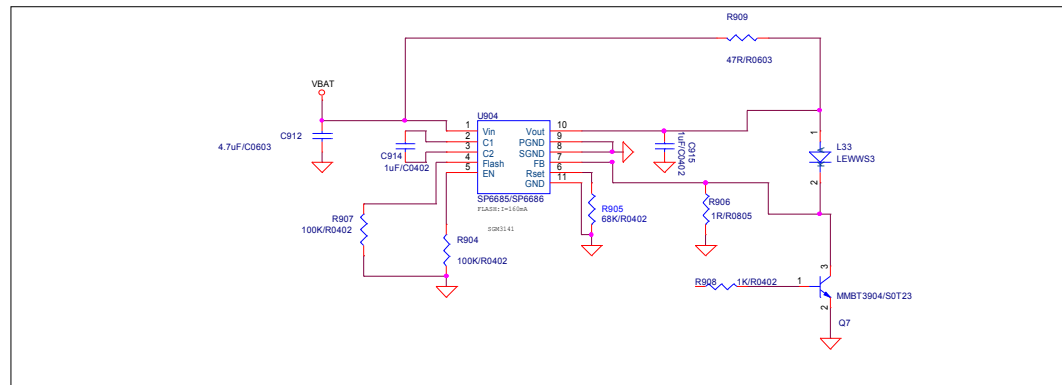
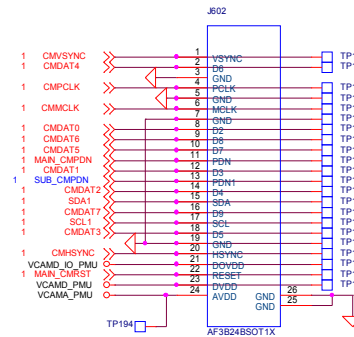
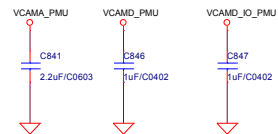


Touch Panel IC circuit

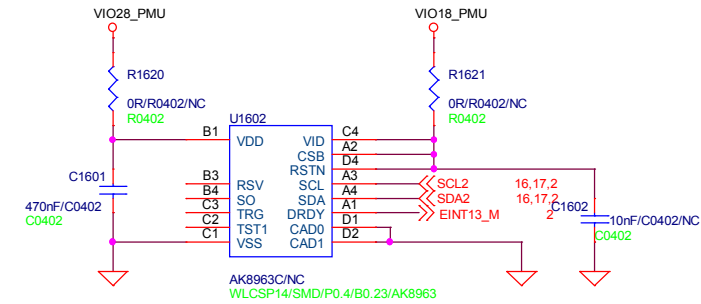
Touch Panel Connector1



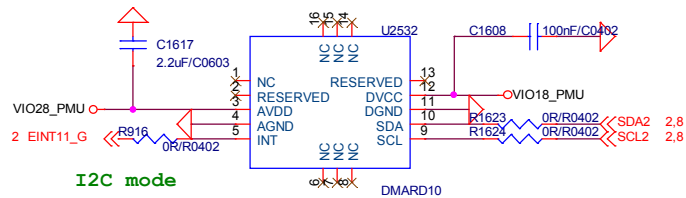
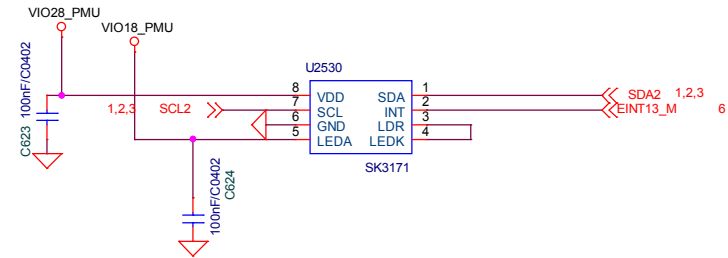
Main/Sub Camera



M-Sensor



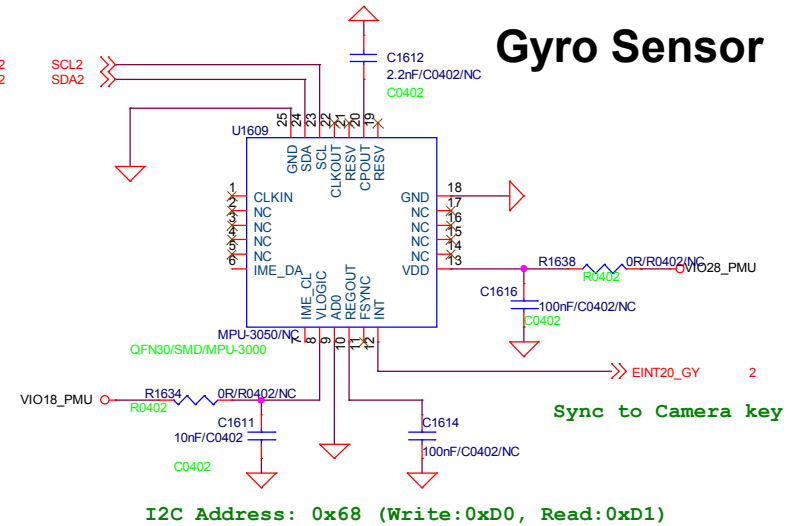
I2C Address: 0x0C (Write:0x18, Read:0x19)



I2C mode

I2C Address: 0x4C (Write:0x98, Read:0x99)

Gyro Sensor



Sync to Camera key

I2C Address: 0x68 (Write:0xD0, Read:0xD1)

MEDIATEK

Title		
21 Sensors, OFN (Key)		
Size	Document Number	Rev
B	MT8382 TABLET	V1.0
Date: Thursday, January 02, 2014		
Sheet 17 of 22		

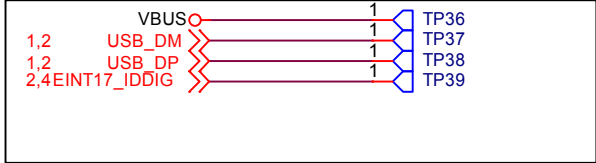
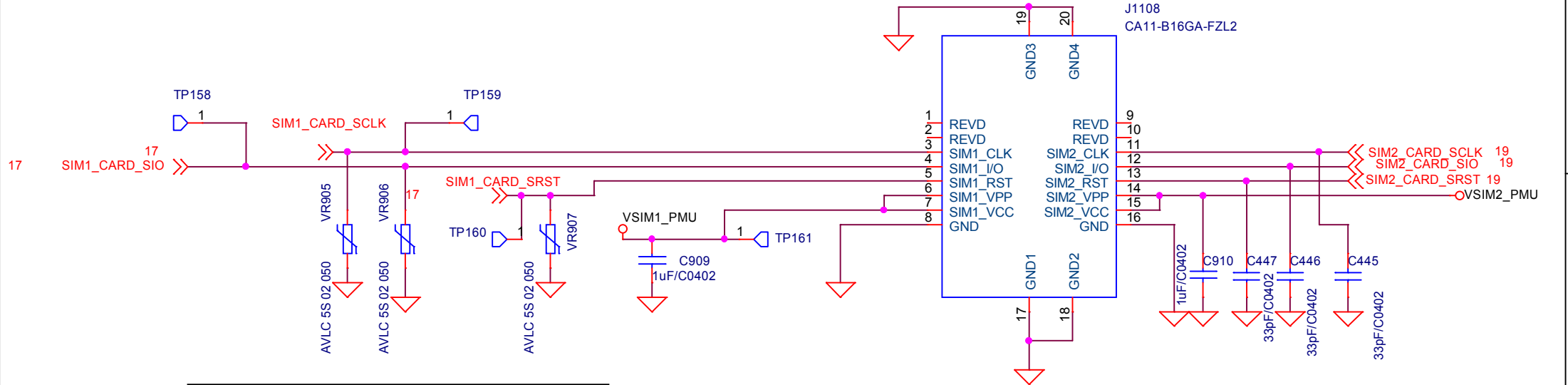
SW: Shielding connector to ground
L: Card insert



Shielding connect to ground



SIM



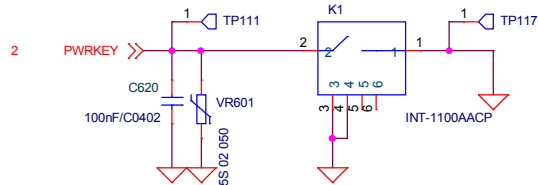
USB

BIG_SIM

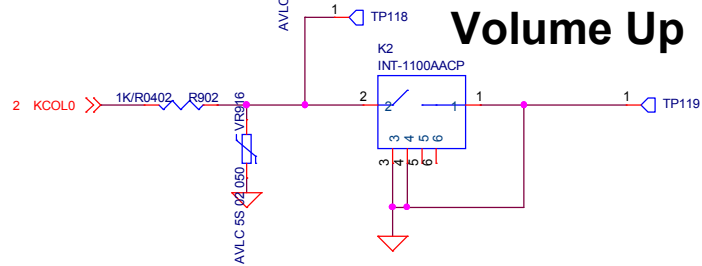
MEDIATEK			
Title			
19 Dual SIM, IC-USB			
Size	Document Number		Rev
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Power Key

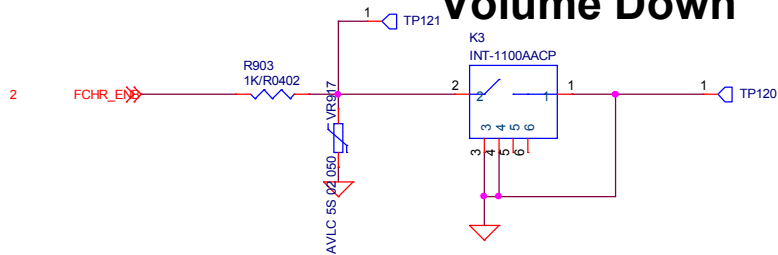
DO NOT put pull-up resistor on PWRKEY



Volume Up

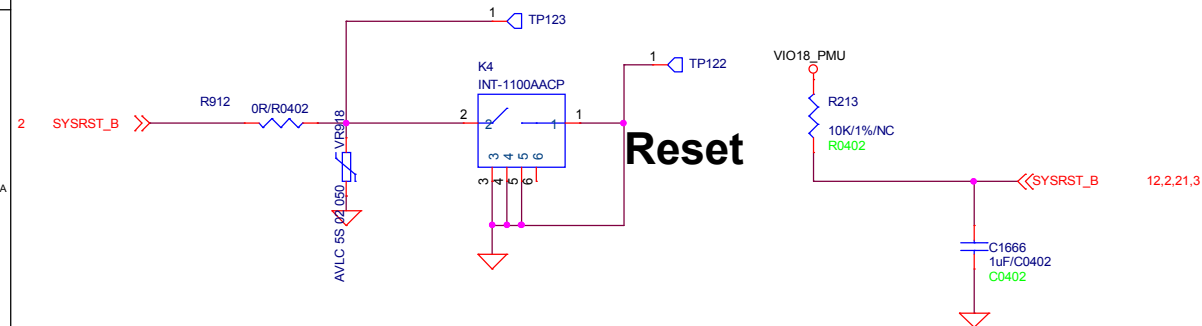


Volume Down



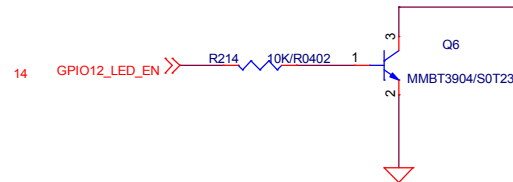
FCHR_ENB can be configured as a normal key function

Reset



LED

Red
Blue

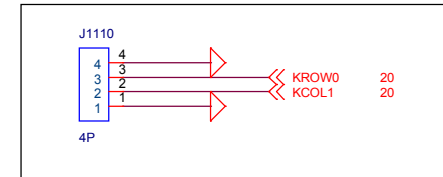
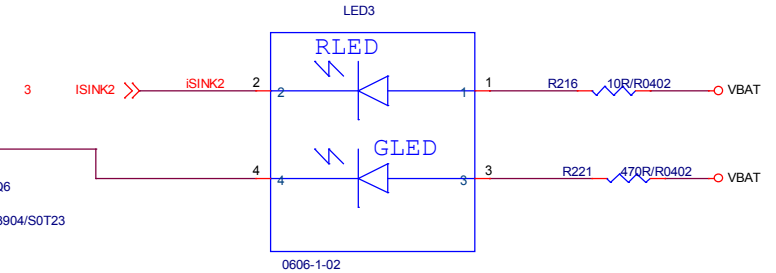


Notice :

1. Due to KCOL0 & KROW0 reset mode = GPIO input mode, "Force USB download mode" will be fail in KCOL0+KROW0. So we change VolumeUp key=KCOL0+GND
2. Keypad matrix will become as (KEY1=KCOL0+GND)

	KCOL0	KCOL1	KCOL2
KROW0	KEY 2	KEY 3	KEY 4
KROW1	KEY 5	KEY 6	KEY 7
KROW2	KEY 8	KEY 9	KEY 10

Indicator LED



Notice :

- There are 3 options for "Long press to shutdown" function
1. PWRKEY + FCHR_ENB
 2. PWRKEY only
 3. FCHR_ENB only

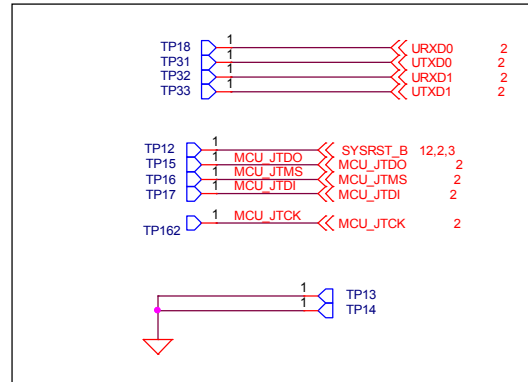
During download mode, default = PWRKEY + FCHR_ENB
For other case (exclude download mode), default = PWRKEY only

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20 Key LEDs

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Net	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5
JTMS	GPIO76	B1:JTMS	I1:CONN_MCU_TMS			
JTCK	GPIO77	I0:JTCK	I0:CONN_MCU_TCK1			
JTDI	GPIO78	I1:JTDI	I0:CONN_MCU_TDI			
JTDO	GPIO79	O:JTDO	O:CONN_MCU_TDO			
EINT1	GPIO1	O:PWM2	O:DPI_D5	I0:MD_EINT1	O: TDD_TDO	O:CONN_MCU_TDO
EINT2	GPIO2	O:CLKM0	O:DPI_D6	I0:MD_EINT2		O:CONN_MCU_DBGACK_N
EINT3	GPIO3	O:CLKM1	O:DPI_D7	I0:SPI_MI	I0:MD_EINT3	I1:CONN_MCU_DBGI_N
EINT4	GPIO4	O:CLKM2	O:DPI_D8	O:SPI_MO	I1:TDD_TCK	I0:CONN_MCU_TCK0
EINT5	GPIO5	I1:UCTS2	O:DPI_D9	O:SPI_CS	I1: TDD_TDI	I0:CONN_MCU_TDI
EINT6	GPIO6	O:URTS2	O:DPI_D10	O:SPI_CK	I0:TDD_TRSTN	I0:CONN_MCU_TRST_B
EINT7	GPIO7	I1:UCTS3	O:DPI_D11	B1:SDA1	I1: TDD_TMS	I1:CONN_MCU_TMS
ANT_SEL0	GPIO47	O:ANT_SEL0	O:PWM0	O:CONN_MCU_DBGACK_N		
ANT_SEL1	GPIO48	O:ANT_SEL1	O:PWM1	I1:CONN_MCU_DBGI_N		
ANT_SEL2	GPIO49	O:ANT_SEL2	O:PWM2	I0:CONN_MCU_TRST_B		

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5					4					3					2					1				
D	4/11 1. Update MT6166 26M Xtal, X600 change to EPSON X1E000021043400 2. U610 change to SAYRF1G88CA0B0A(B2) 3. U613 change to SAFEA2G34FA1F0A 4. Add C613 & C614 for RF request. 5. Reserve L636 for RF tuning. 6. Net: VDD18_6583 chage to VIO18_PMU.					5/31, 1. Update MT8193 Power circuit. 2. Update MT8193 HDMI AVDD33 circuit.					6/3, 1. Add R104/R110/R112/R119/R120/R121/R122/R123 for low power measurement.													
	4/14 1. Remove R1073, and let MT6627 pin#34 NC. 2. L1009 change to NC. 3. Update U2 new part, 鋳セpin #36~38) 鋳T端, pin#36~38鎖結 機. 4. GPS default 叫jexternal LNA path R1010, R1009, R1070,R1071 --> NC R1072, R1019, R1027, C1043, R1008 --> 0 ohm 5. Up date F201 part/footprint to DIPLEXER/6P/SMD/DP1608 6. C1218, C1219 change to 22 pF ; C1214, C1215 change to 1.2 pF. C1216, C1217 change to 68 pF ; C1203 change to 4.7uF 7. C222 change to 4.7uF.					6/18, 1. R221 change to NC. 2. R404 change to 470K for battery low power performance. 3. Add C544 (please refer to vender datasheet to get recommand eMMC VDDI/VCC/VCCQ bypass cap value) 4. MT6166 pin C11 connect to GND. (SYNC with MT6572) 5. Update MT6166 co-clock/ Xtal mode table. (Page#7) 6. Add C321 7. Add notice for MT6323 Buck GND. (Page#3) 8. Change VolumeUp key = KCOL0+GND. Change Volume down key = FCHR_ENB+GND. Add Key notice. (Page #20) 9. C519 & C520 change to 22uF 0805 for audio HP. 10. Remove R1028, and modify MT6627 26M notice. 11. MT6627 26M default TCXO mode: R1206 --> NC R1205, R1208 --> 0 ohm U1005 --> 26M QVL TCXO with 0.5 ppm (2.8V)																		
	4/14 1. Add R101, R108, R106, R109, R102, R104, R116, R117, R118, R111, R113, R114, R115 for low power break down. Customer can delet thiese for cost down. 2. Add TP251 & TP252 for NFC debugging. 3. Change R1247 & R1246 connection net name.					6/20, 1. P7, MT6166 change to Xtal mode: R655, R678 --> 0 ohm. R340, R656, R677 --> NC X600 --> MT6166 QVL Xtal 2. Add R1643, MT8193 INT PD.																		
C	4/15, Remove some RF components for cost down. 1. Remove U602, R615, R628, and delet PDET_ALL net. 2. Remove Page 11 all component, and delet Carket net. 3. Remove U108.																							
	4/16, 1. Add C353, VA_PMU to GND power. 2. Update Page03, ISENSE &BATSNS connection for guage function. 3. Add R339 for CHR_LDO connection.																							
	4/18, 1. Update page#19, SIM card to NFC circuit. 2. Update SIM to Micro-SIM footprint.																							
B	4/19, 1. C223 change to 2.2uF, and C222 change to 100 pF. 2. Add C220 and C218 for WCN tuning. 3. C1011 change to 0 ohm. 4. Add R1254 & R1255 for NFC antenna tuning.																							
	5/6, 1. GPIO12 & GPIO13 can't be used as EINT function. Exchange MT8382 GPIO12/GPIO13/KPROWL/KPCOL2																							
A																								
5					4					3					2					1				