MD251 user manual

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Contents

0 Version History

Data	Version	Description of change	Author
2011-08-01	01.00	Origin	Changchun Zhu
2012-01-09	01.01	Modify the Power Domain of EINT0 and EINT1 from VDDK to VDD	Changchun Zhu

1 Introduction

This document describes the hardware interface of the MD251 GSM/GPRS module which can be integrated with a wide range of applications. This document can help you quickly understand MD251 interface specifications, electrical and mechanical details. With the help of this document and other MD251 application notes, user guide, you can use MD251 module to design and set-up mobile applications quickly.

1.1. Related documents

[1]	GSM 07.07:	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.05:	Digital cellular telecommunications (Phase 2+); Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE –DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[3]	GSM 11.14:	Digital cellular telecommunications system (Phase 2+); Specification of the SIM Application Toolkit for the Subscriber Identity Module –Mobile Equipment (SIM – ME) interface
[4]	GSM 11.11:	Digital cellular telecommunications system (Phase 2+); Specification of the Subscriber Identity Module – Mobile Equipment (SIM – ME) interface
[5]	GSM 03.38:	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[6]	GSM 11.10	Digital cellular telecommunications system (Phase 2)； Mobile Station (MS) conformance specification； Part 1: Conformance specification
[7]	GSM 07.10	Digital Cellular telecommunications system (Phase 2+); Terminal Equipment to Mobile Station multiplexer protocol, verion 7.2.0 Release 1998
[8]	GSM 07.10 V7.1.0	Digital cellular telecommunications system (Phase 2+);Terminal Equipment to Mobile Station (TE-MS)multiplexer protocol
[9]	GSM 07.07 V7.5.0	AT command set for GSM Mobile Equipment
[12]	CMT 09102006	CMT Wirless Phone feature

2. Product concept

Designed for global market, MD251 is a Dual-band GSM/GPRS engine that works on frequencies EGSM 900 MHz/DCS 1800 MHz or GSM850/PCS1900 MHz. MD251 provides GPRS multi-slot class 12 capability.

With a tiny configuration of 24*24*2.9 (mm), MD251 can fit almost all the space requirement in your application, such as Smart phone, PDA phone and wireless phone. The physical link to the interface board is 72 soldering pins.

The MD251 module is designed with power saving technique, the current consumption to as low as 2-3mA in Sleep mode (depends on network condition).

2.1. MD251 features at a glance

Feature	**Implementation**
Power supply	Single supply voltage 3.4V – 4.2V, typical: 3.7V
Power saving	Typical power consumption in Sleep mode to 3-4mA depends on network condition
Frequency bands	MD251 Dual band: EGSM 900/ DCS 1800 or GSM850/PCS 1900.
Transmit power	Class 4 (2W) at EGSM900 Class 1 (1W) at DCS1800 and PCS 1900
GPRS connectivity	GPRS multi-slot class 12 GPRS mobile station class B
Temperature range	Normal operation: -40°C to +85°C
SMS	MT, MO, CB, Text and PDU mode SMS storage: SIM card Support transmission of SMS alternatively over CSD or GPRS. User can choose preferred mode.
FAX	Group 3 Class 1
SIM interface	Supported SIM card: 1.8V/3V
External antenna	Connected via antenna pad
Phonebook management	Supported phonebook types: SM, FD, LD, RC, ON, MC.
SIM Application Toolkit	Supports SAT class 3, GSM 11.14 Release 97
Real time clock	Implemented
Timer function	Programmable via AT command
Physical characteristics	Size: 24*24*2.9 Weight: 6g
Firmware upgrade	Firmware upgradeable over serial interface

3. Hardware Interface

3.1. Module Interface

The 72 pins described in detail in following chapters:
Power supply
Serial interface
Analog audio interfaces
PCM interface
PWM
Antenna
SIM interface
Keyboard interface
LCD interface
Charger Detect
SD/MMC Card
RTC backup battery
IOs
External Interrupt
ADC

3.2. Pin description

Table 1: Pin description

Item	Name	Function	Aux Function0	Aux1	Aux2	PD/PU	Power Domain
P1	Vbat						
P2	Vbat						
P3	GND	Power supply 3.4-4.6V					
P4	MICP0						
P5	MICN0						
P6	AU_OUT0_P						
P7	AU_OUT0_N	Audio 0 chanel					
P8	MP3_OUTR						
P9	MP3_OUTL						
P10	MICP1	Audio 1 chanel					
P11	SPK_N	700mW class-AB amplifier					
P12	SPK_P	output 8ohm load					
P13	RESETB	Power on reset (low active)					
P14	VIO	2.8V power output					
P15	SIM1_IO						
P16	SIM1_CK						
P17	SIM1_RST						
P18	VSIM1	SIM1					
P19	PWM	Pulse-width modulated signal					VDD*

P20	PWRKEY	Power key press input (low active)					
P21	DAIRST	DAI reset signal	GPIO18			PD	VDD
P22	DAISYNC	DAI frame synchronization	GPIO19			PD	VDD
P23	BT_EINT1	External interupt 1	GPIO27			PU	VDD*
P24	KCO0	Keypad(If partly pins are not used as keypad also could use as GPIO)	GPIO7			PU	VDD
P25	KCO1		GPIO6			PU	VDD
P26	KCO2		GPIO5	uart1 cts		PU	VDD
P27	KCO3		GPIO4	uart1 cts		PU	VDD
P28	KCO4		GPIO3	cam_scl		PU	VDD
P29	KROW0		GPIO13		LSDI	PD	VDD
P30	KROW1		GPIO12		LSDA	PD	VDD
P31	KROW2		GPIO11		LSCK	PD	VDD
P32	KROW3		GPIO10	uart1 rts	LSA0	PD	VDD
P33	KROW4		GPIO9	SRCLKENA		PD	VDD
P34	SRCLKENAI	Security Enable	GPIO35			PD	VDD
P35	BT_32K	Bluetooth 32Khz clk	GPIO34	SRCLKENA		PD	VDD
P36	DAIPCMIN	DAI PCM data input	GPIO17			PD	VDD
P37	DAIPCMOUT	DAI PCM data output	GPIO16			PD	VDD
P38	DAICLK	DAI Interface clock output	GPIO15			PD	VDD
P39	EINT0_Headset	External interupt 0	GPIO26			PU	VDD
P40	MCCLK	SDCard	GPIO37			PD	VDDMSDC*
P41	MCCDA0		GPIO38			PD	VDDMSDC
P42	MCCM0		GPIO39			PD	VDDMSDC
P43	LRD_B	Parallel display interface RD					DVDD*
P44	LWR_B	Parallel display interface WR					DVDD
P45	LPA0	Parallel display interface A0					DVDD
P46	MCINS	SD card detect Input	GPIO36	EINT6		PU	DVDD
P47	UCTS1	Uart1 clear to send	GPIO24	EINT5	CAM_SCL	PU	DVDD
P48	URTS1	Uart2 request to send	GPIO25	EINT6	CAM_SDA	PU	DVDD
P49	URXD3	UART	GPIO20	UCTS2			VDD
P50	UTXD2		GPIO23	UCTS1	CAM_SDA		VDD
P51	URXD1			EINT2	LSCK		VDD
P52	UTXD1			EINT3	LSDA		VDD
P53	UTXD3		GPIO21	URTS2			VDD
P54	URXD2		GPIO22	UCTS1	CAM_SCL		VDD
P55	GPIO70		EINT4	CLK32K	CAM_SCL	PD	VDD
P56	LPCE0B	Parallel display interface CS	GPIO14	LSCE0			DVDD
P57	NLD0	Parallel display interface D0		LSCK			DVDD
P58	NLD1	Parallel display interface D1		LSA0			DVDD
P59	NLD2	Parallel display interface D2		LSDA			DVDD
P60	NLD3	Parallel display interface D3		LSDI			DVDD
P61	NLD4	Parallel display interface D4					DVDD
P62	NLD5	Parallel display interface D5					DVDD
P63	NLD6	Parallel display interface D6					DVDD
P64	NLD7	Parallel display interface D7					DVDD
P65	GND	Antenna					
P66	ANT						
P67	GND						

P68	VBACKUP	Supply voltage of RTC 2.8V					
P69	AUX_IN5	Auxillary ADC Input					
P70	LRSTB	Parallel display interface RST	GPIO41			PD	DVDD
P71	LPTE	Parallel display interface	GPIO40			PD	DVDD
P72	Vcdt	Vcharge Detect >Vbat and <6V					

Notice: 1.VDD(2.7V-2.9V) 2.VDDMSDC(2.7V-3.6V) 3.DVDD(1.7V-1.95V)

3.3. Operating modes

The following table summarizes the various operating modes, each operating modes is referred to in the following chapters.

Table 2: Overview of operating modes

Mode	Function	
Normal operation	GSM/GPRS Sleep	Module will automatically go into Sleep mode if there is no air link activation and no hardware interrupt (such as GPIO interrupt or data on serial port). In this case, the current consumption of module will reduce to the minim. During sleep mode, the module can still receive paging message.
	GSM IDLE	Module has registered to the GSM network, and the module is ready to send and receive.
	GSM TALK	CSD connection is going on between two subscribers. In this case, the power consumption depends on network condition and settings such as DTX off/on, FR/EFR/HR, hopping sequences.
	GPRS IDLE	Module is ready for GPRS data transfer, but no data is currently sent or received. In this case, power consumption depends on network settings and GPRS configuration (e.g. multi-slot settings).
	GPRS DATA	There is GPRS data in transfer (PPP or TCP or UDP). In this case, power consumption is related with network settings (e.g. power control level), uplink / downlink data rates and GPRS configuration (e.g. used multi-slot settings).
POWER DOWN	The power management ASIC disconnects the power supply from the base band part of the module, only the power supply for the RTC is remained. Software is not active. The serial interfaces are not accessible.	
Alarm mode	RTC alert function launches this restricted operation while the module is in POWER DOWN mode. MD251 will not be registered to GSM network and only parts of AT commands can be available.	

3.4. Power supply

The power supply must be able to provide sufficient current up to 2A.

For the VBAT input, a local bypass capacitor is recommended. A capacitor (above 100μF, low ESR) is recommended. Multi-layer ceramic chip (MLCC) capacitors can provide the best combination of low ESR and small size but may not be cost effective. A lower cost choice may be a 100 μF tantalum capacitor (low ESR) with a small (1 μF to 10μF) ceramic in parallel, which is illustrated as following figure. And the capacitors should put as closer as possible to the MD251 VBAT (RF) pins. A voltage regulator diode should been add between the Vbat and Gnd, and the BZV55C5V1 of Philips could been used. The following figure is the recommended circuit.

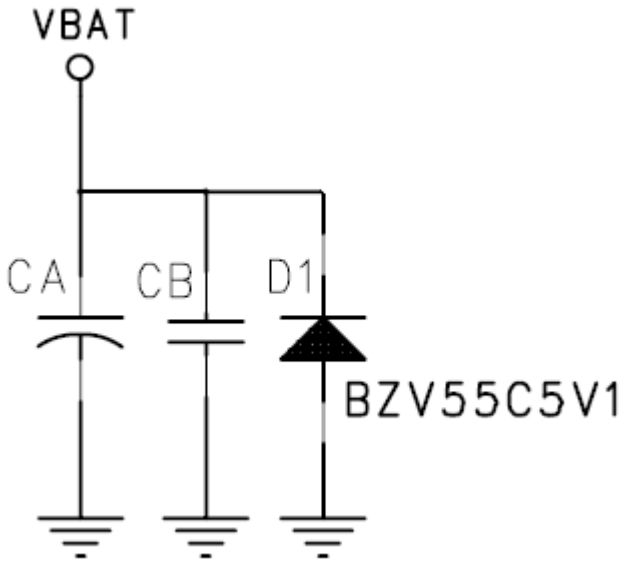


Figure 1：VBAT input

Table3: Power supply pins on the half-circle connector

Num	Name	Function	I/O	Min (V)	Type (V)	Max (V)	Note
1,2	VBAT	Power Supply	Input	3.3	4.2	4.6	Please make sure that the input voltage will never drops below 3.3V even in a transmit burst during which the current consumption may rise up to 2A.
3,65,67	GND	GND	GND				

Minimizing power losses

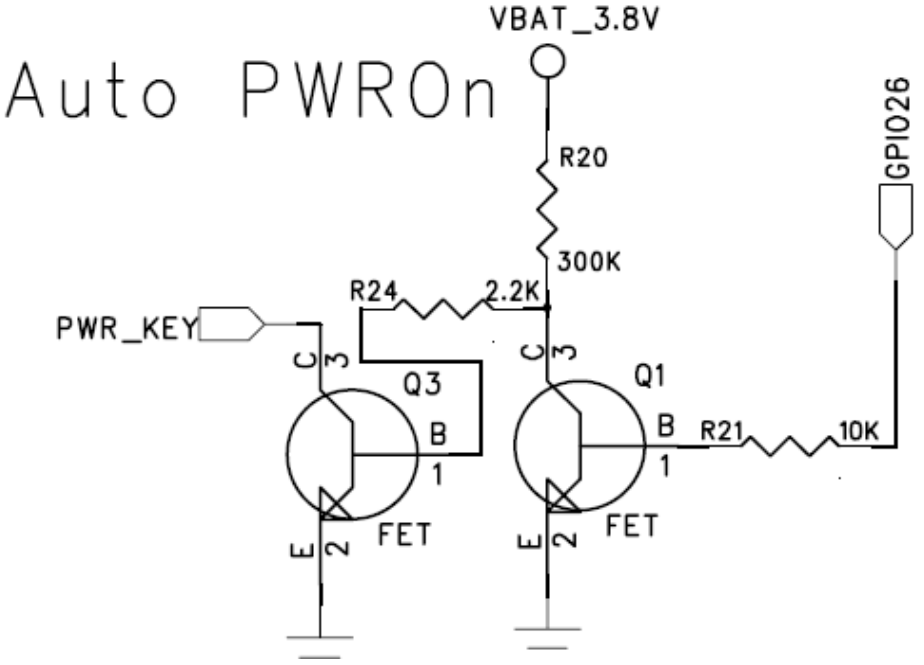
Please pay special attention to the supply power when you are designing your applications. Please make sure that the input voltage will never drops below 3.3V even in a transmit burst during which the current consumption may rise up to 2A. If the power voltage drops below 3.3V, the module may be switched off. You should also take the resistance of the power supply lines on the host board or of battery pack into account.

3.5. Power up and power down scenarios

3.5.1. Turn on MD251

MD251 can be turned on by following two ways:

- Via PWRKEY pin: You can turn on the MD251 to normal operating mode by driving the PWRKEY to a low level voltage for 1500ms;
- Via RTC interrupt: starts ALARM modes;
- For some application system, we can connect the “PWRKEY” to “GND” so that the module will be turn on as soon as the 3.8V power supply to the module. But, if “PWRKEY” linked to “GND”, other keypad pin could not work. Here is a circuit to make the module power on automatically. If the module power on, the GPIO which is PD will output high level, on consequence, the “PWR_KEY” will be high level so that other keypad pin could work.



3.5.2. Turn off MD251

MD251 can be truned off by following two ways:

- Driving the PWRKEY to a low level for 1500ms when module working
- Use “AT + CKPD=”P”, 50” command to turn off MD251 module.

3.5.3. System reset for MD251

You can reset MD251 by driving the “system reset” pin to a low level voltage for 500ms. If MD251 blocked in hardware or software, you can not turn off MD251 by “PWRKEY” pin or by AT command, the only way is driving the “System reset” pin to low level for more than 1s and then high level. The module will reset.

3.5.4. Power saving

3.6. Serial interfaces

MD251 provides 3 UARTs with hardware flow control and speed up to 921600 bps. The UARTs provide full duplex serial communication channels between the module and external devices.
Serial Port can be used for CSD FAX, GPRS service and send AT command of controlling module. Serial port supports the communication rate as following:
1200, 2400, 4800, 9600 (Default), 19200, 38400, 57600, 115200
The serial port
The follow table is the pin definition of UART.

Table4: UART interface of the MD251

Pin	Name	Function	Pin	Name	Function

52	TXD1	UART1-Transmit Data	51	RXD1	UART-Receive Data
50	TXD2	UART2-Transmit Data	54	RXD2	UART2-Receive Data
53	TXD3	UART3-Transmit Data	49	RXD3	UART3-Receive Data
47*	CTS	UART1-Clear To Send	48*	RTS	UART1-Request To Send

Notice: **CTS&RTS the power domian of these 2 pins are VDD_EMI. Don't connect these 2 pins to 2.8V UART interface for the purpose of HardWare flow control.If you need 2.8V Hardware flow control , please use the pin mux of KROW3 and KCOL3 or UTXD2 and URXD2.**

The reference design of standard serial port level witching circuit is as follow figure:

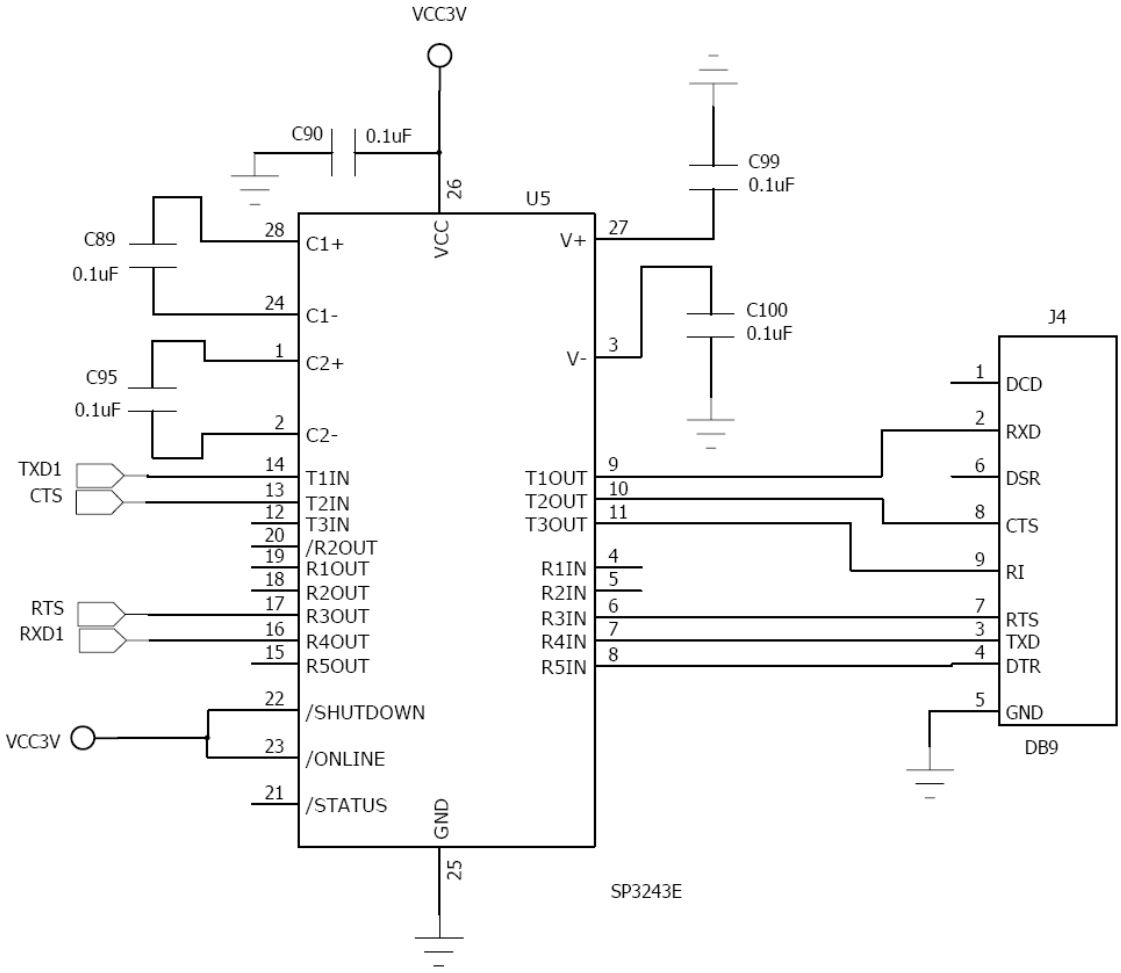


Figure2 The reference diagram of standard serial port level switching circuit

3.7. Audio interfaces

The module provides two audio channels:
EAR and MIC, used for microphone and receiver;
AUXI and AU_MOUT, used for line in and line out;
The audio should be far away from the radio part to reduce TD noise from radio.
The audio pins definitions are as follow table:

Table5: Audio interface of the MD251

Pin	Name	Function	Pin	Name	Function
4	MICP0	Microphone	5	MICN0	Microphone

		amplifier positive input(+) output			amplifier negative input(-) output
6	AU_OUT0_P	Earphone positive output(+)	7	AU_OUT0_N	Earphone negative output(-)
8	MP3_OUTR	Audio analog output right channel	9	MP3_OUTL	Audio analog output left channel
10	MICP1	Audio 1 chanel			
11	SPK_N	Audio amplifier negative output	12	SPK_P	Audio amplifier positive output

It is suggested that you adopt following matching circuit in order to satisfy speaker effect. The difference audio signals have to be layout according to difference signal layout rules. If you want to adopt an amplifier circuit for audio, we commend National company's LM4890. But you can select it according to your needs.

The audio reference design as follow chart：

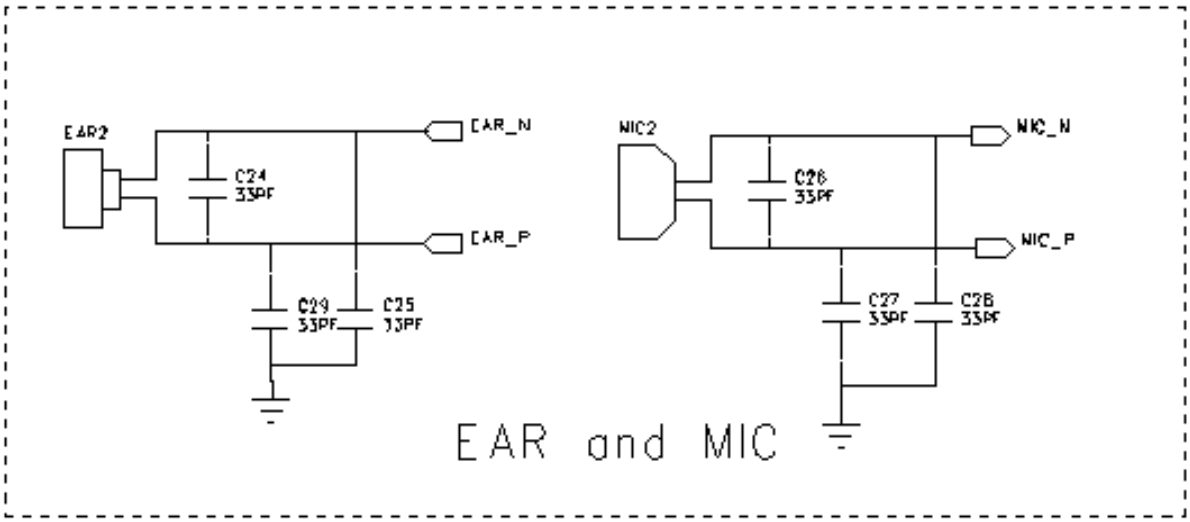


Figure3 The reference design of audio

The microphone bias electric circuit was designed in MD251. The MIC_BIAS DC characteristics see the table 6.

Table 6：MIC_BIAS DC Characteristics

Parameter	Minimum	Typical	Maximum	Units
Microphone Bias Voltage (MIC_BIAS)		1.9		V
Source Current			2	mA

All voice band data paths comply with the GSM 03.50 specification. Mono hands-free audio are also provided. The audio stereo path facilitates CD-quality playback and voice playback through a headset.

MD251 has a built-in high fidelity calss AB audio power amplifier. It is capable of delivering 1 watt of power to an 8 ohm BTL load with less than 10% distortion.

3.8. DAI PCM Interface

The Digital Audio Interface (**DAI**) block communicates with the System Simulator for FTA or external Bluetooth modules. To communicate with the external Bluetooth module,

the master-mode PCM interface and master-mode I2S/EIAJ interface are supported. The clock of PCM interface is 256 kHz, and the frame sync is 8 kHz. Both long sync and short sync interfaces are supported. The PCM interface can transmit 16-bit stereo or 32-bit mono 8 kHz sampling rate voice signal. Table 6 show the pin map of DAI PCM.
I2S/EIAJ interface is designed to transmit high quality audio data. I2S/EIAJ can support 32 kHz, 44.1kHz, and 48kHz sampling rate audio signals. The clock frequency of I2S/EIAJ can be 32×(sampling frequency), or 64×(sampling frequency). For example, to transmit a 44.1 kHz CD-quality music, the clock frequency should be 32 × 44.1 kHz = 1.4112 MHz or 64×44.1 kHz = 2.8224 MHz.

Table 7：Pin mapping of DAI, PCM interfaces

Pin	Name	Function	Pin	Name	Function
21	DAIRST	DAI reset signal input	22	DAISYNC	General purpose Input/Output pin 24
36	DAIPCMIN	DAI PCM data input	37	DAIPCMOUT	DAI PCM data output
38	DAICLK	DAI PCM clock output			

3.9. PWM and Alerter (needs software support)

The output of the PWM signal should supported by software. We can do custom software for users to support PWM signal.

Table8: Alerter and PWM interface of the MD251

Pin	Name	Function
19	PWM	Pulse-width modulated signal

3.10. Antenna

The RF interface has an impedance of 50Ω. The antenna cable can be soldered to the pad.
Pay attention, the line between the MD251 antenna pin and antenna connection should be thick and short. It is better to use filter circuit to fit 50 ohms.

Table9: RF output power：

Frequency	Max	Min
GSM850	33dBm±2dB	5dBm±5dB
E-GSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
PCS1900	30dBm±2dB	0dBm±5dB

Table10: Module RF receive sensitivity：

Frequency	Receive sensitivity
GSM850	<-106dBm
E-GSM900	<-106dBm
DCS1800	<-104dBm

PCS1900	<-104dBm

Table11: MD251 receive/transmit frequency

Frequency	Receive	Transmit
GSM850	869~894MHz	824-849MHz
E-GSM900	925~960MHz	800-915MHz
DCS1800	1710~1785 MHz	1805~1800 MHz
PCS1900	1850~1910 MHz	1930~1990 MHz

According to the application, should use GSM900/DCS1800 Dual-band antenna or GSM850/PCS1900 Dual-band antenna.

3.11. SIM card interface

The MD251 contains a dedicated smart card interface to allow the MCU access to the SIM card. The SIM interface supports the functionality of the GSM Phase 1 specification and also supports the functionality of the new GSM Phase 2+ specification for FAST 64 kbps SIM (intended for use with a SIM application Tool-kit).
The SIM card interface circuitry of PMU meets all ETSI and IMT-2000 SIM interface requirements. It provides level shifting needs for low voltage GSM controller to communicate with either 1.8V or 3V SIM cards. All SIM cards contain a clock input, a reset input, and a bi-directional data input/output. The clock and reset inputs to SIM cards are level shifted from the supply of digital IO (Vio) of baseband chipset to the SIM supply (Vsim). The bi-directional data bus is internal pull high with 10kohm resistor.
All pins that connect to the SIM card (Vsim, SRST, SCLK, SIO) withstand over 5kV of human body mode ESD. In order to ensure proper ESD protection, careful board layout is required.
The interface of SIM is as follow table：

Tbale12: The SIM pins on the Module

Num	Name	Function
15	SIM_IO	SIM card data output and input
16	SIM_CLK	SIM card clock output
17	SIM_RST	SIM card RESET output
18	VRSIM	Power supply for SIM card

Table 13: SIM Interface Electrical Specifications

SIM Voltage					
Output voltage (V_SIM)	Register VSIM_SEL=L	1.71	1.8	1.89	V
	Register VSIM_SEL=H	2.82	3.0	3.18	V
Output current (Isim_max)			20		mA
Line regulation				4	mV
Load regulation				15	mV

Parameter	Conditions	Min.	Typical	Max.	Unit
Interface to 3 V SIM Card					
Volrst	I = 20 μA			0.4	V
Vohrst	I = -200 μA	0.9*VSIM			V
Volclk	I = 20 μA			0.4	V
Vohclk	I = -200 μA	0.9*VSIM			V
Vil				0.4	V
Vihsio , Vohsio	I = ±20 μA	VSIM-0.4			V
Iil	Vil = 0 V			-1	mA
Vol	Iol = 1 mA, SIMIO ≤ 0.23 V			0.4	V
Interface to 1.8 V SIM Card					
Volrst	I = 20 μA			0.2*VSIM	V
Vohrst	I = -200 μA	0.9*VSIM			V
Volclk	I = 20 μA			0.2*VSIM	V
Vohclk	I = -200 μA	0.9*VSIM			V
Vil				0.4	V
Vihsio , Vohsio	I = ±20 μA	VSIM-0.4			V
Iil	Vil = 0 V			-1	mA
Vol	Iol = 1 mA, SIMIO ≤ 0.23 V			0.4	V
SIM Card Interface Timing					
SIO pull-up resistance to VSIM		8	10	12	kΩ
SRST, SIO rise/fall times	VSIM = 3, 1.8 V, load with 30 pF			1	μs
SCLK rise/fall times	VSIM = 3 V, CLK load with 30 pF			18	ns
	VSIM = 1.8 V, CLK load with 30 pF			50	ns
SCLK frequency	CLK load with 30 pF	5			MHz

SCLK duty cycle	SIMCLK Duty = 50%, fsimclk = 5 MHz	47		53	%
SCLK propagation delay			30	50	ns

Following is a reference circuit about SIM interface. We recommend a Electrostatic discharge device ST (www.st.com) ESDA6V1W5 or ONSEMI (www.onsemi.com) SMF05C for "ESD ANTI".

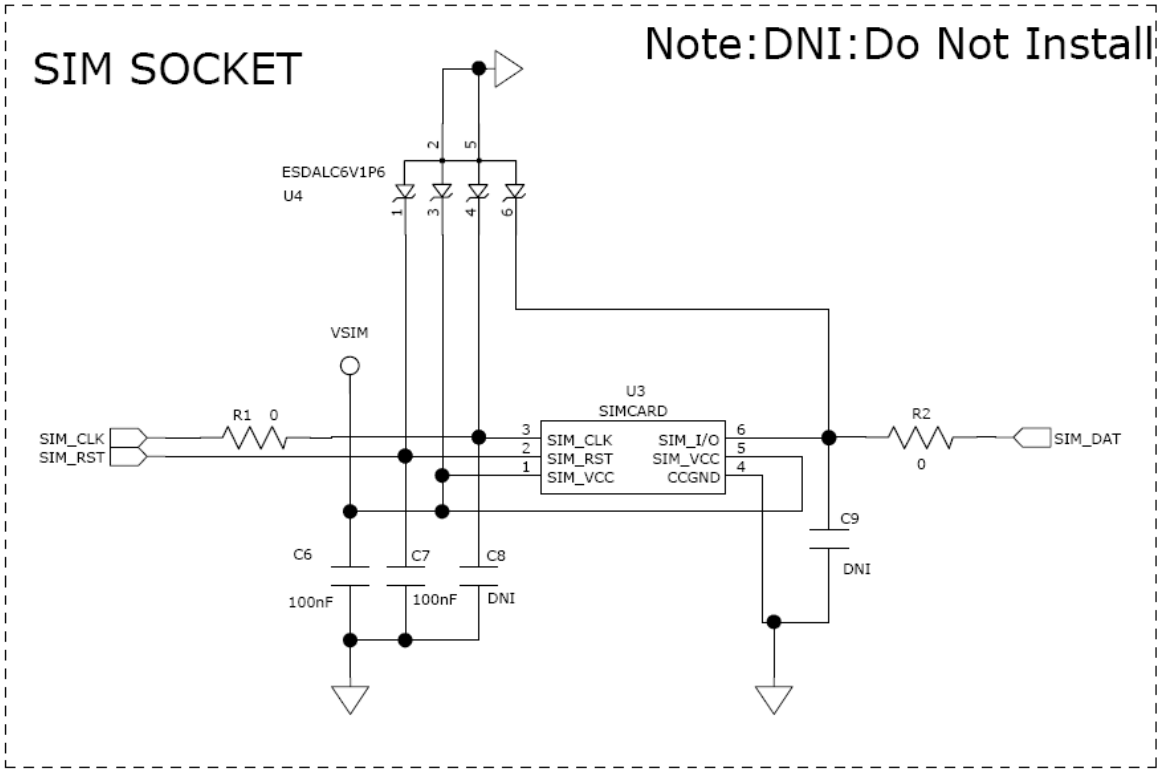


Figure4 The reference design of SIM Socket

3.12. Keypad Interface

The keypad can be divided into two parts: one is the keypad interface including 5 columns and 5 rows with one dedicated power-key, as shown in **Fig. 5.** the other is the key detection block which provides key pressed, key released and de-bounce mechanisms. Each time the key is pressed or released, i.e. something different in the 5 x 5 matrix or power-key, the key detection block senses the change and recognizes if a key has been pressed or released. This keypad can detect one or two key-pressed simultaneously with any combination. Since the key press detection depends on the HIGH or LOW level of the external keypad interface, if keys are pressed at the same time and there exists a key that is on the same column and the same row with the other keys, the pressed key cannot be correctly decoded. For example, if there are three key presses: key1 = (x1, y1), key2 = (x2, y2), and key3 = (x1, y2), then both key3 and key4 = (x2, y1) are detected, and therefore they cannot be distinguished correctly. Hence, the keypad can detect only one or two keys pressed simultaneously at any combination. More than two keys pressed simultaneously in a specific pattern retrieve the wrong information.

There should not be an external pull down resistor on KCOL0 and please use the KCOL1-4 prior if could meet demand. Because KCOL0 connect to GND is used to enter USBDL mode.

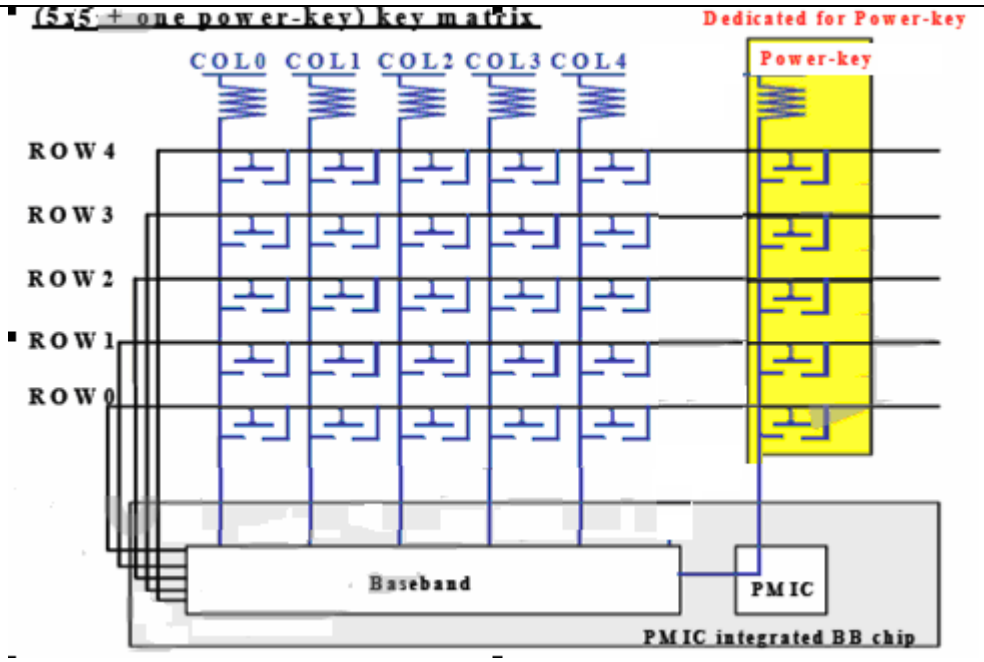


Figure5 The Typical Keypad Interface Circuit

3.13. LCD Interface

MD251 contains a versatile LCD controller which is optimized for multimedia applications. This controller supports many types of LCD modules and contains a rich feature set to enhance the functionality. These features are:

- Up to 320 x 240 resolution
- The internal frame buffer supports 8bpp indexed color, RGB565,RGB888,ARGB8888,PARGB8888 and YUYV422 format
- Supports 8-bpp (RGB332), 12-bpp (RGB444), 16-bpp (RGB565), 18-bit (RGB666) and 24-bit (RGB808) color depths
- 4 Layers Overlay with individual vertical and horizontal size, vertical and horizontal offset, source key, opacity and display rotation control(90°,180°, 270°, mirror and mirror then 90°, 180° and 270°)

For parallel LCD modules, this special LCD controller can reuse external memory interface or use dedicated 8-bit parallel interface to access them and 8080 type interface is supported. It can transfer the display data from the internal SRAM or external SRAM/Flash Memory to the off-chip LCD modules.

For serial LCD modules, this interface performs parallel to serial conversion and supports 8,9,16,18,24 and 32 bit interface. The serial interface may use four pins – LSCE#, LSDA, LSCK and LSA0 or three pins –LSCE#, LSDA, LSCK to enter commands and data. In 3 wire mode, an extra bit representing the LSA0 pin is transferred before the MSB of each transaction.

Figure 6 shows the timing diagram of this serial interface. When the block is idle, LSCK is forced LOW and LSCE# is forced HIGH. Once the data register contains data and the interface is enabled, LSCE# is pulled LOW and remain LOW for the duration of the transmission.

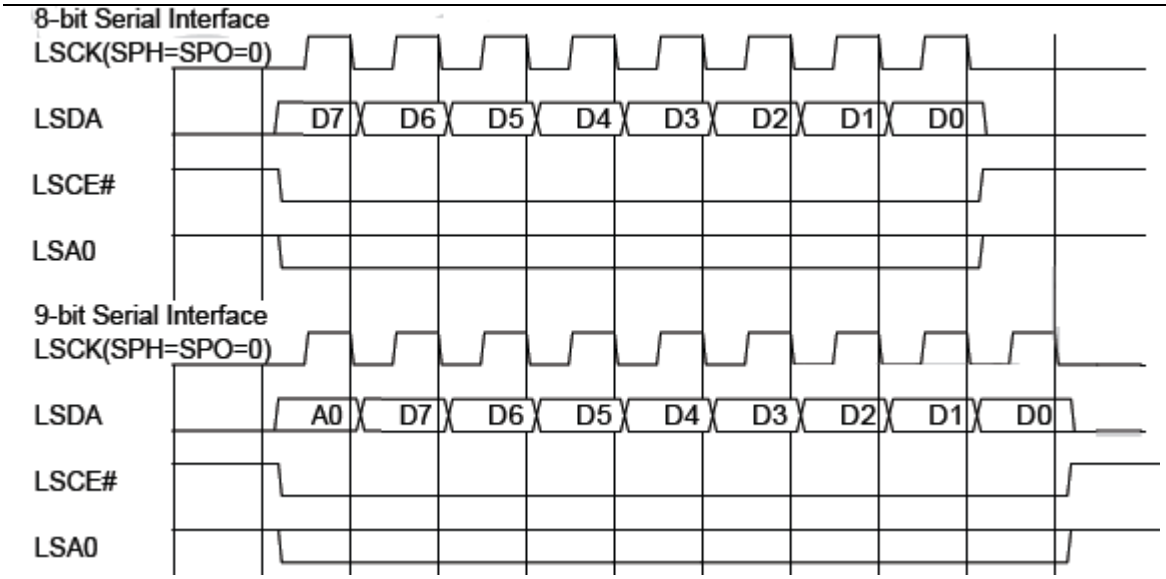


Figure 6 LCD Interface Transfer Timing Diagram

Tbale14: The LCD pins on the Module

Num	Name	Function
43	LRD_B	Parallel display interface Read Signal
44	LWR_B	Parallel display interface Write Signal
45	LPA0	Parallel display interface address output
56	LPCE0B	Parallel display interface chip select 0 output Serial display interface LSCE0
57	LCD_D0	Parallel display interface Data0 Serial display interface LSCK
58	LCD_D1	Parallel display interface Data1 Serial display interface LSA0
59	LCD_D2	Parallel display interface Data2 Serial display interface LSDA
60	LCD_D3	Parallel display interface Data3 Serial display interface LSDI
61	LCD_D4	Parallel display interface Data4
62	LCD_D5	Parallel display interface Data5
63	LCD_D6	Parallel display interface Data6
64	LCD_D7	Parallel display interface Data7
70	LRSTB	Parallel display interface Reset Signal
71	LPTE	Parallel display interface

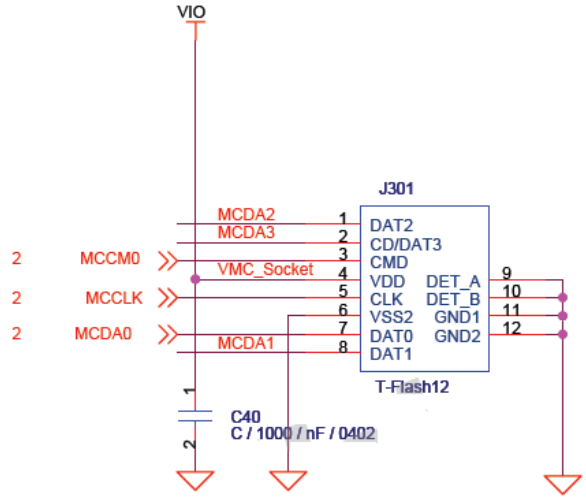
3.14.SD/MMC Memory Card

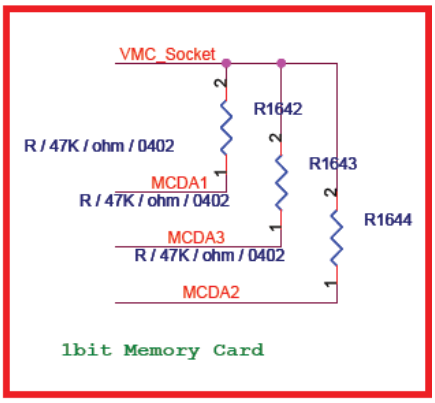
The MD251 fully supports the SD memory Card bus protocol as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 2.0 as well as the MultiMediaCard (MMC) bus protocol as defined in MMC system specification version 4.1. Since SD Memory Card bus protocol is backward compatible to MMC bus protocol, the MD251 is capable of working well as the host on MMC bus under control of proper firmware. Hereafter, the MD251 is also abbreviated as SD/MMC controller.

Num	Name	Function
40	MCCLK	SD Serial Clock/Memory Stick Serial Clock
41	MCDA0	SD Serial Data IO 0/Memory Stick Serial Data

		IO
42	MCCM0	SD Command Output/Memory Stick Bus State Output
46	MCINS	SD Card Detect Input

TF Card





3.15. RTC backup

The Real Time Clock (RTC) module provides time and data information. The clock is based on a 32.768KHz oscillator with an independent power supply. When the module is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor is used through the pin68 of VBACKUP. Figure 7 give the example diagram of the two ways. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core via the BBWAKEUP pin. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g., 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

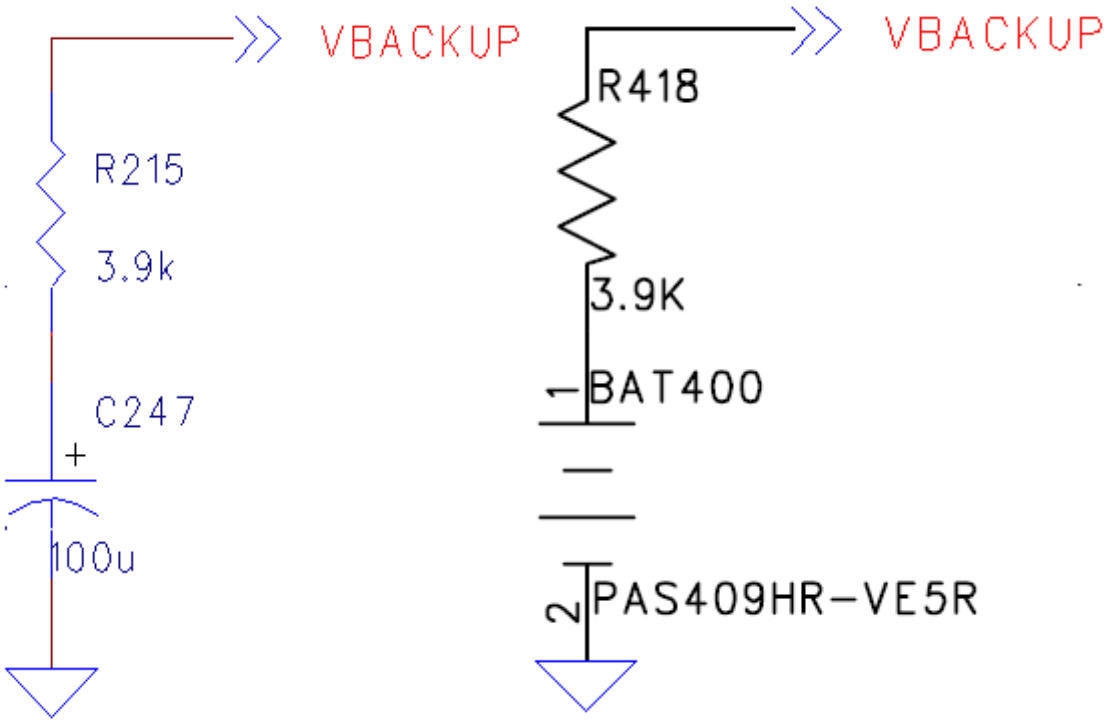


Figure7 The RTC battery diagram for the module

3.16. IOs

MD251 module has several IO pins which are configurable according to customer's requirement. We can do custom software for users.
Upon hardware reset (SYSRST#), IOs are all configured as inputs.

3.17. External Interrupt

MD251 module has several IO pins which are configurable according to customer's requirement. We can do custom software for users.
The four external interrupts can be used for different kind of applications, mainly for event detections: detection of hand free connection, detection of hood opening, detection of battery charger connection.
Since the external event may be unstable in a certain period, a de-bounce mechanism is introduced to ensure the functionality. The circuitry is mainly used to verify that the input signal remains stable for a programmable number of periods of the clock. When this condition is satisfied, for the appearance or the disappearance of the input, the output of the de-bounce logic changes to the desired state. Note that, because it uses the 32 KHz slow clock for performing the de-bounce process, the parameter of de-bounce period and de-bounce enable takes effect no sooner than one 32 KHz clock cycle (~31.25us) after the software program sets them. However, the polarities of EINTs are clocked with the system clock. Any changes to them take effect immediately.
The ENT pins can be configurable to "EDGE/LEVEL" according to the external signal.

3.18.ADC

MD251 provides one auxiliary ADC (General purpose analog to digital converter.) as voltage input pin, which can be used to detect the values of some external items such as voltage 、 temperature etc. For module application, user can use AT command "AT+CADC#" to read the voltage value added on ADC pin.
The functional specifications of the auxiliary ADC are listed in the following table.

Table 19 The Functional specification of Auxiliary ADC

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution		10		Bit
FC	Clock Rate	0.1	1.0833	5	MHz
FS	Sampling Rate @ N-Bit			5/(N+1)	MSPS
	Input Swing	1.0		AVDD	V
T	Operating Temperature	-40		85	℃
	Current Consumption Power-up Power-Down		300 1		μA μA

3.19. Digital Pin Electrical Characteristics

About the digital pin electrical characteristics of MD251, please reference the table 20.

Table 20: Module digital electrical characteristics

PWM		VDD(2.7V-2.9V)
DAIRST	PD	VDD
DAISYNC	PD	VDD
BT_EINT1	PU	VDDK(1.08V-1.32V)
KCO0	PU	VDD
KCO1	PU	VDD
KCO2	PU	VDD
KCO3	PU	VDD
KCO4	PU	VDD
KROW0	PD	VDD
KROW1	PD	VDD
KROW2	PD	VDD
KROW3	PD	VDD
KROW4	PD	VDD
SRCLKENAI	PD	VDD
BT_32K	PD	VDD
DAIPCMIN	PD	VDD
DAIPCMOUT	PD	VDD

DAICLK	PD	VDD
EINT0_Headset	PU	VDDK
MCCLK	PD	VDDMSDC(2.7V-3.6V)
MCCDA0	PD	VDDMSDC
MCCM0	PD	VDDMSDC
LRD_B		DVDD(1.7V-1.95V)
LWR_B		DVDD
LPA0		DVDD
MCINS	PU	DVDD
UCTS1	PU	DVDD
URTS1	PU	DVDD
URXD3		VDD
UTXD2		VDD
URXD1		VDD
UTXD1		VDD
UTXD3		VDD
URXD2		VDD
GPIO70	PD	VDD
LPCE0B		DVDD
NLD0		DVDD
NLD1		DVDD
NLD2		DVDD
NLD3		DVDD
NLD4		DVDD
NLD5		DVDD
NLD6		DVDD
NLD7		DVDD
LRSTB	PD	DVDD
LPTE	PD	DVDD

About the digital IO LDO (VIO) is a regulator that could source 100mA (max) with 2.8V output voltage. It supplies the baseband circuitry of the Module. The LDO is optimized for very low quiescent current and will power up at the same time as the digital core LDO. Table21 show the electrical characteristics of VIO.

Table 21 VIO electrical characteristics

VBAT = 3.4 V ~ 4.6 V, minimum loads applied on all outputs, unless other noted. Typical values are at TA = 25 °C.

Parameter	Conditions	Min.	Typical	Max.	Unit
Digital IO Voltage					
Output voltage (V_IO)		2.7	2.8	2.9	V
Output current (Iio_max)			60		mA
Line regulation				5	mV
Load regulation				30	mV

3.20. Module sleep mode control

Our Module support two ways to control module enter sleep mode or not:

1) Hardware control method: **DSR(Pin34)** is used for hardware sleep mode control.
   LOW Level: disable module enter sleep mode;
   HIGH Level: enable module enter sleep mode.
2) Software control method: AT command "AT+ESLP"
   "AT+ESLP=0": disable module enter sleep mode;
   "AT+ESLP=1": enable module enter sleep mode.

NOTE1: Module default software value is disable enter sleep mode.
NOTE2: If module enter sleep mode, the AT command can not be sent to module normally.

3.21.Behaviors of the RING indication line

MD251: Pin55 (GPIO70) is used for Ring indication when network event. The working state of this pin is listed in following table:

Table 23: The Behaviors of the RING line

State	RI respond
Standby	High
Voice calling	Change low, then: 1) Change to high when establish calling. 2) Sender hang up, change to high.
SMS	When receive SMS, The ring will change to LOW and hold LOW level at least 200 ms, then change to HIGH.

3.22.Network status indication LED lamp

MD251:Pin19(GPIO0) is used to drive a network status indication LED lamp. The working state of this pin is listed in following table:

Table 23: Working state of network status indication LED pin

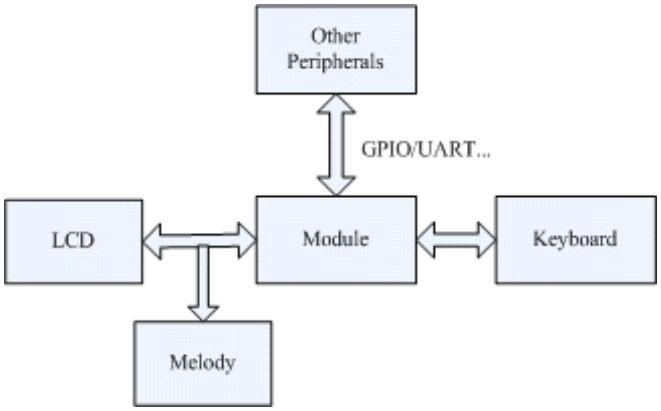
State	Module function
Off	Module is not running
64ms On/800ms Off	Module does not find the network
64ms On/3000ms Off	Module find the network
64ms On/300ms Off	GPRS communication

4. Software application

The module can be used in master mode and slave mode.

4.1. Master mode (such as application for fixed wireless phone)

In master mode, the module acted as main board of mobile terminal. The LCD or melody processor can be connected to the module via data and address bus. Users can control the module via keyboard and the MMI software can be customized according to requirement.



Please get schematic information from chap 6.2.

4.2. Slave mode (standard GSM/GPRS module application)

In slave mode, the module communicated with master MCU via UART interface using AT commands.
Please get schematic information from chap 6.1.

4.2.1. AT command

Please get detail information from refer[10]

4.2.2. The hyper terminal configure method

User can control the MD251 module using hyper terminal to send AT Command. The configuration in hyper terminal:
Bits per second： 115200 (depends on SW)
Data bits: 8

Parity: None
Stop bits: 1
Flow control: None

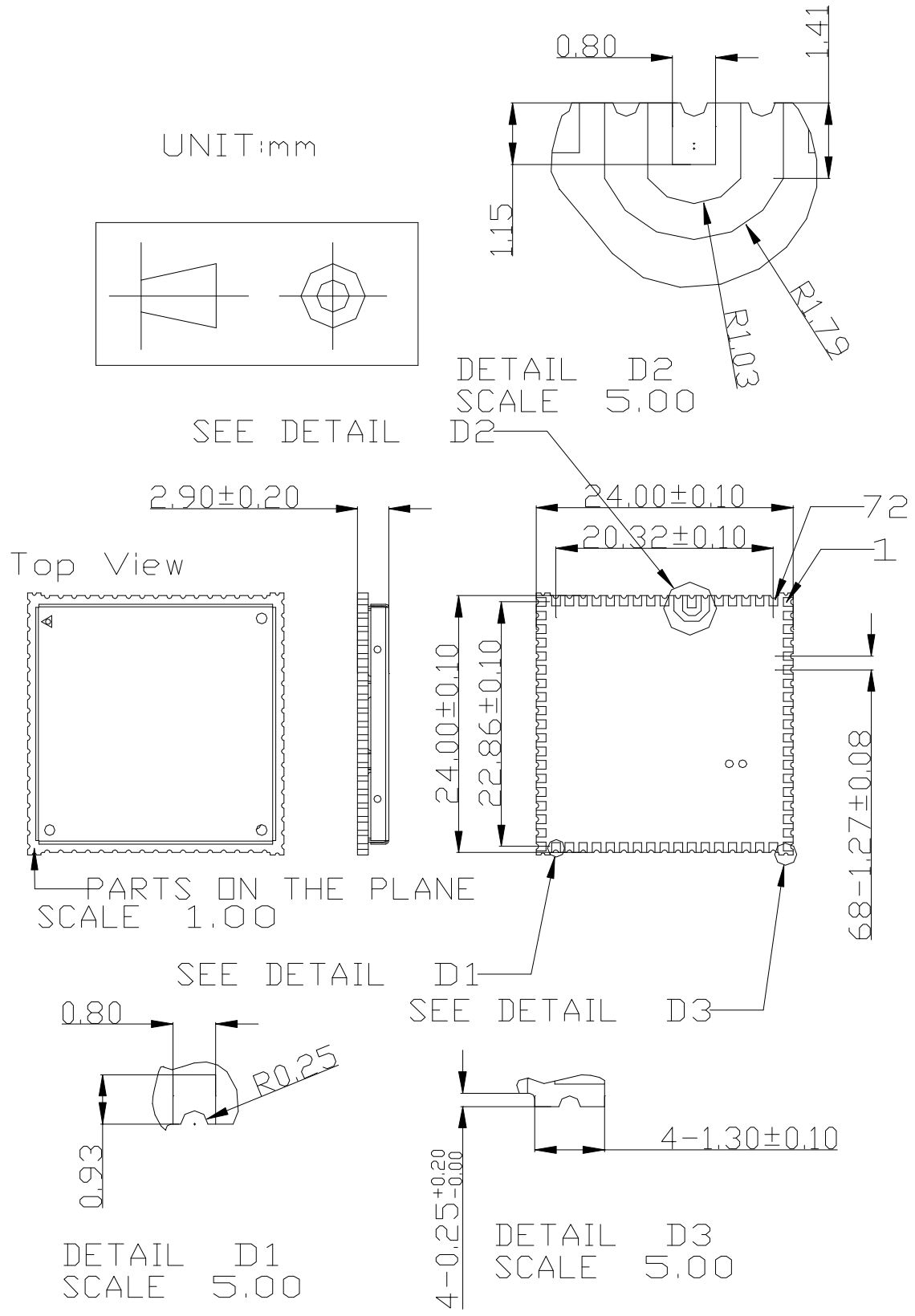
4.2.3. TCP/IP protocol

The module can support TCP/IP protocol. Please get detail information from reference [11].

FCC Warning

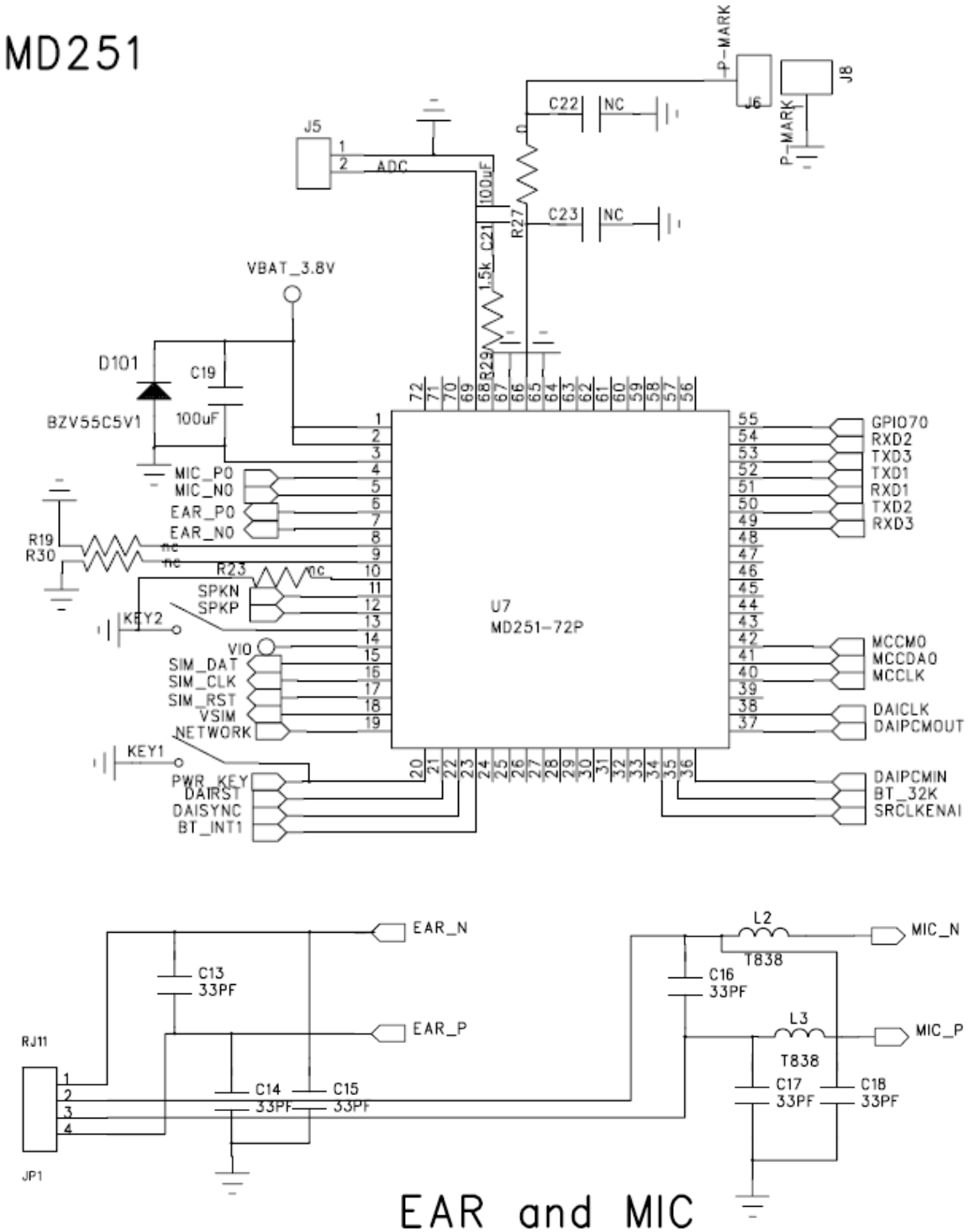
Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

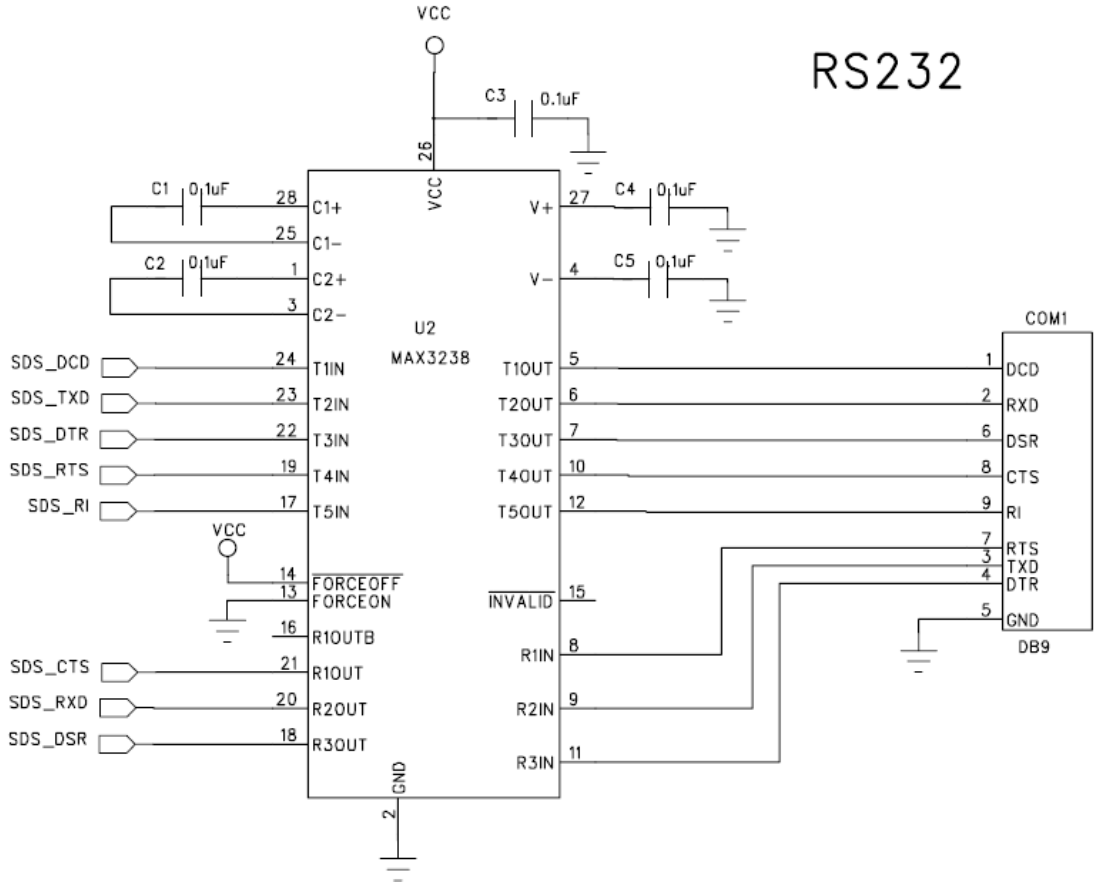
5. Mechanics

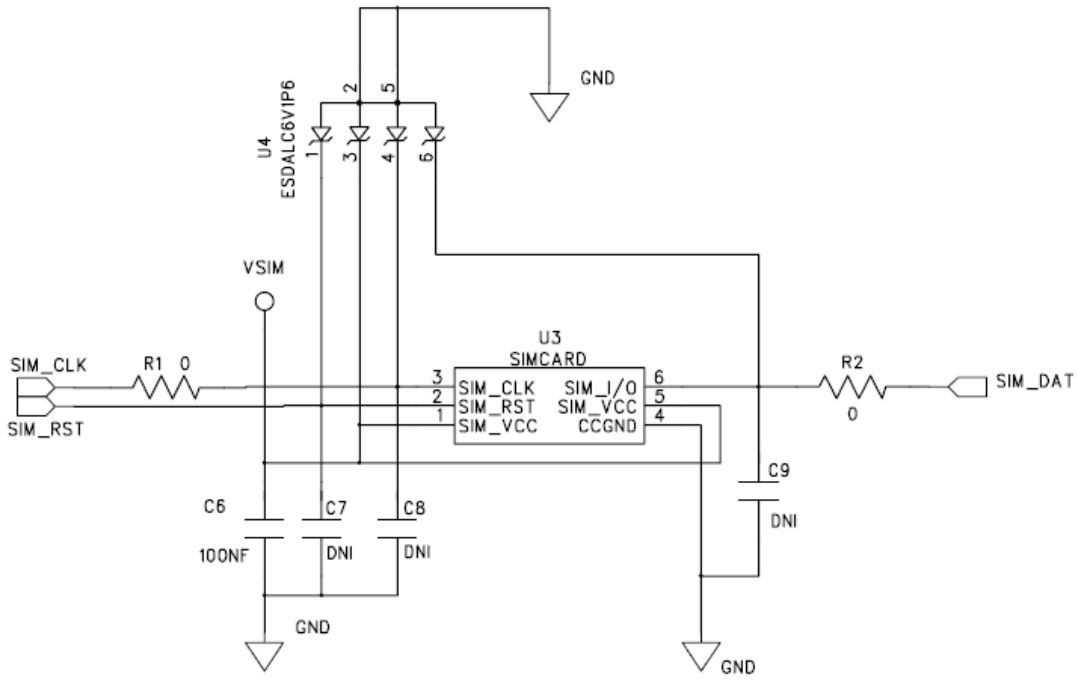

UNIT:mm
0.80
1.41
1.15
R1.03
R1.79
DETAIL D2
SCALE 5.00
SEE DETAIL D2
2.90±0.20
24.00±0.10
20.32±0.10
72
1
Top View
24.00±0.10
22.86±0.10
68-1.27±0.08
PARTS ON THE PLANE
SCALE 1.00
SEE DETAIL D1
SEE DETAIL D3
0.80
R0.25
0.93
DETAIL D1
SCALE 5.00
4-1.30±0.10
4-0.25 +0.20 -0.00
DETAIL D3
SCALE 5.00

6. Interface board Reference EVB

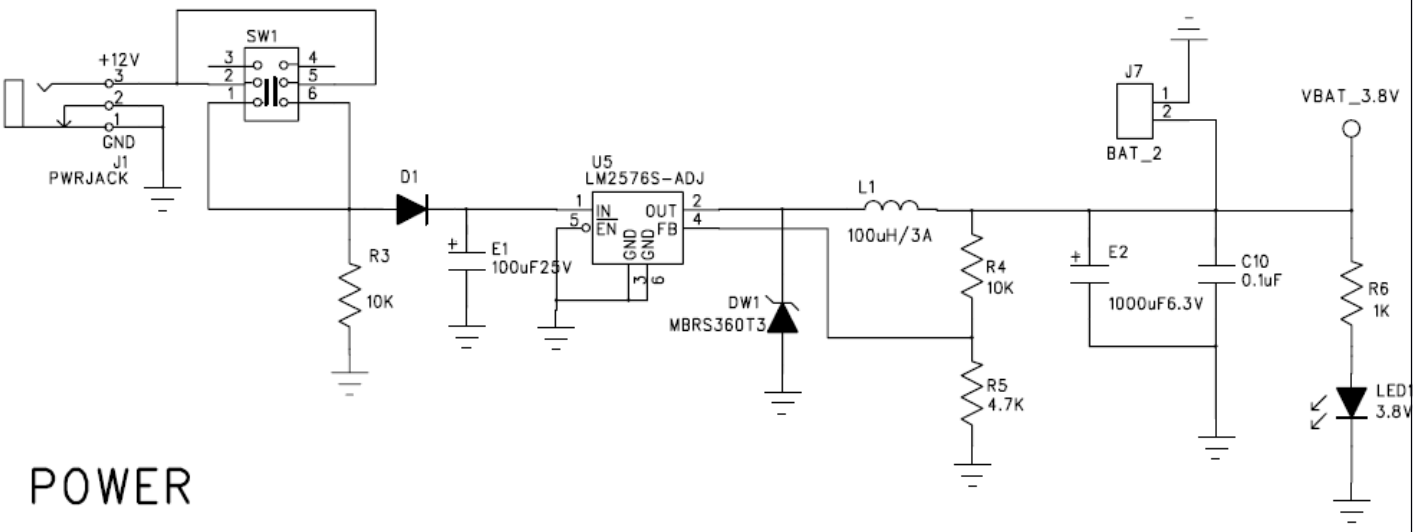
6.1 Standard GSM/GPRS module



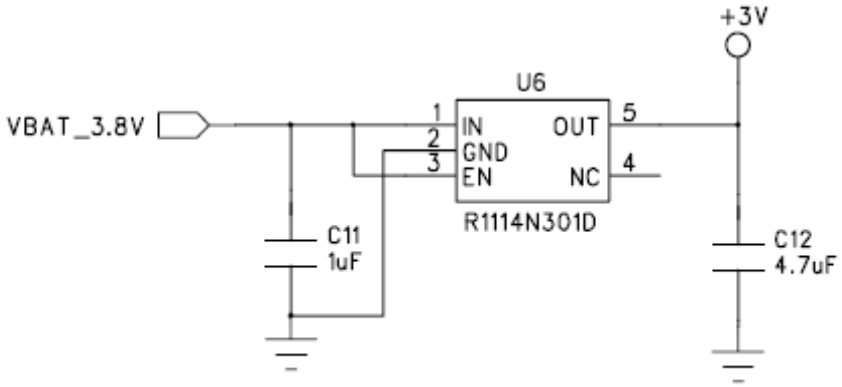

RS232
VCC
C3 0.1uF
26
VCC
C1 0.1uF
28 C1+
25 C1-
C2 0.1uF
1 C2+
3 C2-
U2
MAX3238
V+ 27
C4 0.1uF
V- 4
C5 0.1uF
SDS_DCD 24 T1IN
SDS_TXD 23 T2IN
SDS_DTR 22 T3IN
SDS_RTS 19 T4IN
SDS_RI 17 T5IN
T1OUT 5
T2OUT 6
T3OUT 7
T4OUT 10
T5OUT 12
COM1
1 DCD
2 RXD
6 DSR
8 CTS
9 RI
7 RTS
3 TXD
4 DTR
5 GND
DB9
VCC
14 FORCEOFF
13 FORCEON
INVALID 15
16 R1OUTB
SDS_CTS 21 R1OUT
SDS_RXD 20 R2OUT
SDS_DSR 18 R3OUT
R1IN 8
R2IN 9
R3IN 11
GND
2


GND
U4
ESDALC6VIP6
2
5
1
3
4
6
VSIM
U3
SIMCARD
SIM_CLK R1 0
SIM_RST
3 SIM_CLK
2 SIM_RST
1 SIM_VCC
SIM_I/O 6
SIM_VCC 5
CCGND 4
R2
0
SIM_DAT
C9
DNI
C6
C7
C8
100NF
DNI
DNI
GND
GND

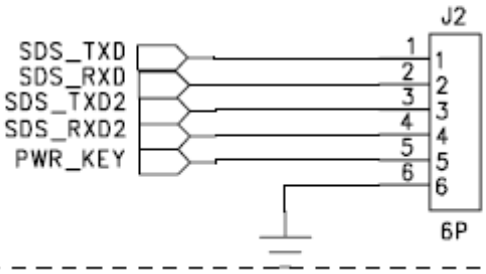
SIM SOCKET

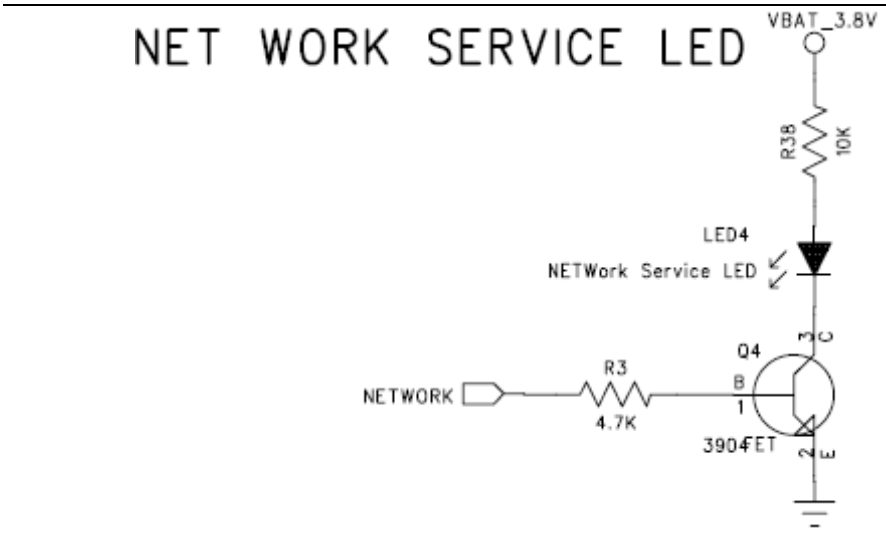


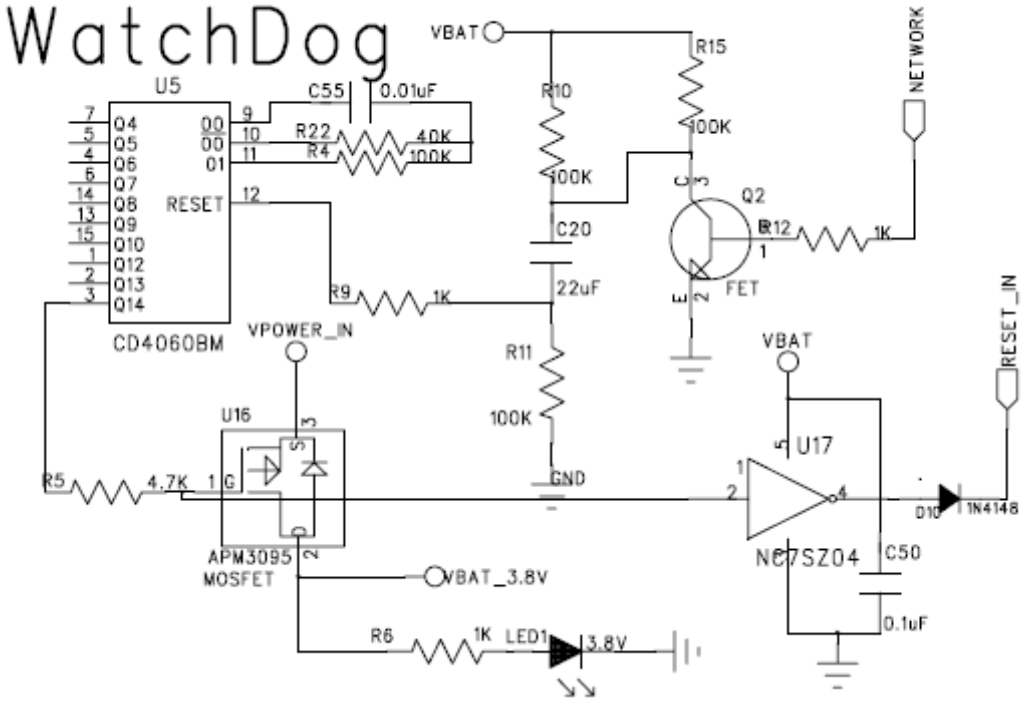
POWER



Download




NET WORK SERVICE LED
VBAT_3.8V
R38
10K
LED4
NETWork Service LED
Q4
C
B
E
R3
4.7K
NETWORK
3904FET


WatchDog
VBAT
U5
C55
0.01uF
R22
40K
R4
100K
R10
100K
R15
100K
NETWORK
Q2
R12
1K
C20
22uF
FET
RESET
CD4060BM
R9
1K
VPOWER_IN
R11
100K
VBAT
RESET_IN
U16
U17
R5
4.7K
GND
D10
1N4148
APM3095
MOSFET
NC7SZ04
C50
0.1uF
VBAT_3.8V
R6
1K
LED1
3.8V