RDA6252 DATA SHEET

Version 1.0

2009-9-27

RDA6252
Power Amplifier Module for
Quad-Band GSM Wireless Communication

RDA6252 Power Amplifier Module

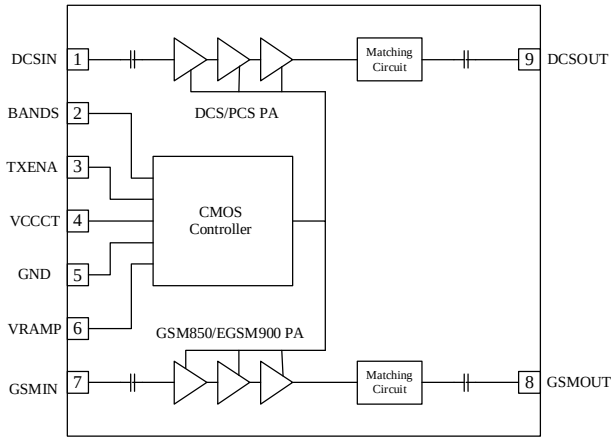
(Quad-Band GSM850/EGSM900/DCS/PCS PA Module)

The RDA6252 is a high-power, high-efficiency quad-band power amplifier Module. This device is designed for GSM850, EGSM900, DCS, and PCS handheld digital cellular equipment. The power amplifiers and their controller are fabricated with GaAs Heterojunction Bipolar Transistor (HBT) and CMOS respectively. The package of this device is 6mm×6mm×1.1mm 9-pins LGA. The input and output are realized on-chip matched to 50Ω. The RDA6252 requires few external components, simplifying PCB layout and reducing PCB board space.

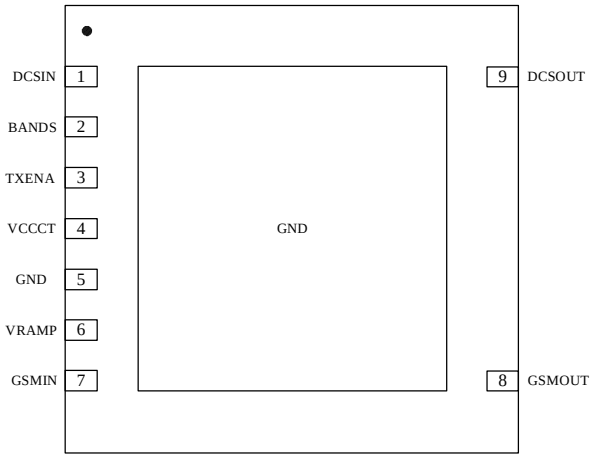
Features

- Ultra-Small 6mm×6mm×1.1mm Package
- Quad-Band Power Amplifier
- Complete Power Control Solution
- High efficiency
- Low supply voltage (3~4.5V)
- Input/Output matched @ 50 Ω
- Advanced HBT/CMOS process

Function Block Diagram



Pin Assignment



Pin Name definition

Pin Number	Pin Name	Description
1	DCSIN	DCS/PCS RF input port
2	BANDS	GSM850/EGSM900 and DCS/PCS selection port
3	TXENA	TX enable port
4	VCCCT	Power supply
5	GND	Ground
6	VRAMP	Ramping control port
7	GSMIN	GSM850/EGSM900 RF input port
8	GSMOUT	GSM850/EGSM900 RF output port
9	DCSOUT	DCS/PCS RF output port

Preliminary Electrical Target Specifications

The following tables list the electrical characteristics of the RDA6252 module. Table 1 lists the absolute maximum ratings. Table 2 shows the recommend operating conditions for this device. Table 3 shows the power truth table. Table 4 shows the electrical specifications for GSM850 mode nominal operating condition. Table 5 shows the electrical specifications for EGSM900 mode nominal operating condition. Table 6 shows the electrical specifications for DCS mode nominal operating condition. Table 7 shows the electrical specifications for PCS mode nominal operating condition.

Table 1. Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	-0.3 to 5	V
Power Control Voltage (Vramp)	-0.3 to 3	V
Input RF Power	+10	dBm
Max Duty Cycle	50	%
Operating Case Temperature	-30 to +110	℃
Storage Temperature	-30 to +150	℃

Table 2. Recommended Operating Conditions

Parameter	Minimum	Nominal	Maximum	Unit
Supply Voltage	3	3.5	4.5	V
Power Control Voltage (V_{VRAMP})	0.23		1.7	V
TX Enable “ON”	1.5			V
TX Enable “OFF”			0.5	V
GSM Band Enable			0.5	V
DCS/PCS Band Enable	1.5			V
Input RF Power	0		5	dBm
Operating Temperature	-20	+25	+80	℃
Leakage current		15	50	uA

Table 3. Power Range Truth Table

	TXENA	BANDS
Power Down	0	-
GSM On	1	0
DCS/PCS On	1	1

Note 1:

‘0’ denotes logic low which is typical 0V~0.5V. ‘1’ denotes logic high which is typical 1.5V~3V.

Table 4. Electrical Specifications for GSM850 Mode Application (1)

Parameters	Condition	Min.	Typ.	Max.	Unit
Frequency Range	-	824		849	MHz
Input Power Range	-	0	3	5	dBm
Maximum Output Power	V_{VRAMP}=1.7V	34	34.5		dBm
Total Efficiency	V_{VRAMP}=1.7V; Pout=34.5dBm	45	55		%
Output Noise Power	RBW=100kHz; 20MHz offset; Pout<34.5dBm		-83	-80	dBm
Harmonics	Pout<34.5dBm			-15	dBm
Forward Isolation 1	TXENA='0'; Pin=6dBm		-45	-30	dBm
Forward Isolation 2	TXENA='1'; Pin=6dBm; V_{VRAMP}=0.23V		-25	-10	dBm
Cross Band Isolation at $2f_0$	V_{VRAMP}=0.23V to 1.7V		-30	-17	dBm
Total Supply Current	V_{VRAMP}=1.7V; Pout=34.5dBm			1.6	A
Input VSWR		-	2:1	-	-
Stability (Spurious output) (2)	6:1 VSWR	-	-	-70	dBc
Ruggedness (No damage) (2)	10:1 VSWR	-	-	-	-
Power Control Range	V_{VRAMP}=0.23V to 1.7V	50			dB

Notes:
(1). V_{CC}=3.5V, Freq = 835MHz, Tc = 25℃, unless otherwise specified.
(2). All phase, time=10s

Table 5. Electrical Specifications for GSM900 Mode Application (3)

Parameters	Condition	Min.	Typ.	Max.	Unit
Frequency Range	-	880		915	MHz
Input Power Range	-	0	3	5	dBm
Maximum Output Power	V_{VRAMP}=1.7V	34	34.5		dBm
Total Efficiency	V_{VRAMP}=1.7V; Pout=34.5dBm	45	55		%
Output Noise Power	RBW=100kHz; 20MHz offset; Pout<34.5dBm		-83	-80	dBm
Harmonics	Pout<34.5dBm			-15	dBm
Forward Isolation 1	TXENA='0'; Pin=6dBm		-45	-30	dBm
Forward Isolation 2	TXENA='1'; Pin=6dBm; V_{VRAMP}=0.23V		-25	-10	dBm
Cross Band Isolation at $2f_0$	V_{VRAMP}=0.23V to 1.7V		-30	-16	dBm
Total Supply Current	V_{VRAMP}=1.7V; Pout=34.5dBm			1.6	A
Input VSWR		-	2:1	-	-
Stability (Spurious output) (4)	8:1 VSWR	-	-	-70	dBc
Ruggedness (No damage) (4)	10:1 VSWR	-	-	-	-
Power Control Range	V_{VRAMP}=0.23V to 1.7V	50			dB

Notes:
(3). V_{CC}=3.5V, Freq = 900MHz, Tc = 25℃, unless otherwise specified
(4). All phase, time=10s

Table 6. Electrical Specifications for DCS Mode Application (5)

Parameters	Condition	Min.	Typ.	Max.	Unit
Frequency Range	-	1710		1785	MHz
Input Power Range	-	0	3	5	dBm
Maximum Output Power	V_{VRAMP}=1.7V	32	32.5		dBm
Total Efficiency	V_{VRAMP}=1.7V; Pout=32.5dBm	42	50		%
Output Noise Power	RBW=100kHz; 20MHz offset; Pout<32.5dBm		-83	-80	dBm
Harmonics	Pout<32.5dBm			-15	dBm
Forward Isolation 1	TXENA='0'; Pin=6dBm		-45	-30	dBm
Forward Isolation 2	TXENA='1'; Pin=6dBm; V_{VRAMP}=0.23V		-25	-10	dBm
Total Supply Current	V_{VRAMP}=1.7V; Pout=32.5dBm			1.2	A
Input VSWR		-	2:1	-	-
Stability (Spurious output) (6)	8:1 VSWR	-	-	-70	dBc
Ruggedness (No damage) (6)	10:1 VSWR	-	-	-	-
Power Control Range	V_{VRAMP}=0.23V to 1.7V	50			dB

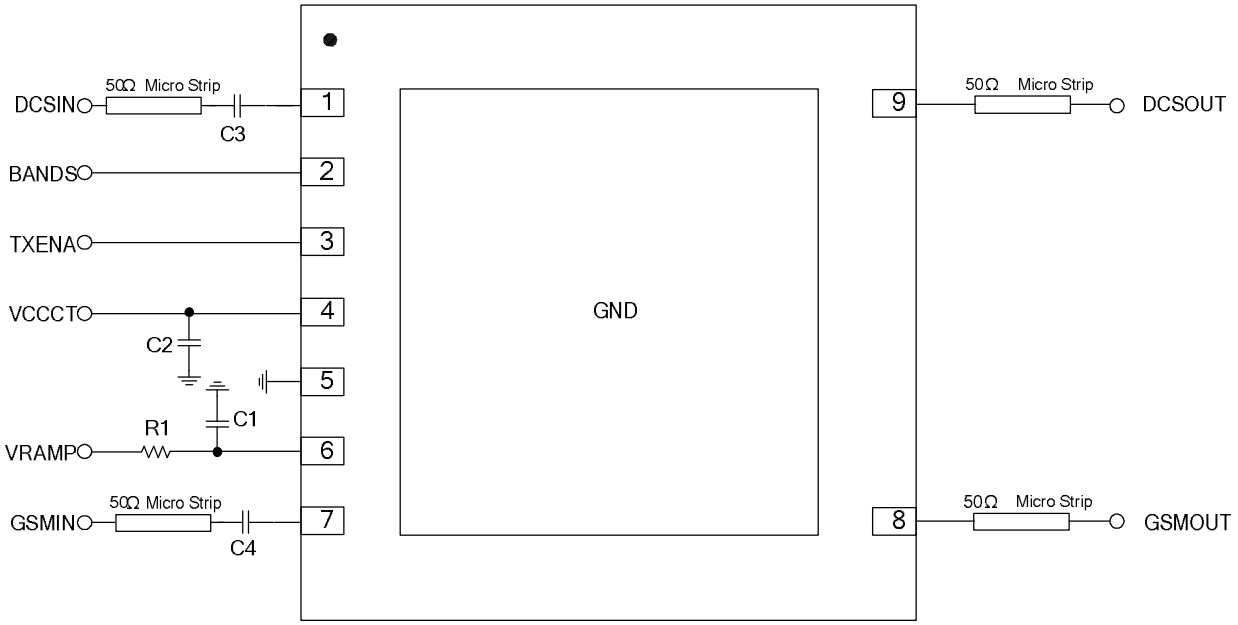
Notes:
(5). V_{CC}=3.5V, Freq = 1750MHz, Tc = 25℃, unless otherwise specified
(6). All phase, time=10s

Table 7. Electrical Specifications for PCS Mode Application (7)

Parameters	Condition	Min.	Typ.	Max.	Unit
Frequency Range	-	1850		1910	MHz
Input Power Range	-	0	3	5	dBm
Maximum Output Power	V_{VRAMP}=1.7V	32	32.5		dBm
Total Efficiency	V_{VRAMP}=1.7V; Pout=32.5dBm	42	50		%
Output Noise Power	RBW=100kHz; 20MHz offset; Pout<32.5dBm		-83	-80	dBm
Harmonics	Pout<32.5dBm			-15	dBm
Forward Isolation 1	TXENA='0'; Pin=6dBm		-45	-30	dBm
Forward Isolation 2	TXENA='1'; Pin=6dBm; V_{VRAMP}=0.23V		-25	-10	dBm
Total Supply Current	V_{VRAMP}=1.7V; Pout=32.5dBm			1.2	A
Input VSWR		-	2:1	-	-
Stability (Spurious output) (8)	8:1 VSWR	-	-	-70	dBc
Ruggedness (No damage) (8)	10:1 VSWR	-	-	-	-
Power Control Range	V_{VRAMP}=0.23V to 1.7V	50			dB

Notes:
(7). V_{CC}=3.5V, Freq = 1880MHz, Tc = 25℃, unless otherwise specified
(8). All phase, time=10s

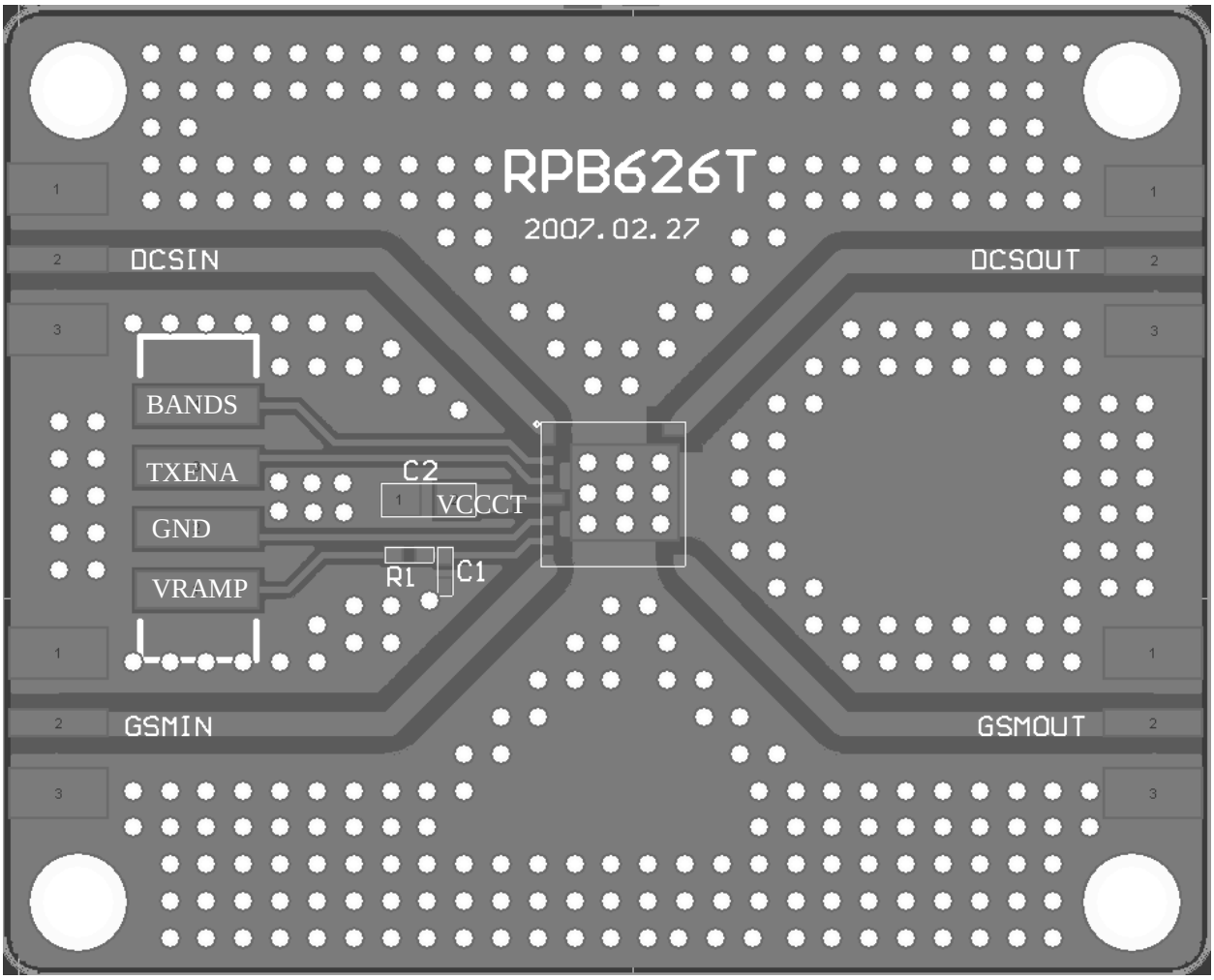
Test Circuitry for RDA6252 Module



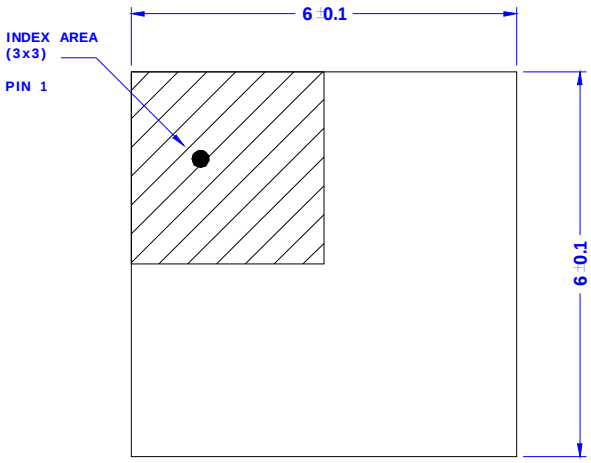
Component Value of Test Circuitry

Component	C1	C2	C3	C4	R1
Value	47pF	22μF	10pF	47pF	10kΩ

Demo Board for RDA6252 Module

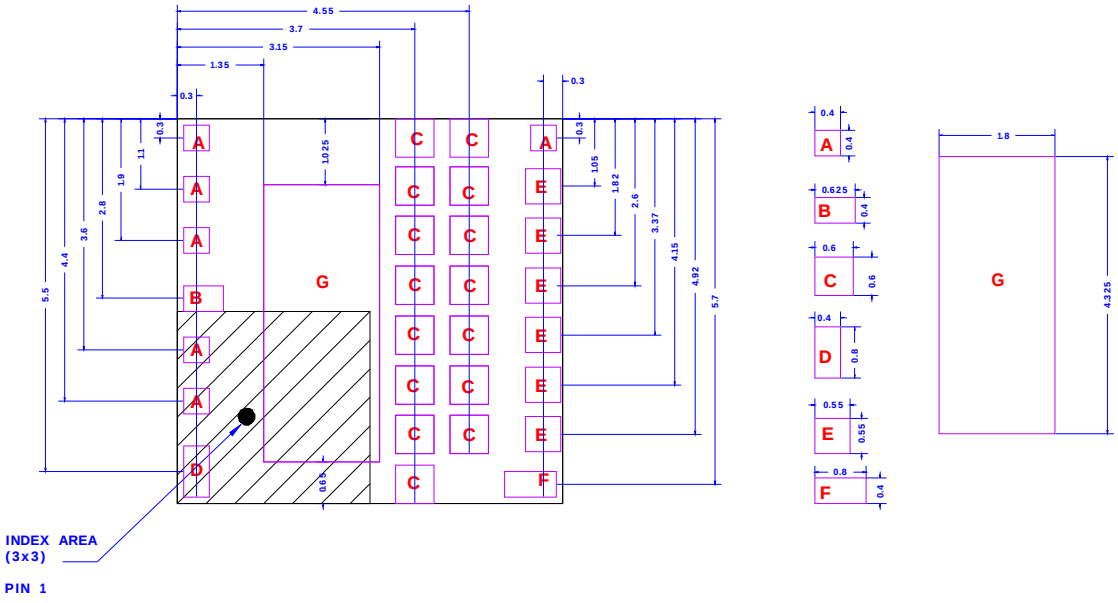


Package Dimensions and Pin Descriptions



TOP VIEW

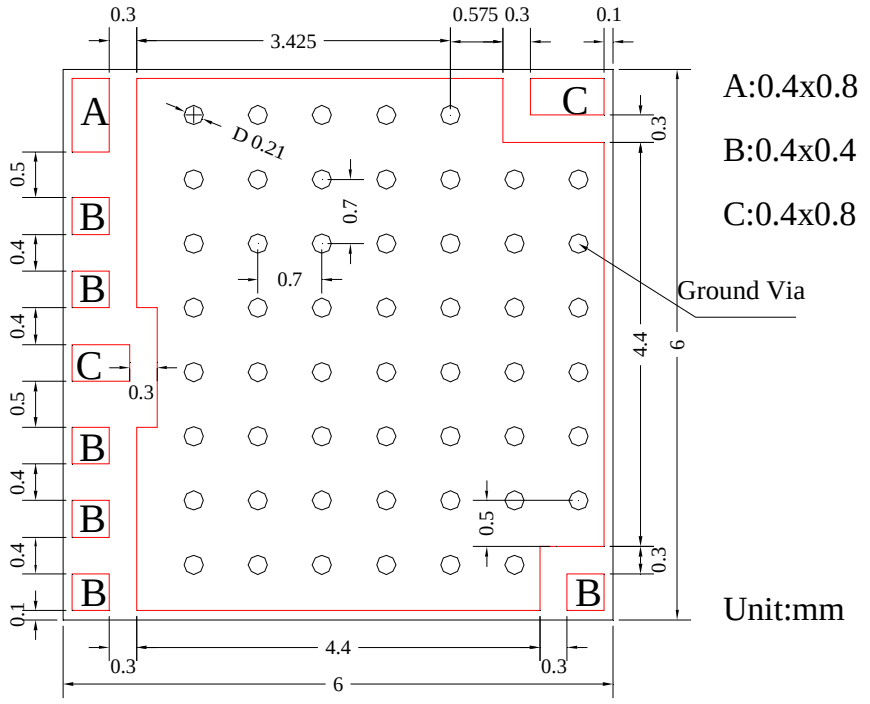
SIDE VIEW



BOTTOM VIEW

unit:mm

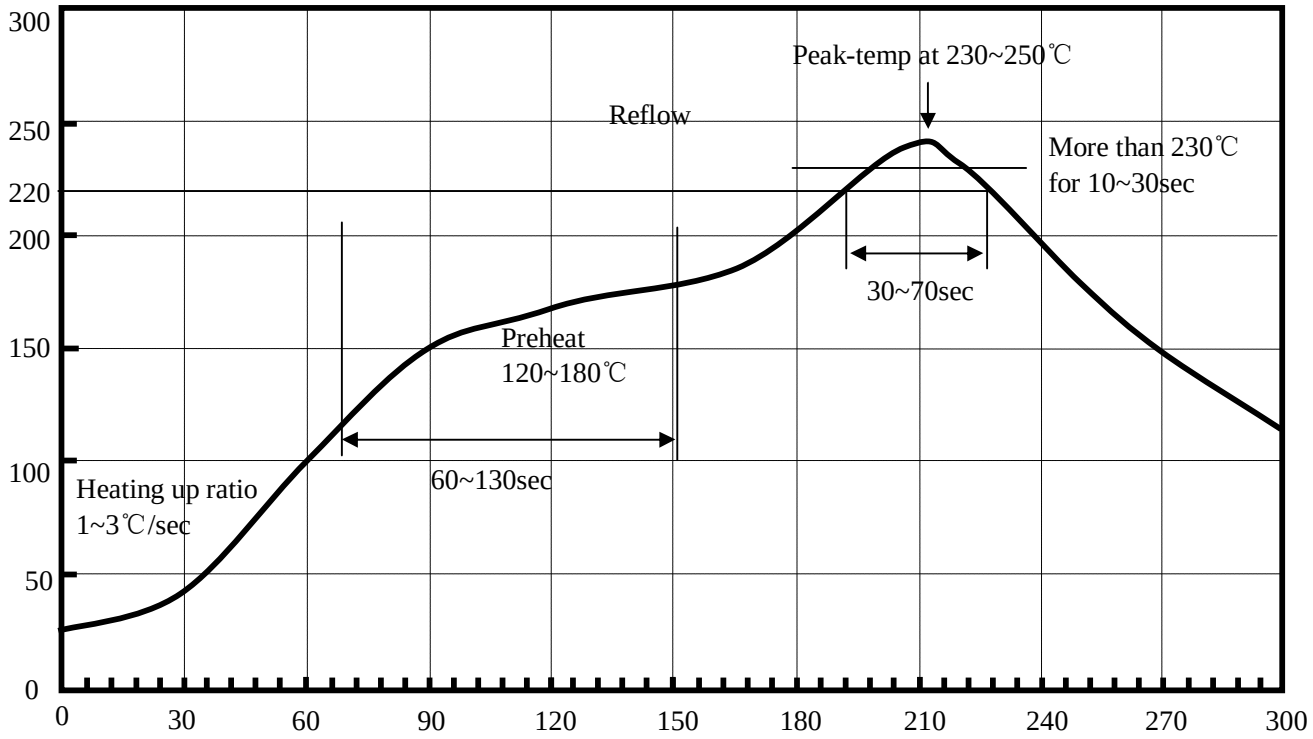
Recommended PCB Land Pattern



Recommended PCB Metal Land Pattern

Recommended PCB Solder Mask Land Pattern

Recommended Solder Temperature



Recommended Temperature Sn95.5Ag4.0Cu0.5

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

Disclaimer

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Attachment 1:

1. Devices Information

1.1 Device Name: RDA6252.
1.2 Package Size: 6×6×1.1 mm^3.
1.3 Moisture Sensitivity Level: 3.

2. Packing Requirement

2.1 RDA6252 uses 13" tape & reel, and one reel inclues 3000 units.

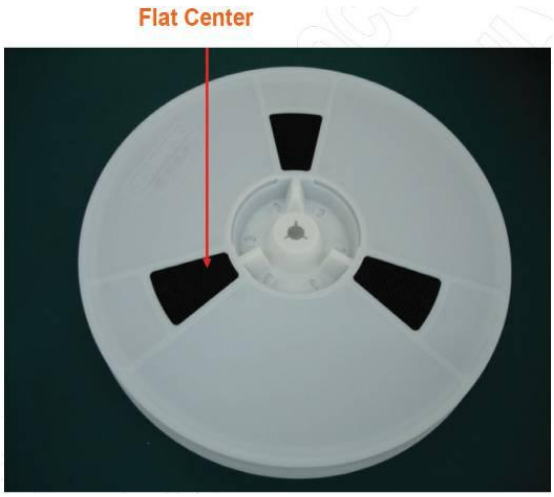

Figure 1

2.2 Pin1 Location:

Pin 1 points to top left corner, and pls see as below:

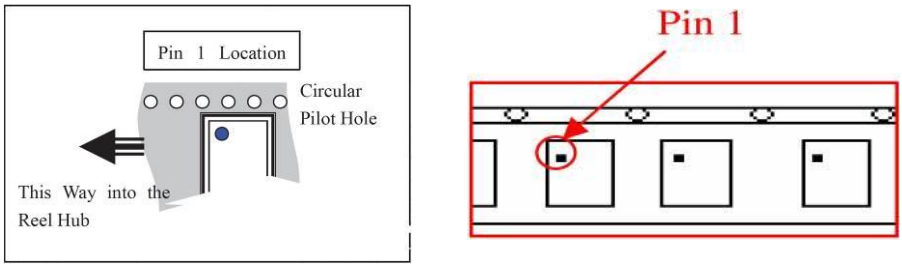

Figure 2

2.3 Label Information

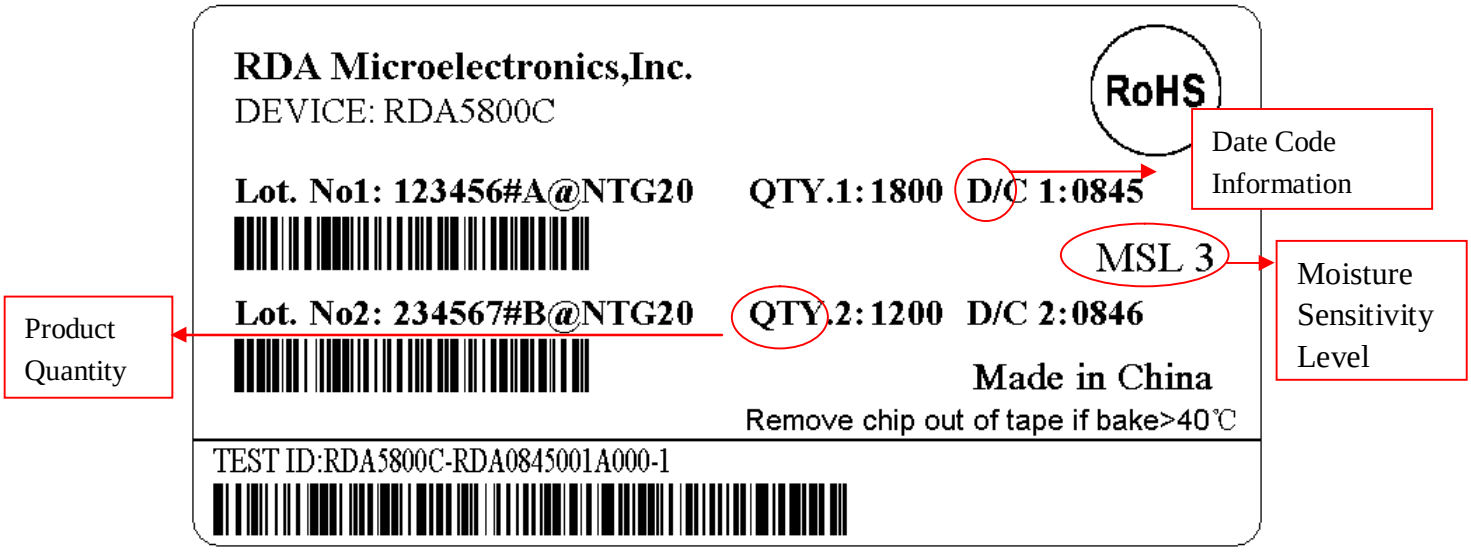

Figure 3

2.4 Baking Requirement

- If need to bake the products, pls remove chip out of tape;
- Bake Condition: 125℃ 8Hours.

Notes: all the MSL3 devices are baked before shipment.

3. Storage and Use Conditions

3.1 Storage and Use Conditions: ≤ 30°C / 60% RH.

3.2 If Moisture Barrier Bag is not opened, the shelf life is 2 years.

3.3 Once opened, the device must be used up within 168 hours, otherwise baking is necessary when it is used again.

4. Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic SMT	Pb-Free SMT
Preheat & Soak		
Temperature min (Tsmin)	100 °C	150 °C
Temperature max (Tsmax)	150 °C	200 °C
Time (Tsmin to Tsmax)(ts)	60-120 seconds	60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3 °C/second max.	3 °C/second max.
Liquidous temperature (TL)	183 °C	217 °C
Time at liquidous (tL)	60-150 seconds	60-150 seconds
Peak package body temperature (Tp)*	See classification temp in Table 4.1	See classification temp in Table 4.2

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Time (tp)** within 5 °C of the specified classification temperature (Tc)	20** seconds	30** seconds
Average ramp-down rate (Tp to Tsmax)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (tp) is defined as a supplier minimum and a user maximum.		

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall bewithin±2°Cofthelive-bugTp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 5-2.For example, if Tc is 260 °C and time tp is 30 seconds, this means the following for the supplier and the user.For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.

Note 3: All components in the test load shall meet the classification profile requirements.

Note 4: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020,JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

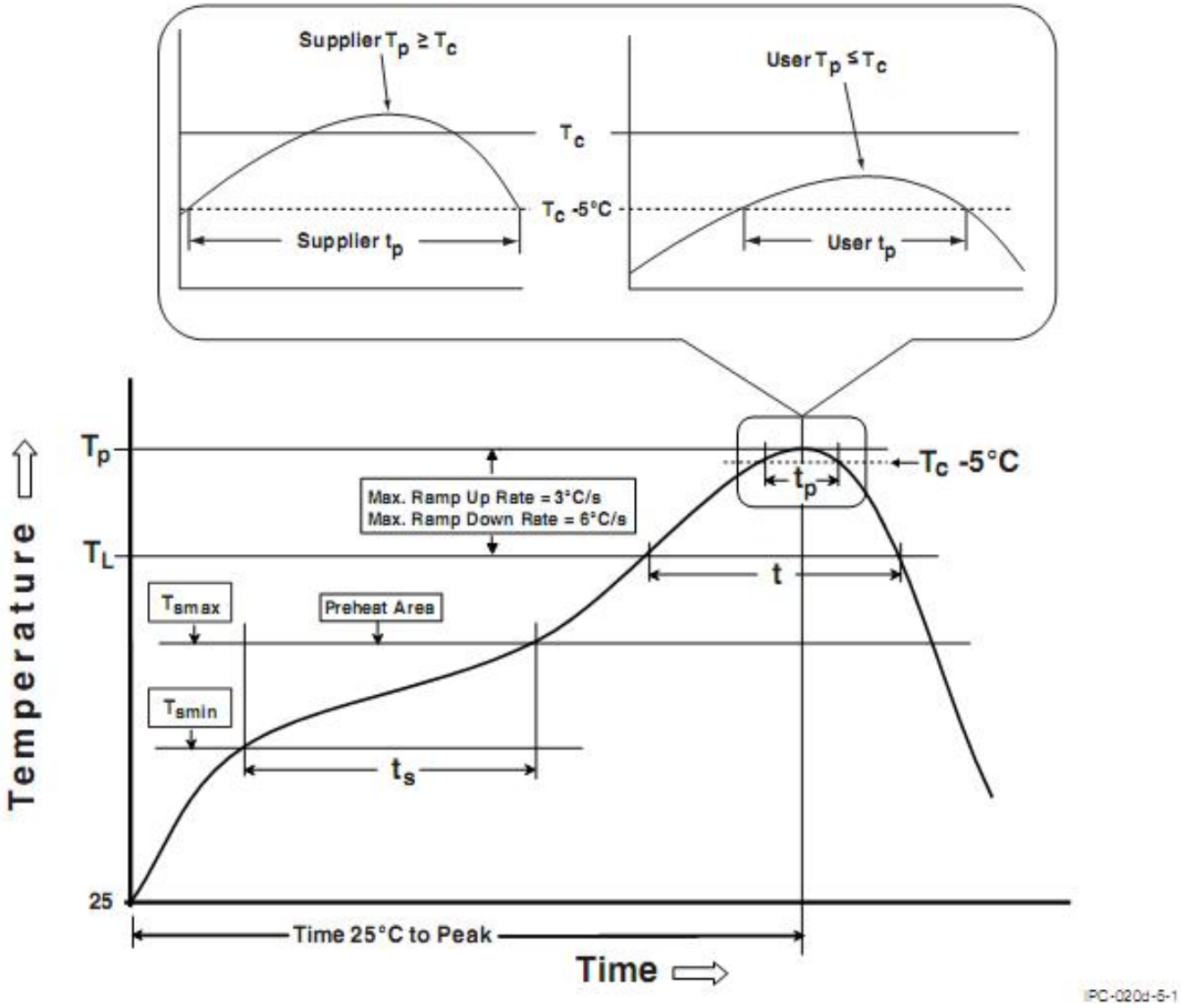

Figure 4

Attachment 2:

RDA6252 mark Description:

Row3: Vendor code+date code (XXX)+ tracing No.(*****)

Sample as followed: