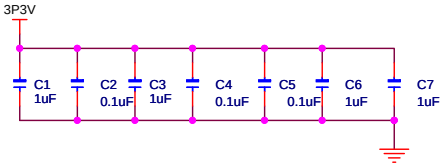
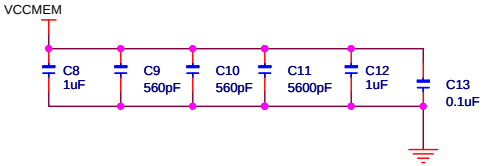
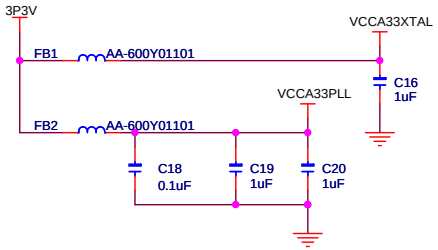
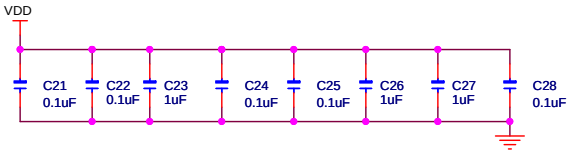
WM8505: Power / Ground

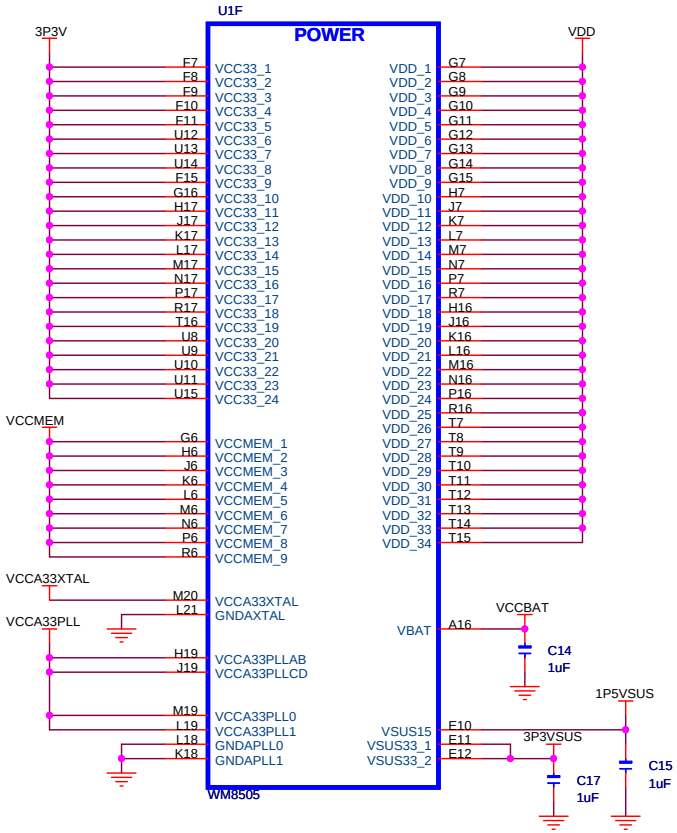
PART: F+G

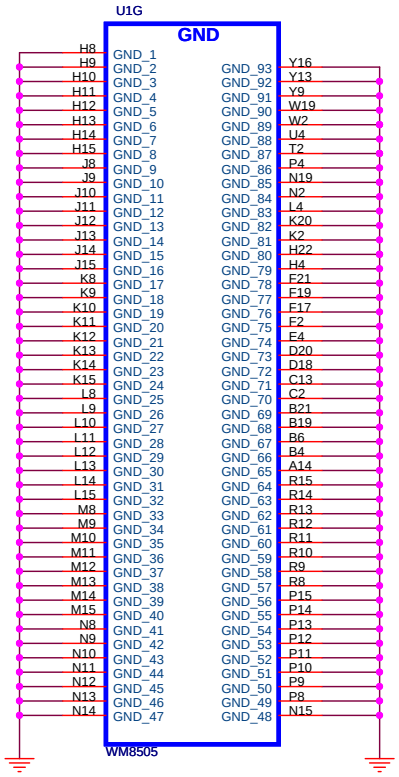












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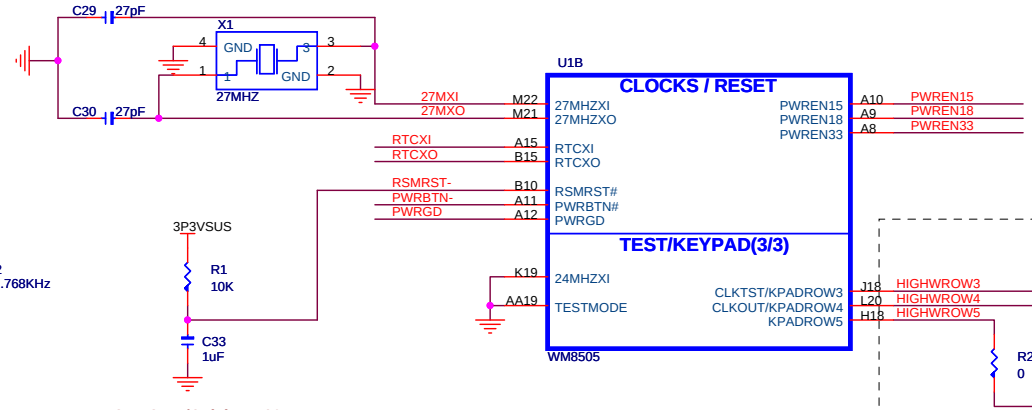
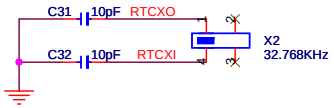
CLOCK + RESET + PMC

PART:B

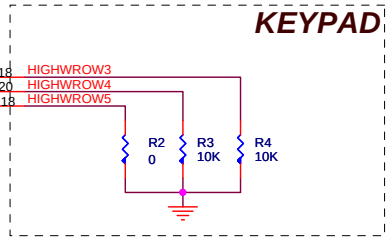
Main CLK:



RTC CLK:

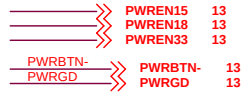


RSMRST R/C delay ~ 20ms



For KEYPAD direct input, need PD 10K

Power Enable:



G-LINK		
Title: A2		
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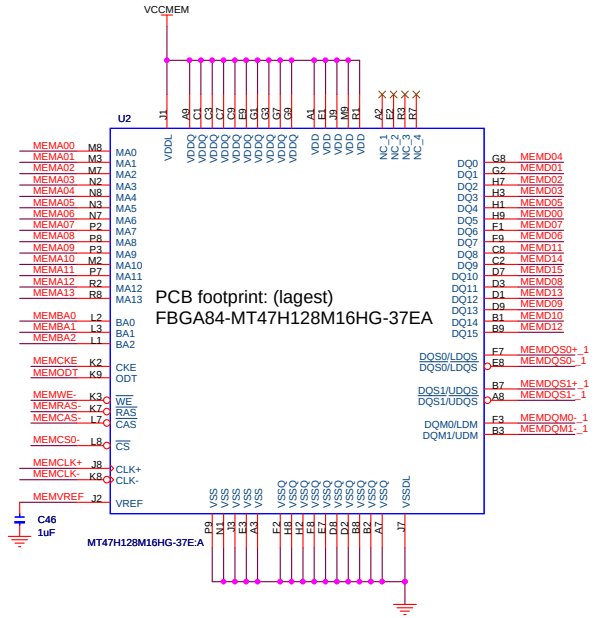
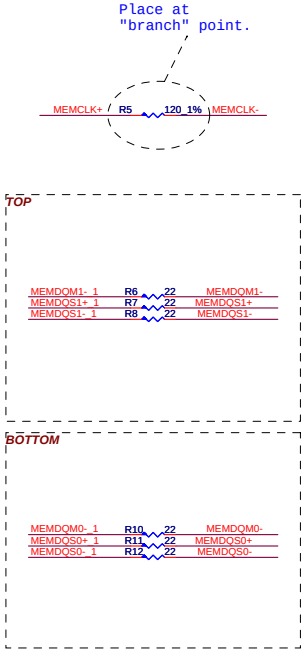
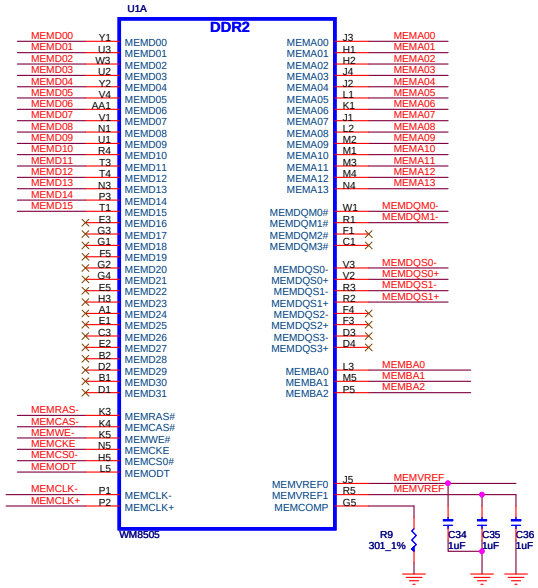
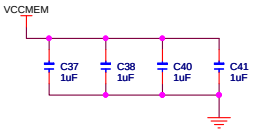
WM8505: DDR2 SDRAM

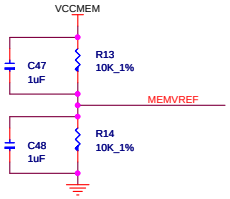


A3R1GE4CFF-G6E 64M x 16bit









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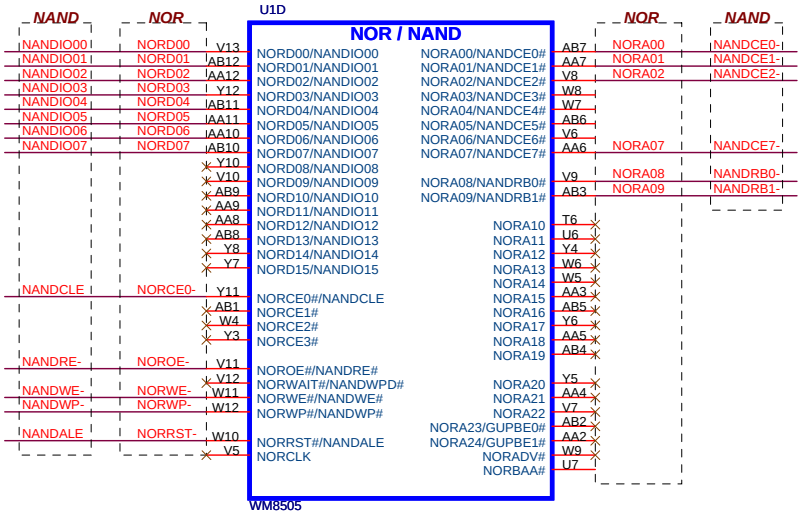
STRRAPPING:

NORA00 11

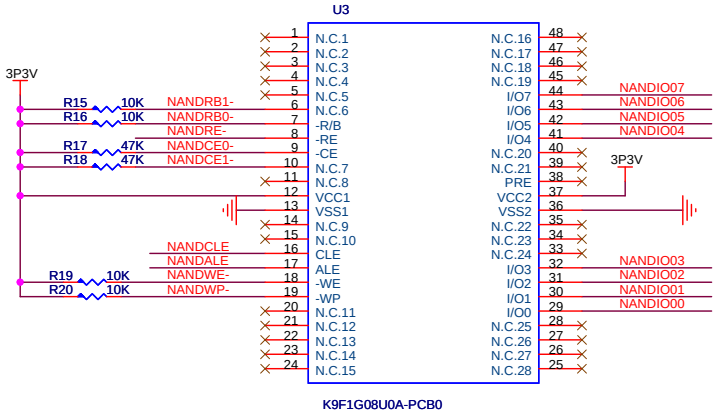
NORA02 11

NORA07 11

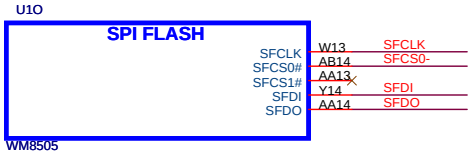
WM8505: NAND FLASH



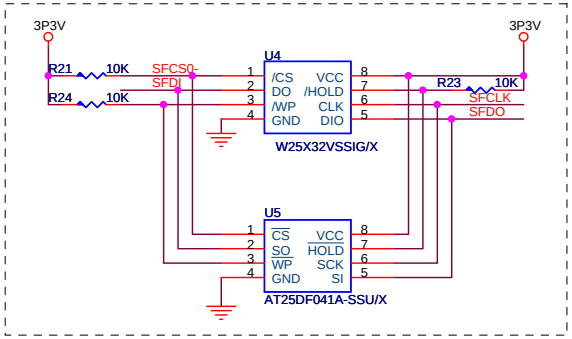
NAND FLASH:



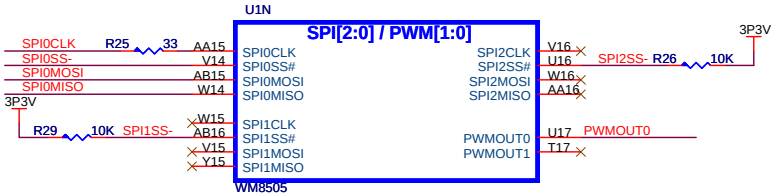
WM8505: SPI FLASH

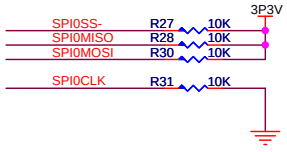


(optional) 8 pins package (co-lay)



WM8505: SPI + PWM





LCD Backlight Control:

PWMOUT0 LCD_BL_DIM 13

LCD 3-wire I2C Control:

SPI0CLK Panel_SCL 13
SPI0MOSI Panel_SDA 13
SPI0SS- Panel_CSB 13

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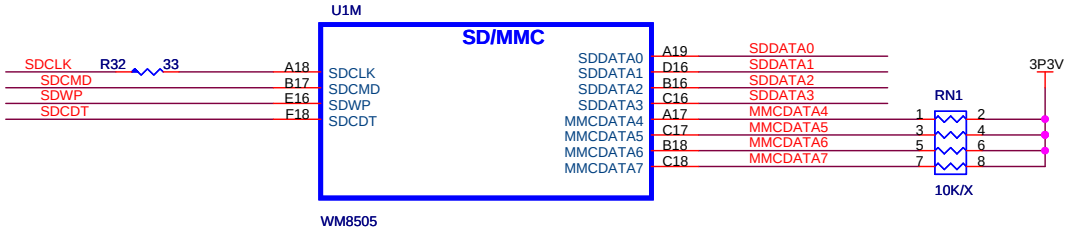
WM8505: SD / MMC

PART: M



G-LINK		
Title: A2		
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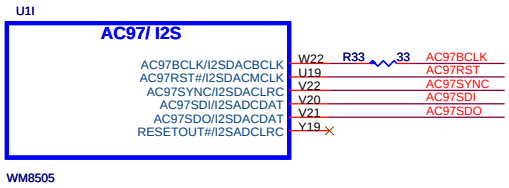
WM8505: I2S

PART: I

(Mike)



G-LINK		
Title: A2		
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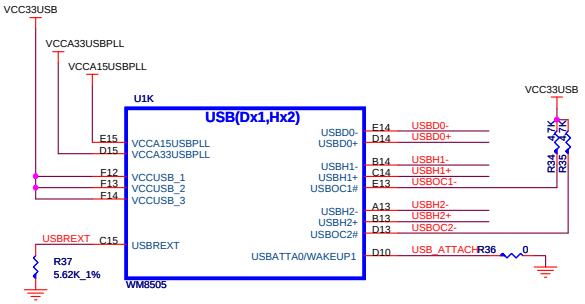
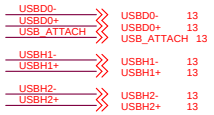
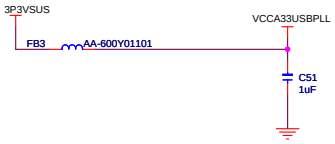
WM8505: USB (HOST+DEVICE)

PART: K

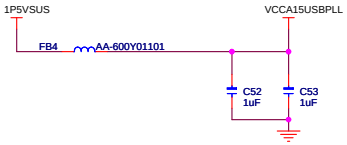




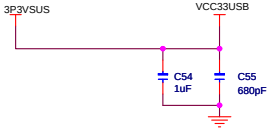
VCCA33USBPLL (suspend power)



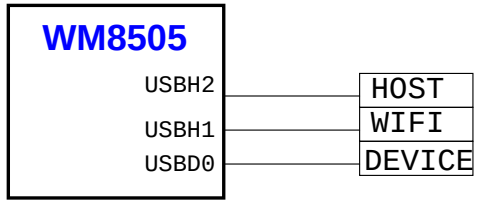
VCCA33USBPLL (suspend power)



VCC33USB (suspend power)



(USBH2) to USB A TYPE HOST single right-angle connector.
(USBH1) to WiFi miniCard connector
(USBD0) to USB mini-B connector.



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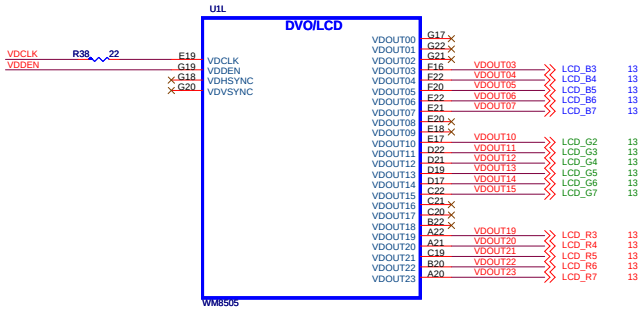
WM8510: DVO / LCD

PART: L

Damping Rs (put close to WM8510) --> deleted. no need!



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Title: A2		
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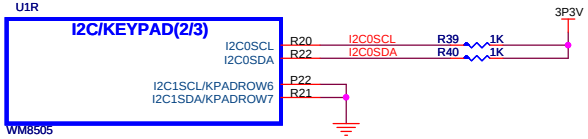
WM8505: I2C / KEYPAD

PART: R



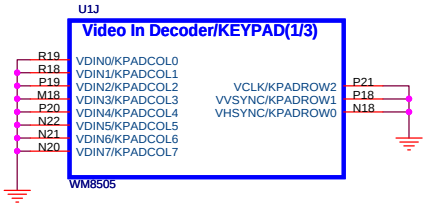
I2C ADDRESS TABLE:

BUS	DEVICE	FUNCTION	ADDRESS
I2C0	VT1602	I2S Codec	0x34

VGA EDID:

WM8505: VDIN / CMOS / KEYPAD

PART: J



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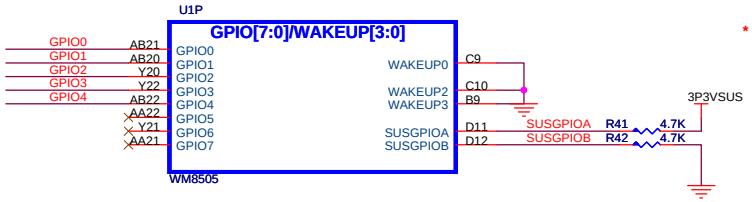
WM8505: GPIO+STRAPPING+WAKEUP

PART: P

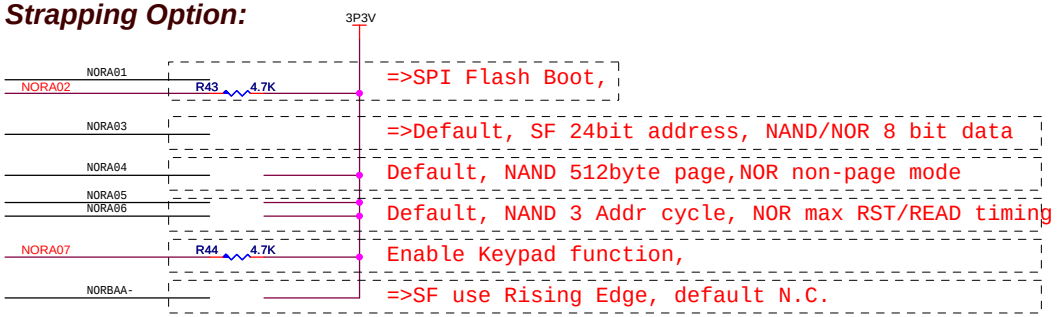


Ethenet MII Mode:

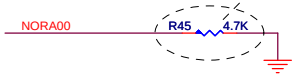
** IMPORTANT: If IO board not use GPIO,please connect GND;*

GPIO Pins:		Function:
GPIO0	DCIN	DCIN Detect
GPIO1	CHARGE	CHAEGE STATE
GPIO2	Wifi_POWER_DN	Wifi_POWER_DN
GPIO3	MuteGPIO	AC97/I2S Amp ShutDown/Mute GPIO:
GPIO4	RF_POWER_DN	RF_PWRDN
GPIO5		Light_INT
GPIO6		To MP1530 LCD Power ENABLE
GPIO7		SD Card Power

Strapping Option:



** IMPORTANT: Need PD in normal use.*



STRAPPING TABLE:

PIN_NAME	RS	ON/OFF	Internal	DESCRIPTIONS
NORA0	R98	ON	PD	Debug Mode, default PD ext.
NORA[2:1]	R221,R109		PD,PD	NOR Boot
		ON-OFF		=>SPI Flash Boot,
NORA3	R220,	OFF	PD	=>Default, SF 24bit address, NAND/NOR 8 bit data
				PU ext. SF 32bit address, NAND/NOR 16 bit data
NORA4	R224	OFF	PD	Default, NAND 512byte page,NOR non-page mode
				PU ext. NAND 2K page,NOR page mode
NORA[6:5]	R223,R110	OFF-OFF	PD,PD	Default, NAND 3 Addr cycle, NOR max RST/READ timing
				PD,PU= NAND 4 Addr cycle
NORA7	R118		PD	Disable Keypad function, default N.C.
		ON		Enable Keypad function,
NORBAA-	R222	OFF	PD	=>SF use Rising Edge, default N.C.
				SF use Falling Edge , need PU ext.
SUSGPIO[A:B]	R204,R58		PD,PD	RGMII Mode.
		ON-OFF		=>MII MODE

WARMING:

ALL others strappings not listed above recommend to use internal settings as default. Otherwise un-expected results may encounter.

STRRAPPING:

NORA00 5

NORA02 5

NORA07 5

USB2 to WiFi Module:

GPIO4 → RF_POWER_DN 13

GPIO2 → Wifi_POWER_DN 13

Mute GPIO:

GPIO3 → MuteGPIO 13

Detect DCIN

GPIO0 → DCIN 13

LCD CONTROL:

GPIO1 → TPINT 13

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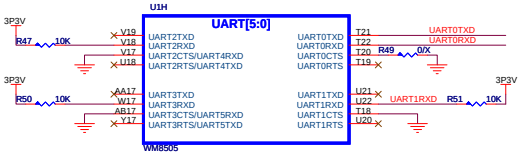
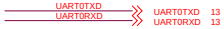
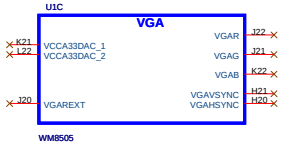
UART/JTAG:



UART0

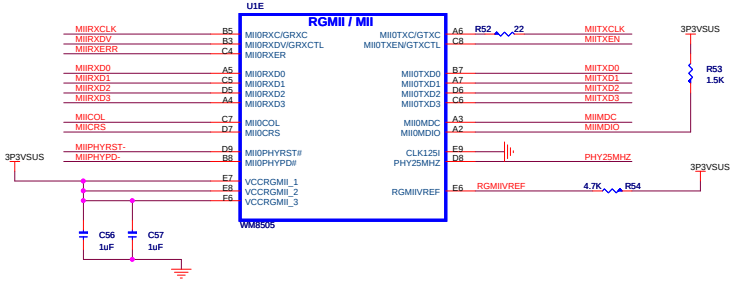


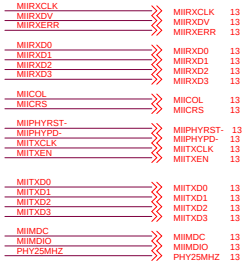
VGA (DAC):



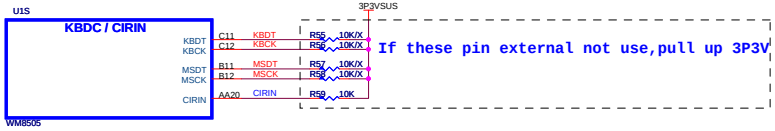
WM8505: RGMII/MII

PART: E





WM8505: PS2 KBDC



G-LINK		
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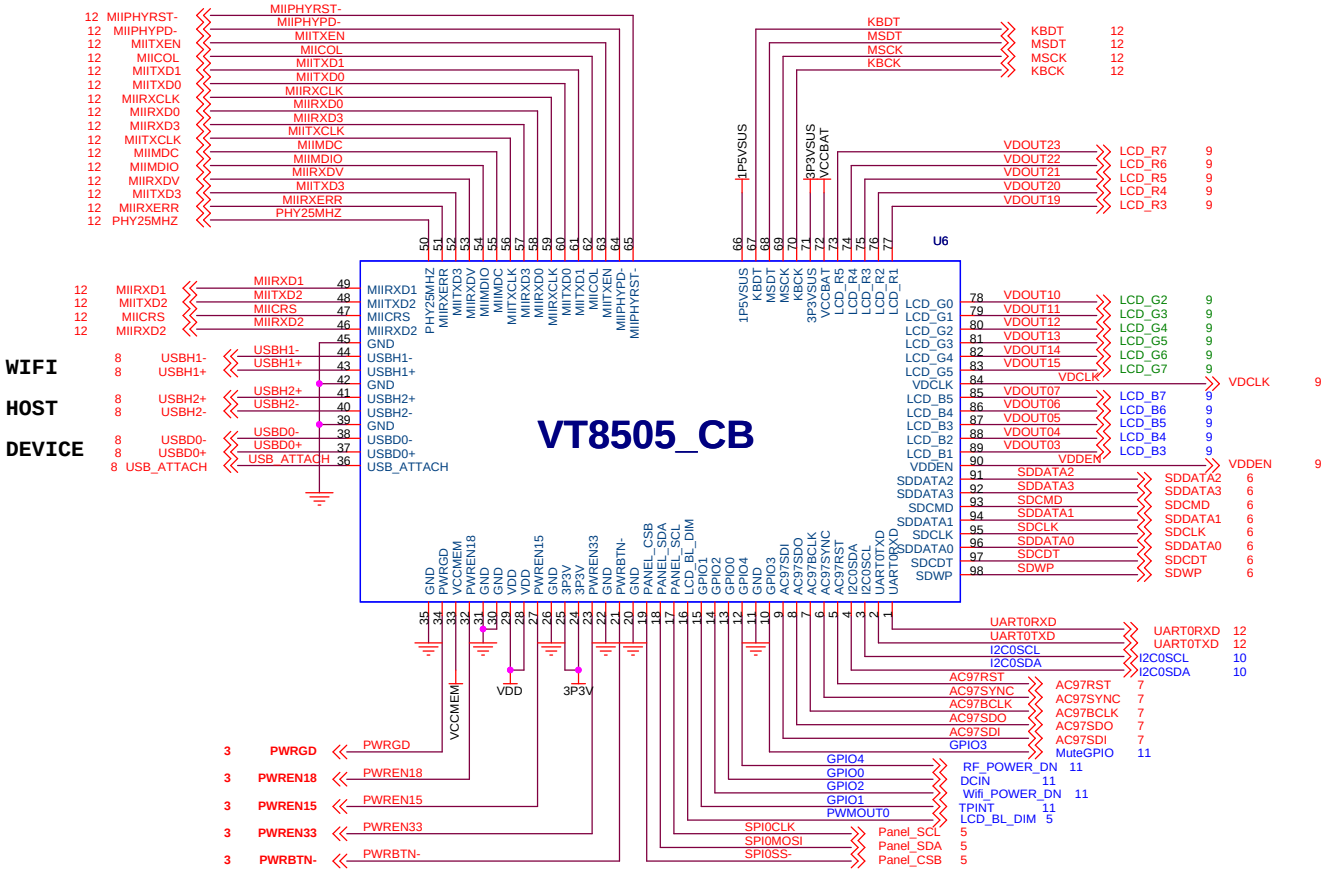

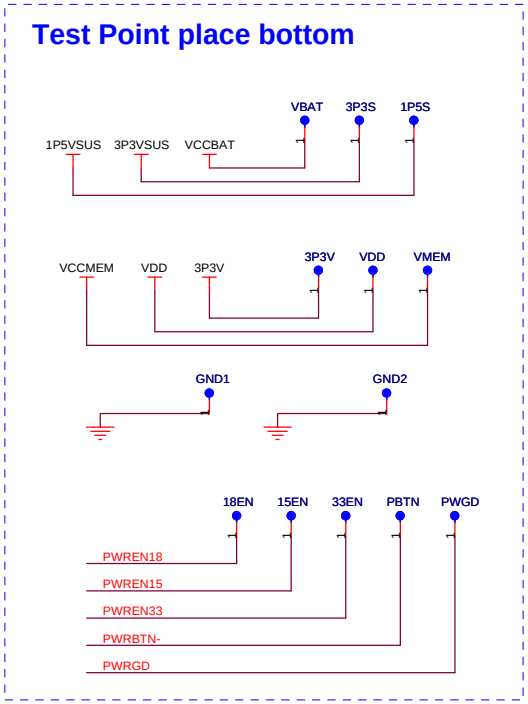

Power must add test point,and place same Bottom layer:
3P3VSUS
1P5VSUS
VCCBAT
VDD
3P3V
VCCMEM
GND(2)

PWRBTN
PWREN15
PWREN33
PWREN18

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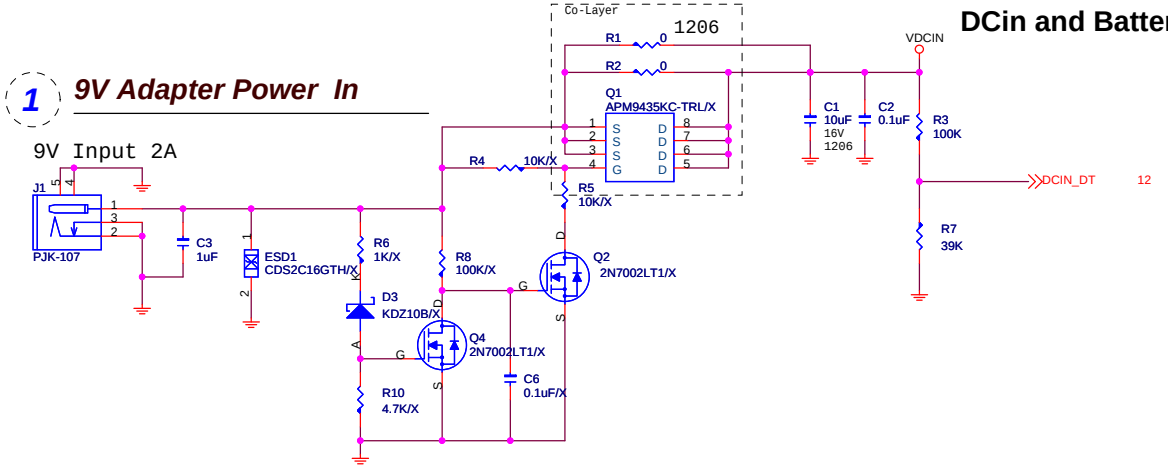
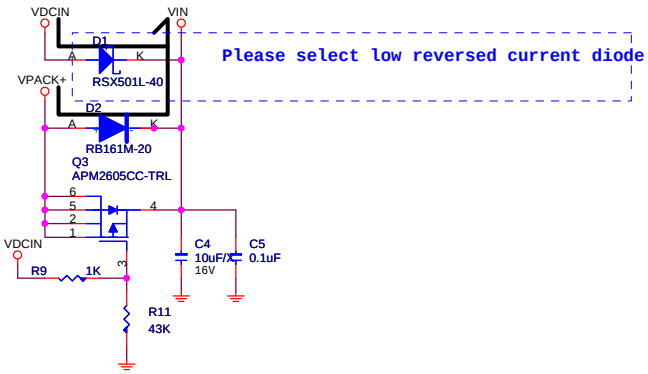
DCin and Battery

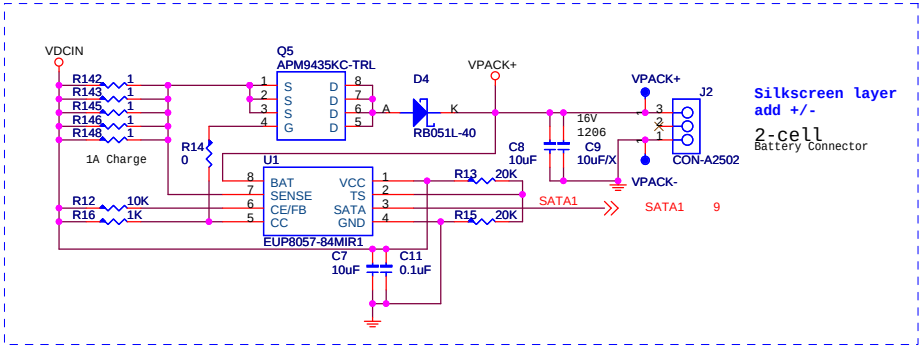
1 9V Adapter Power In

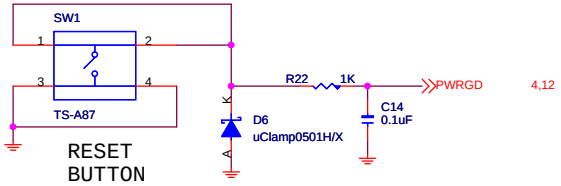
9V Input 2A

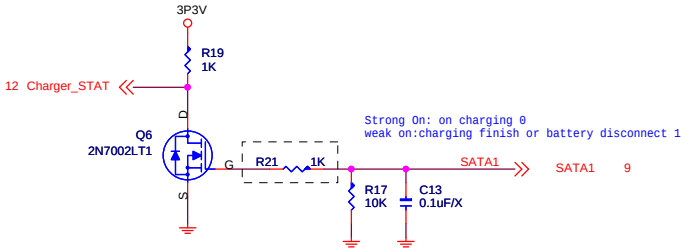


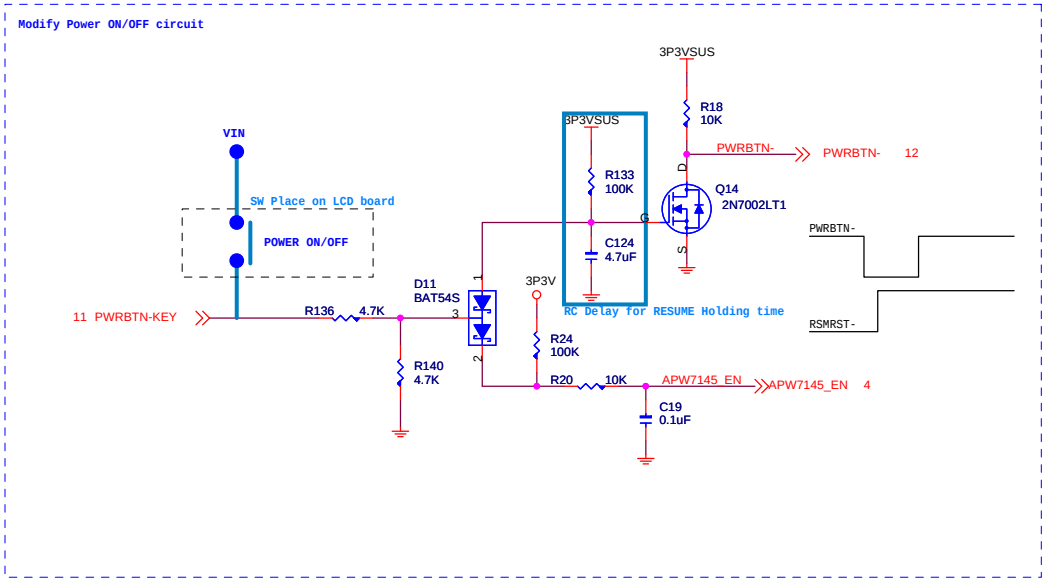
1.5A Rating











G-LINK		
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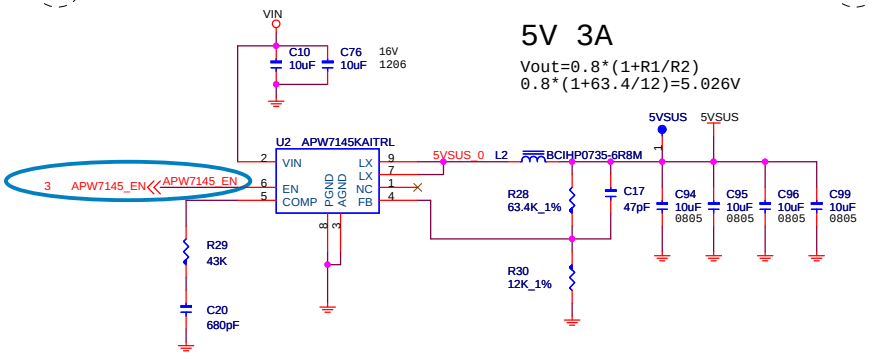
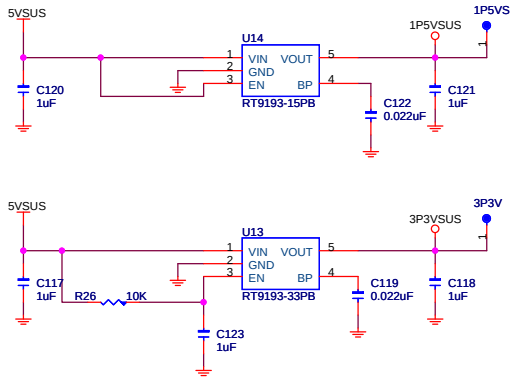
Size: Custom	Document Number <Doc>	Rev 1.0
Date: Saturday, February 06, 2010	Sheet 3 of 13	

Voltage Regulators

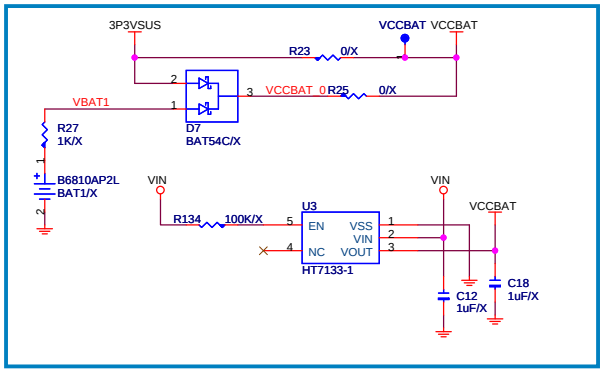
2 12V -> 5VSUS (SoC Power, USB VBUS Power)



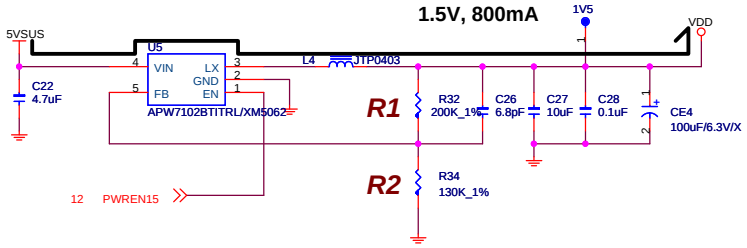
3/4 5VSUS -> 1P5VSUS/3P3VSUS (300mA each)



RTC POWER:

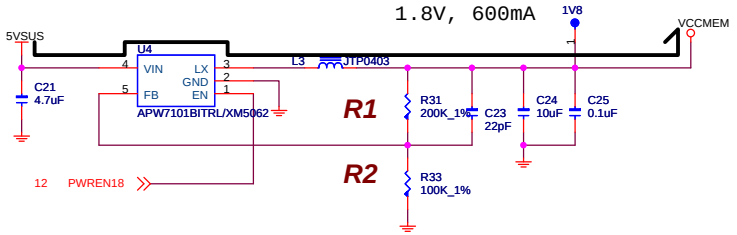


5 5VSUS -> VDD



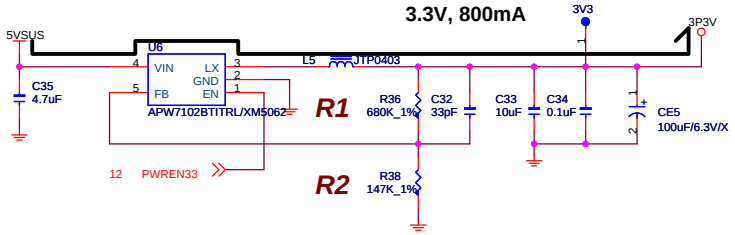
7 5VSUS -> VCCMEM (SoC+DDR2 Chip Power)

Vout=0.6*(1+R1/R2)
06*(1+400/200)=1.8v@1A

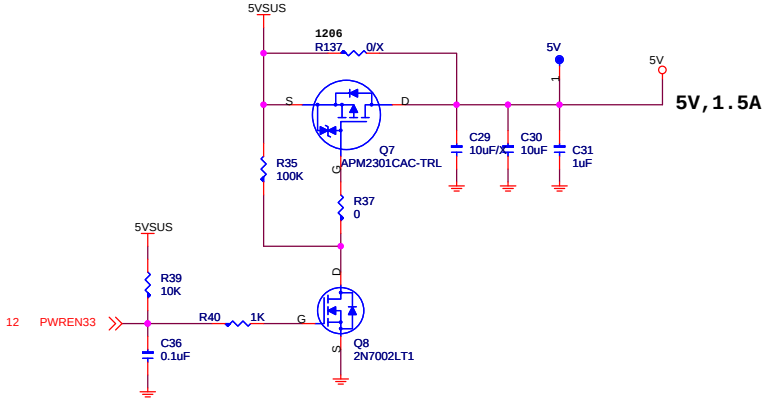


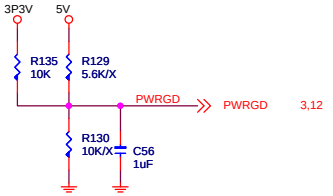
6 5VSUS -> 3P3V

Vout=0.6*(1+R1/R2)
0.6*(1+180K/39K)=3.37v@1A



8 5VSUS -> 5V (Device Power) (LCD,I2S,UART)





Power Enable:

PWREN15 12
PWREN18 12
PWREN33 12

G-LINK		
Title: A2		
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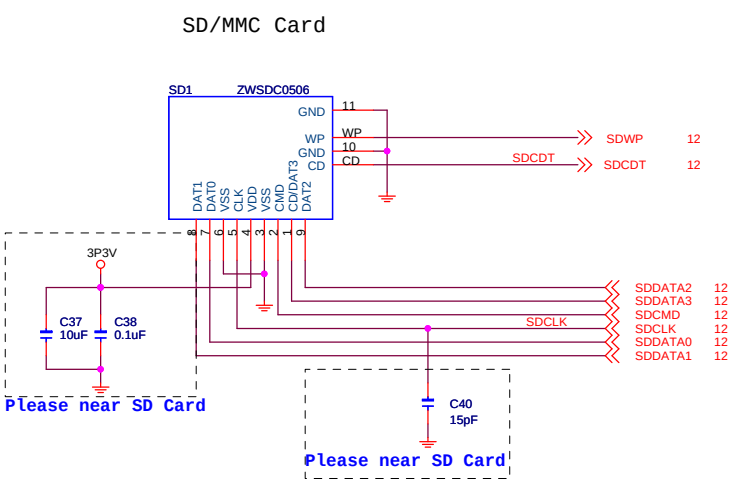
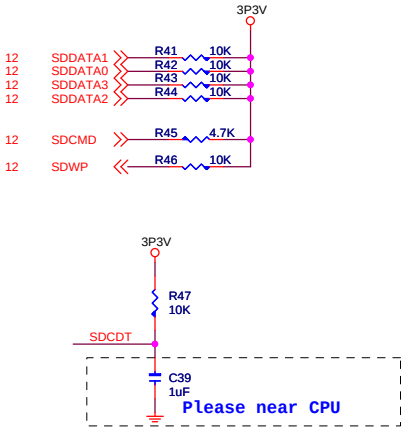
SD Socket (SD/MMC only)



PU Resistors:



G-LINK		
Title: A2		
Size: Custom	Document Number: <Doc>	Rev: 1.0
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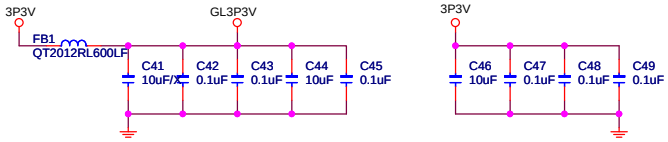
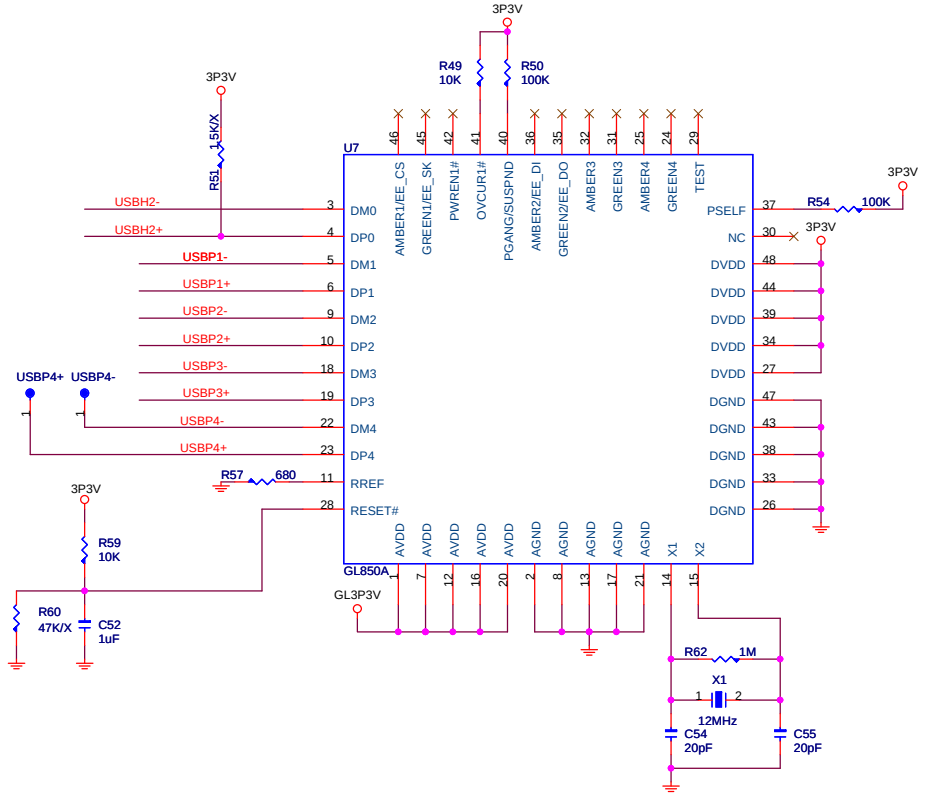
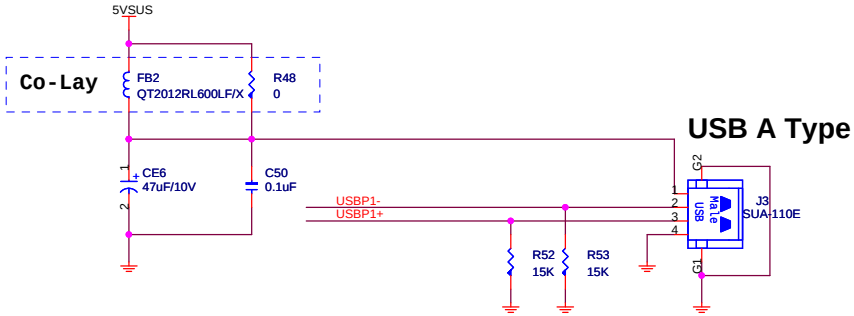
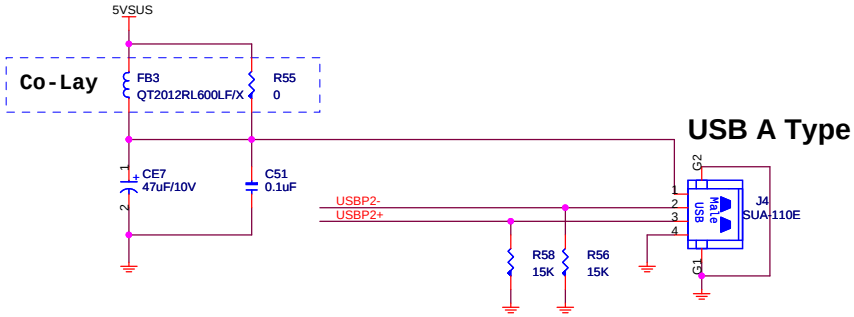
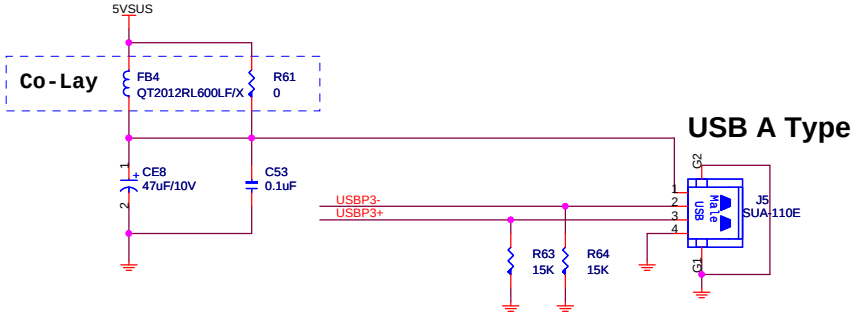
USB HUB

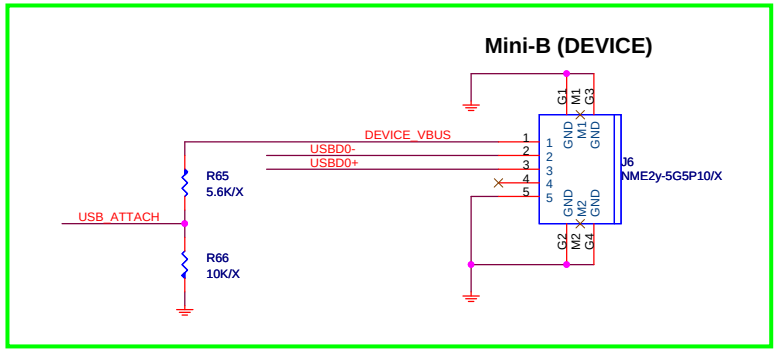












USBH2- → USBH2- 12
USBH2+ → USBH2+ 12
HOST

USBD0- → USBD0- 12
USBD0+ → USBD0+ 12
USB_ATTACH → USB_ATTACH 12
DEVICE

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Title: A2		
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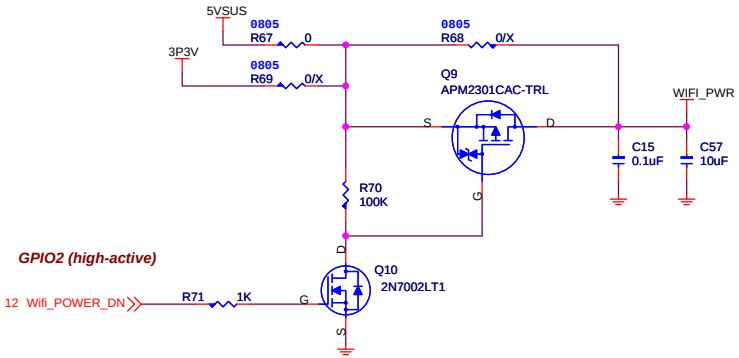
3.3V WiFi POWER:



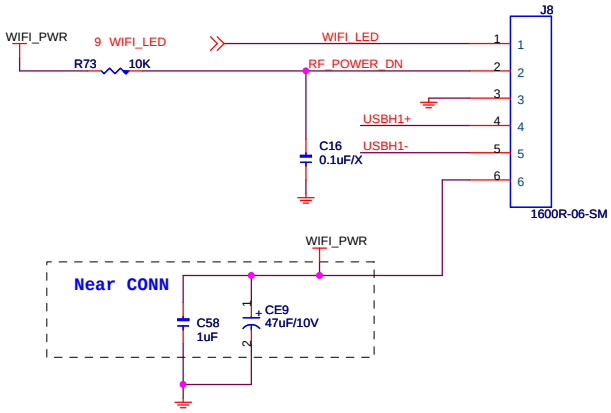
12 Wifi_POWER_DN <<< Wifi_POWER_DN

12 USBH1-
12 USBH1+
<<< USBH1-
USBH1+

WiFi Mini-Card Connector (ref to standard PCIE-minicard)

Delete WiFi Mini-card Connector

Modify WiFi Radio On/off circuit



G-LINK		
Title: A2		
Size: Custom	Document Number: <Doc>	Rev: 1.0
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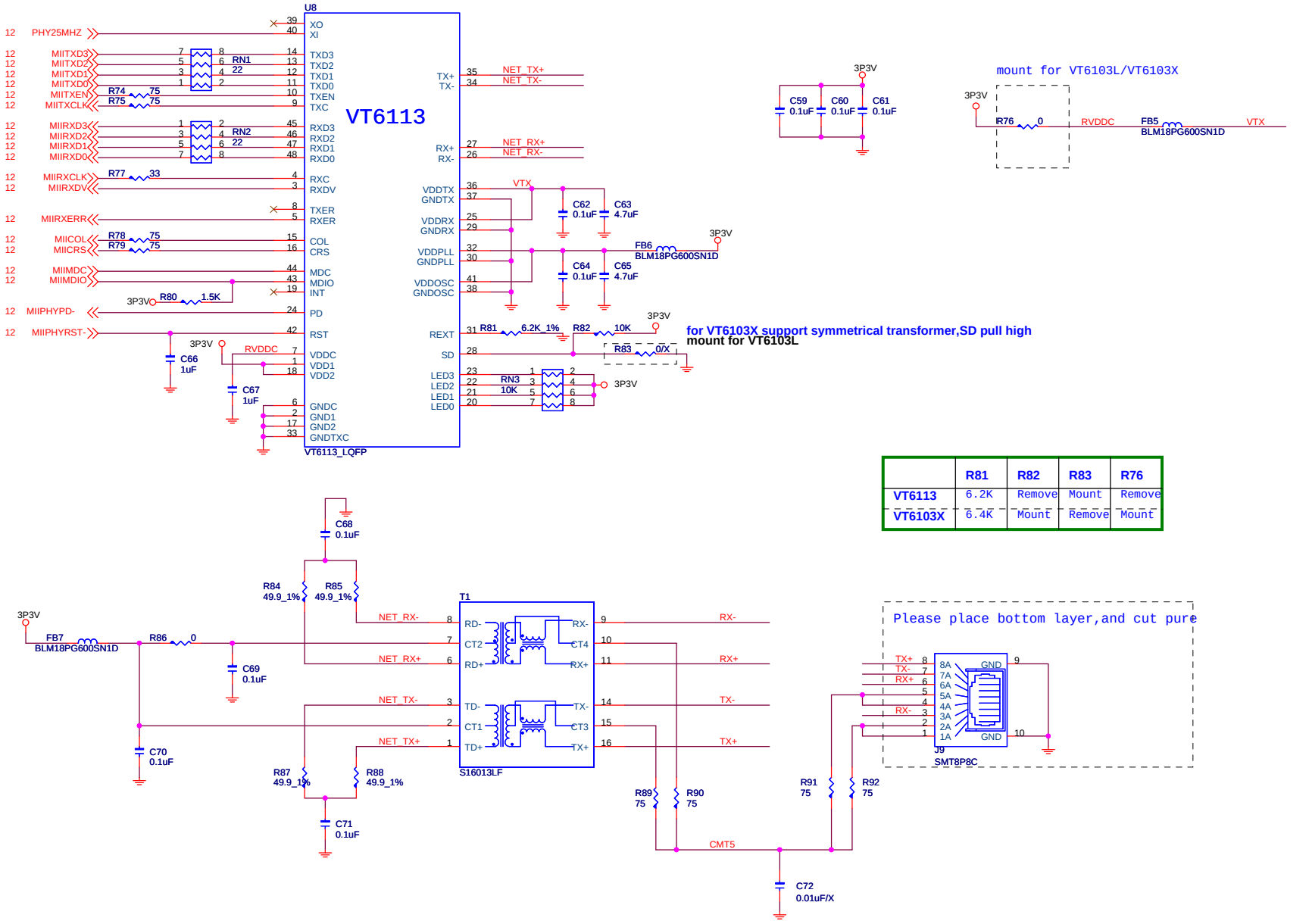
Ethernet PHY



	R81	R82	R83	R76
VT6113	6.2K	Remove	Mount	Remove
VT6103X	6.4K	Mount	Remove	Mount

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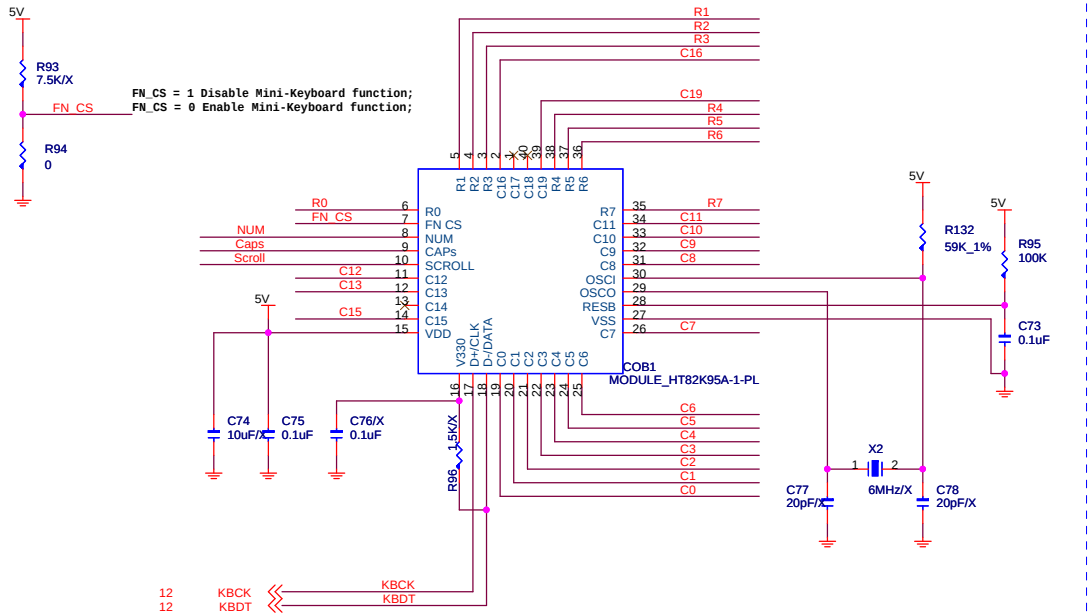
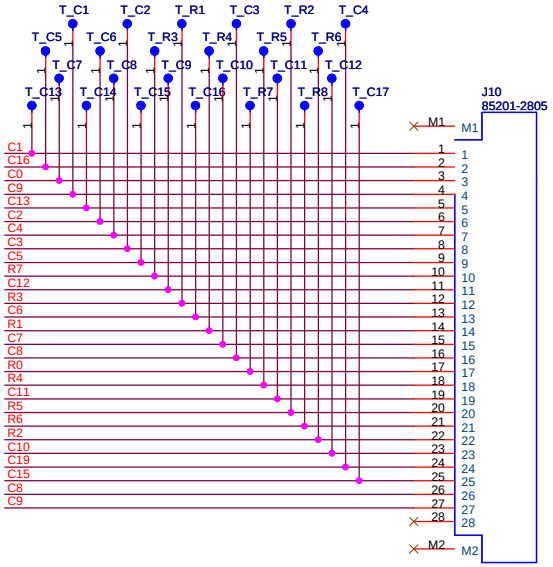
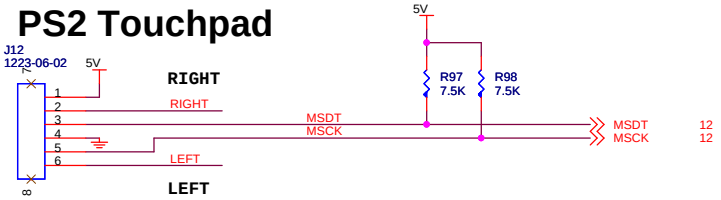
PS2/USB Keyboard



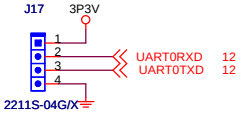
	R76	R96	C77	C78	X2	R132
HT82K95A-1	Mount	Mount	Mount	Mount	Mount	Remove
HT82K68A-01A	Remove	Remove	Remove	Remove	Remove	Mount

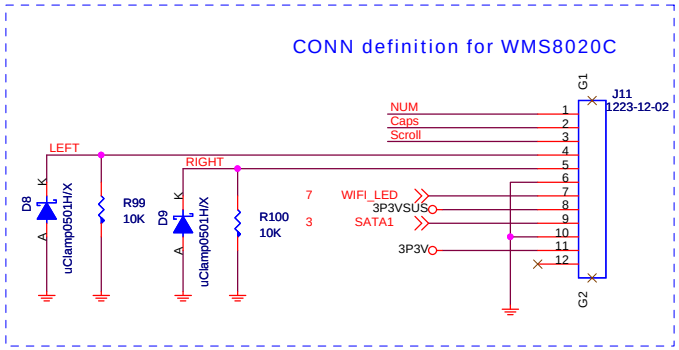


PS2 Touchpad



Reversed for debug





G-LINK			
Title	A2		
Size	Document Number		Rev
Custom	<Doc>		1.0
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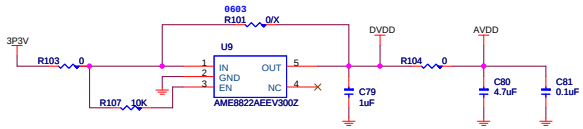
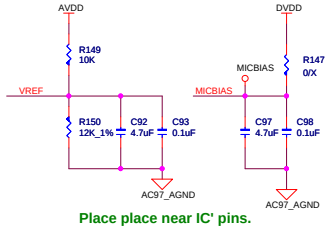
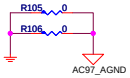
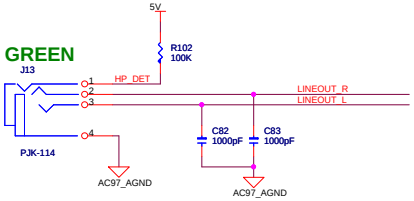
AC97 CODEC

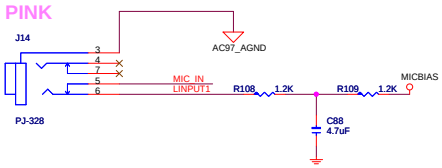


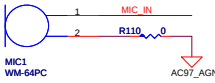


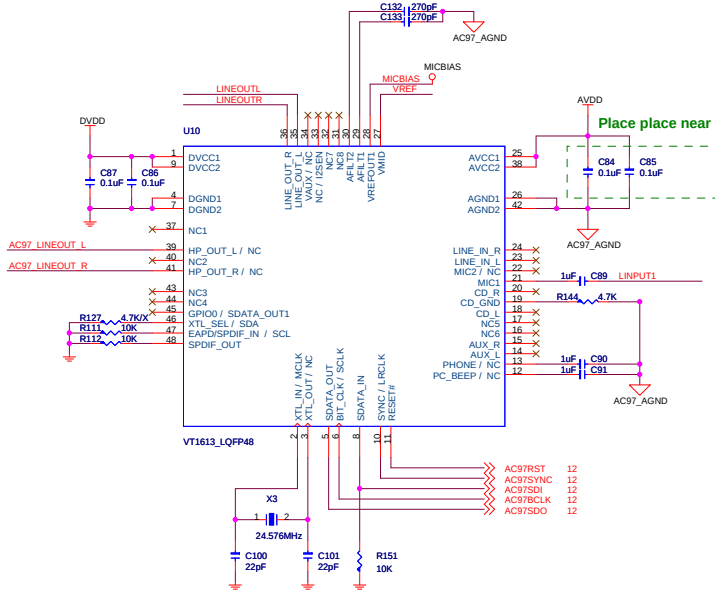
Place place near IC' pins.

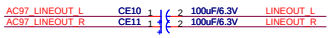




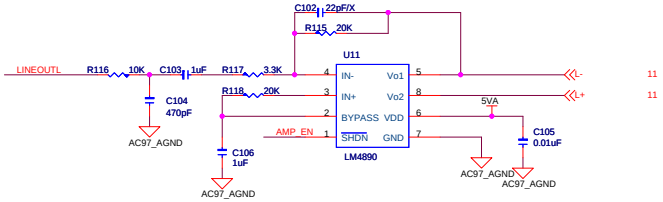


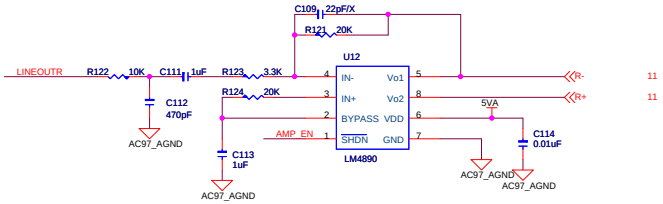




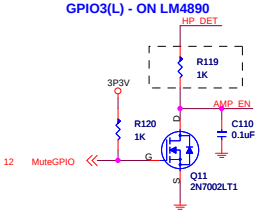


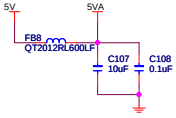
Please near to codec





GPIO3(H) - OFF LM4890;
GPIO3(L) - ON LM4890





G-LINK		
Title: A2		
Size: C	Document Number: <Doc>	Rev: 1.0
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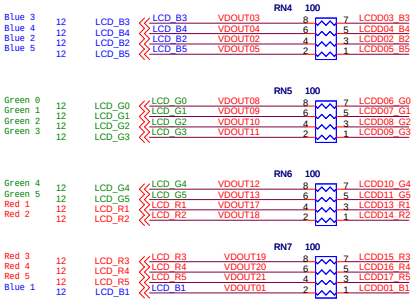

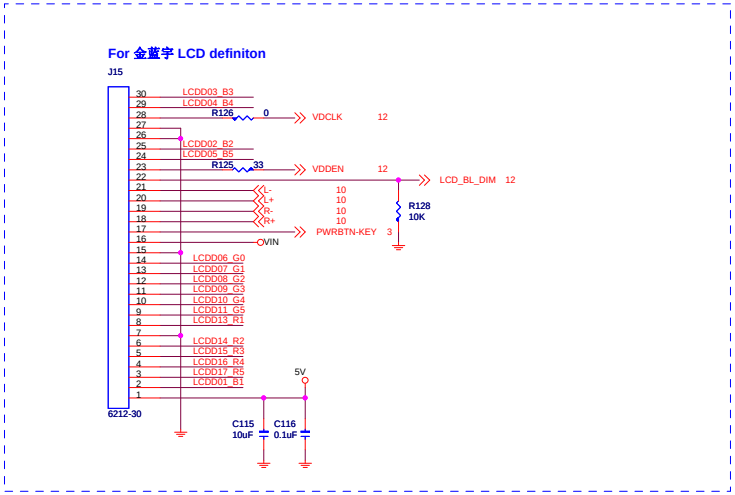

G-LINK			
Title: A2			
Size: C	Document Number: <Doc>		Rev: 1.0
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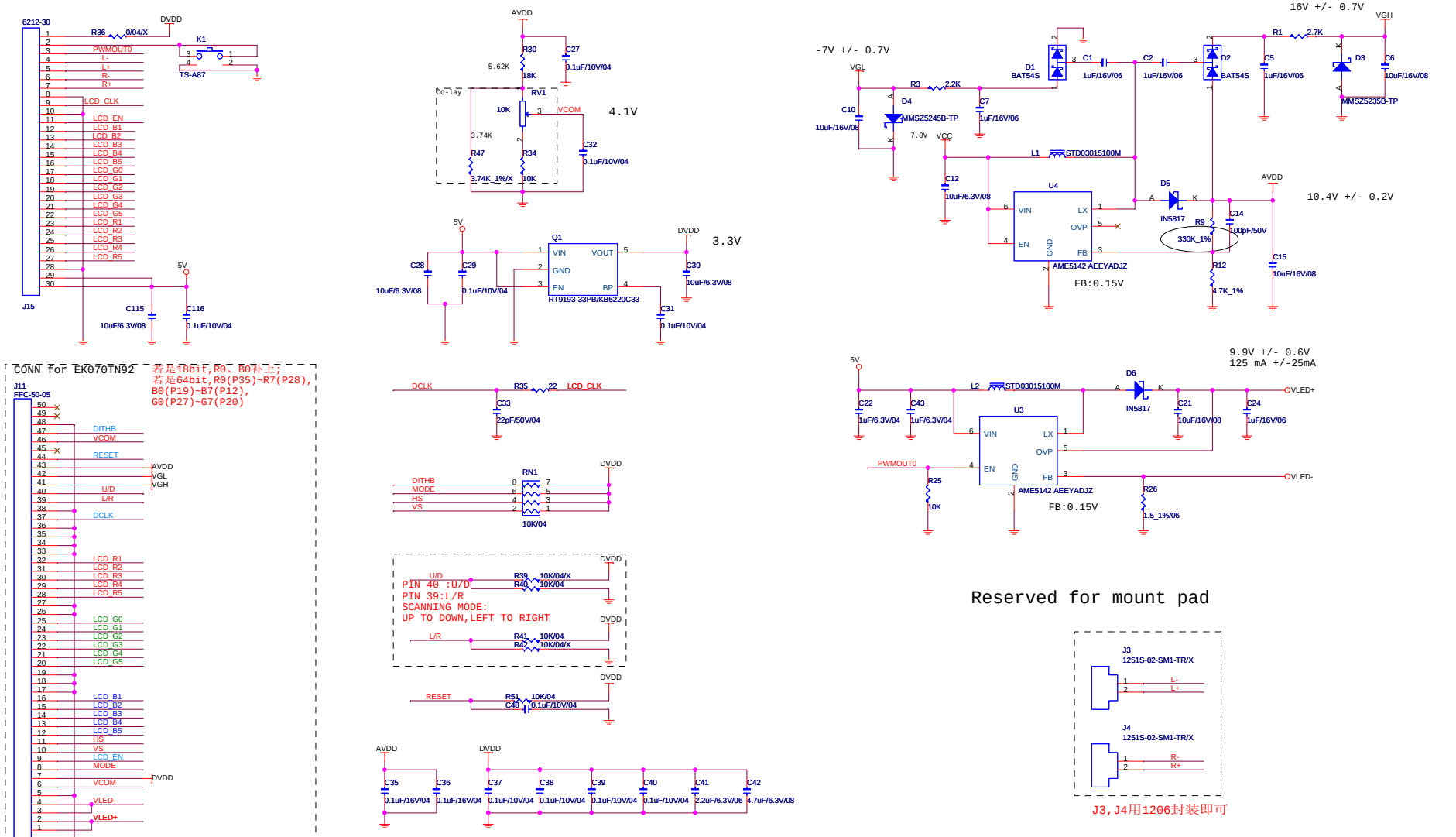
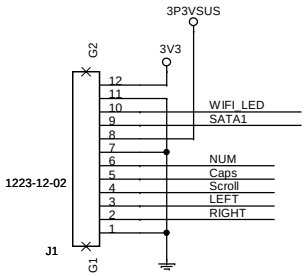
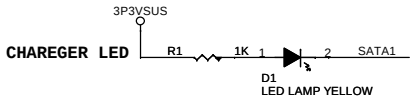
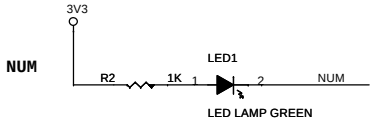
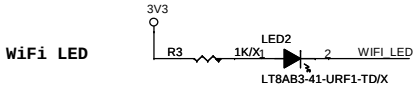


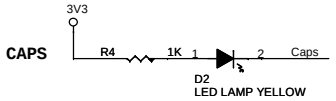
VIA TECHNOLOGIES INC.	
Title	LCD
Size: Custom	Document Number: PID
Rev	0.4
Date: Thursday, June 17, 2010	Sheet 1 of 1

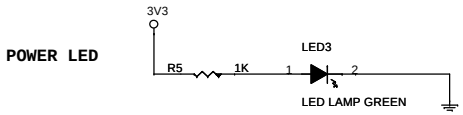


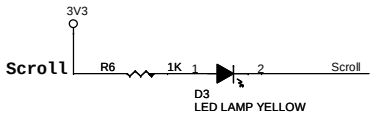






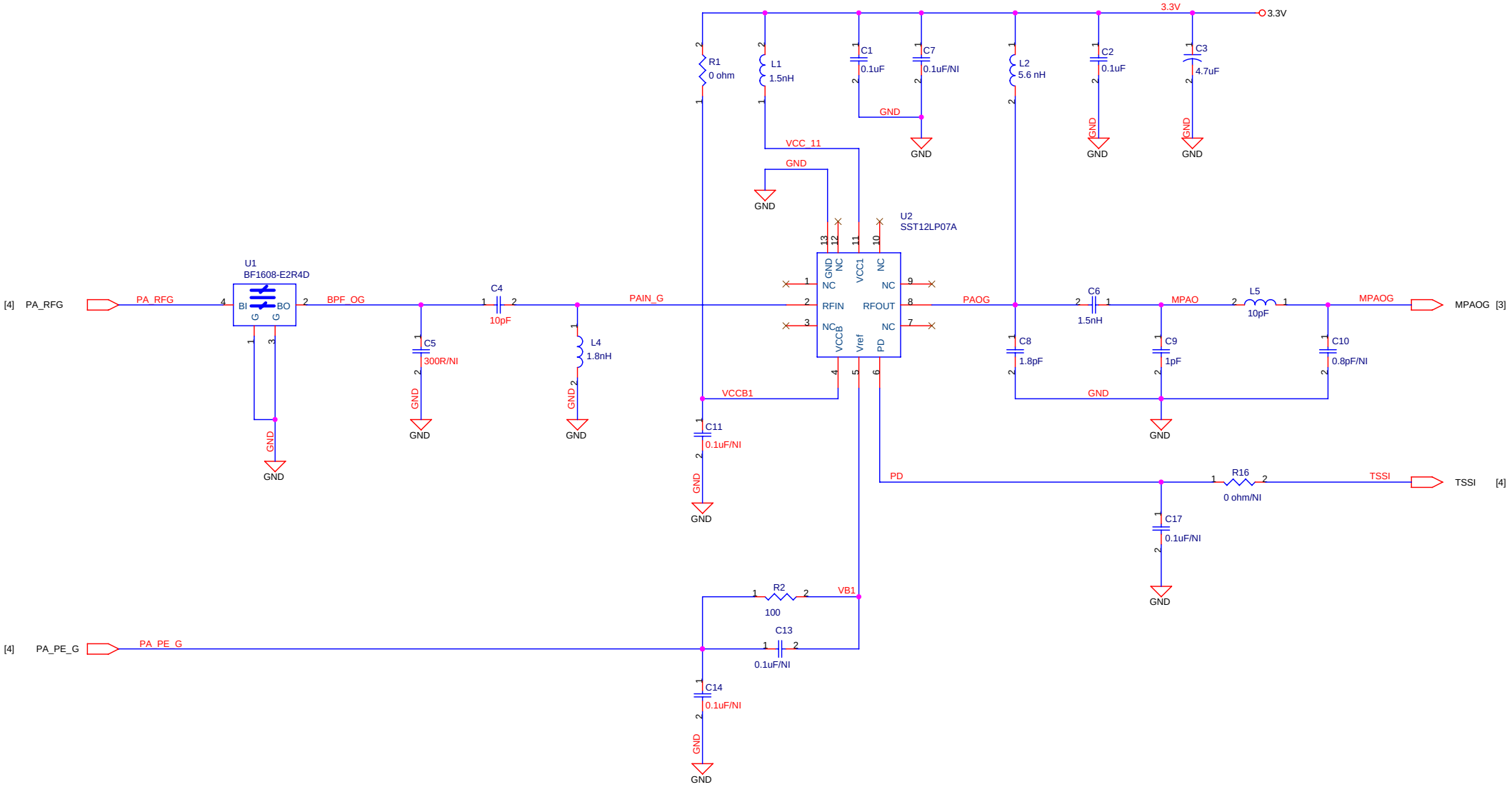




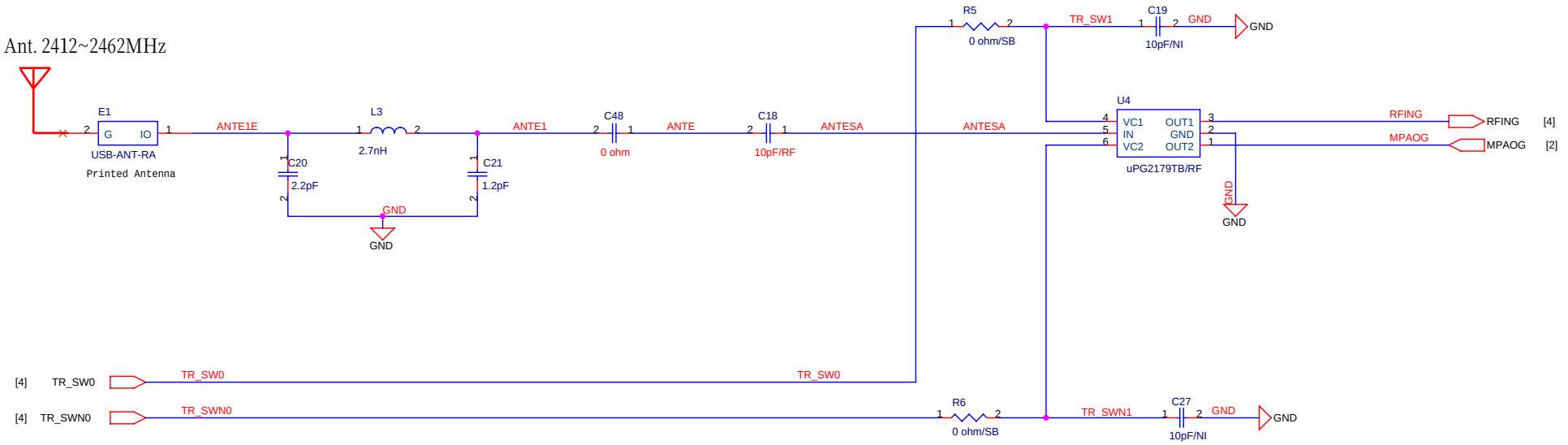


WonderMedia Technologies, Inc.

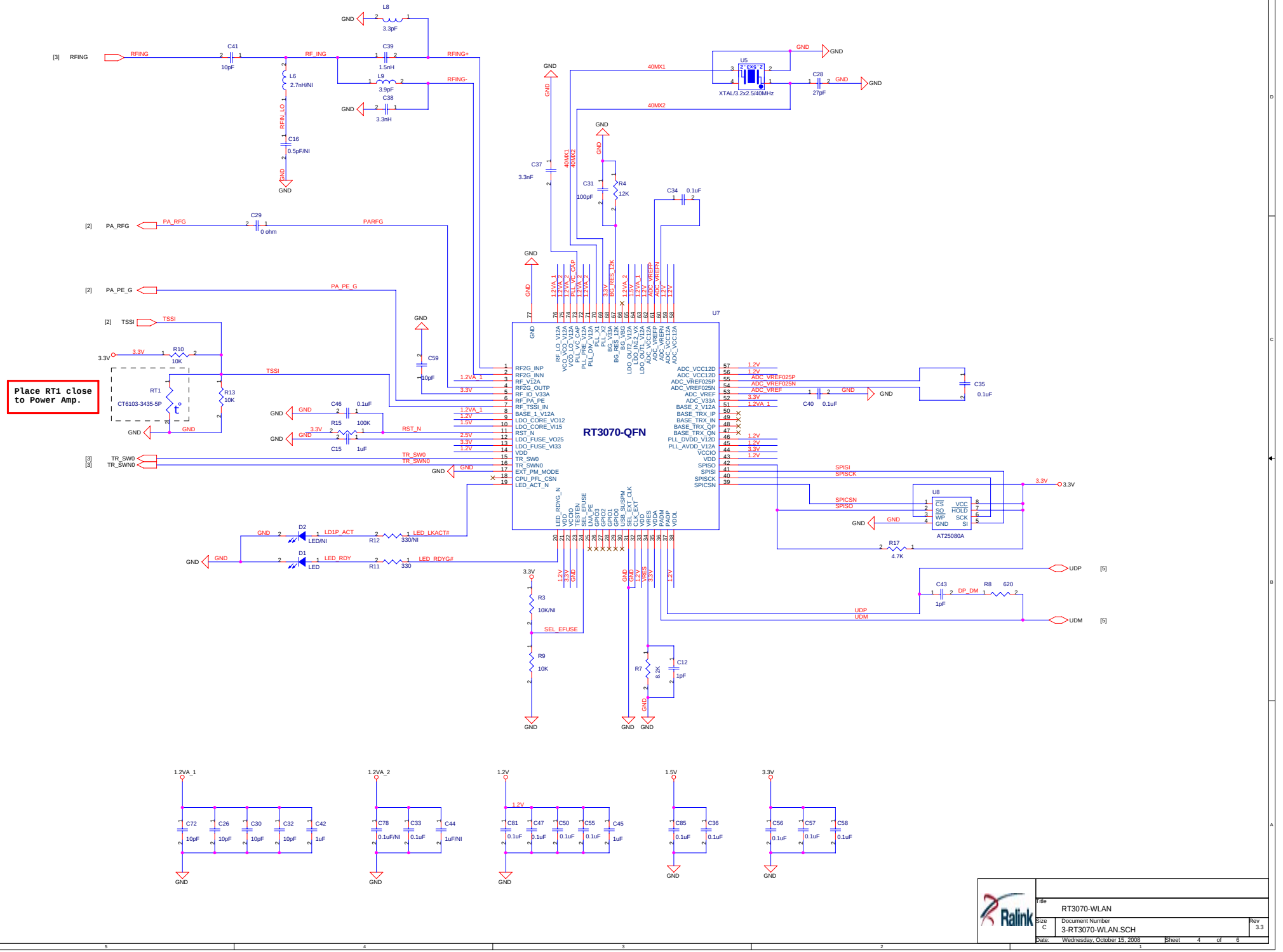
Title: Button and LED		
Size: C	Document Number: WMS8055B	Rev: 1.0
Date: Monday, December 14, 2009	Sheet 1 of 1	



Title	2.4GHz PA	
Size B	Document Number 1-PA-SST12LP07A.SCH	Rev 3.3
Date: Wednesday, October 15, 2008	Sheet 2 of 6	



Title	Front-End	
Size B	Document Number 2-FrontEnd.SCH	Rev 3.3
Date: Wednesday, October 15, 2008	Sheet 3 of 6	


RT3070-QFN
Place RT1 close to Power Amp.
U5
XTAL/3.2x2.5/40MHz
U7
U8
AT25080A
D1
LED
D2
LED/NI
CT6103-3435-5P
RT1
L8
3.3pF
L6
2.7nH/NI
L9
3.9pF
C38
3.3nH
C41
10pF
C39
1.5nH
C16
0.5pF/NI
C37
3.3nF
C31
100pF
R4
12K
C34
0.1uF
C28
27pF
C29
0 ohm
C59
10pF
C46
0.1uF
R15
100K
C15
1uF
R10
10K
R13
10K
C40
0.1uF
C35
0.1uF
R3
10K/NI
R9
10K
R7
8.2K
C12
1pF
R17
4.7K
C43
1pF
R8
620
R11
330
R12
330/NI
C72
10pF
C26
10pF
C30
10pF
C32
10pF
C42
1uF
C78
0.1uF/NI
C33
0.1uF
C44
1uF/NI
C81
0.1uF
C47
0.1uF
C50
0.1uF
C55
0.1uF
C45
1uF
C85
0.1uF
C36
0.1uF
C56
0.1uF
C57
0.1uF
C58
0.1uF
RFING
RF_ING
RFING+
RFING-
RFIN_LO
PA_RFG
PARFG
PA_PE_G
TSSI
RST_N
TR_SW0
TR_SWN0
LED_RDY
LED_RDY#
LD1P_ACT
LED_LKACT#
SEL_EFUSE
40MX1
40MX2
ADC_VREFP
ADC_VREFN
ADC_VREF
ADC_VREF025P
ADC_VREF025N
SPISI
SPISCK
SPICSN
SPISO
UDP
UDM
DP_DM
BS_RES_12K
GND
3.3V
1.2V
1.5V
2.5V
1.2VA_1
1.2VA_2
RF2G_INP
RF2G_INN
RF_V12A
RF2G_OUTP
RF_IO_V33A
RF_PA_PE
RF_TSSI_IN
BASE_1_V12A
LDO_CORE_VO12
LDO_CORE_VI15
RST_N
LDO_FUSE_VO25
LDO_FUSE_VI33
VDD
TR_SW0
TR_SWN0
EXT_PM_MODE
CPU_PFL_CSN
LED_ACT_N
ADC_VCC12D
ADC_VCC12D
ADC_VREF025P
ADC_VREF025N
ADC_VREF
ADC_V33A
BASE_2_V12A
BASE_TRX_IP
BASE_TRX_IN
BASE_TRX_QP
BASE_TRX_QN
PLL_DVDD_V12D
PLL_AVDD_V12A
VCCIO
VDD
SPISO
SPISI
SPISCK
SPICSN
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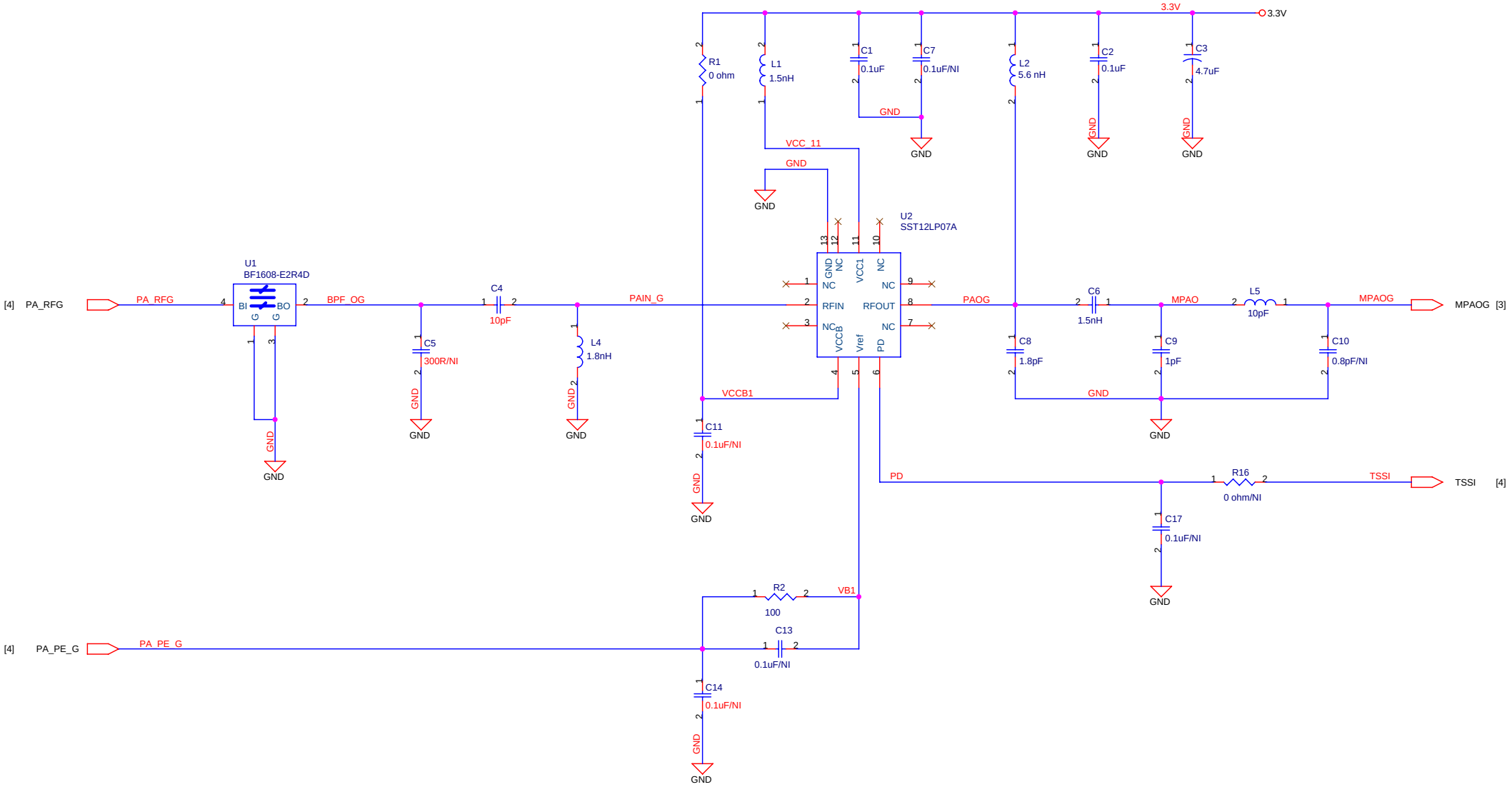

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