

# QLC200 User Manual

## Contents

Contents .....	1
Table Index.....	2
Figure Index .....	3
0. Revision History .....	4
1. Introduction.....	5
2. Product Concept.....	6
3. Placement.....	8
3.1 Pin Assignment.....	8
3.2 Placement recommendation .....	18
3.3 Placement clearance .....	19
4. Digital I/O Connection.....	20
5. Serial Interface and Debug Interface.....	21
6. SIM Card.....	22
7. SLEEP Mode.....	23
8. RF Design Guide .....	24
8.1 Recommended Impedance Matching Circuit .....	24
8.2 Matched RF Transmission Line Design .....	25
8.3 PCB Layout Consideration.....	26

## Table Index

TABLE 1: DIGITAL I/O ELECTRICAL CHARACTERISTICS.....	20
--	----

Queclink  
Confidential

## Figure Index

FIGURE 1: PIN ASSIGNMENT .....	<a href="#"><u>9</u></a>
FIGURE 3: PLACEMENT CLEARANCE .....	<a href="#"><u>19</u></a>
FIGURE 4: CIRCUIT OF THE SIM CARD .....	<a href="#"><u>22</u></a>
FIGURE 5: $\Pi$ -TYPE MATCHING CIRCUIT .....	<a href="#"><u>24</u></a>
FIGURE 6: QLC200 RF_ANT PCB LAYOUT .....	<a href="#"><u>25</u></a>
FIGURE 7: REFERENCE PCB DESIGN IN A FOUR-LAYER PCB .....	<a href="#"><u>28</u></a>
FIGURE 8: STACK-UP OF THE FOUR -LAYER PCB .....	<a href="#"><u>29</u></a>

## 0. Revision History

Revision	Date	Author	Description of Change
1.00	2022-05-30	Jensen.mo Green.hu	Initial

## 1. Introduction

The QLC200 requires 3.6V to 4.2V power supply. It has a 26MHz crystal for clock counting and system working. This device is a multi-network standard LTE 4G module. Built-in rich network protocols, integration of a number of industry standard interfaces, and support a variety of driver and software functions. It can meet the frequency band coverage of different countries and regions. It has band LTE-FDD in Europe and GSM 850/900/1800/1900MHz.

With a tiny profile of 32.2mm x 29.5mm x 2.35 mm, the module can meet almost all the requirements for M2M applications, including Tracking and Tracing, Intelligent Instrument, Wireless POS, Security, Telematics, Remote Controlling, etc.

QLC200 is an SMD type module, which can be embedded in customer application through its 142-pin pads. It provides all hardware interfaces between the module and customer's host board..

## 2. Product Concept

The QLC200 is a Quad-band GSM/GPRS engine that works at frequency bands of LTE-FDD in Europe and GSM 850/1900/900/1800MHz.

The QLC200 is an SMD type module with 142-pin pads and a tiny profile of 32.2mm x 29.5mm x 2.35 mm, which can fit into almost all customers' applications. It provides all hardware interfaces between the module and customer' host board.

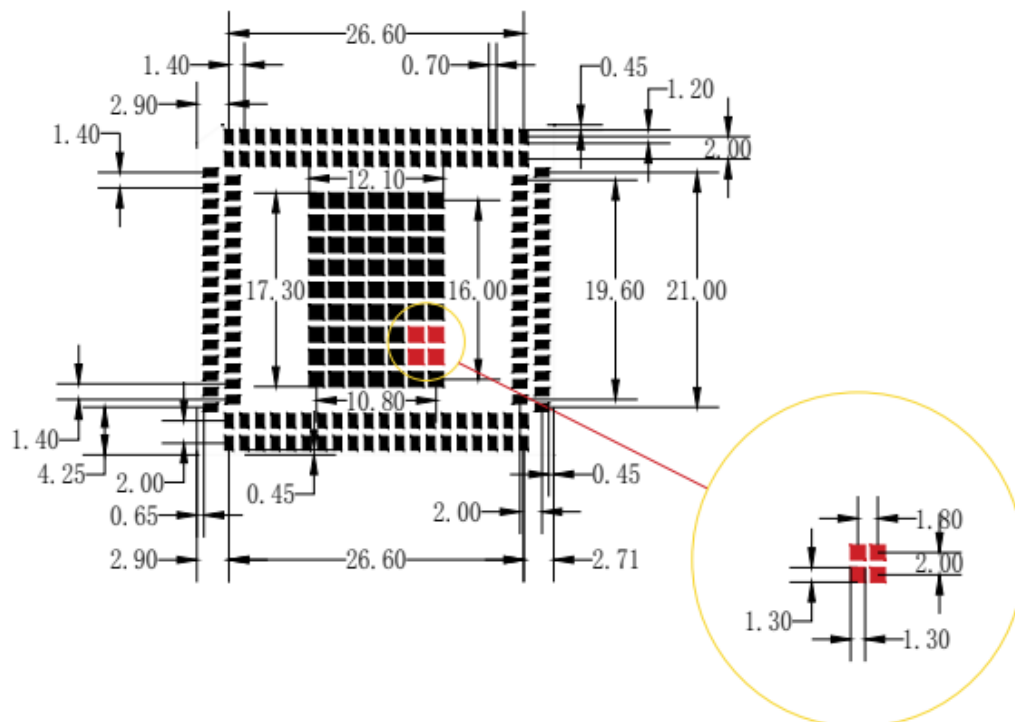
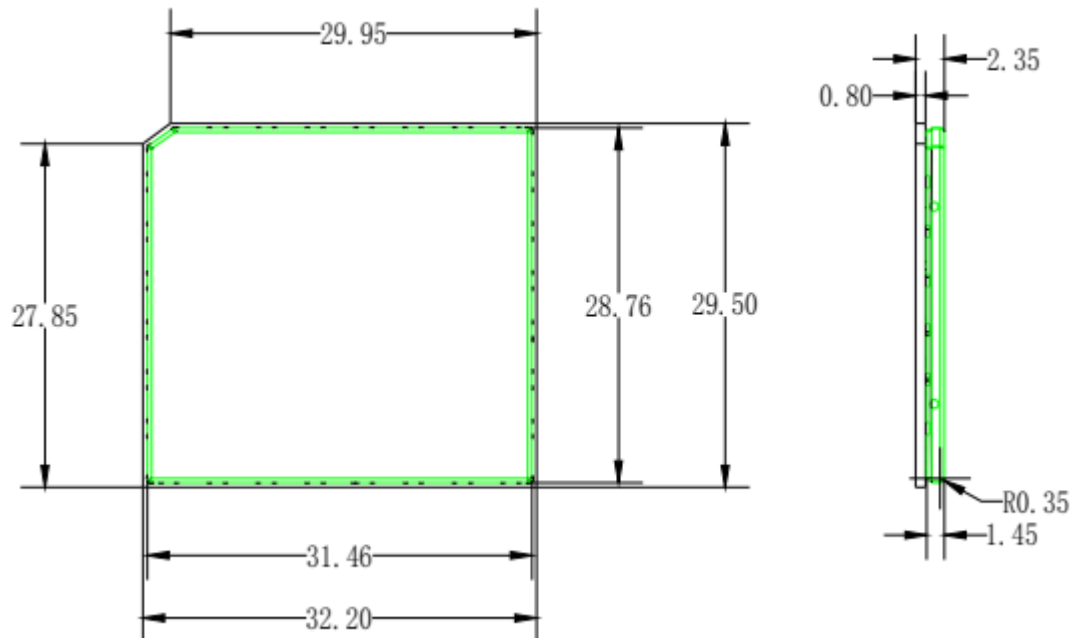
External controller can communicate with QLC200 through its main UART port.

The module is designed with power saving technique so that the current consumption could be very low.

TCP/IP protocol stack has been integrated in the module. Moreover, extended TCP/IP AT commands have been developed for customer to use the internal TCP/IP protocol easily, which is very useful for data transfer application.

The module is fully RoHS compliant to EU regulation.

## Mechanical dimensions of module





### 3. Placement

#### 3.1. Pin Assignment

**Please pay attention to the placement and the PCB layout in your application design.**

The pin assignment of the QLC200 module is shown in Figure 1. Placement of module should be carefully considered to make the RF pad as close as possible to antenna so as to reduce overall RF trace length. The longer the RF trace to antenna, the larger the RF insertion loss. In addition, please keep RF part and antenna from the system crystal and the audio part in host board as far as possible to reduce possible RF interference due to GSM transmission bursts from antenna and RF trace.

QLC200 module include the following major functional parts:

The GSM baseband part

The GSM radio frequency part

The SMT pads interface

—USB2.0 interface

—SIM card interface

—Audio interface

—I2C interface

—SPI interface

—PWM interface

—PCM interface

—ADC interface

—UART interface

—Power supply

—RF interface

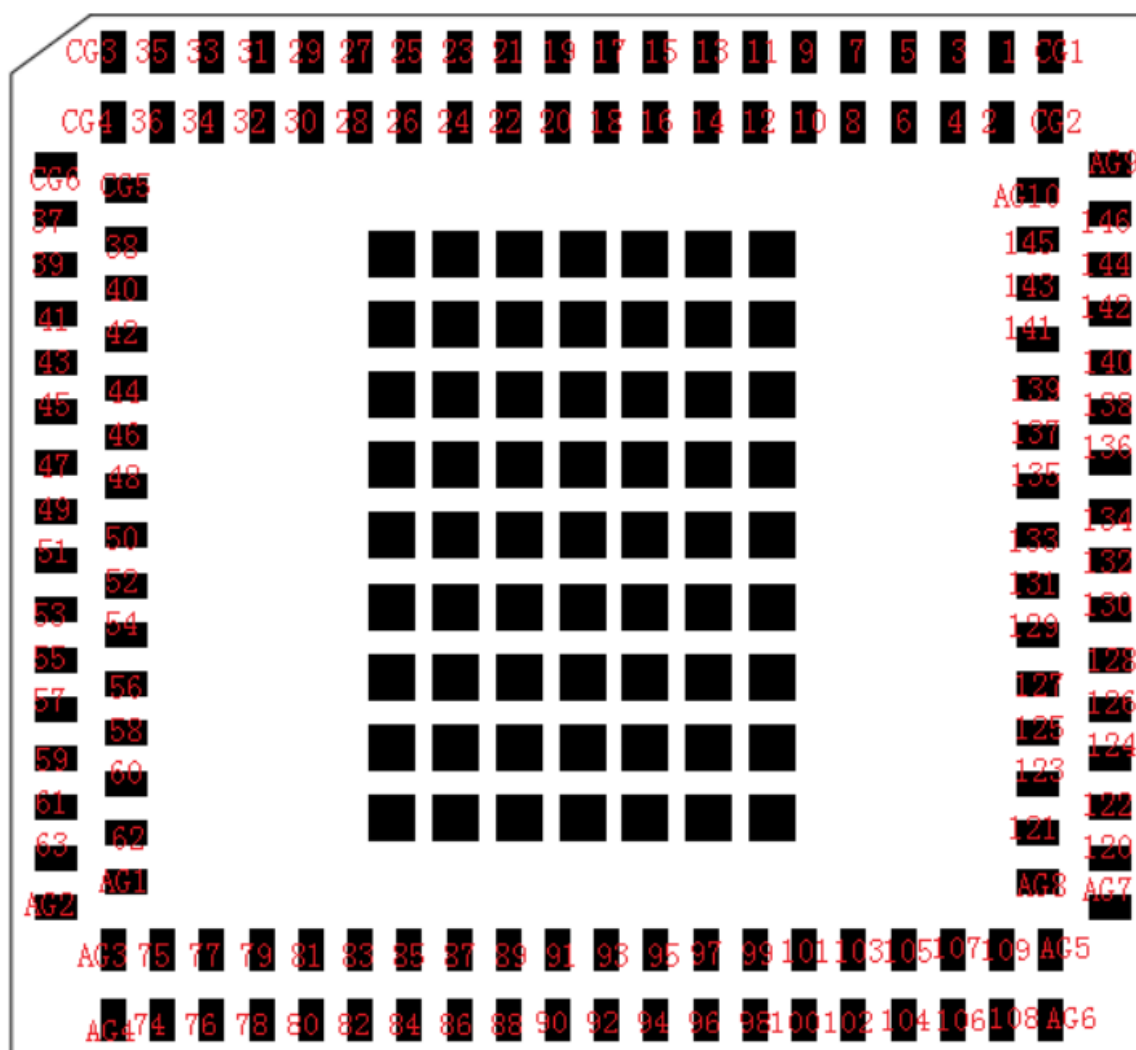


Figure 1: Pin assignment

PIN NO	PIN NAME	I/O		PIN NO	PIN NAME	I/O
1	ANT_CTRL2	0		31	PCM_RXD/SSPO_TXD/GPIO19	I/O
2	ANT_CTRL1	0		32	PCM_CLK/SSPO_CLK/GPIO16	I/O
3	LD01_2V8_RF	0		33	PWM1/PWM3/GPIO8	I/O
4	/			34	PWM1/GPIO31	I/O
5	GND			35	FORCE_USB_DOWNLOAD	I
6	GND			36	GND	
7	GND			37	SSP2_TXD/GPIO15	I/O
8	GND			38	SSP2_RXD/GPIO14	I/O
9	MAIN_ANT	0		39	SSP2_FRM/GPIO13	I/O
10	GND			40	SSP2_SCLK/GPIO12	I/O
11	GND			41	AP_UART1_TXD	0
12	GND			42	AP_UART1_RXD	I
13	UART3_RXD/GPIO53	I		43	GND	
14	UART3_TXD/GPIO54	0		44	USB_DN	I/O
15	CP_UART2_TXD/GPIO52	0		45	VBUS	I
16	CP_UART2_RXD/GPIO51	I		46	USB_DP	I/O
17	GPIO122	I/O		47	GND	
18	GPIO121	I/O		48	GND	
19	SSPO_TXD/SSP2_TXD/GPIO36	I/O		49	USIM_CLK	I/O
20	SSPO_RXD/SSP2_RXD/GPIO35	I/O		50	USIM_RST_N	I/O
21	SSPO_FRM/SSP2_FRM/GPIO34	I/O		51	USIM_DATA	I/O
22	SSPO_CLK/SSP2_CLK/GPIO33	I/O		52	LD03_3V0_USIM	0
23	SSP1_TXD/GPIO7	I/O		53	GND	
24	SSP1_RXD/GPIO6	I/O		54	GND	
25	SSP1_FRM/GPIO5	I/O		55	E_MIC2_P	0
26	SSP1_SCLK/GPIO4	I/O		56	E_MIC2_N	I
27	I2C2_SDA/GPIO11	I/O		57	DACL_P	0
28	I2C2_SCL/GPIO10	I/O		58	DACL_N	I
29	PCM_TXD/SSPO_RXD/GPIO18	I/O		59	GND	
30	PCM_SYNC/SSPO_FRM/GPIO17	I/O		60	GND	

PIN NO	PIN NAME	I/O		PIN NO	PIN NAME	I/O
61	VBUCK2_1V8	0		101	GND	
62	PWR_KEY	I		102	GND	
63	RESET_IN_N_DBG	I		103	GND	
74	VBAT_BB			104	GND	
75	VBAT_BB			105	GND	
76	VBAT_BB			106	GND	
77	VBAT_BB			107	GND	
78	GND			108	GND	
79	GND			109	GND	
80	GND			120	GND	
81	GPADC0	I		121	GND	
82	GPADC1	I		122	GND	
83	LDO4_3V0_SD	0		123	GND	
84	GPIO23	I/O		124	GND	
85	GPIO25/AP_I2C_4_SCL	I/O		125	GND	
86	GPIO26/AP_I2C_4_SDA	I/O		126	GND	
87	GPIO22	I/O		127	GND	
88	GPIO24	I/O		128	GND	
89	GPIO20	I/O		129	GND	
90	GPIO21	I/O		130	GND	
91	GPIO28	I/O		131	GND	
92	PWM2/GPIO32	I/O		132	GND	
93	GPIO2	I/O		133	GND	
94	GPIO124	I/O		134	GND	
95	UART4_TXD/GPIO1	I/O		135	GND	
96	GPIO27	I/O		136	GND	
97	UART4_RXD/GPIO0	I/O		137	GND	
98	GPIO3	I/O		138	GND	
99	CI2C_SCL/GPIO49	I/O		139	GND	
100	CI2C_SDA/GPIO50	I/O		140	GND	

PIN NO	PIN NAME	I/O
141	GND	
142	GND	
143	VBAT_RF	
144	VBAT_RF	
145	VBAT_RF	
146	VBAT_RF	
CG1	GND	
CG2	GND	
CG3	GND	
CG4	GND	
CG5	GND	
CG6	GND	
AG1	GND	
AG2	GND	
AG3	GND	
AG4	GND	
AG5	GND	
AG6	GND	
AG7	GND	
AG8	GND	
AG9	GND	
AG10	GND	

Ball #	Name	Type	Power Domain	Functional Description
A1	VSS	G		Digital Core ground
A2	QSPI_CS1	I/O, PU	1.8v/3.3v	QSPI flash Chip Select #1
A4	USIM2_UCLK	I/O, PU	1.8v/3.3v	USIM #2 UCLK
A6	GPIO_121	I/O, PU	1.8v	GPIO 121
A7	GPIO_53	I/O, PU	1.8v	GPIO 53
A9	GPIO_36	I/O, PU	1.8v	GPIO 36
A10	GPIO_30	I/O, PU	1.8v	GPIO 30
A12	GPIO_29	I/O, PU	1.8v	GPIO 29
A13	GPIO_26	I/O, PU	1.8v	GPIO 26
A15	GPIO_24	I/O, PD	1.8v	GPIO 24
A17	PSRAM_VDD	P	1.8v	PSRAM PHY power
A18	NC-A18			Not connected
B1	QSPI_DAT1	I/O, PD	1.8v/3.3v	QSPI flash DAT 1
B2	USIM_UCLK	I/O, PU	1.8v/3.3v	USIM #1 UCLK
B3	USIM2_URSTN	I/O, PU	1.8v/3.3v	USIM #2 RSTN
B4	USIM2_UIO	I/O, PU	1.8V/3.3v	USIM #2 UIO
B6	GPIO_122	I/O, PD	1.8v	GPIO 122
B7	GPIO_54	I/O, PU	1.8v	GPIO 54
B8	GPIO_51	I/O, PU	1.8v	GPIO 51
B9	GPIO_35	I/O, PU	1.8v	GPIO 35
B10	GPIO_31	I/O, PU	1.8v	GPIO 31
B11	GPIO_34	I/O, PU	1.8v	GPIO 34
B12	GPIO_28	I/O, PD	1.8v	GPIO 28
B13	GPIO_25	I/O, PU	1.8v	GPIO 25
B14	GPIO_23	I/O, PU	1.8v	GPIO 23
B16	PSRAM_VSS	G		PSRAM PHY ground
B17	PSRAM_VDD	P	1.8v	PSRAM PHY power
B18	PSRAM_VDD	P	1.8v	PSRAM PHY power
C3	QSPI_DAT2	I/O, PD	1.8v/3.3v	QSPI flash DAT 2
C4	GPIO_01	I/O, PD	1.8v	GPIO 01
C5	GPIO_124	I/O, PD	1.8v	GPIO 124
C6	GPIO_02	I/O, PD	1.8v	GPIO 02
C7	GPIO_52	I/O, PU	1.8v	GPIO 52
C9	GPIO_50	I/O, PU	1.8v	GPIO 50
C10	GPIO_49	I/O, PU	1.8v	GPIO 49
C12	GPIO_33	I/O, PU	1.8v	GPIO 33
C14	GPIO_21	I/O, PD	1.8v	GPIO 21
C15	GPIO_22	I/O, PD	1.8V	GPIO 22
D1	QSPI_DAT3	I/O, PD	1.8V/3.3v	QSPI flash DAT 3
D2	USIM_UIO	I/O, PU	1.8V/3.3v	USIM #1 UIO

D3	USIM_URSTN	I/O, PU	1.8v/3.3v	USIM #1 RSTN
D4	GPIO_00	I/O, PD	1.8v	GPIO 00
D5	GPIO_03	I/O, PD	1.8v	GPIO 03
D6	GPIO_64	I/O, PD	1.8v	GPIO 64
D9	QSPI_CS2	I/O, PD	1.8v	QSPI flash chip select #2
D10	GPIO_79	I/O, PU	1.8v	GPIO 79
D11	QSPI_DQM	I/O, PD	1.8v	QSPI flash DQM
D12	GPIO_32	I/O, PU	1.8v	GPIO 32
D13	GPIO_27	I/O, PD	1.8v	GPIO 27
D14	GPIO_20	I/O, PD	1.8v	GPIO 20
D18	GPIO_14	I/O, PD	1.8v	GPIO 14
E3	QSPI_CLK	I/O, PD	1.8V/3.3v	QSPI flash clock
E4	QSPI_VMODE	I/O PU	1.8v	QSPI 1.8v/3.3v I/O selection, 1 = 1.8v I/O, 0 = 3.3v I/O
E6	GPIO_65	I/O, PD	1.8v	GPIO 65
E8	GPIO_66	I/O, PD	1.8v	GPIO 66
E9	GPIO_63	I/O, PD	1.8v	GPIO 63
E16	PSRAM_VSS	G		PSRAM PHY ground
E18	GPIO_15	I/O, PD	1.8v	GPIO 15
F1	VCC18_QSPI	power	1.8v	QSPI LDO cap, connect to CAP
F2	QSPI_DAT0	I/O, PD	1.8V/3.3v	QSPI flash DAT 0
F3	MN_CLK_REQ	I/O, PD	1.8v	VCXO clock request
F5	MPLL_TST_AD	AIO	1.8v	Analog Test Point
F7	VCC18_USIM	P	1.8v	Connect to 1.8v power
F8	GPIO_62	I/O, PD	1.8v	GPIO 62
F10	GPIO_61	I/O, PD	1.8v	GPIO 61
F11	GPIO_80	I/O, PU	1.8v	GPIO 80
F12	AVSS09	G		Digital ground
F13	AVDD09_PSRAM	P	0.9v	PSRAM PHY digital power
F15	PSRAM_VSS	G		PSRAM PHY ground
F18	GPIO_12	I/O, PD	1.8v	GPIO 12
G1	VCXO_OUT	I/O, PD	1.8v	VCXO output
G2	DVC_1	I/O, PD	1.8v	PMIC DVC control bit 1
G4	AVDD18_USB2	P	1.8v	USB 1.8v power
G5	AVSS09_USB2	G		USB PHY digital ground
G7	VCC18_USIM2	P	1.8v	Connect to 1.8v power
G8	GPIO_60	I/O, PD	1.8v	GPIO 60
G10	VCC18_GPIO1	Power	1.8v	GPIO1 I/O domain power
G11	VSS	G		Digital core ground
G12	AVDD18_PSRAM	P	1.8V	PSRAM PHY analog power
G14	VQPS	P	1.8V	1.8v fuse programming power
G16	PSRAM_VSS	G		PSRAM PHY ground
G17	GPIO_13	I/O, PD	1.8v	GPIO 13
H2	DVC_0	I/O, PD	1.8V	PMIC DVC control bit 0
H3	AVSS_USB2	G		USB ground

H5	AVDD08_USB2	P	0.9v	USB PHY digital power
H7	VCC33_USIM	P	3.3v/1.8v	UIM 3.3v/1.8v power supply
H8	VCC_M1	P	0.9v	Digital Core power
H10	VSS	G		Digital core ground
H11	VSS	G		Digital core ground
H12	VCC18_TDS	P	1.8v	GPIO2_1 I/O domain 1.8v power
H16	VBUS_ON	I	1.8v	VBUS detection
J1	USB_P	AIO	1.8V	USB2 data P
J2	VCXO_REQ	I/O, PD	1.8v	VCXO request
J4	VCC33_QSPI	P	3.3v/1.8v	QSPI 3.3v/1.8v power supply
J5	AVDD33_USB2	P	3.3v	USB 3.3v power
J7	VCC33_USIM2	P	3.3v/1.8v	Usim2 3.3v/1.8v power supply
J8	VCC_M1	P	0.9v	Digital Core power
J10	VCC_M1	P	0.9v	Digital Core power
J11	VSS	G		Digital Core ground
J14	PMIC_INT	I	1.8V	PMIC interrupt (active low)
J15	PRI_TMS	I/O, PU	1.8v	Primary JTAG TMS
J17	GPIO_11	I/O, PU	1.8v	GPIO 11
J18	GPIO_06	I/O, PD	1.8v	GPIO 06
K1	USB_N	AIO	1.8V	USB2 data N
K2	GPIO_70	I/O, PD	1.8v	GPIO 70
K3	GPIO_08	I/O, PD	1.8v	GPIO08
K4	GPIO_09	I/O, UP	1.8v	GPIO 09
K10	VCC_M1	P	0.9v	Digital Core power
K11	VSS	G		Digital Core ground
K14	PRI_TCK	I/O, PD	1.8v	Primary JTAG TCK
K15	PRI_TRST_N	I	1.8V	Primary JTAG port reset_n
K16	PRI_TDI	I/O, PU	1.8v	Primary JTAG TDI input
K17	GPIO_10	I/O, PU	1.8v	GPIO 10
K18	GPIO_05	I/O, PD	1.8v	GPIO 05
L2	GPIO_69	I/O, PD	1.8v	GPIO 69
L3	GPIO_18	I/O, PD	1.8v	GPIO 18
L4	GPIO_19	I/O, PD	1.8v	GPIO 19
L6	BG_OUT	AO	0.6v	Analog bandgap voltage output
L7	VSS	G		Digital core ground
L8	VCC_M1	P	0.9v	Digital core power
L10	VCC18_PMIC1	P	1.8v	PMIC I/O domain power
L14	PRI_TDO	I/O, PU	1.8V	Primary JTAG TDO output
L15	VCXO_EN	O	1.8v	VCXO enable
L16	GPIO_07	I/O, PU	1.8v	GPIO 07
L17	GPIO_04	I/O, PD	1.8v	GPIO 04
M1	AUD_EARP_PAD	AO	1.8v	Receiver Positive output
M2	AUD_EARN_PAD	AO	1.8v	Receiver Negative output
M4	GPIO_17	I/O, PD	1.8v	GPIO 17



M5	GPIO_16	I/O, PD	1.8v	GPIO 16
M6	VCC18_TD2	P	1.8V	GPIO2_2 I/O 1.8v power
M7	AVDD18_PLLM	P	1.8v	PLL power
M17	PWR_SDA	I/O, PU	1.8v	PMIC I2C SDA
M18	PWR_SCL	I/O, PU	1.8v	PMIC I2C SCL
N1	AUD_MICP_PAD	AI	1.8V	Audio MIC Positive input
N2	AUD_MICN_PAD	AI	1.8V	Audio MIC Negative input
N3	AUD_REFGND_DAC	G		Audio DAC reference ground
N4	AUD_AVSS18	G	1.8V	Audio ground
N5	AUD_AVDD18	P	1.8V	Audio power
N6	AVDD09_PLLM	G	0.9v	PLL digital ground
N7	AVSS_PLLM	G		PLL analog ground
N12	PDET_RF_RIN	AI	1.8v	Power Detector input
N13	ALARM_WAKEUP	O	1.8v	Alarm wakeup output to PMIC in single crystals mode
N14	GND_TCXO	G		TCXO ground
N15	TCXO_IN	AIO	1.8v	TCXO crystal input
N17	EXT_32K_IN	I	1.8v	32K clock input
N18	RESET_IN_N	I	1.8v	SoC reset input
P2	AUD_AUREFGND	G		Audio reference ground
P3	AUD_AUREF10_PAD	AIO	1.8v	Audio reference
P4	AUD_MICBIAS_PAD	AIO	1.8v	Audio MICBIAS
P7	VSSU_PLLM	G		PLL analog ground
P11	VAPT	AIO	1.8v	APT voltage for RF PA
P12	GND_DNW_PDET	GND	1.8v	Power detector GND
P14	AFCDAC_OUT	AIO	1.8v	RF AFC DAC output
P15	OCLK1	AIO	1.8v	Reference clock buffer output #1
P16	OCLK2	AIO	1.8v	Reference clock buffer output #2
P17	AUXDAC	AIO	1.8v	Aux DAC output
P18	DCS_MODE	I	1.8V	Control single crystal mode or dual crystal mode
R2	MPLL_TST_CK	AIO	1.8v	PLL test point
R5	VDD18_RX_BB	P	1.8v	RF power supply
R6	GND_RX_BB	G		RF RX digital ground
R7	VDD18_PLLRX_LO	P	1.8v	RF RX PLL low band power
R9	GND_PLLRX_LO	G		RF PLL RX ground
R10	VDD18_PLLTX_LO	P	1.8v	RF power supply
R11	GND_PLLTX_LO	G		RF TX PLL ground
R12	GND_TXGUARD	G		RF TX ground
R13	GND_TX_ANA	G		RF TX Analog ground
R14	GND_RF_DIG	G		RF digital ground
R16	VDD18_TCXOIN	P	1.8v	TCXO input power
R17	VDDTCXO_OUT	P	1.8v	TCXO buffer power
R18	XTAL_IN	AIO	1.8v	DCXO crystal input
T1	RTN_AUXADCIN2	AIO	1.8v	Aux ADC input
T2	RTP_AUXADCIN1	AIO	1.8v	Aux ADC input

T5	VDD18_RX_LNA	P	1.8v	RF RX LNA power
T7	GND_LNA_MHB_ISL	G		RF MHB LNA ground
T14	GND_TXMHB	G		RF TX MHB ground
T15	VDD18_RF_DIG	P	1.8v	RF digital power
T18	XTAL_OUT	AIO	1.8v	DCXO crystal output
U3	LNA1_MHB	AIO	1.8v	RF MHB LNA1
U4	LNA5_MHB	AIO	1.8v	RF MHB LNA5
U5	GND_RX_LNA	G		RF RX LNA ground
U6	LNA6_MHB	AIO	1.8v	RF LNA6 MHB
U7	LNA8_LMB	AIO	1.8v	RF LNA8 MHB
U8	LNA10_LMB	AIO	1.8v	RF MHB LNA10
U9	GND_PLLRX	G		RF PLL RX ground
U10	VDD18_PLLTX	P	1.8v	RF power supply
U11	GND_PLLTX	G		RF TX PLL ground
U12	TXLB2	AIO	1.8v	RF TX Low band 2
U13	GND_TXLB	G		RF TX Low band ground
U15	TXMHB1	AIO	1.8v	RF TX MHB 1
U17	VDD18_TX_ANA	P	1.8v	RF power supply
U18	CLK_SEL	AIO	1.8v	CLK select for vcxo source
V1	NC-AA1			Not connected
V2	LNA2_MHB	AIO	1.8v	RF MHB LNA2
V3	LNA3_MHB	AIO	1.8v	RF LNA3 MHB
V4	LNA4_MHB	AIO	1.8v	RF MHB LNA4
V6	LNA7_LMB	AIO	1.8v	RF MHB LNA7
V8	LNA9_LMB	AIO	1.8v	RF LNA9 MHB
V9	VDD18_PLLRX	P	1.8v	RF RX PLL low band power
V11	TXLB1	AIO	1.8v	RF TX low band 1
V13	TXLB3	AIO	1.8v	RF Tx low band 3
V14	TXMHB3	AIO	1.8v	TX MH Band 3
V15	TXMHB2	AIO	1.8v	TX MH band 2
V18	NC-AA18			Not connected

### 3.2. Placement recommendation

The analog part components such as microphone should be placed far away from antenna and power supply. General placement recommendation is shown in Figure 2.

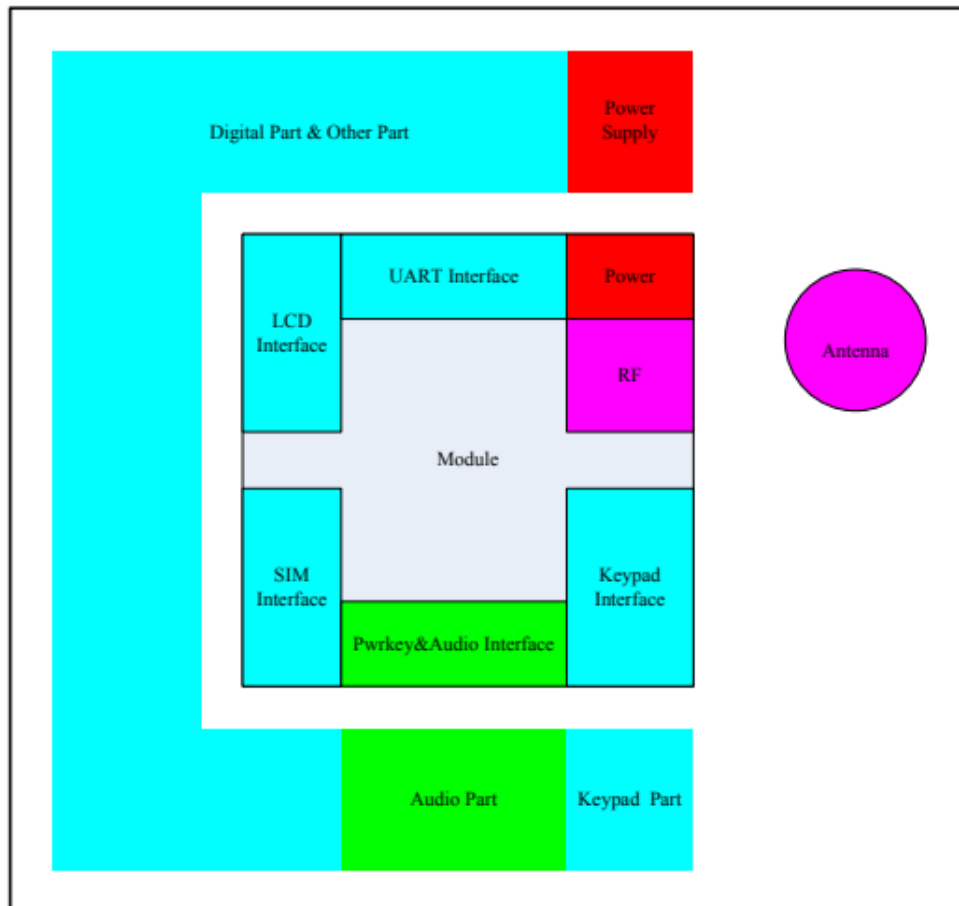


Figure 2: Recommendation of placement

### 3.3. Placement clearance

The module mounts with 142 SMT pads. For easy maintenance of this module and accessing to these pads, please keep a distance no less than 2mm between QLC200 and other components.

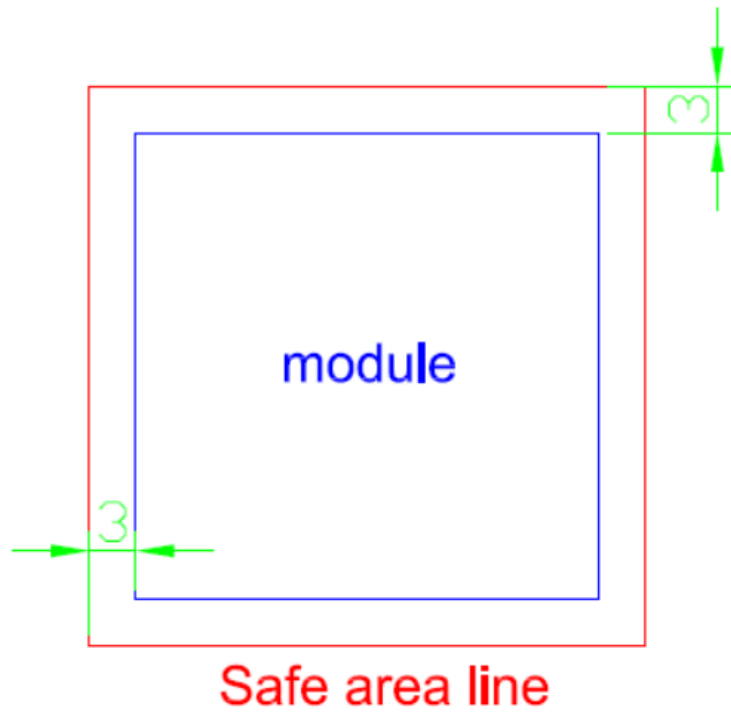


Figure 3: Placement clearance

## 4. Digital I/O Connection

If the voltage level of peripheral interface circuit does not match module interface, the power consumption of the system could increase, and could even cause the module damaged.

Each digital I/O of the module operates in a 1.8V logic level inside the module. The voltage level of those digital interfaces connected to the module should match the electrical characteristics of the module listed in Table 2. Otherwise, a level shifter circuit must be inserted between the host and the module.

**Table 1: Digital I/O electrical characteristics**

SYMBOL	MIN	MAX	UNITS
VIL	-0.4	$0.3V_{CC}$	V
VIH	$V_{CC} \times 0.7$	$V_{CC} + 0.4$	V
VOL		0.2V	V
VOH	$V_{CC} - 0.2V$		V

For direct connection between I/Os, please pay attention to I/Os' input or output configuration. If the I/O direction configuration conflicts with each other, the power consumption could increase, and the module could be very hot, and even be damaged. For example, it is forbidden that user's I/O outputs a low level while module's connected I/O outputs a high level.

## 5. Serial Interface and Debug Interface

The TXD, RXD, PWRKEY and GND pins can also be used for software upgrade and high-level acoustic parameters configuration. The DBG\_TXD and DBG\_RXD pins are only used for software debug. Please note that the PWRKEY pin should be pulled to low level when the QLC200 is being upgraded..Notes: It's recommended to connect the pins necessary for firmware upgrade to external interface.

## 6.SIM Card

As shown in Figure 4, connecting a large volume capacitor such as 10uF in the SIM\_VDD line could lead to failure of detecting the SIM card. A capacitor between 100nF and 1uF is recommended.

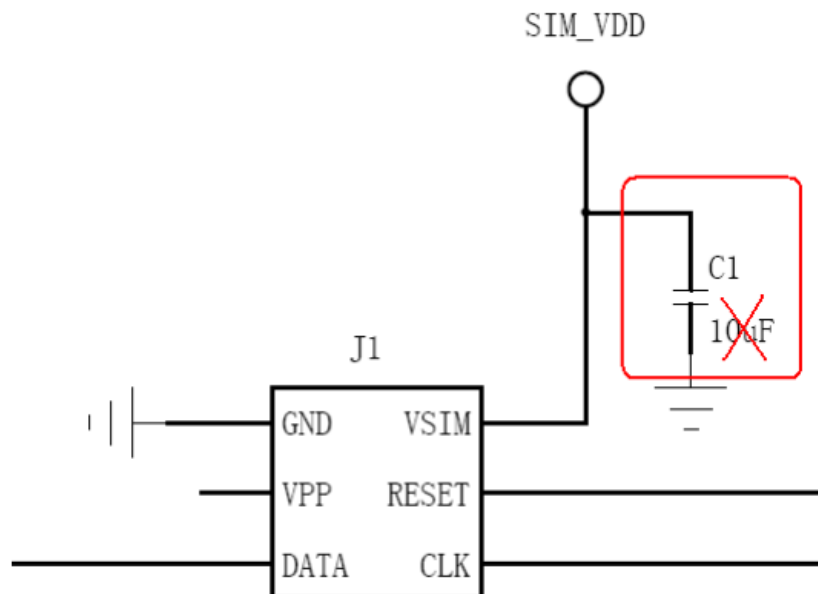


Figure 4: Circuit of the SIM card

## 7.SLEEP Mode

The command AT+ESLP can enable or disable SLEEP mode. When the SLEEP mode is enabled, It would drive the module into SLEEP mode; When the SLEEP mode is disabled the module would exit from SLEEP mode.



## 8.RF Design Guide

Correct RF design is essential for RF performance such as transmitting power, receiving sensitivity and harmonics. Following this RF design guide could benefit to improve the RF performance of customer's product.

### 8.1. Recommended Impedance Matching Circuit

The impedance of QLC200 RF\_ANT port is  $50\ \Omega$ . If the impedance of antenna is close to  $50\ \Omega$  in all working frequency bands, the antenna could be connected to the RF\_ANT port directly via  $50\ \Omega$  transmission line. But if the impedance of antenna is not close to  $50\ \Omega$ , a  $\pi$ -type matching circuit should be inserted between transmission line and antenna. The matching components should be placed as close as possible to the antenna's feed point.

Figure 1 shows the reference designs of  $\pi$ -type matching circuits.

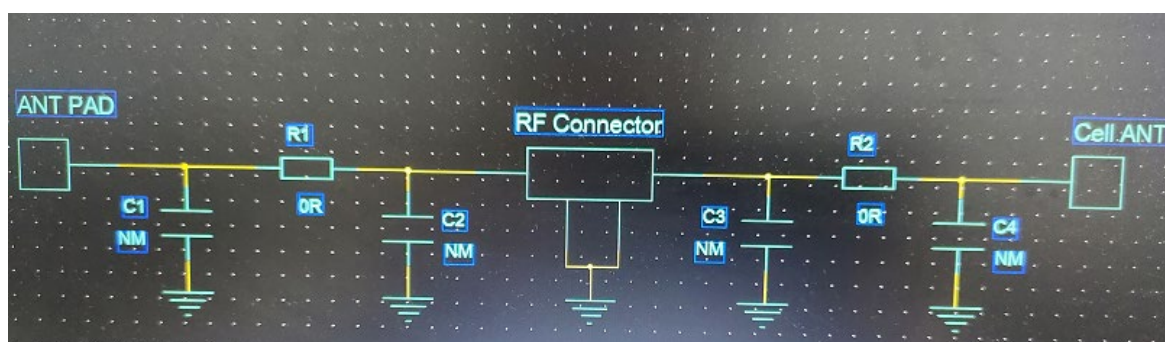


Figure 5:  $\pi$ -type matching circuit

NOTE: The impedance of traces in Bold type must be  $50\ \Omega$ .

## 8.2. Matched RF Transmission Line Design

In PCB layout, a matched RF transmission line has a fixed characteristic impedance, which is called  $Z_0$ , from its source to its load. The source should have an internal resistance of  $Z_0$  and the resistance of matching load should close to  $Z_0$ .

Since the impedance of QLC200 RF\_ANT port is  $50\ \Omega$ , the impedance of the RF transmission line from this port to the antenna or the matching circuit should also be made to  $50\ \Omega$ .

More than ten different types of transmission line can be created on a PCB simply by controlling trace geometry, and some of them are shown in Figure 2.

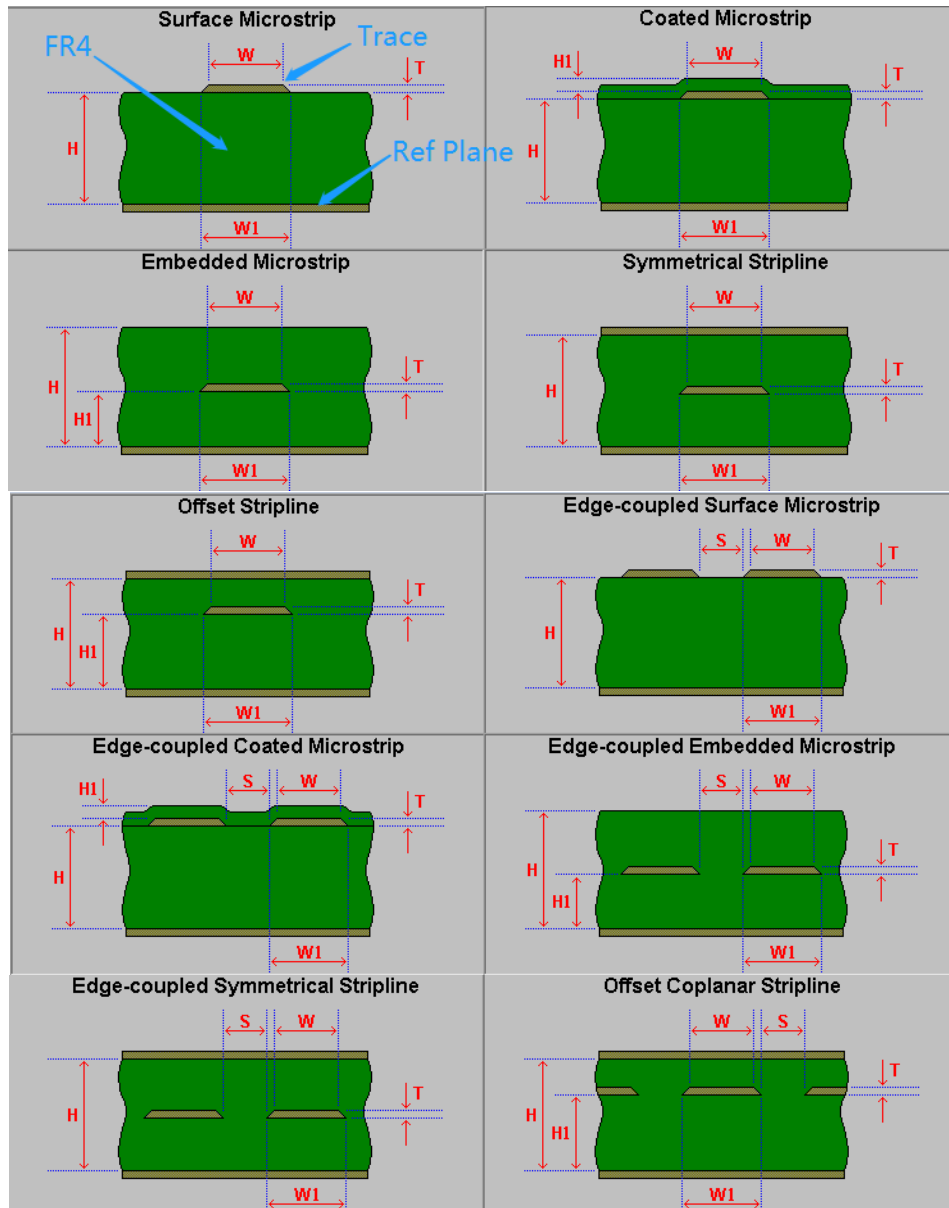


Figure 6: QLC200 RF\_ANT PCB layout

Customer may adopt one or certain types of them to design RF trace. Upon the demand of application design, the number of PCB layer can be different such as two and four. Each type of PCB has corresponding “stack-up”. The “stack-up” is the name given to the order of the various etched copper foil and dielectric layers that are laminated

together under pressure and heat to make a PCB.

### 8.3. PCB Layout Consideration

PCB Layout is essential to the performance of customer's product. Here are some rules that should be followed:

- Impedance control

Control the impedance of RF trace as close as possible to  $50\Omega$ . If the thickness between RF\_ANT pad and the ground layer is less than 0.4mm, it could significantly decrease the output power. Therefore, when they are too close, we strongly suggest removing the copper in the layer beneath the RF\_ANT pad. If RF trace routes to another layer, add GND via along with it to keep GND integral. The clearance between RF trace and ground plane in same layer should be twice the RF trace width.

- Make RF trace as short as possible

Place the module and the matching circuit near the antenna pad. Shorten the length of RF trace. Place the antenna PAD in the corner or at the edge of host board.

- Protect RF trace

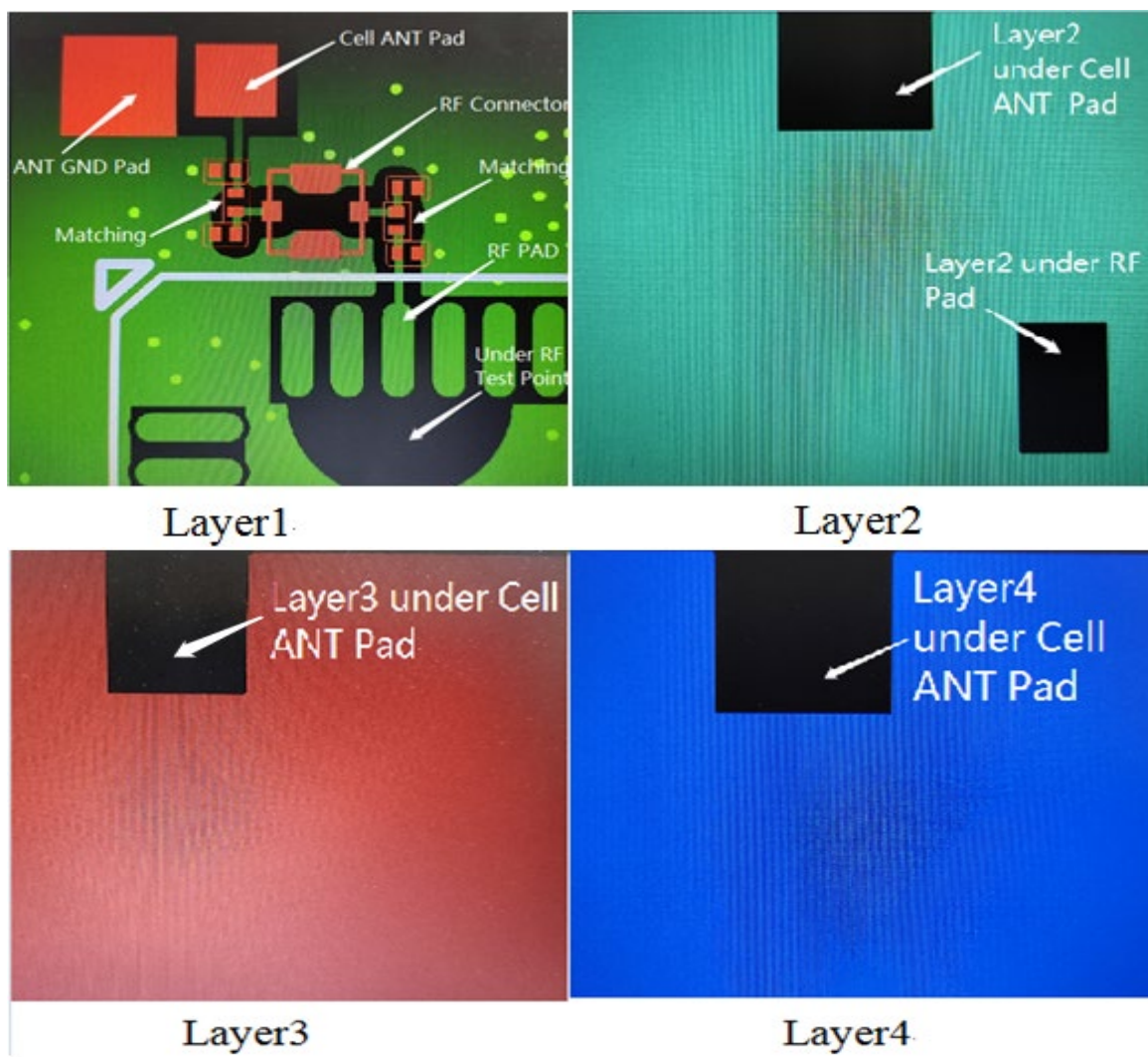
Avoid placing noise generating traces such as digital signal or clock line near RF trace in the same layer. Carefully route other traces in the layers adjacent to the RF trace, remember not to route in parallel with the RF trace. If possible, keep those traces far away from the RF trace.

- An RF test point is located at the bottom side of QLC200 for manufacture purpose.

The copper which is close to this test point in the top layer of customer's host board must be kept out or removed. No signal trace should be placed in the top layer and the second layer beneath this test point.

- Customer can use either antenna PAD or RF connector to connect the antenna.

If antenna PAD is adopted, Figure 3 is a reference design for a four-layer PCB. Make the space on all layers beneath antenna pad keep-out. Place a ground PAD near the antenna PAD. The distance between GND PAD and antenna PAD can be around 1.8mm. The size of antenna PAD can be 1.8mm\*1.8mm, and the GND PAD should be a little bigger, e.g. 2.5mm\*2.5mm. Add several GND via near or on the GND PAD to reduce impedance from the GND PAD to the RF reference ground.



If RF connector is adopted, place the RF connector close to module RF\_ANT, and add several GND via close to the GND PAD of RF connector. Figure 4 is the reference PCB design.

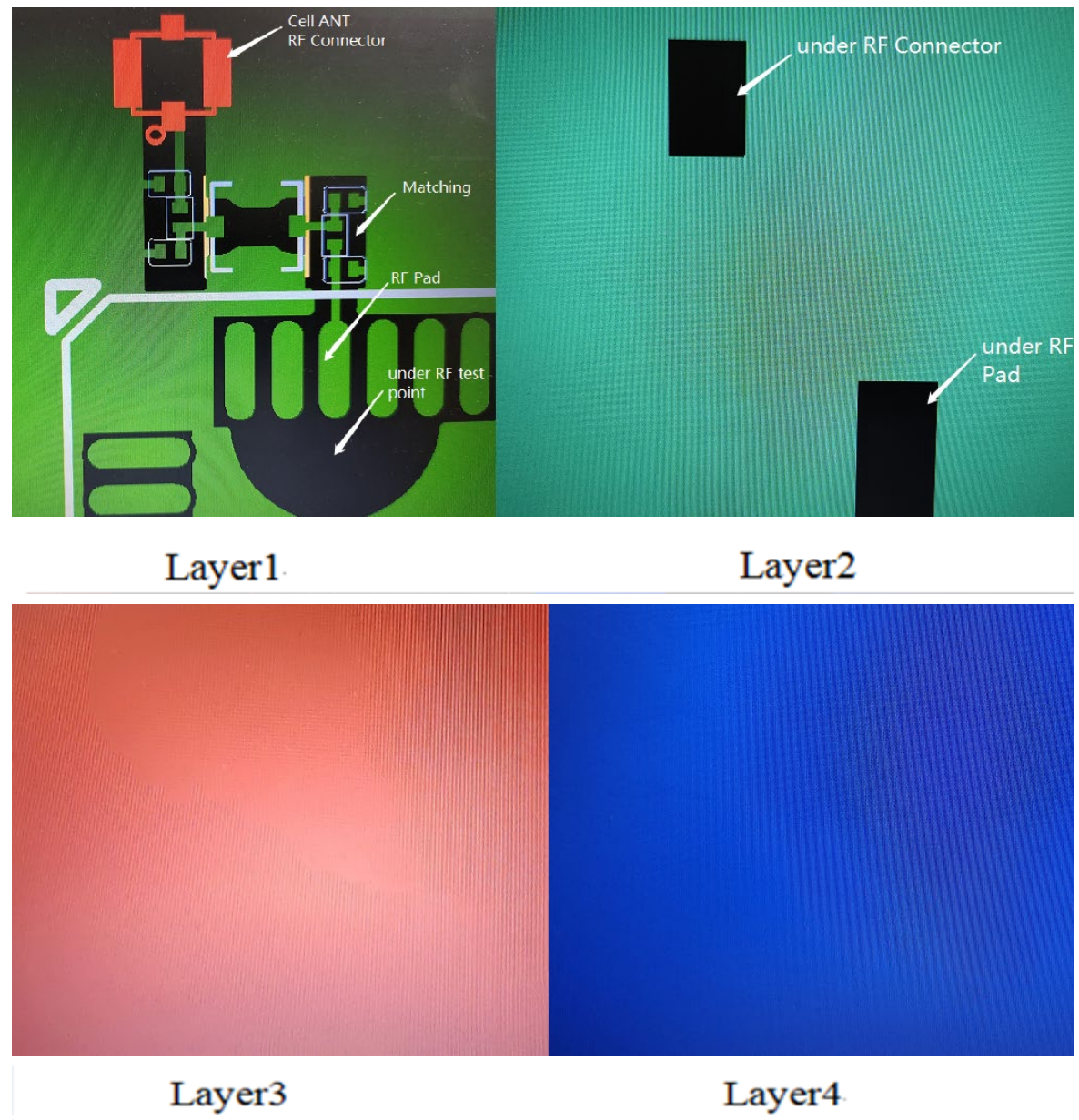


Figure 7: Reference PCB design with RF connector in a four-layer PCB



The stack-up of the four-layer PCB is shown in Figure 8.

### MATERIAL STACK-UP <sup>↕</sup>

	Solder Mask		18.0 $\mu\text{m}$ . <sup>↕</sup>
	Chemical Gold		0.05 $\mu\text{m}$ . <sup>↕</sup>
	Electroless Nickel		2.54 $\mu\text{m}$ . <sup>↕</sup>
	Copper Plating		13 $\mu\text{m}$ . <sup>↕</sup>
LAYER1	Copper		12.0 $\mu\text{m}$ . <sup>↕</sup>
	1080LDP		200.0 $\mu\text{m}$
			standard via 1-4. <sup>↕</sup>
LAYER2	Copper		18.0 $\mu\text{m}$ . <sup>↕</sup>
	Prepreg	2116	500 $\mu\text{m}$ . <sup>↕</sup>
LAYER3	Copper		18.0 $\mu\text{m}$ . <sup>↕</sup>
	1080LDP		200.0 $\mu\text{m}$ . <sup>↕</sup>
LAYER4	Copper		12.0 $\mu\text{m}$ . <sup>↕</sup>
	Copper Plating		13 $\mu\text{m}$ . <sup>↕</sup>
	Electroless Nickel		2.54 $\mu\text{m}$ . <sup>↕</sup>
	Chemical Gold		0.05 $\mu\text{m}$ . <sup>↕</sup>
	Solder Mask		18.0 $\mu\text{m}$ . <sup>↕</sup>

**TOTAL OVERALL THICKNESS**      **1.0  $\pm$  0.1 mm<sup>↕</sup>**

Figure 8: Stack-up of the four -layer PCB

Operating Temperature:-30°C ~ +70°C

RF exposure *statement*

*RF exposure information:* The Maximum Permissible Exposure (MPE) level has been calculated based on a distance of d=20 cm between the device and the human body. To maintain compliance with RF exposure requirement, use product that maintain a 20cm distance between the device and human body.

GSM900: 33.34 dBm

GSM1800: 30.61 dBm

Band 1: 24.63 dBm

Band 3: 24.12 dBm

Band 7: 25.59 dBm

Band 8: 22.55 dBm

Band 20: 23.96 dBm

Band 28: 22.03 dBm

Hereby, Queclink Wireless Solutions Co., Ltd. declares that the radio equipment it is in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity is available at the following internet address:

<http://www.queclink.com/>

---

## **FCC MODULAR APPROVAL INFORMATION EXAMPLES for Manual**

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference.
- (2) This device must accept any interference received, including interference that may cause undesired operation.

**CAUTION:** Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**NOTE:** This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

### **FCC Radiation Exposure Statement:**

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.



---

## **OEM INTEGRATION INSTRUCTIONS:**

This device is intended only for OEM integrators under the following conditions:

The module must be installed in the host equipment such that 20 cm is maintained between the antenna and users, and the transmitter module may not be co-located with any other transmitter or antenna. The module shall be only used with the internal on-board antenna that has been originally tested and certified with this module. External antennas are not supported. As long as these 3 conditions above are met, further transmitter test will not be required.

However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.). The end-product may need Verification testing, Declaration of Conformity testing, a Permissive Class II Change or new Certification. Please involve a FCC certification specialist in order to determine what will be exactly applicable for the end-product.

### **Validity of using the module certification:**

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization. In such cases, please involve a FCC certification specialist in order to determine if a Permissive Class II Change or new Certification is required.

### **Upgrade Firmware:**

The software provided for firmware upgrade will not be capable to affect any RF parameters as certified for the FCC for this module, in order to prevent compliance issues.

### **End product labeling:**

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains FCC ID: YQD-QLC200".

### **Information that must be placed in the end user manual:**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

---

## **FCC MODULAR APPROVAL INFORMATION EXAMPLES for Manual**

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference.
- (2) This device must accept any interference received, including interference that may cause undesired operation.

**CAUTION:** Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

## **WARNING**

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

“CAUTION : Exposure to Radio Frequency Radiation.

Antenna shall be mounted in such a manner to minimize the potential for human contact during normal operation. The antenna should not be contacted during operation to avoid the possibility of exceeding the FCC radio frequency exposure limit.

## Requirement per KDB996369 D03

### 2.2 List of applicable FCC rules

List the FCC rules that are applicable to the modular transmitter. These are the rules that specifically establish the bands of operation, the power, spurious emissions, and operating fundamental frequencies. DO NOT list compliance to unintentional-radiator rules (Part 15 Subpart B) since that is not a condition of a module grant that is extended to a host manufacturer. See also Section 2.10 below concerning the need to notify host manufacturers that further testing is required.<sup>3</sup>

**Explanation: This module meets the requirements of FCC FCC 47 CFR Title47 Part22 SubpartH CFR Title47 Part24 SubpartE CFR Title47 CFR Part 27 CFR Title47 Part15 SubpartB 47 CFR Part 2**

### 2.3 Summarize the specific operational use conditions

Describe use conditions that are applicable to the modular transmitter, including for example any limits on antennas, etc. For example, if point-to-point antennas are used that require reduction in power or compensation for cable loss, then this information must be in the instructions. If the use condition limitations extend to professional users, then instructions must state that this information also extends to the host manufacturer's instruction manual. In addition, certain information may also be needed, such as peak gain per frequency band and minimum gain, specifically for master devices in 5 GHz DFS bands.

**Explanation: The EUT has a PIFA Antenna, and the antenna use a permanently attached antenna which is not replaceable.**

### 2.4 Limited module procedures

If a modular transmitter is approved as a "limited module," then the module manufacturer is responsible for approving the host environment that the limited module is used with. The manufacturer of a limited module must describe, both in the filing and in the installation instructions, the alternative means that the limited module manufacturer uses to verify that the host meets the necessary requirements to satisfy the module limiting conditions.

A limited module manufacturer has the flexibility to define its alternative method to address the conditions that limit the initial approval, such as: shielding, minimum signaling amplitude, buffered modulation/data inputs, or power supply regulation. The alternative method could include that the limited module manufacturer reviews detailed test data or host designs prior to giving the host manufacturer approval. This limited module procedure is also applicable for RF exposure evaluation when it is necessary to demonstrate compliance in a specific host. The module manufacturer must state how control of the product into which the modular transmitter will be installed will be maintained such that full compliance of the product is always ensured. For additional hosts other than the specific host originally granted with a limited module, a Class II permissive change is required on the module grant to register the additional host as a specific host also approved with the module.

**Explanation: The module is not a limited module.**

### 2.5 Trace antenna designs

For a modular transmitter with trace antenna designs, see the guidance in Question 11 of KDB Publication 996369 D02 FAQ – Modules for Micro-Strip Antennas and traces. The integration information shall include for the TCB review the integration instructions for the following aspects: layout of trace design, parts list (BOM), antenna, connectors, and isolation requirements.

- a) Information that includes permitted variances (e.g., trace boundary limits, thickness, length, width, shape(s), dielectric constant, and impedance as applicable for each type of antenna);
- b) Each design shall be considered a different type (e.g., antenna length in multiple(s) of frequency, the wavelength, and antenna shape (traces in phase) can affect antenna gain and must be considered);
- c) The parameters shall be provided in a manner permitting host manufacturers to design the printed circuit (PC) board layout;
- d) Appropriate parts by manufacturer and specifications;
- e) Test procedures for design verification; and
- f) Production test procedures for ensuring compliance.

The module grantee shall provide a notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify the module grantee that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

**Explanation: Yes, The module with trace antenna designs, refer to the RF Link schematic diagram and refer to PCB Layout.**

## 2.6 RF exposure considerations

It is essential for module grantees to clearly and explicitly state the RF exposure conditions that permit a host product manufacturer to use the module. Two types of instructions are required for RF exposure information:

- (1) to the host product manufacturer, to define the application conditions (mobile, portable – xx cm from a person’s body); and (2) additional text needed for the host product manufacturer to provide to end users in their end-product manuals. If RF exposure statements and use conditions are not provided, then the host product manufacturer is required to take responsibility of the module through a change in FCC ID (new application).

**Explanation: This module complies with FCC RF radiation exposure limits set forth for an uncontrolled environment, This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body." This module is designed to comply with the FCC statement, FCC ID is: YQD-QLC200.**

## 2.7 Antennas

A list of antennas included in the application for certification must be provided in the instructions. For modular transmitters approved as limited modules, all applicable professional installer instructions must be included as part of the information to the host product manufacturer. The antenna list shall also identify the antenna types (monopole, PIFA, dipole, etc. (note that for example an “omni-directional antenna” is not considered to be a specific “antenna type”)). For situations where the host product manufacturer is responsible for an external connector, for example with an RF pin and antenna trace design, the integration instructions shall inform the installer that unique antenna connector must be used on the Part 15 authorized transmitters used in the host product. The module manufacturers shall provide a list of acceptable unique connectors.

**Explanation: The EUT has a PIFA Antenna, and the antenna use a permanently attached antenna which is unique.**max antenna gain as list:

Antenna Type	Manufacturer	Frequency(MHz)	Gain (dBi)
PIFA Antenna	WaveLink	824 ~ 849 MHz	-0.65
		1850 ~ 1910 MHz	1
		1850 ~ 1910 MHz	3.03
		1710 ~ 1755 MHz	1.47
		824 ~ 849 MHz	-0.65
		2500 ~ 2570 MHz	3.86

## 2.8 Label and compliance information

Grantees are responsible for the continued compliance of their modules to the FCC rules. This includes advising host product manufacturers that they need to provide a physical or e-label stating “Contains FCC ID” with their finished product. See Guidelines for Labeling and User Information for RF Devices – KDB Publication 784748.

**Explanation: The host system using this module, should have label in a visible area indicated the following texts: “Contains FCC ID: YQD-QLC200”**

## 2.9 Information on test modes and additional testing requirements<sup>5</sup>

Additional guidance for testing host products is given in KDB Publication 996369 D04 Module Integration Guide. Test modes should take into consideration different operational conditions for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product. The grantee should provide information on how to configure test modes for host product evaluation for different operational conditions for a stand-alone modular transmitter in a host, versus with multiple, simultaneously transmitting modules or other transmitters in a host. Grantees can increase the utility of their modular transmitters by providing special means, modes, or instructions that simulates or characterizes a connection by enabling a transmitter. This can greatly simplify a host manufacturer’s determination that a module as installed in a host complies with FCC requirements.

**Explanation: Top band can increase the utility of our modular transmitters by providing instructions that simulates or characterizes a connection by enabling a transmitter.**

## 2.10 Additional testing, Part 15 Subpart B disclaimer

The grantee should include a statement that the modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

**Explanation: The module without unintentional-radiator digital circuitry, so the module does not require an evaluation by FCC Part 15 Subpart B. The host should be evaluated by the FCC Subpart B.**

