GS2101M Low Power WiFi Module

Data Sheet

GS2101M-DS-001270

GainSpan® 802.11b/g/n Low Power WiFi® Series Modules

Release 1.0, 05/19/2016

FCC Communications Commission (FCC) Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate frequency energy and, if not installed and used in accordance with the instructions may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

FCC Caution: To assure continued compliance, (example - use only shielded interface cables when connecting to computer or peripheral devices). Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC & IC Radiation Exposure Statement

This equipment complies with FCC & IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. This device intended only for OEM integrators under the following conditions:

1. The antenna must be installed such that 20cm is maintained between the antenna and users, and
2. The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE: In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC & IC authorizations are no longer considered valid and the FCC & IC IDs cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining separate FCC & IC authorizations.

End Product Labeling: This transmitter module is authorized only for use in device where the antenna may be installed such that 20cm may be maintained between the antenna and users (for example access points, routers, wireless ADSL modems, and similar equipment). the final product must be labeled in a visible area with the corresponding FCC ID number.

IC Certification - Canada

The labeling requirements for Industry Canada are similar to those of the FCC. A visible label on the outside of the final product must display the IC labeling. The user is responsible for the end product to comply with IC ICES-003 (Unintentional radiators).

English

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:

1. This device may not cause harmful interference
2. This device must accept any interference received, including received, including interference that may cause undesired operation of the device.

French

Cet appareil est conforme à Industrie Canada une licence standard RSS exonérés (s). Son fonctionnement est soumis aux deux conditions suivantes:

1. Cet appareil ne doit pas provoquer d'interférences
2. Cet appareil doit accepter toute interférence reçue, y compris les interférences pouvant provoquer un fonctionnement indésirable de l'appareil.

Manual Information That Must be Included

The user's manual for end users must include the following information in a prominent location.

IMPORTANT NOTE: To comply with FCC & IC RF exposure compliance requirements, the antenna used for this transmitter must be installed to provide a separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

Additional Notations: GainSpan modules have been built or under development for near body exposure applications. The 20cm statement is a standard note because absorption rate testing (commonly knowns as SAR or Specific absorption rate) is not modularly transferable for FCC/IC. Thus, if a radio is being used against the body, the end user is still responsible to test for regulatory near body exposure testing (for USA, please refer to the following):

- FCC Part 1.1037
- FCC Part 2.1091 Mobile Devices
- FCC Part 2.1093 Portable Devices
- FCC Part 15.247 (b) (4)

Table of Contents

About This Manual

This manual describes the GS2101M Low Power module hardware specification.

Refer to the following sections:

Revision History

This version of the *GainSpan GS2101M Low Power WiFi Data Sheet* contains the following new information listed in Table 1, page 8.

Table 1 Revision History

Version	Date	Remarks
1.0	May 2016	Initial release.

Audience

This manual is designed to help system designers build low power, cost effective, flexible platforms to add WiFi connectivity for embedded device applications using the GainSpan GS2101M based module.

Standards

The standards that are supported by the GainSpan modules are IEEE 802.11b/g/n.

Documentation Conventions

This manual uses the following text and syntax conventions:

- Special text fonts represent particular commands, keywords, variables, or window sessions
- Color text indicates cross-reference hyper links to supplemental information
- Command notation indicates commands, subcommands, or command elements

Table 2, page 9, describes the text conventions used in this manual for software procedures that are explained using the AT command line interface.

Table 2 Document Text Conventions

Convention Type	Description
command syntax monospaced font	This monospaced font represents command strings entered on a command line and sample source code. `AT XXXX`
Proportional font description	Gives specific details about a parameter. `<Data> DATA`
UPPERCASE Variable parameter	Indicates user input. Enter a value according to the descriptions that follow. Each uppercased token expands into one or more other token.
lowercase Keyword parameter	Indicates keywords. Enter values exactly as shown in the command description.
[ ] Square brackets	Enclose optional parameters. Choose none; or select one or more an unlimited number of times each. Do not enter brackets as part of any command. `[parm1|parm2|parm3]`
? Question mark	Used with the square brackets to limit the immediately following token to one occurrence.
<ESC> Escape sequence	Each escape sequence <ESC> starts with the ASCII character 27 (0x1B). This is equivalent to the Escape key. `<ESC>C`
<CR> Carriage return	Each command is terminated by a carriage return.
<LF> Line feed	Each command is terminated by a line feed.
<CR> <LF> Carriage return Line feed	Each response is started with a carriage return and line feed with some exceptions.

Table 2 Document Text Conventions (Continued)

Convention Type	Description
< > Angle brackets	Enclose a numeric range, endpoints inclusive. Do not enter angle brackets as part of any command. `<SSID>`
= Equal sign	Separates the variable from explanatory text. Is entered as part of the command. `PROCESSID = <CID>`
. dot (period)	Allows the repetition of the element that immediately follows it multiple times. Do not enter as part of the command. `.AA:NN can be expanded to 1:01 1:02 1:03.`
A.B.C.D IP address	IPv4-style address. `10.0.11.123`
X:X::X:X IPv6 IP address	IPv6-style address. `3ffe:506::1` Where the : : represents all 0x for those address components not explicitly given.
LINE End-to-line input token	Indicates user input of any string, including spaces. No other parameters may be entered after input for this token. `string of words`
WORD Single token	Indicates user input of any contiguous string (excluding spaces). `singlewordnospaces`

Table 3, page 11, describes the symbol conventions used in this manual for notification and important instructions.

Table 3 Symbol Conventions

Icon	Type	Description
	Note	Provides helpful suggestions needed in understanding a feature or references to material not available in the manual.
	Alert	Alerts you of potential damage to a program, device, or system or the loss of data or service.
	Caution	Cautions you about a situation that could result in minor or moderate bodily injury if not avoided.
	Warning	Warns you of a potential situation that could result in death or serious bodily injury if not avoided.
	Electro-Static Discharge (ESD)	Notifies you to take proper grounding precautions before handling a product.

Documentation

The GainSpan documentation suite listed in Table 4, page 12 includes the part number, documentation name, and a description of the document. The documents are available from the GainSpan Portal. Refer to Accessing the GainSpan Portal, page 16 for details.

Table 4 Documentation List

Part Number	Document Title	Description
GS2K-QS-001205	GainSpan GS2000 Based Module Kit Quick Start Guide	Provides an easy to follow guide on how to unpack and setup GainSpan GS2000 based module kit for the GS2011M and GS2100M modules.
GS2K-EVB-FP-UG-001206	GainSpan GS2000 Based Module Programming User Guide	Provides users steps to program the on-board Flash on the GainSpan GS2000 based modules using DOS or Graphical User Interface utility provided by GainSpan. The user guide uses the evaluation boards as a reference example board.
GS2011-S2W-APP-PRG-RG-001208	GainSpan Serial-to-WiFi Adapter Application Programmer Reference Guide	Provides a complete listing of AT serial commands, including configuration examples for initiating, maintaining, and evaluating GainSpan WiFi GS2011M series modules.
GS2100-S2W-APP-PRG-RG-001208	GainSpan Serial-to-WiFi Adapter Application Programmer Reference Guide	Provides a complete listing of AT serial commands, including configuration examples for initiating, maintaining, and evaluating GainSpan WiFi GS2100M series modules.
GS2K-EVB-HW-UG-001210	GainSpan GS2000 Based Module Evaluation Board Hardware User Guide.	Provides instructions on how to setup and use the GS2000 based module evaluation board along with component description, jumper settings, board specifications, and pinouts.
GS2011M-DS-001211	GainSpan GS2011M Low Power WiFi Module Data Sheet	Provides information to help WiFi system designers to build systems using GainSpan GS2011M module and develop wireless applications.
GS2100M-DS-001212	GainSpan GS2100M Low Power WiFi Module Data Sheet	Provides information to help WiFi system designers to build systems using GainSpan GS2100M module and develop wireless applications.

Table 4 Documentation List (Continued)

Part Number	Document Title	Description
GS2011MxxS-DS-001214	GainSpan GS2011MxxS Low Power WiFi Module Data Sheet	Provides information to help WiFi system designers to build systems using GainSpan GS2011MxxS module and develop wireless applications.
GS2101M-DS-001270	GainSpan GS2101M Low Power WiFi Module Data Sheet	Provides information to help WiFi system designers to build systems using GainSpan GS2101M module and develop wireless applications.
GS2K-IP2WIFI-APP-PRG-RG-001247	GainSpan GS2000 Based Module IP-to-WiFi Adapter Application Programmer Reference Guide	Provides a complete listing of AT serial commands, including configuration examples for initiating, maintaining, and evaluation GainSpan IP-to-WiFi GS2000 based modules.

Documentation Feedback

We encourage you to provide feedback, comments, and suggestions so that we can improve the documentation. You can send your comments by logging into GainSpan Support Portal. If you are using e-mail, be sure to include the following information with your comments:

- Document name
- URL or page number
- Hardware release version (if applicable)
- Software release version (if applicable)

Contacting GainSpan Technical Support

Use the information listed in Table 5, page 14, to contact the GainSpan Technical Support.

Table 5 GainSpan Technical Support Contact Information

North America	1 (408) 627-6500 - techsupport@gainspan.com
Outside North America	Europe: EUsupport@gainspan.com China: Chinasupport@gainspan.com Asia: Asiasupport@gainspan.com
Postal Address	GainSpan Corporation 3590 North First Street Suite 300 San Jose, CA 95134 U.S.A.

For more Technical Support information or assistance, perform the following steps:

1. Point your browser to http://www.gainspan.com.
2. Click **Contact**, and click **Request Support**.
3. Log in using your customer **Email** and **Password**.
4. Select the **Location**.
5. Select **Support Question** tab.
6. Select **Add New Question**.
7. Enter your technical support question, product information, and a brief description.

The following information is displayed:

- Telephone number contact information by region
- Links to customer profile, dashboard, and account information
- Links to product technical documentation
- Links to PDFs of support policies

Returning Products to GainSpan

If a problem cannot be resolved by GainSpan technical support, a Return Material Authorization (RMA) is issued. This number is used to track the returned material at the factory and to return repaired or new components to the customer as needed.

NOTE: *Do not return any components to GainSpan Corporation unless you have first obtained an RMA number. GainSpan reserves the right to refuse shipments that do not have an RMA. Refused shipments will be returned to the customer by collect freight.*

For more information about return and repair policies, see the customer support web page at: https://www.gainspan.com/secure/login.

To return a hardware component:

1. Determine the part number and serial number of the component.
2. Obtain an RMA number from Sales/Distributor Representative.
3. Provide the following information in an e-mail or during the telephone call:
   - Part number and serial number of component
   - Your name, organization name, telephone number, and fax number
   - Description of the failure
4. The support representative validates your request and issues an RMA number for return of the components.
5. Pack the component for shipment.

Guidelines for Packing Components for Shipment

To pack and ship individual components:

- When you return components, make sure they are adequately protected with packing materials and packed so that the pieces are prevented from moving around inside the carton.
- Use the original shipping materials if they are available.
- Place individual components in electrostatic bags.
- Write the RMA number on the exterior of the box to ensure proper tracking.

CAUTION! *Do not stack any of the components.*

Accessing the GainSpan Portal

To find the latest version of GainSpan documentation supporting the GainSpan product release you are interested in, you can search the GainSpan Portal website by performing the following steps:

NOTE: *You must first contact GainSpan to set up an account, and obtain a customer user name and password before you can access the GainSpan Portal.*

1. Go to the GainSpan Support Portal website.
2. Log in using your customer **Email** and **Password**.
3. Click the **Getting Started** tab to view a Quick Start tutorial on how to use various features within the GainSpan Portal.
4. Click the **Actions** tab to buy, evaluate, or download GainSpan products.
5. Click on the **Documents** tab to search, download, and print GainSpan product documentation.
6. Click the **Software** tab to search and download the latest software versions.
7. Click the **Account History** tab to view customer account history.
8. Click the **Legal Documents** tab to view GainSpan Non-Disclosure Agreement (NDA).

Ordering Information

To order GainSpan's GS2101Mxx low power module contact a GainSpan Sales/Distributor Representative. Table 6, page 17 lists the GainSpan device information.

Table 6 GS2101Mxx Ordering Information

Device Description	Ordering Number	Revision
Low power module with on-board antenna	GS2101MIP	1.0
Low power module with external antenna	GS2101MIE	1.0

NOTE: *Modules ship with test code ONLY. Designers must first program the modules with a released firmware version. Designers should bring out GPIO31 pin (option to pull this pin to VDDIO during reset or power-on) and UART0 or SPI0 pins to enable programming of firmware into the module. For details refer to the Programming the GainSpan Modules document.*

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Chapter 1 GS2101M Overview

This chapter describes the GainSpan® GS2101M low power module hardware specification overview.

1.1 Product Overview

The GS2101M based modules provide cost effective, low power, and flexible platform to add WiFi® connectivity for embedded devices for a variety of applications, such as wireless sensors and thermostats. It uses the GS2000 SoC, which combines ARM® Cortex M3-based processors with a 802.11b/g/n Radio, MAC, security, & PHY functions, RTC and SRAM, up to 4 MB FLASH, and on-board and off module certified antenna options. The module provides a WiFi and regulatory certified IEEE 802.11b/g/n radio with concurrent network processing services for variety of applications, while leverage existing 802.11 wireless network infrastructures.

1.2 GS2101M Module Product Features

- Family of modules with different antenna and output power options:
  - GS2101MIx 18mm (0.71in) x 25 mm (0.98in) x 2.5mm (0.098in) 40-pin PCB Surface Mount Package. Two SKU's are:
    - GS2101MIP (on-board PCB antenna)
    - GS2101MIE (external antenna)
  - The two SKUs are pin to pin compatible
  - Simple API for embedded markets covering a large range of applications
- Fully compliant with IEEE 802.11b/g/n and regulatory domains:
    - 802.11n: 1x1 single stream, 20 MHz channels, 400/800ns GI, MCS0 – 7
      - Data rates of 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65.0, 72.2 Mbps
    - 802.11g: OFDM modulation for data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mb/s.
    - 802.11b: CCK modulation rates of 5.5 and 11 Mbps; DSSS modulation for data rate of 1 and 2 Mbps.

- WiFi Solution:
  - WiFi security (802.11i)
    - WPA™ - Enterprise, Personal
    - WPA2™ - Enterprise, Personal
    - Vendor EAP Type(s)
      - EAP-TTLS/MSCHAPv2, PEAPv0/EAP-MSCHAPv2, PEAPv1/EAP-GTC, EAP-FAST, EAP-TLS
  - Hardware-accelerated high-throughput AES and RC4 encryption/decryption engines for WEP, WPA/WPA2 (AES-CCMP and TKIP).
  - Additional dedicated encryption HW engine to support higher layer encryption such as IPSEC (IPv4 and IPv6), SSL/TLS, HTTPs, PKI, digital certificates, RNG, etc.
- Dual ARM Cortex M3 Processor Platform:
  - 1st Cortex M3 processor (WLAN CPU) for WLAN software
    - Implements 802.11 b/g/n WLAN protocol services
      - 320 KB dedicated SRAM
      - 512 KB dedicated ROM
  - 2nd Cortex M3 processor (APP CPU) for networking software
    - Implements networking protocol stacks and user application software
      - 384 KB dedicated SRAM
      - 512 KB dedicated ROM
  - 64KB shared dual ported SRAM for inter-processor communications
  - 320KB assignable (under SW control) SRAM
  - Support processor clock frequencies for both CPU of up to 120MHz
  - Based on Advanced Microprocessor Bus Architecture (AMBA) system
    - AMBA Multilayer High-Speed Bus (AHB)
    - AMBA Peripheral Bus (APB)
  - On-module flash controller:
    - Manages read/write/program/erase operations to the 2 MB flash memory device on the module
    - Supports higher performance QUAD SPI protocol operations
    - Active power management

- Interfaces:
  - SDIO:
    - Compliant to SDIO v2.0 specification
    - Interface clock frequency up to 40 MHz

NOTE: *Tested with current test platform up to 33 MHz.*

    - Data transfer modes: 4-bit, 1-bit SDIO, SPI
    - Device mode only (slave)
  - SPI:
    - One (1) general-purpose SPI interfaces (each configurable independently as master or slave)
    - The SPI pins are muxed with other functions such as GPIO
    - Supports clock rates of up to 30 MHz (master mode) and up to 10 MHz (slave mode)
    - Protocols supported include: Motorola SPI, TI Synchronous Serial Protocol (SSP) and National Semiconductor Microwire
    - Supports SPI mode 0 thru 3 (software configurable)
  - UART:
    - Two (2) multi-purpose UART interfaces operating in full-duplex mode
      - 16450/16550 compatible
      - Optional support for flow control using RTS/CTS signaling for high data transfer rates
      - Standard baud rate from 9600 bps up to 921.6K baud (additional support for higher non-standard rates using baud rates up to 7.5 MHz)
  - GPIOs:
    - Up to 16 configurable general purpose I/O
  - Single 3.3V supply option
  - Three (3) PWM output
  - I^2C master/slave interface
  - Three (3) 16-bit Sigma Delta ADC channels, for sensors and measurements
  - One (1) RTC I/O that can be configured as:
    - Alarm input to asynchronously awaken the chip
    - Support control outputs for sensors
- Embedded RTC (Real Time Clock) can run directly from battery

- Power supply monitoring capability
- Low-power mode operations:
  - Standby, Sleep, and Deep Sleep
- FCC/IC/ETSI/TELEC/WiFi Certification

Chapter 2 GS2101M Architecture

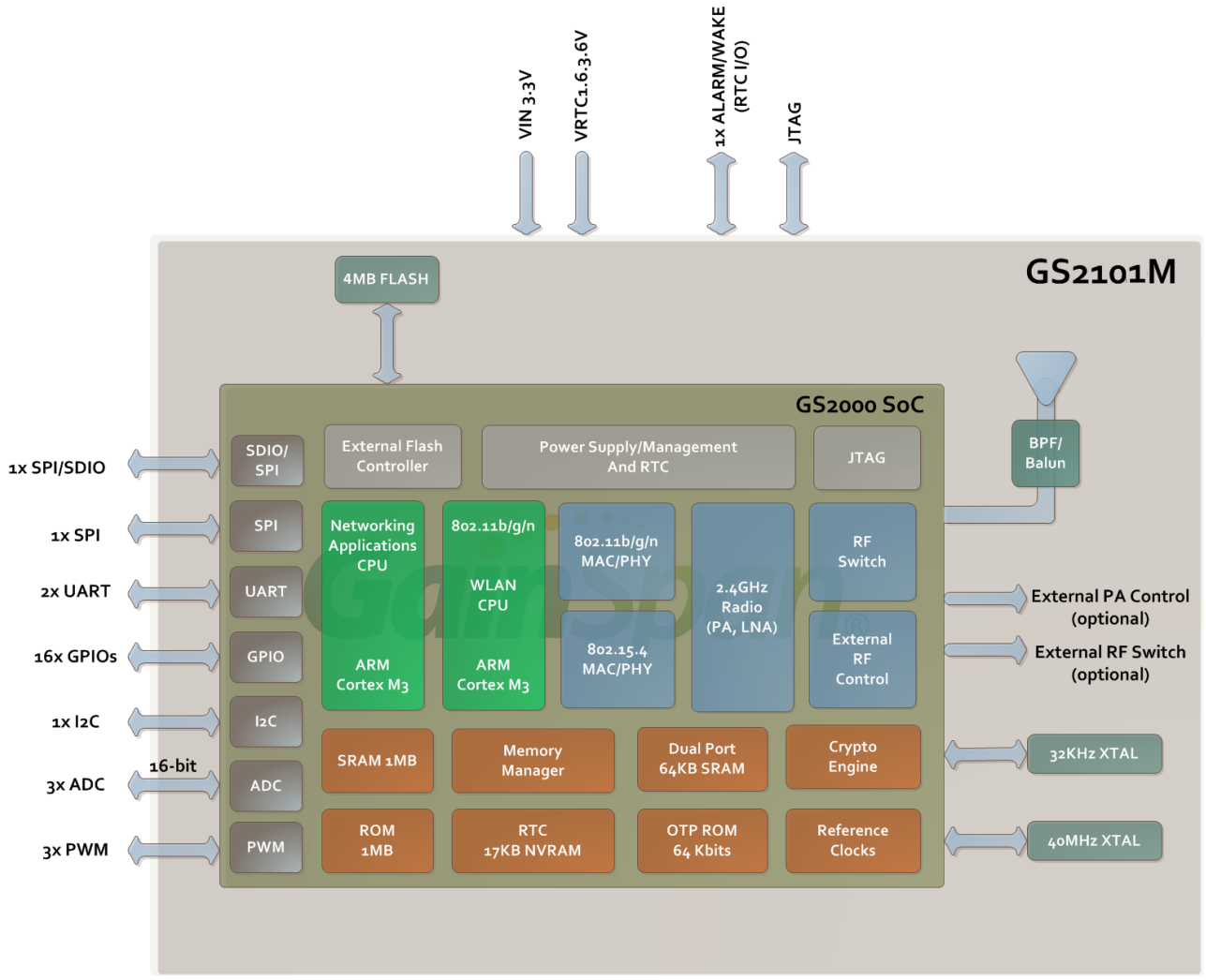
This chapter describes the GainSpan® GS2101M Low Power module architecture.

2.1 Architecture Description

The GainSpan GS2101M module (see Figure 1, page 24) is based on a highly integrated GS2000 ultra low power WiFi System-on-Chip (SoC) that contains the following:

- The GS2000 SoC contains two ARM Cortex M3 CPUs, a compatible 802.11 radio, security, on-chip memory, and variety of peripherals in a single package.
  - One ARM core is dedicated to Networking Subsystems, and the other dedicated to Wireless LAN Subsystems.
  - The module carries an 802.11/g/n radio with on-board 32KHz & 40MHz crystal circuitries, RF, and on-board antenna or external antenna options.
- On module 4 Mega Byte FLASH device that contains the user embedded applications and data such as web pages.
- Variety of interfaces are available such as two UART blocks using only two data lines per port with optional hardware flow controls, two SPI blocks (one SDIO is shared function with one for the SPI interfaces), I^2C with Master or slave operation, JTAG port, low-power 12-bit ADC capable of running at up to 2M samples/Sec., GPIO's, and LED Drivers/GPIO with 16mA capabilities.
- GS2101Mxx has a VRTC pin that is generally connected to always available power source such as battery or line power. This provides power to the Real Time Clock (RTC) block on the SoC. The module also has VIN_3V3 power supply input to provide the logic signal level for the I/O pins.

Figure 1 GS2101M Block Diagram



2.1.1 Wireless LAN and System Control Subsystem

The WLAN CPU subsystem consists of the WLAN CPU, its ROM, RAM, 802.11b/g/n MAC/PHY, and peripherals. This CPU is intended primarily to implement the 802.11 MAC protocols. The CPU system has GPIO, Timer, and Watchdog for general use. A UART is provided as a debug interface. A SPI interface is provided for specific application needs. The WLAN CPU can access the RTC registers through an asynchronous AHB bridge. WLAN CPU has only Flash read access to the on-board flash memory. The WLAN subsystem interacts with the App subsystem through a set of mailboxes and shared dual–port memories.

The CPUs provide debug access through a JTAG/serial port. For GS2101M module, the complete JTAG port is brought out for both CPUs. The CPUs also include code and data trace and watch point logic to assist in-system debugging of SW.

The WLAN subsystem includes an integrated power amplifier, and provides management capabilities for an optional external power amplifier. In addition, it contains hardware support for AES-CCMP encryption (for WPA2) and RC4 encryption (for WEP & WPA TKIP) encryption/decryption.

2.1.2 On-board Antenna / RF Port / Radio

The GS2101Mxx modules have fully integrated RF frequency synthesizer, reference clock, and PA. Both TX and RX chain in the module incorporate internal power control loops. The GS2101Mxx modules also incorporate an on board antenna option or an external antenna connector.

2.1.2.1 802.11 MAC

The 802.11 MAC implements all time critical functionality of the 802.11b/g/n protocols. It works in conjunction with the MAC SW running on the CPU to implement the complete MAC functionality. It interfaces with the PHY to initiate transmit/receive and CCA. The PHY registers are programmed indirectly through the MAC block. The MAC interfaces to the system bus and uses DMA to fetch transmit packet data and save receive packet data. The MAC SW exchanges packet data with the HW though packet descriptors and pointers.

Key Features

- Compliant to IEEE 802.11 (2012)
- Compliant to IEEE 802.11b/g/n (11n – 2009)
- Long and short preamble generation on frame-by-frame basis for 11b frames
- Transmit rate adaptation
- Transmit power control
- Frame aggregation (AMPDU, AMSDU)
- Block ACK (Immediate, Compressed)
- RTS/CTS, CTS-to-self frame sequences and SIFS

- Client and AP modes support
- Encryption support including: AES-CCMP, legacy WPA-TKIP, legacy WEP ciphers and key management
- WiFi Protected Setup 2.0 (WPS2.0) including both PIN and push button options
- 802.11e based QoS (including WMM, WMM-PS)
- WiFi Direct with concurrent mode, including Device/Service Discovery, Group Formation/Invitation, Client Power Save, WPS-PIN/Push Button

2.1.2.2 802.11 PHY

The 802.11 PHY implements all the standard required functionality and GainSpan specific functionality for 802.11b/g/n protocols. It also implements the Radar detection functionality to support 802.11h. The PHY implements the complete baseband Tx and Rx pipeline. It interfaces with the MAC to perform transmit and receive operations. It interfaces directly to the ADC and DAC. The PHY implements the Transmit power control, receive Automatic Gain Control and other RF control signals to enable transmit and receive. The PHY also computes the CCA for MAC use.

Key Features

- Compliant to 2.4GHz IEEE 802.11b/g/n (11n – 2009)
- Support 802.11g/n OFDM with BPSK, QPSK, 16-QAM and 64-QAM; 802.11b with BPSK, QPSK and CCK
- Support for following data rates:
  - 802.11n (20MHz): MCS0 - 7; 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65.0, 72.2 Mbps
  - 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
  - 802.11b: 1, 2, 5.5, 11 Mbps
- Support Full (800ns) & Half (400ns) Guard Interval (GI) modes (SGI and LGI)
- Support Space time block coding (STBC) for receive direction
- Complete front-end radio integration including PA, LNA and RF Switch
- Support for external PA, LNA and control of external RF Switch (GS2101MIE only)

2.1.2.3 RF/Analog

The RF/Analog is a single RF transceiver for IEEE 802.11b/g/n (WLAN). The RF Interface block provides the access to the RF and analog control and status to the CPU. This block is accessible only from the WLAN CPU. It implements registers to write static control words. It provides read only register interface to read static status. It generates the dynamic control signals required for TX and RX based on the PHY signals. The AGC look up table to map the gain to RF gain control word is implemented in this block.

2.1.3 Network Services Subsystem

2.1.3.1 APP CPU

The Network services subsystem consists of an APP CPU which is based on an ARM CORTEX M3 core. It incorporates an AHB interface and a JTAG debug interface. The network RTOS, network stack, and customer application code run on this CPU.

2.1.3.2 Crypto Engine

The Network services subsystem contains a separate hardware crypto engine that provides a flexible framework for accelerating the cryptographic functions for packet processing protocols. The crypto engine has the raw generic interface for cipher and hash/MAC functions such as AES, DES, SHA, and RC4. It also includes two optional engines to provide further offload; the PKA and RNG modules. These provide additional methods for public key acceleration functions and random number generation. The engine includes a DMA engine that allows the engine to perform cryptographic operation on data packets in the system memory without any CPU intervention.

2.1.4 Memory Subsystem

The GS2101M module contains several memory blocks.

2.1.4.1 SRAM

The system memory is built with single port and dual port memories. Most of the memory consists of single port memory. A 64KB dual port memory is used for exchange of data between the two CPU domains. All the memories are connected to the system bus matrix in each CPU subsystem. All masters can access any of the memory within the subsystem.

The APP subsystem has 384KB of dedicated SRAM for program and data use.

The WLAN subsystem has 320KB of dedicated SRAM for program and data use.

These memories are divided into banks of 64KB each. The bank structure allows different masters to access different banks simultaneously through the bus matrix without incurring any stall. Code from the external Flash is loaded into the SRAM for execution by each CPU.

In addition, a static shared SRAM is provided. This consists of five 64KB memory blocks.

At any time, any of these memory blocks can be assigned to one of the CPU subsystem. These should be set up by the APP CPU SW at initialization time. The assignment is not intended to change during operation and there is no HW interlock to avoid switching in the middle of a memory transaction. The assignment to the WLAN CPU should be done starting from the highest block number going down to lowest block number. This result in the shared memory appearing as a single bank for each CPU subsystem, independent of the number of blocks assigned. The shared memory is mapped such that the SRAM space is continuous from the dedicated SRAM to shared SRAM.

A 64KB dual port memory is used for exchange of data between the two CPU domains. Each CPU subsystem can read or write to this memory using an independent memory port. SW must manage the memory access to avoid simultaneous write to the same memory location. The dual port memory appears as a single bank to each CPU subsystem.

2.1.4.2 ROM

ROM is provided in each CPU subsystem to provide the boot code and other functional code that are not expected to change regularly. Each CPU has 512KB of ROM.

2.1.4.3 OTP ROM

The GS2000 device includes a 64Kbit OTP ROM used for storing MAC ID and other information such as security keys etc. The APP and WLAN subsystem each contain 32Kbits (4Kbytes) of OTP memory.

2.1.4.4 Flash Interface

The GS2000 SoC has only internal ROM and RAM for code storage. There is no embedded Flash memory on the SoC. Any ROM patch code and new application code must reside in the on-module Flash device of the GS2101M module. Flash access from the two CPUs are independent. The APP CPU is considered the system Master and the code running on this CPU is required to initialize the overall chip and common interfaces. WLAN CPU access to the Flash is restricted to read DMA. Any write to the Flash from the WLAN CPU must be done through the APP CPU. The operational parameters of the DMA accesses are set by the APP CPU at system startup. The Flash code is transferred to internal RAM before execution.

2.1.5 Clocks

The GS2101M includes four basic clock sources:

- Low power 32KHz clock (see 2.1.6 Real Time Clock (RTC) Overview, page 29)
- 40MHz Xtal Oscillator
- PLL to generate the internal 120MHz (CPU) and 80MHz (PHY) clocks from the 40MHz Xtal.
- High speed RC oscillator 80MHz

Intermediate modes of operation, in which high speed clocks are active but some modules are inactive, are obtained by gating the clock signal to different subsystems. The clock control blocks within the device are responsible for generation, selection and gating of the clocked used in the module to reduce power consumption in various power states.

2.1.6 Real Time Clock (RTC) Overview

To provide global time (and date) to the system, the GS2101Mxx module is equipped with a low-power Real Time Clock (RTC). The RTC is the always on block that manages the Standby state. This block is powered from a supply pin (VRTC) separate from the digital core and may be powered directly from a battery. The RTC implementation supports a voltage range of 1.6V to 3.6V.

2.1.6.1 RTC Main Features

- One 48-bit primary RTC counter as the primary reference for all timing events and standby awake management
- 1 programmable IO pins with specific default behavior. These pins are in the RTC IO domain.
  - Alarm inputs to wake up the GS2101M module from its sleep states (deep-sleep/standby)
- Startup control counters with HW and SW override registers
- Power-on-reset control with brown-out detector
- RTC registers to hold RTC and wakeup control bits while the core domain is off
- 1Kbyte latch based memory (1.6-3.6V capable)
- 16KB of SRAM memory, divided into 4 equal blocks (1.2V capable)
- uLDO to supply the SRAM memory
- RTC logic is 1.6-3.6V capable
- 32 KHz RC oscillator
- 32768Hz crystal oscillator
- APB interface for CPU access
- Interrupts to CPU

The RTC contains a low-power 32.768KHz RC oscillator which provides fast startup at first application of RTC power. It also supports an optional 32.768KHz crystal oscillator which can be substituted for the RC oscillator under software control. In normal operation the RTC is always powered up.

The standby programmable counter is 48-bits and provides up to 272 years worth of standby duration. For the RTC_IO pin, the programmable embedded counter (32-bit) is provided to enable periodic wake-up of the remainder of the external system, and provide a 1.5 days max period. The RTC_IO pin can be configured as input (ALARM) or output (WAKE UP) pin.

The RTC includes a Power-On Reset (POR) circuit, to eliminate the need for an external component. The RTC contains low-leakage non-volatile (battery-powered) RAM, to enable storage of data that needs to be preserved. It also includes a brown-out detector that can be disabled by SW.

2.1.6.2 Real Time Clock Counter

The Real Time Counter features:

- 48-bit length (with absolute duration of 272 years).
- Low-power design.

This counter is automatically reset by power-on-reset.

This counter wraps around (returns to “all-0” once it has reached the highest possible “all-1” value).

2.1.6.3 RTC I/O

There is one (1) RTC I/O that can be used to control external devices, such as sensors or wake up the module based on external events or devices.

2.1.7 GS2101M Peripherals

2.1.7.1 SDIO Interface

The SDIO interface is a full / high speed SDIO device (slave). The device supports SPI, 1-bit SD and 4-bit SD bus mode. The SDIO block has an AHB interface, which allows the CPU to configure the operational registers residing inside the AHB Slave core. The CIS and CSA area is located inside the internal memory of CPU subsystem. The SDIO Registers (CCCR and FBR) are programmed by both the SD Host (through the SD Bus) and CPU (through the AHB bus) via Operational registers. The SDIO block implements the AHB master to initiate transfers to and from the system memory autonomously.

During the normal initialization and interrogation of the card by the SD Host, the card will identify itself as an SDIO device. The SD Host software will obtain the card information in a tuple (linked list) format and determine if that card’s I/O function(s) are acceptable to activate. If the Card is acceptable, it will be allowed to power up fully and start the I/O function(s) built into it.

The SDIO interface implements Function 1 in addition to the default Function 0. All application data transfers are done through the Function 1.

The primary features of this interface are

- Meets SDIO card specification version 2.0.
- Conforms to AHB specification.
- Host clock rate variable between 0 and 40 MHz

NOTE: *Tested with current test platform up to 33 MHz.*

- All SD bus modes supported including SPI, 1 and 4 bit SD.
- Allows card to interrupt host in SPI, 1 and 4 bit SD modes.

- Read and Writes using 4 parallel data lines
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity-CRC checking optional in SPI mode
- Programmable through a standard AHB Slave interface
- Writing of the I/O reset bit in CCCR register generates an active low reset output synchronized to AHB Clock domain.
- Card responds to Direct read/write (IO52) and Extended read/write (IO53) transactions.
- Supports Read wait Control operation.
- Supports Suspend/Resume operation.

2.1.7.2 SPI Interface

The SPI interface is a master slave interface that enables synchronous serial communications with slave or master peripherals having one of the following: Motorola SPI-compatible interface, TI synchronous serial interface or National Semiconductor Microwire interface. In both master and slave configuration, the block performs parallel-to-serial conversion on data written to an internal 16-bit wide, 8-deep transmit FIFO and serial to parallel conversion on received data, buffering it in a similar 16-wide, 8 deep FIFO. It can generate interrupts to the CPU to request servicing transmit and receive FIFOs and indicate FIFO status and overrun/underrun. The clock bit rate is SW programmable. In master mode, the SPI block in GS2000 can perform up to 30 MHz and in slave mode up to 10 MHz serial clock. Clock rates higher than 20MHz in master mode or 6.66MHz in slave mode requires activation of the PLL's 120MHz clock source. The interface type, data size and interrupt masks are programmable. It supports DMA working in conjunction with the uDMA engine.

2.1.7.3 UART Interface

The UART interface implements the standard UART protocol. It is 16450/16550 compatible. It has separate 32 deep transmit and receive FIFOs to reduce CPU interrupts. The interface supports standard asynchronous communication protocol using start, stop and parity bits. These are added and removed automatically by the interface logic. The data size, parity and number of stop bits are programmable. It supports HW based flow control through CTS/RTS signaling. A fractional baud rate generator allows accurate setting of the communication baud rate. It supports DMA working in conjunction with the uDMA engine.

2.1.7.4 I^2C Interface

The I^2C interface block implements the standard based two wire serial I^2C protocol. The interface can support both master and slave modes. It supports multiple masters, high speed transfer (up to 3.4MHz), 7 or 10 bit slave addressing scheme, random and current address transfer. It also supports clock stretching to interface with slower devices. It can generate

interrupts to the CPU to indicate specific events such as FIFO full/empty, block complete, no ack error, and arbitration failure.

2.1.7.5 GPIO

The GPIO block provides programmable inputs and outputs that can be controlled from the CPU SW through an APB interface. Any number of inputs can be configured as an interrupt source. The interrupts can be generated based on the level or the transition of a pin. At reset, all GPIO lines defaults to inputs. Each pin can be configured as input or output from SW control.

2.1.7.6 Sigma Delta ADC

The ADC and DAC are 16-bit sigma-delta converters. There are 3 ADC channels, each having a differential pair for a total of six input pins. The sample rate can be 32KHz to 80KHz. The sigma delta converter ratio is 250. The ADC is a 3 channel converter. Each channel can have an optional pre-amplifier stage. The gain can be set to 0db, 6db, 12db, 18db, or 24db. The delay between the second and third channels of the ADC can be adjusted under SW control. The digital interface for the ADCs and the DAC are 2's complement. ADC channel 0 (only) can alternatively be used as a differential DAC.

2.1.7.7 PWM

The PWM consists of three identical PWM function blocks. The PWM function blocks can be used in two modes of operations:

- Independent PWM function blocks providing output signal with programmable frequency and duty cycle
- Synchronized PWM function blocks with programmable phase delay between each PWM output

The PWM has the following features:

- 32-bit AMBA APB interface to access control, and status information
- Three identical PWM function blocks
- Each PWM block can be enabled independently
- All three PWM blocks can be started synchronously or chained with programmable delay
- Programmable 6-bit prescaler for the input clock (see 2.1.5 Clocks, page 28)
- Programmable frequency and duty cycle using 16-bit resolution in terms of clock cycles for ON and OFF interval time
- Combined interrupt line with independent masking of interrupts

2.1.8 System States

The system states of the GS2101Mxx system are as follows:

Power OFF: No power source connected to the system.

Standby: In the standby state, the GS2101M is in its lowest power state. In this state power is on to the VRTC and VIN_3V3 input. The RTC portion of the GS2000 chip is powered from the VRTC pin.

In standby state, the 32.768KHz oscillator is running and RTC RAM retains the state (how many banks retain their state is SW configurable). SRAM, CPUs and I/Os are powered off using the internal switches within the device thus reducing overall power consumption.

Exit from standby occurs when a pre-specified wakeup time occurs, or when the RTC_IO configured as alarm inputs sees the programmed polarity of signal edge.

NOTE: *During first battery plug, i.e., when power is applied the first time to the RTC power rail (VRTC), the power detection circuit in the RTC also causes a wakeup request.*

System Configuration: When a power-up is requested, the system transitions from the Standby state to the System Configuration state. In this state, the APP CPU is released from reset by the RTC. The WLAN CPU remains in the reset state during System Configuration. The APP CPU then executes the required system configurations, releases the WLAN CPU from reset, and transitions to the Power-ON state.

The System Configuration state is also entered on transition from the Power-ON state to the Standby state, to complete necessary preparations before shutting off the power to the core system.

Power-ON: This is the active state where all system components can be running. The Power-ON state has various sub-states, in which unused parts of the system can be in sleep mode, reducing power consumption. Sleep states are implemented by gating the clock signal off for a specific system component. Additionally, unneeded clock sources can be turned off. For example, receiving data over a slave SPI interface could be done with only the 80MHz RC oscillator active, and the 40MHz crystal and PLL turned off.

Sleep: In the Sleep state, the 40MHz crystal and the 80MHz RC oscillator remains running, but it is gated off to one or both CPUs. Each CPU can independently control its own entry into Sleep state. Any enabled interrupt will cause the interrupted CPU to exit from Sleep state, and this will occur within a few clock cycles.

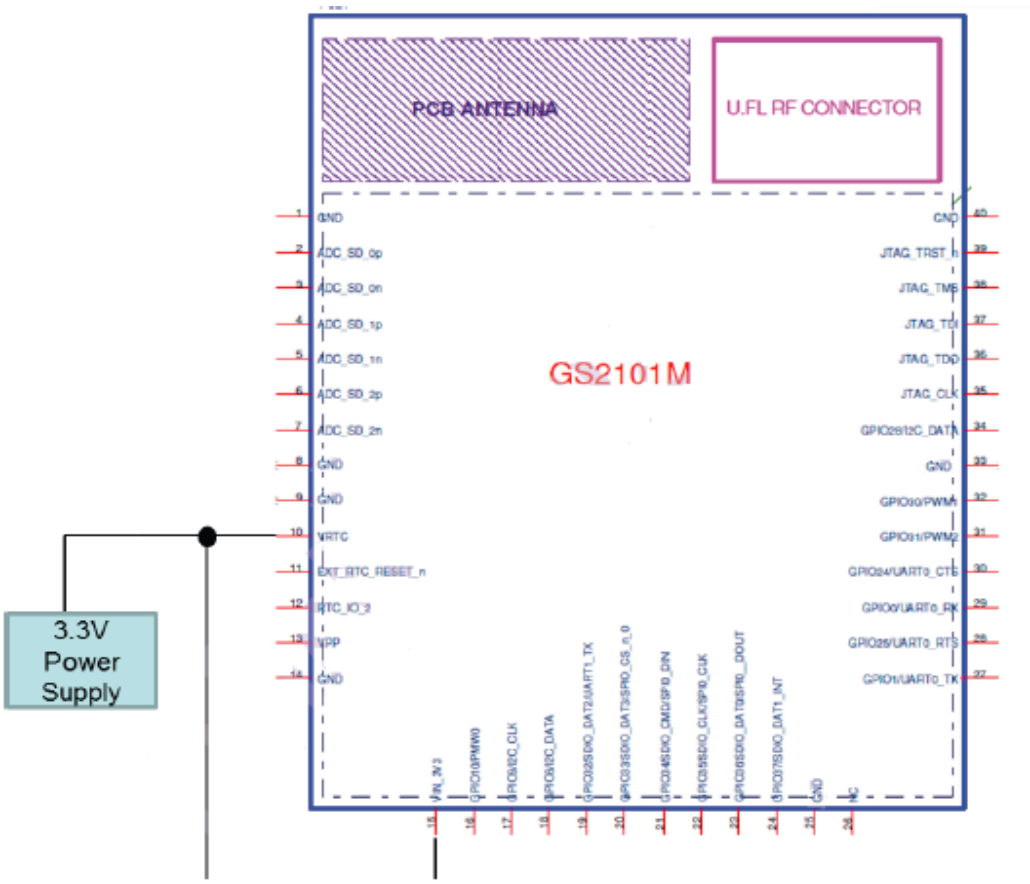
Deep Sleep: Deep sleep is entered only when both CPUs agree that the wakeup latency is OK. In Deep Sleep mode, the 40MHz crystal oscillator and 80MHz RC oscillator are turned off to save power, but all power supplies remain turned on. Thus all registers, memory, and I/O pins retain their state. Any enabled interrupt will cause an exit from Deep Sleep state.

EXT_RTC_RESET_n pin: This is an input pin for resetting the entire module, including the RTC section of the device. This pin should not be left floating. An external 10K pull up resistor to VRTC is recommended.

2.1.9 Power Supply

This section shows various application power supply connections. Figure 2, page 34 shows the GS2101Mxx power supply connection.

Figure 2 GS2101Mxx Always ON Power Supply Connection



Note:

1. Always ON connection connects VRTC and VIN_3V3 together to a 3.3V power supply.

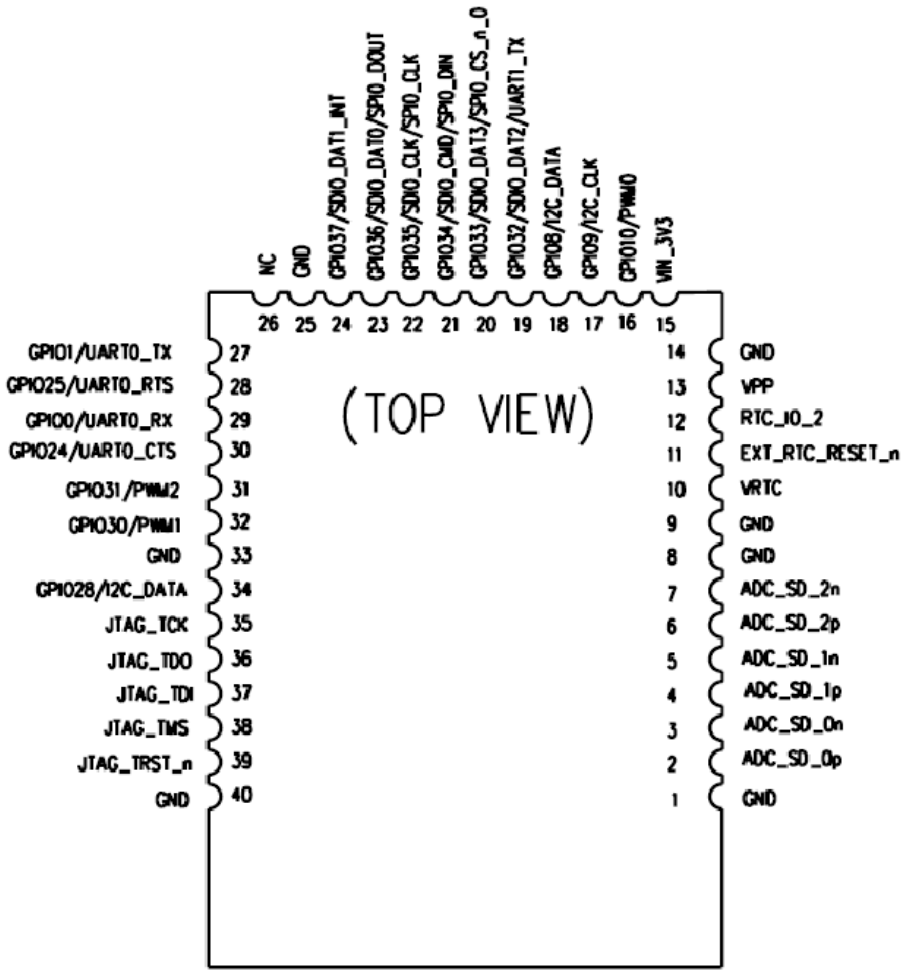
Chapter 3 Pin-out and Signal Description

This chapter describes the GainSpan® GS2101M Low Power module architecture.

3.1 GS2101Mxx Device Pin-out

Figure 3, page 35 shows the GS2101Mxx device pin-out diagram.

Figure 3 GS2101Mxx Device Pin-out Diagram (Module Top View)



3.1.1 GS2101Mxx Module Pins Description

Table 7, page 36 describes the GS2101Mxx module pin signal description.

Table 7 GS2101Mxx Module Pin Signal Description

Pins	Name	Voltage Domain	Internal Bias after Hardware Reset	Drive Strength (mA)	Signal State	Description
1	GND	0V	Not Applicable		Analog port	Ground
2	ADC_SD_0p	VIN_3V3	Not Applicable		Analog port	Sigma Delta ADC differential positive input 0 or Sigma Delta DAC positive output 0
3	ADC_SD_0n	VIN_3V3	Not Applicable		Analog port	Sigma Delta ADC differential negative input 0 or Sigma Delta DAC negative output 0
4	ADC_SD_1p	VIN_3V3	Not Applicable		Analog port	Sigma Delta ADC differential positive input 1
5	ADC_SD_1n	VIN_3V3	Not Applicable		Analog port	Sigma Delta ADC differential negative input 1
6	ADC_SD_2p	VIN_3V3	Not Applicable		Analog port	Sigma Delta ADC differential positive input 2
7	ADC_SD_2n	VIN_3V3	Not Applicable		Analog port	Sigma Delta ADC differential negative input 2
8	GND	0V	Not Applicable		Analog Port	Ground
9	GND	0V	Not Applicable		Analog Port	Ground
10	VRTC	VRTC	Not Applicable		Analog port	Embedded Real Time Clock Power Supply
11	EXT_RTC_RESET_n	VRTC	None		Digital Input	Device Reset Input
12	RTC_IO_2 (see Note 2)	VRTC	None	1	RTC Digital Input/Output	Embedded Real Time Clock Input/Output 2
13	VPP (see Note 7)	VPP	Not Applicable		Analog port	Programming Voltage for OTP Memory
14	GND (see Note 3)	0V	Not Applicable	4	Analog port	Ground
15	VIN_3V3	VIN_3V3	Not Applicable		Analog port	Single Supply Port
16	GPIO10/PWM0 (see Note 3)	VIN_3V3	Pull-down	4	Digital Input/Output	GPIO/Pulse Width Modulator 0
17	GPIO9/I2C_CLK (see Note 3 and Note 5)	VIN_3V3	Pull-down	12	Digital Input/Output	GPIO/Inter-Integrated Circuit Clock

Table 7 GS2101Mxx Module Pin Signal Description (Continued)

Pins	Name	Voltage Domain	Internal Bias after Hardware Reset	Drive Strength (mA)	Signal State	Description
18	GPIO8/I2C_DATA (see Note 3 and Note 5)	VIN_3V3	Pull-down	12	Digital Input/Output	GPIO/Inter-Integrated Circuit Data
19	GPIO32/SDIO_DAT2/ UART1_TX (see Note 3)	VIN_3V3	Pull-down	4	Digital Input/Output	GPIO/SDIO_DATA Bit 2/UART1 Transmitter Output
20	GPIO33/SDIO_DAT3/ SPI0_CS_n_0 (see Note 3)	VIN_3V3	Pull-up	4	Digital Input/Output	GPIO/SDIO Data Bit 3/SPI0 Chip Select Input 0 from the HOST (Active Low)
21	GPIO34/SDIO_CMD/ SPI0_DIN (see Note 3)	VIN_3V3	Pull-down	4	Digital Input/Output	GPIO/SDIO Command Input/SPI0 Receive Data Input
22	GPIO35/SDIO_CLK/ SPI0_CLK (see Note 3)	VIN_3V3	Pull-down	4	Digital Input/Output	GPIO/SDIO Clock/SPI0 Clock Input from the HOST
23	GPIO36/SDIO_DAT0/ SPI0_DOUT (see Note 3) (see Errata E-1)	VIN_3V3	Pull-down	4	Digital Input/Output	GPIO/SDIO Data Bit 0/SPI0 Transmit Data Output to the HOST
24	GPIO37/ SDIO_DAT1_INT (see Note 3 and Note 8)	VIN_3V3	Pull-down	4	Digital Input/Output	GPIO/4-bit SDIO DATA Bit 1/SDIO SPI Mode Interrupt
25	GND	0V	Not Applicable		Analog Port	Ground
26	NC		Not Applicable			Not Connected
27	GPIO1/UART0_TX (see Note 3)	VIN_3V3	Pull-down	4	Digital Input/Output	GPIO/UART0 Transmitter Output.
28	GPIO25/UART0_RTS (see Note 3 and Note 6)	VIN_3V3	Pull-down	12	Digital Input/Output	GPIO/UART0 Request to Send Output. This pin is used for Program Select.
29	GPIO0/UART0_RX (see Note 3)	VIN_3V3	Pull-down	4	Digital Input Output	GPIO/UART0 Receive Input
30	GPIO24/UART0_CTS (see Note 3 and Note 6)	VIN_3V3	Pull-down	12	Digital Input/Output	GPIO/UART0 Clear to Send Input
31	GPIO31/PWM2 (see Note 3 and Note 4)	VIN_3V3	Pull-down	16	Digital Input/Output	GPIO/Pulse Width Modulation Output 2. This pin is used for Program Mode.
32	GPIO30/PWM1 (see Note 3)	VIN_3V3	Pull-down	16	Digital Input/Output	GPIO/Pulse Width Modulation Output 1

Table 7 GS2101Mxx Module Pin Signal Description (Continued)

Pins	Name	Voltage Domain	Internal Bias after Hardware Reset	Drive Strength (mA)	Signal State	Description
33	GND	0V	Not Applicable		Analog Port	Ground
34	GPIO28/I2C_DATA (see Note 3 and Note 5)	VIN_3V3	Pull-down	12	Digital Input/Output	GPIO/Inter-Integrated Circuit Data
35	JTAG_TCK	VIN_3V3	Pull-up		Digital Input	JTAG Test Clock
36	JTAG_TDO	VIN_3V3	Pull-down		Digital Output	JTAG Test Data Out
37	JTAG_TDI	VIN_3V3	Pull-up		Digital Input	JTAG Test Data In
38	JTAG_TMS	VIN_3V3	Pull-up		Digital Input	JTAG Test Mode Select
39	JTAG_TRST_n	VIN_3V3	Pull-up		Digital Input	JTAG Test Mode Rest (Active Low)
40	GND	0V	Not Applicable		Analog Port	Ground

Notes:

1. Recommend 10K external pull up resistor to VRTC.
2. Can be left as no connect.
3. Pins with drive strength 4, 12, and 16 have one pull resistor (either up or down, not both), which is enabled at reset.
4. This pin enables programming of the module. If GPIO31/PWM2 is high during reset or power on, then the GS2101M will wait for Flash download via UART0 or SPI0 interface. Route this pin on the base board so it can be pulled up to VIN_3V3 for programming the module.
5. If I^2C interface is used, provide 2K Ohm pull-ups, to VIN_3V3, for I2C_CLK and I2C_DATA.
6. CTS and RTS signals indicate it is clear to send or ready to send when they are LOW. If signals are high, indicates device is not ready.
7. This pin is generally reserved for GainSpan use, but if a design requires to OTP during production, then design must take into account connection to this pin. Otherwise, it should be left as a No Connect.
8. In the Serial-to-WiFi firmware when using SPI interface this pin is the host wake-up signal or the Ready to Send signal.
   a. GPIO37 - when using SPI interface this pin is the host wake-up signal or the Ready to Send signal.

Errata

E1. The SPI0_DOUT and SPI1_OUT signals do not disable their drive and become Hi-Z when the associated chip select pin is high. This applies to all pin MUX locations for the SPI_DOUT signals. If there are multiple write only devices on the same SPI bus, then this is not an issue. This only becomes an issue when there are other read/write devices on the same SPI bus. The workaround is to add an external buffer chip, such as 74LVC1G125

between the SPI_DOUT pin and the SPI bus, with the enable connected to the chip select signal.

3.1.2 GS2101M Pin MUX Function

The GS2101M pins have multiple functions that can be selected using mux function by software. Table 8, page 39 shows the various MUX functions for each pin. Each pin can be independently configured. Table below shows the various mux functions for each pin. All I/O pins are GPIO inputs at reset. For pins that are inputs to functional blocks only one pin may be assigned to any input function. For example, UART1_RX may be assigned to GPIO9 but not to both GPIO9 and GPIO37.

Table 8 GS2101M Pin MUX Description

				Alternate Functions Available				
Pin#	**Pin Name**	**Internal Pull Resistor**	**mA**	**Mux3**	**Mux4**	**Mux5**	**Mux7**	**Comments**
1	GND							
2	adc_sd_0p							
3	adc_sd_0n							
4	adc_sd_1p							
5	adc_sd_1n							
6	adc_sd_2p							
7	adc_sd_2n							
8	GND							
9	GND							
10	VRTC							
11	ext_rtc_reset_n	pull-up (u)						
12	rtc_io_2	u/d	1					Alarm or wake up pin
13	VPP							Programming voltage for OTP memory
14	GND							
15	VIN_3V3							
16	gpio10/pwm0	pull-down (d)	4	pwm0	uart1_tx	spi1_clk	clk_rtc	
17	gpio9/i2c_clk	d	12	i2c_clk	uart1_rx	spi1_din	i2s_lrclk	
18	gpio8/i2c_data	d	12	i2c_data	uart1_tx	spi1_dout[1]	reserved	
19	gpio32/sdio_dat2/uart1_tx	d	4	sdio_data2	wuart_tx	uart1_tx	spi1_cs_n_12	
20	gpio33/sdio_dat3/spi0_cs_n_0	u	4	sdio_data3	reserved	uart1_rts	spi0_cs_n_0	
21	gpio34/sdio_cmd/spi0_din	d	4	sdio_cmd	reserved	usart1_cts	spi0_din	
22	gpio35/sdio_clk/spi0_clk	d	4	sdio_clk	reserved	i2c_clk	spi0_clk	Note: only 4mA for i2C
23	gpio36/sdio_dat0_dout	d	4	sdio_data0	reserved	i2c_data	spi0_dout[1]	

Table 8 GS2101M Pin MUX Description (Continued)

				Alternate Functions Available				
Pin#	**Pin Name**	**Internal Pull Resistor**	**mA**	**Mux3**	**Mux4**	**Mux5**	**Mux7**	**Comments**
24	gpio37/sdio_dat1_int	d	4	sdio_data1	wuart_rx	uart1_rx	spi0_cs_n_10	
25	GND							
26	NC							
27	gpio1/uart0_tx	d	4	uart0_tx	wuart_tx	pwm1	spi1_dout[1]	
28	gpio25/uart0_rts	d	12	uart0_rts	wuart_rts	spi1_cs_n_7	spi1_clk	
29	gpio0_uart0_rx	d	4	uart0_rx	wuart_rx	pwm2	spi1_din	
30	gpio24/uart0_cts	d	12	uart0_cts	wuart_cts	pwm0	spi1_cs_n_0	
31	gpio31/pwm2	d	16	pwm2	spi1_dout[1]	uart1_tx	wuart_tx	
32	gpio30/pwm1	d	16	pwm1	spi1_din	uart1_rx	wuart_rx	
33	GND							
34	gpio28/i2c_data	d	12	i2c_data	spi1_clk	clk_hs_rc	spi1_cs_n_21	
35	jtag_tck							
36	jtag_tdo							
37	jtag_tdi							
38	jtag_tms							
39	jtag_trst_n							
40	GND							

Note 1: The SPI0_DOUT and SPI1_OUT signals do not disable their drive and become Hi-Z when the associated chip select pin is high. This applies to all pin MUX locations for the SPI_DOUT signals. If there are multiple write only devices on the same SPI bus, then this is not an issue. This only becomes an issue when there are other read/write devices on the same SPI bus. The workaround is to add an external buffer chip, such as 74LVC1G125 between the SPI_DOUT pin and the SPI bus, with the enable connected to the chip select signal.

3.1.3 GS2101M Program and Code Restore Options

Table 9, page 41 describes the options available for device program mode and code restore capabilities. The respective GPIO pins are sampled at reset by device and depending on the values seen on these pins goes into the appropriate mode. Code for the GS2101M resides on the internal flash of the module and up to two back-up copies could be stored in flash. If a software designer wants to restore the execution code to one of the backup copy, it can be accomplished by asserting the appropriate GPIO pins as shown in the table below during power up or reset.

Table 9 GS2101M Pin Program and Code Restore

Boot Control	Program Mode (GPIO 31)	Program Select/Previous Restore (GPIO 25)	Interfaces for Program Load
(see Note 1)	0	0	Normal boot
	0	1	Previous Code Restore. Restores the prior code revision by invalidating the present code image. Will NOT invalidate the last remaining image.
	1	0	Program Mode: UART0 @ 115.2Kbaud; nothing on GPIO15-18; SPI0 on SDIO pins. Note: this is the default you get if you don't pull the Program Select pin high.
	1	1	Program Mode using: UART0 @921.6Kbaud; SPI0 on GPIO15-18. Note: GPIO15-18 are only available on GS2000 SoC, and not on modules.

Note:

1. In Run Mode, boot ROM leaves all GPIO pins as input with pull resistor enabled until flash code sets them otherwise. In Program Mode, only the pins required for the Program Mode specified interfaces are set to non-GPIO mode.

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Chapter 4 Electrical Characteristics

This chapter describes the GainSpan® GS2101M electrical characteristics.

4.1 Absolute Maximum Ratings

Conditions beyond those cited in Table 10, page 43 may cause permanent damage to the GS2101Mxx, and must be avoided. Sustained operation, beyond the normal operating conditions, may affect the long term reliability of the module.

Table 10 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Storage Temperature	T_{ST}	-55		+125	^{o}C
RTC Power Supply	VRTC	-0.5		4.0	V
Single Supply Port	VIN_3V3	0.5		4.0	V
OTP Supply	VPP		TBD		V
Signal Pin Voltage[1]	VI	-0.3		Voltage Domain + 0.3	V

Note:

1. Reference domain voltage is the Voltage Domain per section GS2101Mxx Module Pins Description. For limitations on state voltage ranges, please consult section on GS2101Mxx Module Pins Description.

4.2 Operating Conditions

Table 11, page 44 lists the operating conditions of the GS2101Mxx module.

Table 11 Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Extended Temperature Range	T_A	-40		+85	^oC
RTC Power Supply	VRTC	1.6	3.3	3.6	V
Single Supply Port GS2101MIx	VIN_3V3	2.7	3.3	3.6	V
Signal Pin Voltage[1]	VI	0		Voltage Domain	V
VPP[2]	VPP	5.5	5.75	6.0	V

Notes:

1. Reference domain voltage is the Voltage Domain per section GS2101Mxx Module Pins Description.
2. The VPP pin should be left floating when not doing OTP programming operations.

4.3 I/O DC Specifications

4.3.1 I/O Digital Specifications (Tri-State) Pin Types 4mA, 12mA, and 16mA

The specifications for these I/O's are given for voltage ranges: 2.7V to 3.6V.

4.3.1.1 I/O Digital Specifications for VDDIO=2.7V to 3.6V

Table 12, page 45 lists the parameters for I/O digital specification for VDDIO 2.7V to 3.6V for Pin Types 4mA, 12mA, and 16mA.

Table 12 I/O Digital Parameters for VDDIO=2.7V to 3.6V

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Note
I/O Supply Voltage	V_{DDIO}	2.7	3.3	3.6	V	
Input Low Voltage	V_{IL}	-0.3		$0.3*V_{DDIO}$	V	
Input High Voltage	V_{IH}	$0.7*V_{DDIO}$		V_{DDIO}	V	
Input Leakage Current	I_L			10	µA	Pull up/down disabled
Tri-State Output Leakage Current	I_{OZ}			10	µA	Pull up/down disabled
Pull-Up Resistor	R_u	34K	51K	100K	Ω	
Pull-Down Resistor	R_d	35K	51K	100K	Ω	
Output Low Voltage	V_{OL}			0.4	V	
Output High Voltage	V_{OH}	$0.8*V_{DDIO}$			V	
Low Level Output Current @ V_{OL} max	I_{OL}	4 12 16			mA	Pin Type 4mA Pint Type 12mA Pint Type 16mA
High Level Output Current @ V_{OH} min	I_{OH}	4 12 16			mA	Pin Type 4mA Pin Type 12mA Pin Type 16mA
Output rise time 10% to 90% load, 30pF	t_{TRLH}	3.1 1.8 1.5	4.2 2.4 2.0	7 4 3.4	ns	Pin Type 4mA Pint Type 12mA Pin Type 16mA
Output fall time 90% to 10% load, 30pF	t_{TFHL}	3.8 1.8 1.5	5.0 2.5 2.1	8 4.2 3.5	ns	Pin Type 4mA Pin Type 12mA Pin Type 16mA

4.3.2 RTC I/O Specifications

Table 13, page 46 lists the RTC I/O parameters.

Table 13 RTC I/O Parameters

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Note
Supply Voltage	VRTC	1.6		3.6	V	
Input Low Voltage	V_{IL}	-.03		$0.3*V_{RTC}$	V	
Input High Voltage	V_{IH}	$0.7*V_{RTC}$		VRTC+0.3	V	
Input Leakage Current	I_L			0.1	µA	
Pullup Current	I_{PU}		1		µA	
Pulldown Current	I_{PU}		1		µA	
Output Low Voltage	V_{OL}			0.4	V	IL=1mA or 4mA*
Output High Voltage	V_{OH}	VRTC-0.4			V	IL=1mA or 4mA*

*RTC I/O's are software selectable as 1mA or 4mA drive strength.

4.4 Power Consumption

Table 14, page 47 lists the power consumption for the GS2101Mxx. Typical conditions are: VIN_3V3=VRTC=3.3V Temp=25^{o}C.

Table 14 Power Consumption in Different States

System State	Current (Typical)[1]
Standby (VIN_3V3 ON)	50µA
Deep Sleep (see Note 2)	615µA
WLAN Continuous Transmit (1 Mbps, 16 dBm)	355 mA
WLAN Continuous Receive (1 Mbps, -90 dBm sensitivity)	135 mA
IEEE 802.11 PS-Poll, DTIM=1 (see Note 3)	7 mA
IEEE 802.11 PS-Poll, DTIM=3 (see Note 3)	2.5 mA
IEEE 802.11 PS-Poll, DTIM=10 (see Note 3)	1.2 mA

Notes:

1. Depends on firmware version.

2. One Sigma ($\pm$200µA).

3. This is average current draw measurements.

4.5 802.11 Radio Parameters

Table 15, page 48 lists the 802.11 Radio parameters. Test conditions are: VIN_3V3=VRTC=3.3V Temp=25^{o}C.

Table 15 802.11 Radio Parameters - (Typical - Nominal Conditions)

Parameter	Minimum	Typical	Maximum	Unit	Notes
RF Frequency Range	2400		2497	MHz	N/A
Radio bit rate	1		HT20 MCS7	Mbps	N/A
Transmit/Receive Specification for GS2011M					
Output power (average)		15 12 11 14 14 8 14 11 4		dBm	11b, 1Mbps 11b, 5.5Mbps 11b, 11Mbps 11g, 6Mbps 11g, 18Mbps 11g, 54Mbps 11n, MCS0 11n, MCS3 11n, MCS7
Spectrum Mask				dBr	Meets 802.11 requirement for selected data rates
Receive Sensitivity at antenna port		-90 -84 -86 -71 -86 -67		dBm	11b, 1Mbps, BPSK/DSSS 11b, 11Mbps 11g, 6Mbps 11g, 54Mbps, 64-QAM/OFDM 11n, MSC0 11n, MCS7, 64-QAM/OFDM

NOTE: *TX output power and RX sensitivity are firmware dependent. All the values provided for these parameters are measured at the antenna port based on 5.2.1 GA firmware.*

4.6 Sigma Delta ADC Parameters

Table 16, page 49 lists the Sigma Delta ADC parameters. Test conditions are: VIN_3V3=VRTC=3.3V Temp=25°C.

Table 16 ADC Parameters

Parameter	Minimum	Typical	Maximum	Unit	Notes
D/A DC Performance (see Note 1)					
Resolution	-	16	-	Bits	
Full Scale		2.4	0	V	See Note 2
Output common-mode level		VIN_3V3/2			
Gain Error	-	-	±5	%	See Note 2
Offset	-	-	±20	mV	
D/A Dynamic Performance					
Data Rate	32	-	80	KHz	
Clock Frequency	8	-	20	MHz	See Note 3
Signal to Noise Ratio (SNR)		67	-	dB	See Note 4
Total Harmonic Distortions (THD)	-	-74		dB	
Output load	10			KΩ	
Output load			30	pF	
A/D DC Performance (Preamplifier Gain=0db)					
Resolution		16		Bits	
Full Scale		2.0		V	
Input common-mode level		VIN_3V3/2			
Gain Error			±3	%	
Offset			±10	LSB	
A/D Dynamic Performance (Preamplifier Gain=0db)					
Data Rate	32		80	KHz	
Clock Frequency	8		20	MHz	See Note 3
Signal-to-Noise Ratio (SNR)		80		dB	See Note 4
Total Harmonic Distortion (THD)		-85		dB	See Note 4
Input Resistance	100			KΩ	

Notes:

1. The D/A output is fully differential. The Analog power supply is 3.3V +/- 10%.
2. Full scale (FS) can be trimmed in the reference generator. The gain error specified is on top of the reference level error.
3. The master clock frequency is always 250 times higher than data clock rate.
4. Assumes a -1 dB full scale input and corrected for full scale. Fin can be from 0 to 10KHz. The SNR is met for all master clock frequencies.

Chapter 5 Package and Layout Guidelines

This chapter describes the GainSpan® GS2101M package and layout guidelines.

5.1 GS2101Mxx Recommended PCB Footprint and Dimensions

Figure 4, page 51 shows the GS2101MIx Module PCB Footprint. Figure 5, page 52 shows the GS2101MIx Module Dimensions.

Figure 4 GS2101MIx Module Recommended PCB Footprint (in millimeters)

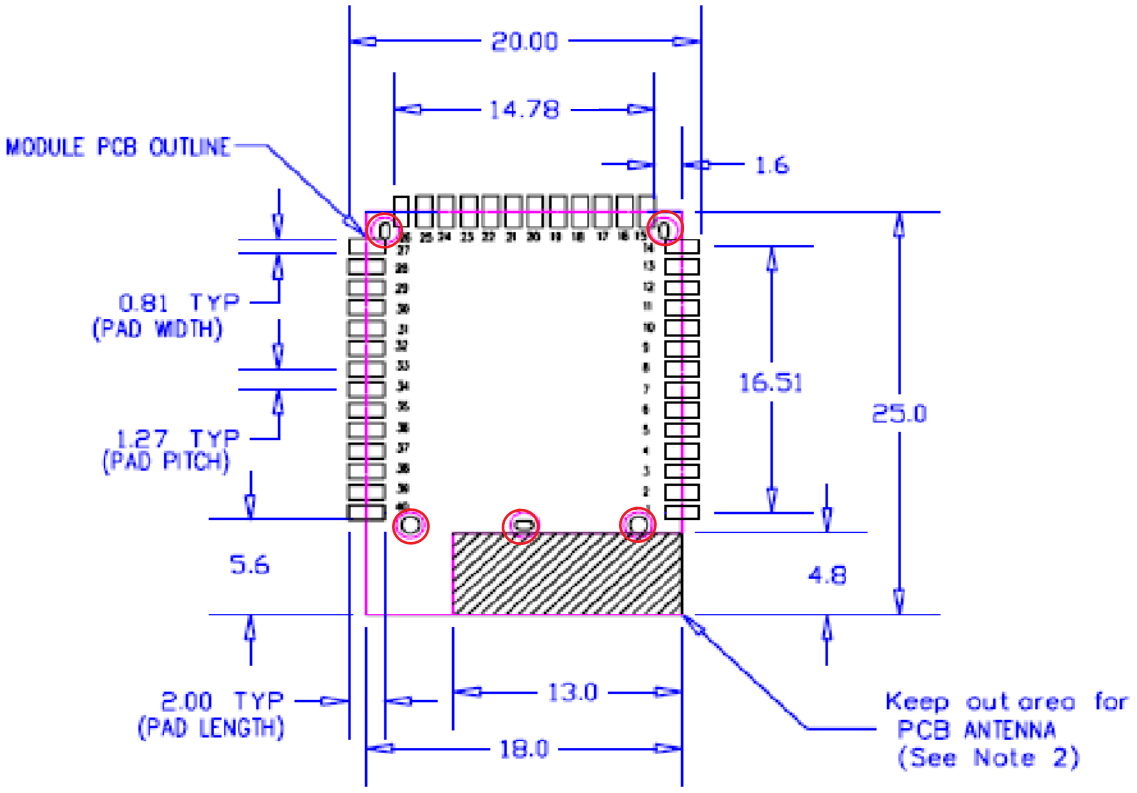
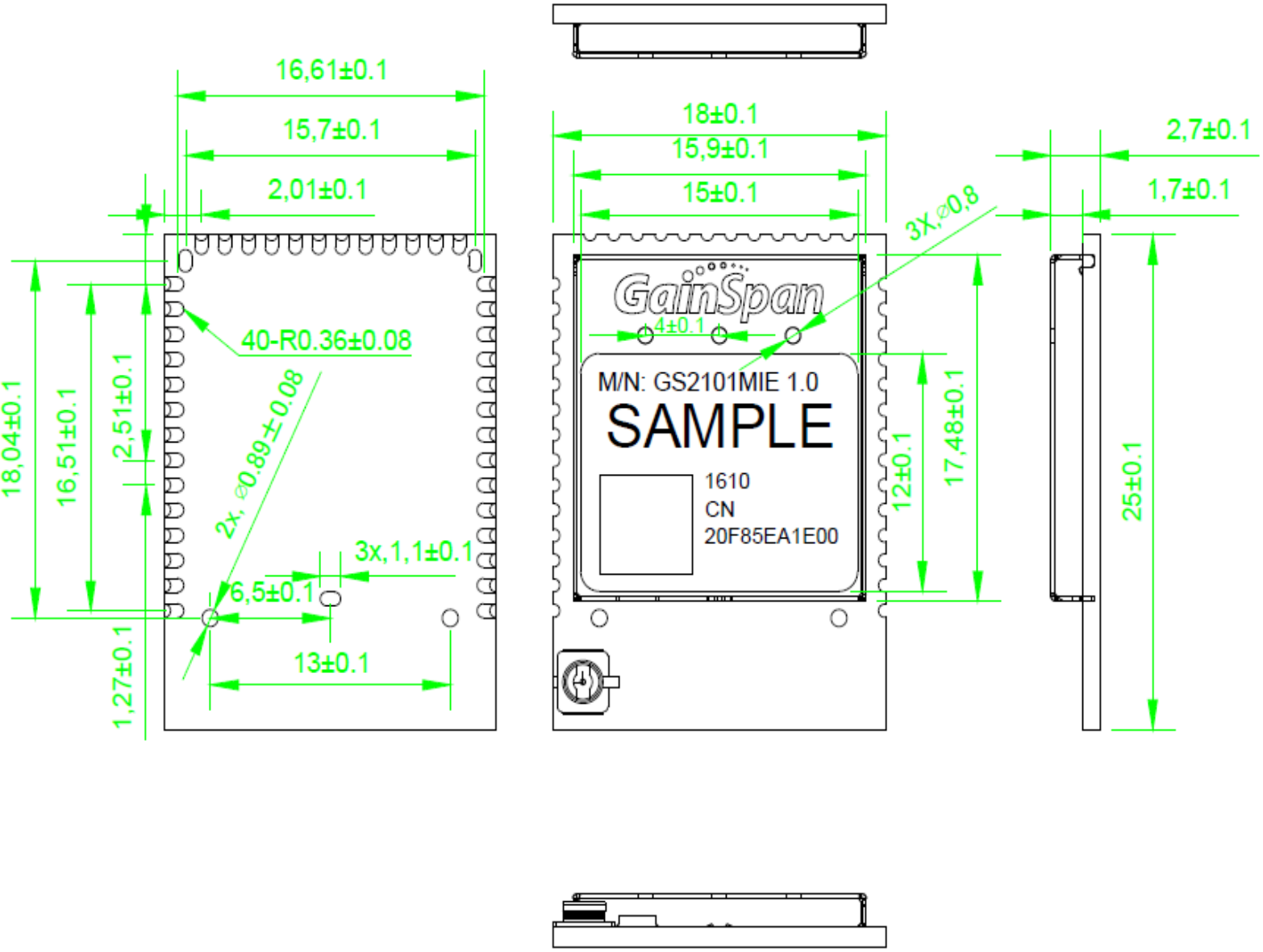


Figure 5 GS2101MIx Module Dimensions (in millimeters)



Notes:

1. All Dimensions are in millimeters (mm).
2. For Boards using PCB Antenna, we recommend:
   - Have Only Air on BOTH sides of antenna.
   - Hang Antenna over edge of base board (best)
   - Or Cut notch in base board under antenna area
     - 5mm beyond module edge on both sides is good
     - Full module width is minimum
   - No metal or FR4 encircling antenna area

- Antenna at edge of base board, not interior of base board
- Nothing conductive near antenna (e.g. battery, display, wire)

3. The 3 RF shield mounting holes and 2 test fixture alignment holes (circled in red in Figure 4, page 51) have exposed metal. These areas must not have metal on the customer board.
4. For best RF performance, we recommend:
   - Using power(PWR) or the GND planes from module back to power supply.
   - Isolating PWR/GND from high frequency or high current components. For example, a notch in GND plane to isolate from host uC
   - Using at least 3 vias when either power or GND changes layers. This applies particularly at the module GND pins and at the VIN_3V3 pins.
   - Providing a 10 uF capacitor at the VIN_3V3 pin and using 3 vias both sides of the capacitor.
   - Keep high speed signals away from RF areas of module.
5. For area under Module, other than antenna area, we recommend two options:
   - No metal of any kind under module “not on any layer”
   - Having full GND plane under module (layer 1 or layer 2) with no “HOT” vias under module (over 100KHz) and may route signals below GND plane. Also no metal traces are to be present in the circle, around shield and alignment holes (see datasheet). This option is best for 2 layer boards. If GND plane is on layer 1, then use thermal relief pads for the GND pins of the module footprint.
6. If any metal is present on layer 1, then extra thick solder mask under the module is required.
7. In performing SMT or manual soldering of the module to the base board, first align the row of pins from #15 through #26 onto the base board and then match the other two rows.

In addition to the guidelines, note the following suggestions:

1. External Bypass capacitors for all module supplies should be as close as possible to the module pins.
2. Never place the antenna very close to metallic objects.
3. External monopole antennas need a reasonable ground plane area for antenna efficiency.
4. Do not use a metallic or metalized plastic for the end product enclosure when using on-board antenna.
5. If the module is enclosed in a plastic case, have reasonable clearance from plastic case to on-board antenna.

5.1.1 Surface Mount Assembly

The reflow profile is shown in Figure 6, page 54. The recommended reflow parameters are summarized in Table 17, page 54.

Figure 6 Reflow Temperature Profile

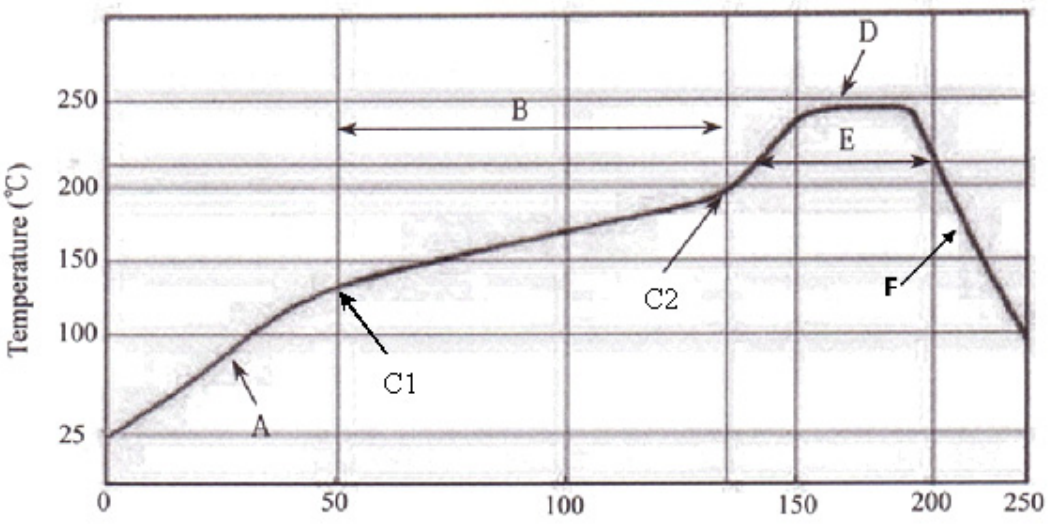


Table 17 Recommended Reflow Parameters

Preheat	
Temperature Ramp up rate for (A)[2]	1.5~3.5 °C/s
Pre-heat time (B)[3]	80 to 130 seconds
Pre-heat starting temperature (C1)	125 to 135 °C
Pre-heat ending temperature (C2)	180 to 200 °C
Heating[5]	
Peak Temperature range (D)	240 to 250 °C
Melting time[4] that is the time over 220 °C (E)	50 to 75 seconds
Cool Down Ramp (F)	>2 °C/s

Notes:

1. Perform adequate test in advance as the reflow temperature profile will vary according to the conditions of the parts and boards, and the specifications of the reflow furnace.
2. Max number of reflow supported are two.
3. Temperature uniformity inside the IR reflow oven must be tightly controlled and multiple thermocouples should be used. An example of possible thermocouple locations is given in Figure 7, page 56. The locations should also include multiple points INSIDE the module RF shield (e.g., TC1, TC5, and TC7 in Figure 7, page 56). The temperature profile of ALL thermocouples must meet the requirements of Table 17, page 54.

4. Pay close attention to “Melting Time over 220^{o}C”. Sufficient time is necessary to completely melt all solder.
5. Be careful about rapid temperature rise in preheat zone as it may cause excessive slumping of the solder paste.
6. If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will generate in clusters at a time.
7. If the temperature is too low, non-melting tends to be caused in the area with large heat capacity after reflow.
8. Be careful about sudden rise in temperature as it may worsen the slump of solder paste.
9. Be careful about slow cooling as it may cause the positional shift of parts and decline in joining at times.
10. A no clean flux should be used during SMT process.

The modules are shipped in sealed trays with the following conditions (see Figure 8, page 57).

Figure 7 Thermocouple Locations

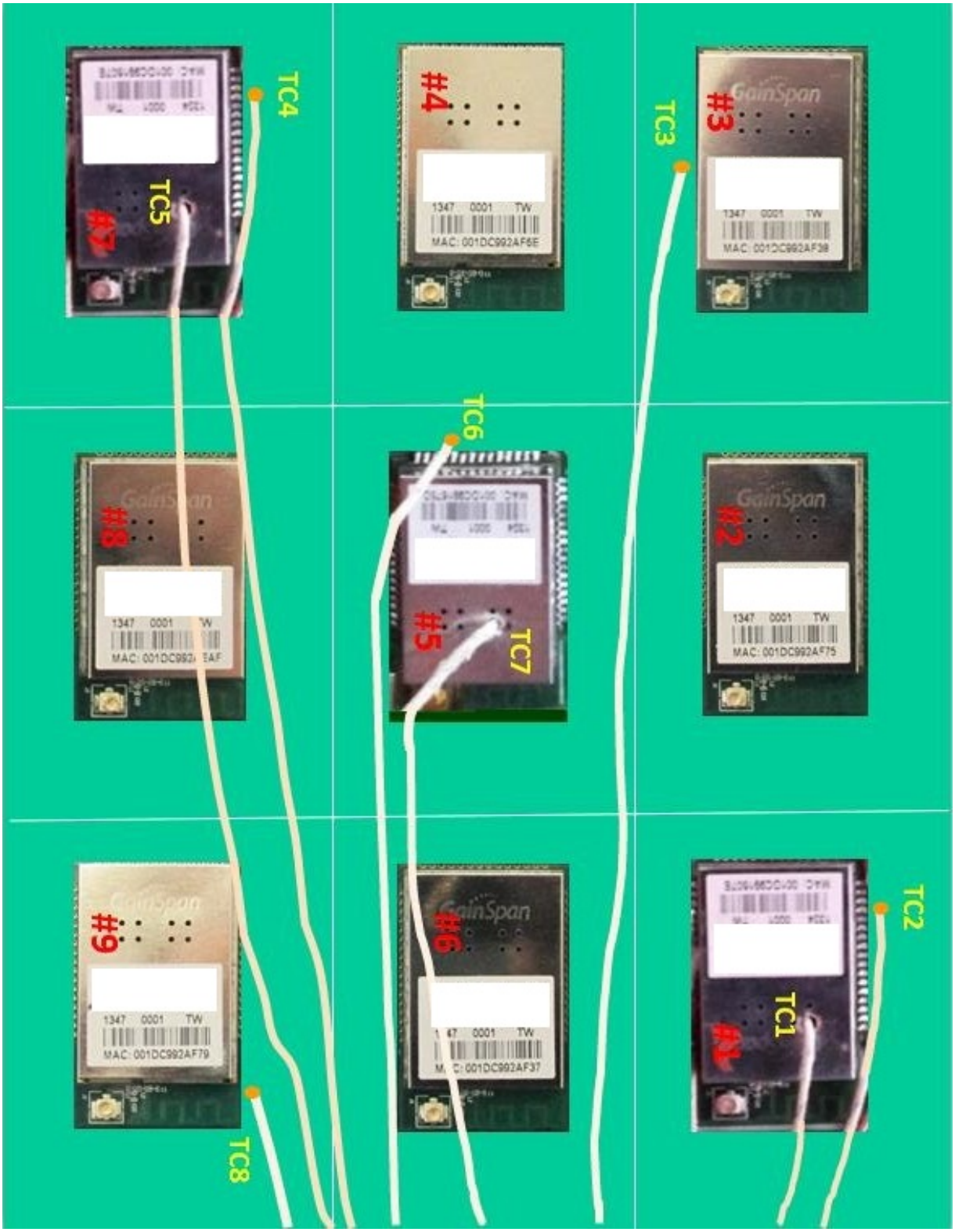


Figure 8 Module Moisture Conditions