Product function:

1. **GPRS Multi-slot Class: 12**

- Programmable GSM/GPRS modem
- Packet switched data with CS1/CS2/CS3/CS4 coding schemes

2. **FM**

- Support 76~108 MHz band

3, Bluetooth

- Fully compliant with Bluetooth specification 3.0 + EDR
- Low out-of-band spurious emissions support simultaneous operation with GPS and GSM/GPRS worldwide radio systems
- Low-IF architecture with high degree of linearity and high order channel filter
- Integrated T/R switch and Balun
- Fully integrated PA provides 10dBm output power
- -95dBm sensitivity with excellent interference rejection performance
- Hardware AGC dynamically adjusts receiver performance in changing environments

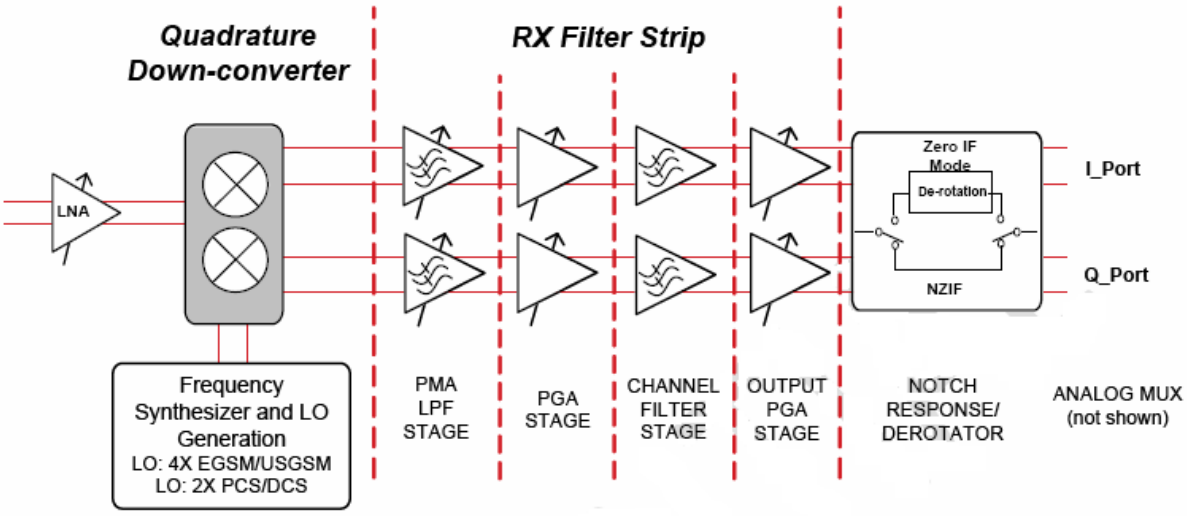
RF portion(GSM/GPRS)

Receiver operation

The frequency ranges of the synthesizer for RX mode are
RX mode GSM850 869 – 894 MHz,
GSM900 925-960 MHz
DCS1800 1805~1880 MHz
PCS 1930 – 1990 MHz

Ø ZOF receive architecture
Ø Typical Cascaded noise figure is 2.8dB *
Ø 90dB total gain for RX MT6260
Ø Digitally selectable gain with 1dB steps

Figure 1: MT6260 **Receive Chain**

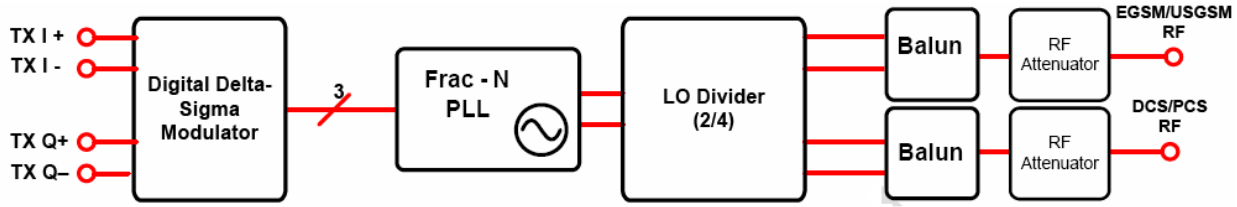


The receiver in the MT6260 can be set to Zero-IF or to a Near Zero-IF mode (NZIF). The receiver mode is programmed over the RCB. The RF portion of the receiver for each frequency of operation includes an LNA with adjustable gain settings to maximize the dynamic range of the receiver. The down-converter portion of the receiver is split into two sections, a high band down-converter for PCS and DCS, and a low-band down-converter for EGSM and USGSM. The receive ports are balanced and matched for 200Ω to support standard RF SAW filters. The RX filter strip in the receiver paths comprises a PMA low pass filter (3rd order Chebyshev) PGA stage, Channel Filter (3rd order Legendre). This is the same for ZIF mode and NZIF mode. This ensures operation over a broad range of gain settings. The channel filter ensures rejection of strong in-band and out-of-band blockers.

In order to minimize the set-up of the MT6260, extensive on-chip automatic calibration has been implemented. Random DC offsets generated in the MT6260 are calibrated out. Automatic DC calibration ensures that externally generated DC offsets do not overload the receive chain. An on-chip state machine generates the timing control signals for this DC calibration and the calibration routine is initiated via the RCB. In normal operation the state machine is started, the RX filter strip is powered up and any inherent DC offsets are removed. These correction signals are then held constant as the RF front end is powered up for the receive chain to process the incoming signal. None of these calibrations require any interaction with the baseband sub-system.

TX mode

GSM850 824 – 849 MHz,
GSM900 880-915 MHz
DCS1800 1710~1785MHz
PCS 1850 – 1910MHz

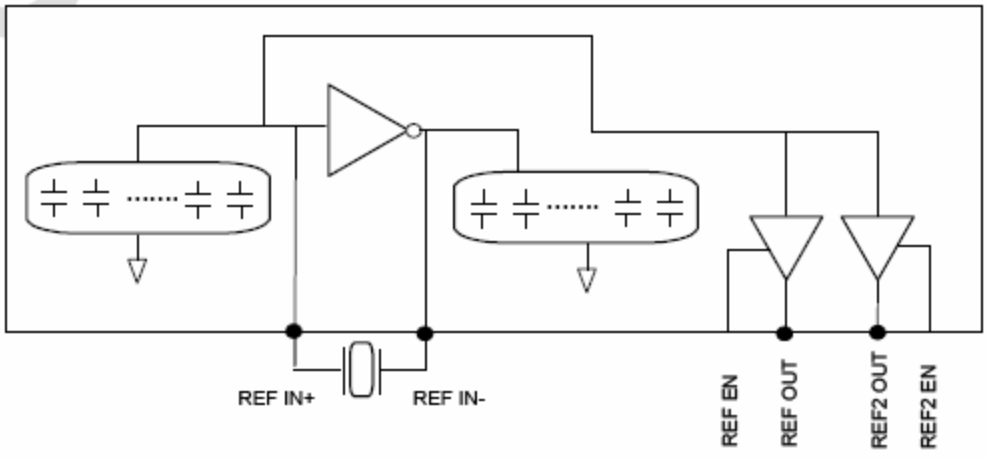


The transmit chain of the MT6260 consists of a direct LO modulation transmit path for GSM (GMSK). The LO is modulated directly by the baseband signal by a digital delta-sigma modulator. The modulated output of the modulator is mixed with a DC voltage and the resultant output is then converted to a single ended waveform via an on chip balun. The RF output power level is adjusted to an appropriate level via the on chip RF attenuator.

The RF ports of the transmitter are single-ended and matched to 50Ω. No off-chip RF baluns or filters are required.

FREQUENCY SYNTHESIS

Figure 3: Reference Oscillator Configuration



There are two frequency sources on the MT6260 The first is the RF frequency synthesizer, which serves as the LO for both receive and transmit chains. The VCO for the synthesizer is fully integrated and no calibration is required as this is all performed automatically on the MT6260. During reception or transmission in normal operation, the frequency synthesizer is operated at twice the desired channel of operation in PCS and DCS modes and at four times the desired channel of operation in EGSM and USGSM modes. On-chip dividers (÷2 for PCS/DCS and ÷4 EGSM/USGSM) reduce the frequency of the signal. The outputs of these dividers are buffered before being applied to the up or down converters. The loop filter of the frequency synthesizer is fully integrated. This reduced component count and form factor minimizes the number of sensitive components in the design.

Table 14: MT6260 LO Frequencies of Operation

FREQUENCY BAND	Transmitter Frequency	Receiver Frequency	Transmitter Synthesizer Frequency	Receiver Synthesizer Frequency
USGSM	824-849	869-894	3296-3396	3476-3576
EGSM	880-915	925-960	3520-3660	3700-3840
DCS1800	1710-1785	1805-1880	3420-3570	3610-3760
PCS1900	1850-1910	1930-1990	3700-3820	3860-3980

The second frequency source is the Digitally Controlled Crystal Oscillator (DCXO). The DCXO is designed to accept a crystal with fundamental frequency of 26MHz. After power-on of the chip, the DCXO starts oscillating. It continues oscillating until power-off or programming of doze mode.

The reference oscillator can be used with a 26MHz crystal. In this configuration, the reference frequency is controlled by on-chip capacitor banks that can be switched in via the RCB. This allows for precise tuning of the crystal when implemented with a conventional Automatic Frequency Control (AFC) loop.

The MT6260 can also be supplied with an external reference such as a 26MHz VCTCXO or other frequency source.

The reference clock signal generated in the chip is buffered before being sent to the Phase Locked Loop in the frequency synthesizer block. Either a square wave or a clipped sine wave can be selected. The buffer is capable of driving a reference clock line with a load capacitance of 10pF.

There are two 26MHz reference clock output ports on the MT6260, REF OUT and REF2 OUT. Each output is independently controlled by its enable ports, REF EN and REF2 EN.

FM portion

The receiver employs a digital low-IF architecture that reduces external components, and integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (65 to 108MHz), an automatic gain control (AGC) circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers, an image-reject mixer down converts the RF signal to low-IF, The mixer output is amplified by a programmable gain control (PGA), and digitized by a high resolution analog-to-digital converters (ADCs). An audio DSP finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomous switch from stereo to mono to limit the output noise.

Bluetooth

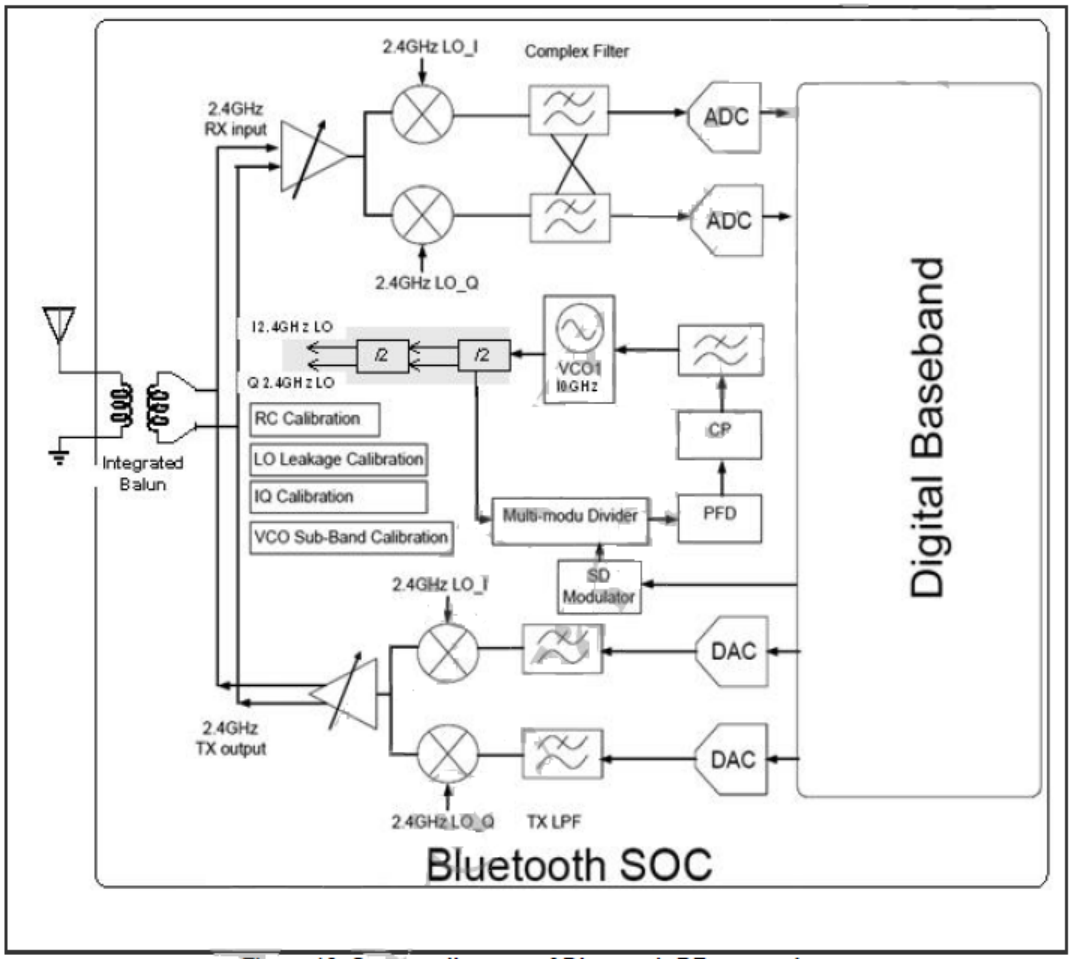


*Figure 16. **System diagram of Bluetooth RF transceiver***

The Bluetooth RF subsystem contains a fully integrated transceiver.

For TX path, the baseband transmit data are digitally modulated in the baseband processor then up-converted to 2.4GHz RF channels through the DA converter, filter, IQ up-converter and the power amplifier. The power amplifier is capable of transmitting 10dBm power for class-1.5 operation.

For RX path, MT6260A is a low IF receiver architecture. An image-reject mixer down-converts the RF signal to the IF with the LO from the synthesizer, which supports different clock frequencies as the reference clock. The mixer output is then converted to digital signal and down-converted to baseband for demodulation. A fast AGC enables the effective discovery of device within the dynamic range of the receiver.