EXHIBIT 2

TECHNICAL DESCRIPTION, Part 2.1033(c)

TYPES OF EMISSION, Parts 2.1033(c)(4), 80.207(d), 90.207(c)

VOICE Mode: 16K0F3E and 11K2F3E
DSC Mode: 13K5G2D
GMSK Mode: 11K2F2D

FREQUENCY RANGE, Part 2.1033(c)(5):

Transmit: 156.0 to 157.5 MHz
Receive: 155.0 to 164.0 MHz

RANGE OF OPERATING POWER LEVELS, Part 2.1033(c)(6):

Two carrier power levels are provided: 25 watts and 1 watt. Power level is held constant by a closed-loop operating from a sample of the RF output. See Part 2.1033(c)(10) below for details.

MAXIMUM POWER LEVEL, Part 2.1033(c)(7): 25 watts carrier.

The transmitter complies with 80.215 and 90.215 concerning allowable maximum power, manual and automatic power reduction and manual power override.

DC VOLTAGES AND CURRENTS APPLIED TO FINAL AMPLIFIER,

Part 2.1033(c)(8):

Test conditions:

DC voltage measured at pin 3 (Hi dc) of RF power amplifier module U16 which is the dc power input point to final power amplifier stage (See transmitter schematic diagram in Preliminary Maintenance Manual.) DC current measured into same pin as above. Transmitter operated on a frequency in the middle of its range and set to 25 watts average output power.

DC Voltage: 13.6 Volts DC Current: 5.5 Amps

TUNE-UP PROCEDURE, Part 2.1033(c)(9)

See SEA 157S Preliminary Maintenance Manual (Enclosed), Chapter 4, "Installation" and Chapter 6, "Maintenance".

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FREQUENCY DETERMINING AND STABLILIZATION CIRCUITS, Part 2.1033(c)(10)

Block and schematic diagrams referenced below are located in Section 7 of the Preliminary Maintenance Manual. See the List Of Figures for aid in locating applicable reference drawings.

FREQUENCY SYNTHESIZER:

GENERAL: Refer to the functional block and schematic diagrams. The SEA 157S makes use of a multi-loop synthesizer system to provide conversion frequencies for the Receiver, and the Transmitter. The Main Transmitter synthesizer also serves as the first conversion loop for the Main Receiver and consists of the voltage controlled oscillator (VCO) Q1, RF buffers/amplifiers Q4 and Q3, synthesizer LSI chip U10, reference oscillator VCTCXO Y1, and the loop filter.

VCO: The low-noise VCO is a grounded-gate JFET oscillator operating in two frequency bands as selected by Q2 and D2. D2 is "off" for transmit and L5 and L6 set the frequency band to the 155-159mHzrange. D2 is "on" for receive and L6 sets the 176.4-185.4mHz receiver local oscillator (LO) range. The tuning voltage from the loop filter is applied to varactors D4 and D5. The tuning voltage ranges from 1 to 4 volts. As the cathodes of D4 and D5 are referenced to the +8 volt supply, lower voltages correspond to higher frequencies. The entire VCO and two stage buffer is on a separate pc board located in a shielded “pocket” in the chassis casting.

VCO RF AMPLIFIERS: Q4 and Q3 amplify the VCO signal up to +10 dBm (10 mW) nominal. The signal is then fed to the receiver mixer U3 via a resistive attenuator and also to the transmitter pre-driver Q10 via the Main Board diode D3. D3 is turned "on" only during transmission to supply approximately +10 dBm excitation to the transmitter amplifier chain.

SYNTHESIZER CHIP: A sample of the amplified VCO signal is derived from the output of Q3 and fed to the N and A dividers of U10. The N and A divider modulus is preset by the microcomputer via the clock, data and enable digital lines. The total frequency division (N and A) reduces the RF signal down to a 12.5kHz comparison frequency at U10's internal phase detector. For example, the total division for transmission on 156.80mHzis 156,800/12.5 = 12544. For a receive frequency of 156.mHz the required LO frequency is 156.80mHz+ 21.40mHz= 178.20mHzrequiring a division factor of 178.200/12.5 = 14,256.

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The 21.85mHz master reference oscillator is divided by a fixed 1748 modulus to produce the 12.5kHz reference frequency. The U10 phase detector output at pin 5 is tri-state and drives the loop filter. A separate lock detect (LD) output from U10 pin 14 goes low when out of lock. The LD signal is fed back to the microcomputer which disables the transmitter while in the unlocked state thus preventing the transmission of RF power outside the maximum frequency difference limits prescribed by Parts 80.209, 90.213, and 90.214".

MASTER REFERENCE OSCILLATOR: The master clock is provided by highly stable VCTCXO at 21.85mHz Y1. This oscillator has a specified frequency stability of +/-1ppm from –20 to 70 degrees C. The oscillator output is connected the input of the CMOS gate of the synthesizer IC, U10 pin 1. The output of this gate, U10 pin 2 provides a buffered 21.85mHz signal to the main and Channel 70 receiver boards.

LOOP FILTER: R64 on the main PCB and R3,R4,R13,C2,C4,C5,and C19 on the VCO PCB comprise the synthesizer loop filter

DESCRIPTION OF MODULATION LIMITING, POWER LIMITING AND SPURIOUS RADIATION SUPPRESSION CIRCUITRY, Part 2.1033(c)(10)

MODULATION CIRCUIT:

TRANSMITTER AUDIO PROCESSING: After a 20dB boost by amplifier IC U21, located on the main PCB, microphone audio is sent to be processed by the digital signal processor (DSP), U13, located on the Mezzanine PCB. The microphone audio signal is applied to the MICIN input of 16-bit audio CODEC, U8, where it is digitized and sent to the DSP. The DSP then feeds it through a digital filter/limiter process which filters the transmitter audio with a 3kHz lowpass filter. It then applies a 6db per octave pre-emphasis, limits the audio in a low distortion process and finally filters the audio again with a 3kHz lowpass filter. This method maximizes the average voice energy within the set deviation limit while minimizing audio harmonic distortion levels.

DSC DATA: The digital modulation signal is generated internally in a phase continuous digital sine wave generator. It is then fed into the transmitter audio processing (within the DSP) at the input of the pre-emphasis and then applied at a level below the limiting threshold of the audio processing and factory calibration for a modulation index of 2.

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FREQUENCY DEVIATION CONTROL: The transmitter peak deviation is controlled digitally by a factory set deviation multiplier constant which is stored in flash memory (U3 and U4). D2 on the VCO PCB is switched "on" during receive mode to switch VCO ranges and to insure that no modulation is applied to the synthesizer during receive operation.

TRANSMIT AMPLIFIER CHAIN:

GENERAL: Referring to Sheet 4 of the Mainboard Schematic Diagram, the transmit amplifier chain of the SEA 157S consists of the discrete RF amplifiers Q10 and Q9 and a two-stage hybrid RF power amplifier module U16.

PRE-DRIVERS: The buffered output signal from the frequency synthesizer is first amplified by Q10 and its output is coupled to the input of Q9. Q9 further amplifies the signal and applies it to the input (IN) of the power amplifier module U16. The RF signal from Q9 is however only available to the input of the power amplifier module when in the transmit mode and 13Vdc is present on 13V_TX bus to power Q10.

FINAL AMPLIFIER: U16 is a hybrid power amplifier module containing two gain stages. When the radio is on, 13.6Vdc is applied to the power amplifier module at all times. The power amplifier module will however only produce RF power when the radio is in the transmit mode and the RF signal from Q9 is available at the module input (IN). The amount of RF output produced by the power amplifier module is dependent on the level of bias voltage available to pin 2(PA) of the power amplifier module and to Q9 via R5, R6, and L5. This bias voltage is controlled by the amplifier consisting of Q5, Q13 and their associated components and the amount of control voltage available at the 1W_25W bus.

ANTENNA INTERFACE CIRCUITS:

TRANSMIT/RECEIVE SWITCHING: Antenna changeover between transmit and receive is accomplished by the PIN diode switches D33 on the Mainboard and D1 on the Receiver Board. In the transmit mode, voltage is applied to the 13_VTX bus and current passes through R43, R72, R62, L7, R2, R2A, L1, and D33 on the mainboard and finally to ground through L1 and D1 on the Receiver board. This current through D33 causes it to become forward biased and pass RF power from the power amplifier module to the low-pass filter consisting of L2, L3, L4, and their associated capacitors.

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The DC current flow though D1 also causes it to become forward biased and short-circuits the input to the receiver. The short-circuit in addition causes the input impedance of the 1/4 wave matching section comprised of C1, L1, and, C2 on the Receiver board to become high and effectively isolates the receiver from the transmitter RF.

TRANSMIT/RECEIVE ANTENNA FILTERING: The 7-section low-pass filter comprised of C4, L1, C5, C7, L2, C126, C8, L3, C127, C9, L4, and C10 provides VHF and UHF attenuation of the transmitter harmonics and receiver images.

AUTOMATIC RF POWER CONTROL (APC) AND TX LOGIC:

In transmit mode a negative feedback control system continuously monitors and if necessary, corrects the output power level at the antenna terminals. C119 samples the RF voltage at the RF power amplifier module output terminal (4). Diode D34 converts this RF signal to a DC level representing the output power level. This DC power level signal is fed to one channel of the internal A/D converter of CPU IC, U1, located on the Mezzanine board. The digitized signal is processed by a power control routine, which, through the D/A converter U17, drives the DC amplifier consisting of Q5 and Q13 to provide the correct DC supply voltage to Q9 and bias to the power amplifier module U16. This RF power level closed-loop system thus maintains the RF output power at the proper level. Two references are used in the control routine which correspond to 1 watt or 25 watt output levels. When adjusted according to the alignment instructions, the APC system will closely maintain the 1W or 25W output level (as selected) over a wide range of power supply voltage and ambient temperatures. In the unlikely event that the automatic power control system should fail, the power amplifier cannot produce much more 30 watts.