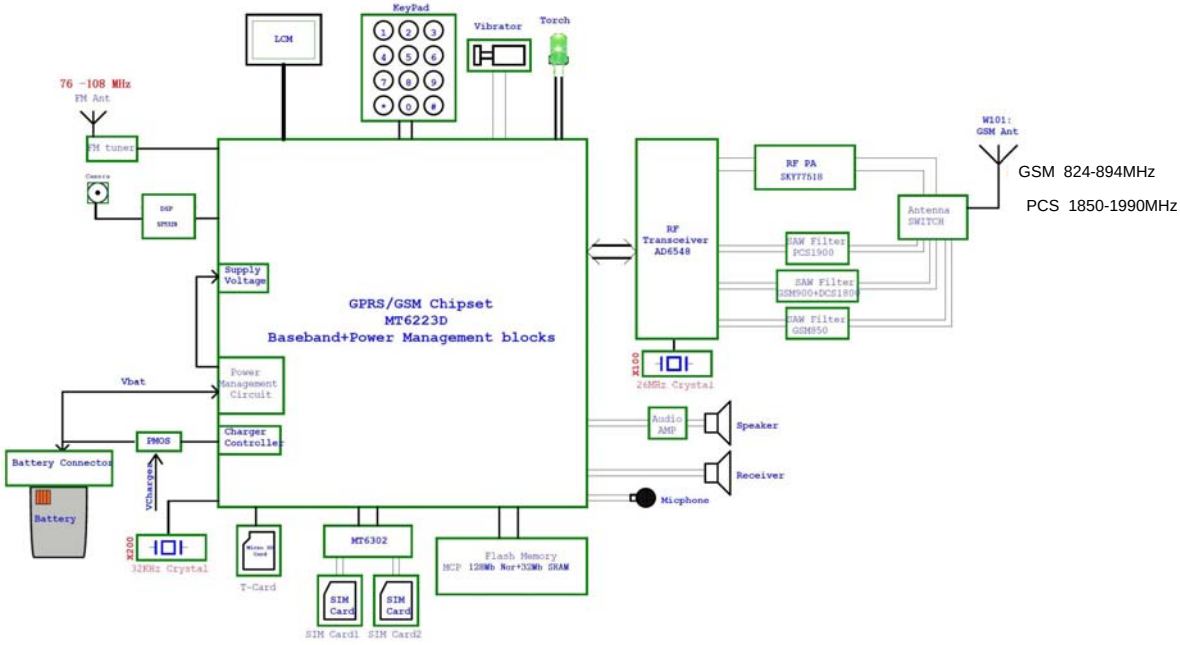
V600 MainBoard System design

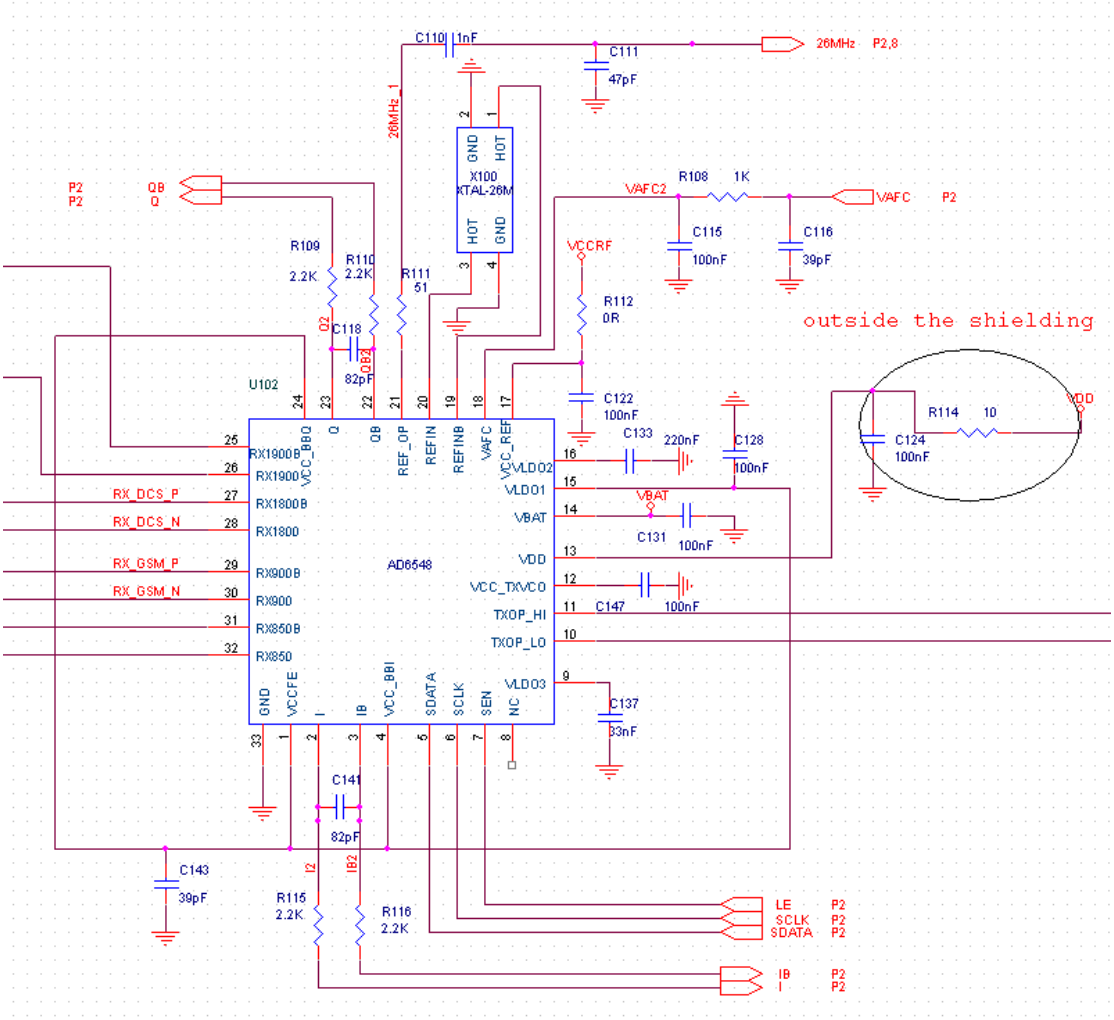
1. General description

V600 Mainboard is based on MTK6223D platform to develop and design. It support dual-band RF communication; 300,000 pixel camera sensor; T-Flash Card; FM radio; mp3 / MPEG4 player and so on.



2. RF

Transeiver



U100 is baseband IC: AD6548 **Single Chip GSM Radio**

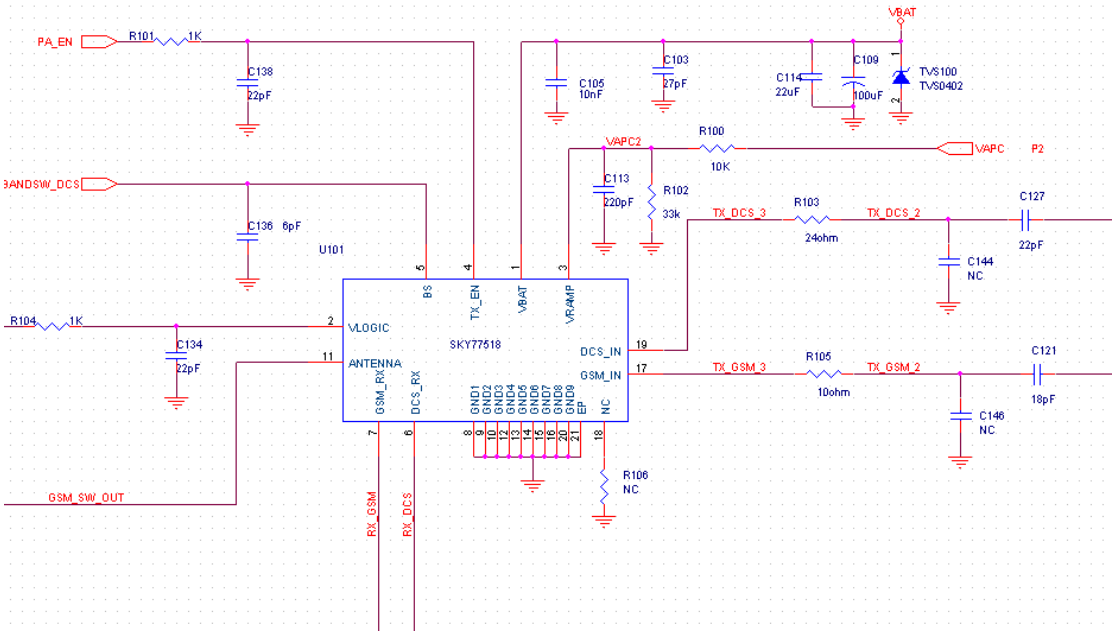
The AD6548 provides a highly integrated direct conversion radio solution that combines, on a single chip, all radio and power management functions necessary to build the most compact GSM radio solution possible. The only external components required for a complete radio design are the Rx SAWs, PA, Switchplexer and a few passives enabling an extremely small cost effective GSM Radio solution.

The AD6548 uses the industry proven direct conversion receiver architecture of the OthelloTM family. For Quad band applications the front end features four fully integrated programmable gain differential LNAs. The RF is then downconverted by quadrature mixers and then fed to the baseband programmable-gain amplifiers and active filters for channel selection. The Receiver output pins can be directly connected to the baseband analog processor. The Receive path features automatic calibration and tracking to remove DC offsets.

The transmitter features a translation-loop architecture for directly modulating baseband signals onto the integrated TX VCO. The translation-loop modulator and

TX VCO are extremely low noise removing the need for external SAW filters prior to the PA.
The AD6548 uses a single integrated LO VCO for both the receive and the transmit circuits. The synthesizer lock times are optimized for GPRS applications up to and including class 12. To dramatically reduce the BOM both TX Translational loop and main PLL Loop Filters are fully integrated into the device.
AD6548 incorporates a complete reference crystal calibration system. This allows the external VCTCXO to be replaced with a low cost crystal. No other external components are required.
The AD6548 also contains on-chip low dropout voltage regulators (LDOs) to deliver regulated supply voltages to the functions on chip, with a battery input voltage of between 2.9V and 5.5V. Comprehensive power down options are included to minimize power consumption in normal use.
A standard 3 wire serial interface is used to program the IC. The interface features low-voltage digital interface buffers compatible with logic levels from 1.6V to 3.0V.

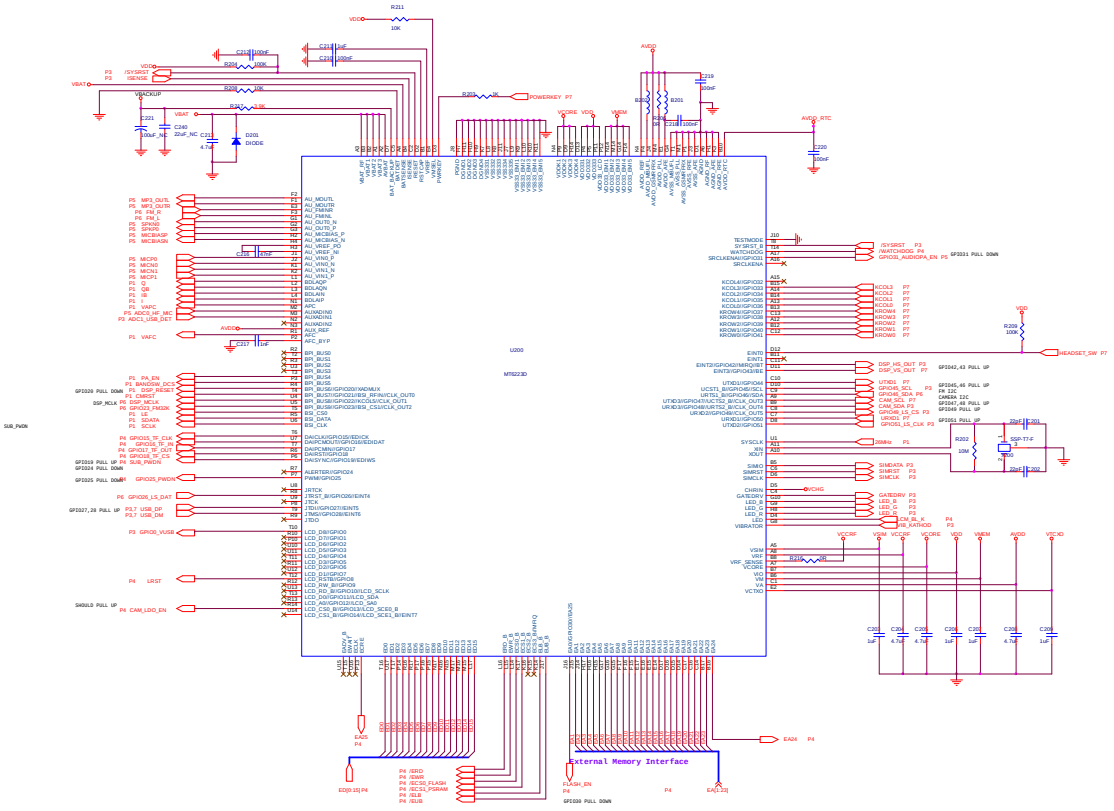
PA



The SKY77518-21 is a transmit and receive front-end module (FEM) with Integrated Power Amplifier Control (iPAC™) for dual-band cellular handsets comprising GSM850/GSM900 and DCS1800/PCS1900 operation. Designed in a low profile, compact form factor, the SKY77518-21 offers a complete Transmit VCO-to-Antenna and Antenna-to-Receive SAW filter solution. The FEM also supports Class 12 General Packet Radio Service (GPRS) multi-slot operation.
The module consists of a GSM850/GSM900 PA block and a DCS1800/PCS1900 PA block, impedance-matching circuitry for 50 Ω input and output impedances, TX harmonics filtering, high linearity and low insertion loss PHEMT RF switches, diplexer and a Power Amplifier Control (PAC) block with internal current sense resistor. A custom BiCMOS integrated circuit provides the internal PAC function and

decoder circuitry to control the RF switches. The two Heterojunction Bipolar Transistor (HBT) PA blocks are fabricated onto a single Gallium Arsenide (GaAs) die. One PA block supports the GSM850/GSM900 band and the other PA block supports the DCS1800/PCS1900 band. Both PA blocks share common power supply pads to distribute current. The output of each PA block and the outputs to the two receive pads are connected to the antenna pad through PHEMT RF switches and a diplexer. The GaAs die, PHEMT die, Silicon (Si) die and passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic overmold.
Band selection and control of transmit and receive modes are performed using two external control pads. The band select pad (BS) selects between GSM and DCS modes of operation. The transmit enable (TX_EN) pad controls receive or transmit mode of the respective RF switch (TX = logic 1). Proper timing between transmit enable (TX_EN) and Analog Power Control (VRAMP) allows for high isolation between the antenna and TX-VCO while the VCO is being tuned prior to the transmit burst.
The SKY77518-21 is compatible with logic levels from 1.2 V to VCC for BS and TX_EN pads, depending on the level applied to the VLOGIC pad. This feature provides additional flexibility for the designer in the selection of FEM interface control logic.
the main signal include:
VBAT: Battery input voltage
VLOGIC: Control logic level selection/Standby control
VRAMP: Analog power control voltage input
TX_EN: TX / RX select (mode control)
BS: Band Select (mode control)
DCS_RX: DCS Receive RF Output (1805-1880 MHz)/ PCS Receive RF Output(1930-1990 MHz)
GSM_RX: GSM900 Receive RF Output (920-960 MHz)/ GSM850 Receive RF Output (869-894 MHz)
ANT: RF_IN / RF_OUT to Antenna
GSM_IN: RF input 880–915 MHz/824-849 MHz
DCS_IN: RF input 1710-1785 MHz
PCS_IN: RF input 1850-1910 MHz

3. BB



U200 is baseband IC: **MT6223D GSM/GPRS Baseband Processor**

MT6223D is an entry level chipset solution with class 12 GPRS/GSM modem. It integrates not only analog baseband but also power management blocks into one chip and can greatly reduce the component count and make smaller PCB size. Besides, MT6223D is capable of SAIC (Single Antenna Interference Cancellation) and AMR speech. Based on 32 bit ARM7EJ-STM RISC processor, MT6223D provides an unprecedented platform for high quality modem performance.

Typical application diagram is shown in **Figure** 1.

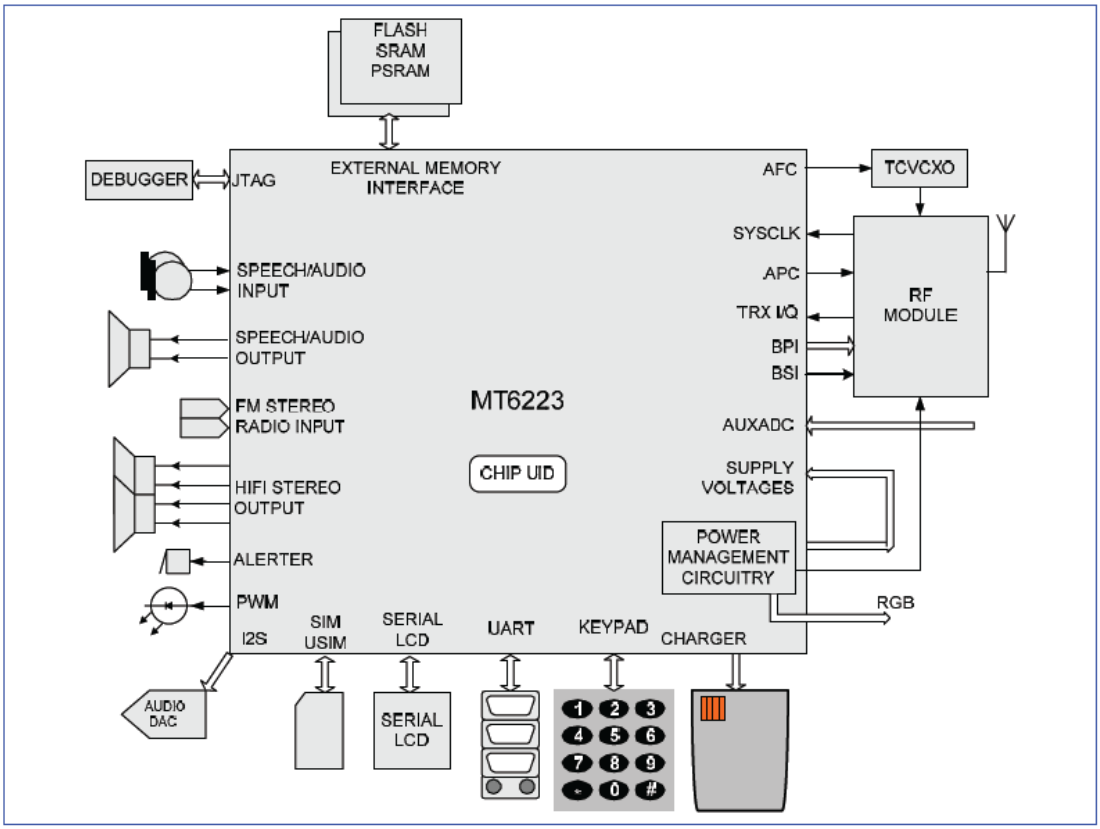


Figure 1 Typical application of MT6223D.

Platform

MT6223D runs the ARM7EJ-STM RISC processor at up to 52Mhz, thus providing best trade-off between system performance and power consumption.

For large amount of data transfer, high performance DMA (Direct Memory Access) with hardware flow control is implemented, which greatly enhances the data movement speed while reducing MCU processing load.

Targeted as a modem-centric platform for mobile applications, MT6223D also provides hardware security digital rights management for copyright protection. For further safeguarding, and to protect manufacturer's development investment, hardware flash content protection is also provided to prevent unauthorized porting of software load.

Memory

MT6223D supports up to 2 external state-of-the-art devices through its 16-bit host interface. Devices such as burst/page mode Flash, page mode SRAM, and Pseudo SRAM are supported. To minimize power consumption and ensure low noise, this interface is designed for flexible I/O voltage and allows lowering of supply voltage down to 1.8V. The driving strength is configurable for signal integrity adjustment. The data bus also employs retention technology to prevent the bus from floating during turn over.

Multi-media

MT6223D utilize high resolution audio DAC, digital audio, and audio synthesis technology to provide superior audio features., e.g. MP3 ring tone.

Connectivity, and Storage

MT6223D supports UART as well as Bluetooth interface. Also, necessary peripheral blocks are embedded for a voice centric phone: Keypad Scanner with the capability to detect multiple key presses, SIM Controller, Alerter, Real Time Clock, PWM, Serial LCD Controller, and General Purpose Programmable I/Os.

Audio

Using a highly integrated mixed-signal Audio Front-End, architecture of MT6223D allows for easy audio interfacing with direct connection to the audio transducers. The audio interface integrates D/A and A/D Converters for Voice band,as well as high resolution Stereo D/A Converters for Audio band. In addition, MT6223D also provides Stereo Input and Analog Mux. MT6223D also supports AMR codec to adaptively optimize speech and audio quality.

Radio

MT6223D integrates a mixed-signal Baseband front-end in order to provide a well-organized radio interface with flexibility for efficient customization. It contains gain and offset calibration mechanisms, and filters with programmable coefficients for comprehensive compatibility control on RF modules. This approach also allows the usage of a high resolution D/A Converter for controlling VCXO or crystal, thus reducing the need for expensive TCVCXO. MT6223D achieve great MODEM performance by utilizing 14-bit high resolution A/D Converter in the RF downlink path. Furthermore, to reduce the need for extra external current-driving component, the driving strength of some BPI outputs is designed to be configurable.

Low Power Features

MT6223D offers various low-power features to help reduce system power consumption. These features include Pause Mode of 32KHz clocking at Standby State, Power Down Mode for individual peripherals, and Processor Sleep Mode. In addition, MT6223D are also fabricated in advanced low leakage CMOS process, hence providing an overall ultra low leakage solution.

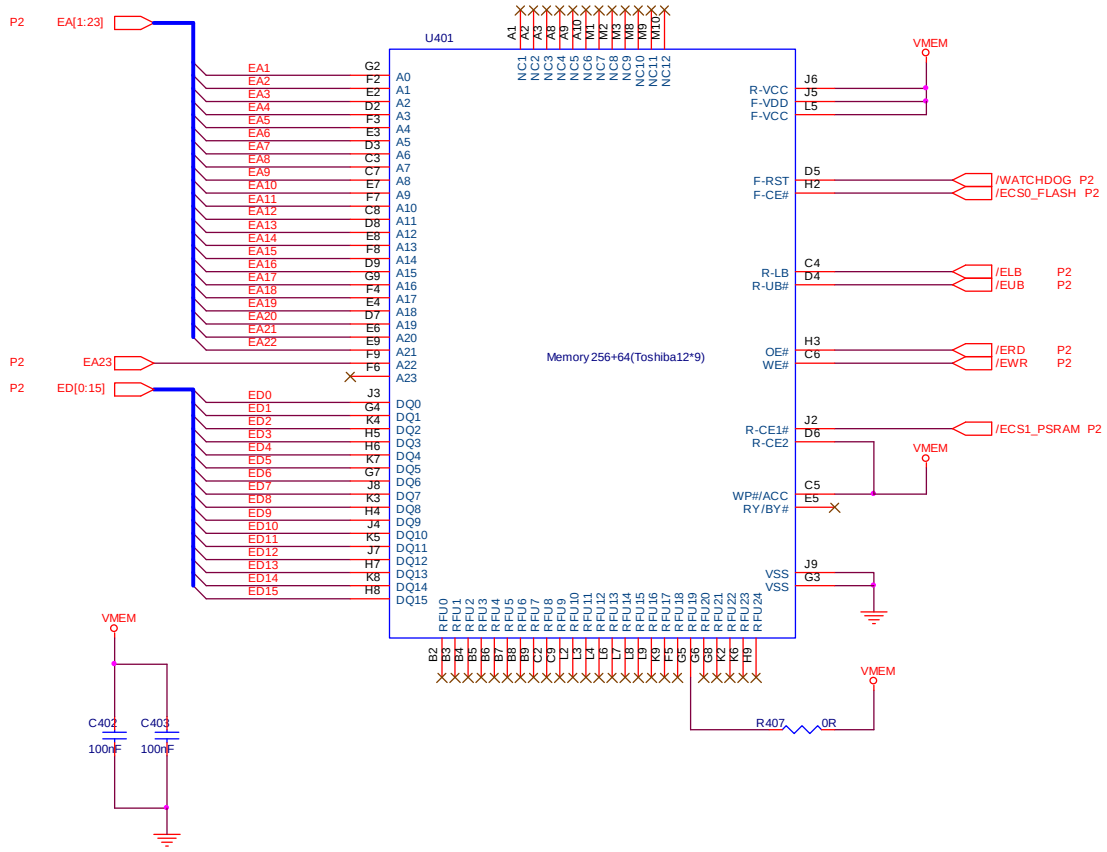
Power Management

MT6223D integrates all regulators that a voice-centric phone needs. Seven LDOs optimized for Specific GSM/GPRS baseband sub-systems are included, and a RF

transceiver needed LDO is also built-in. Besides Li-Ion battery charge function, SIM card level shifter interface, two open-drain output switches to control the LED and vibrator are equipped. Other power management schemes such as thermal overload protection, Under Voltage Lock-out Protection (UVLO), over voltage protection and oower-on reset and start-up timer are also MT6223D features. Besides, 3 NMOS switches controlling the RGB LEDs are also embedded to reduce BOM coount.

4. Sub circuit modules

(1)Memory



U401 is external MCP(Nor Flash + RAM), code and data are stored in this module.

VMEM: 2.8V, power for memory U401,come form external memory LDO output of BB chip U200

EA[1:23]: External memory address bus;

ED[0:15]: External memory data bus;

/ECS0_FLASH: External nor flash select;

/ECS1_PSRAM: External ram select;

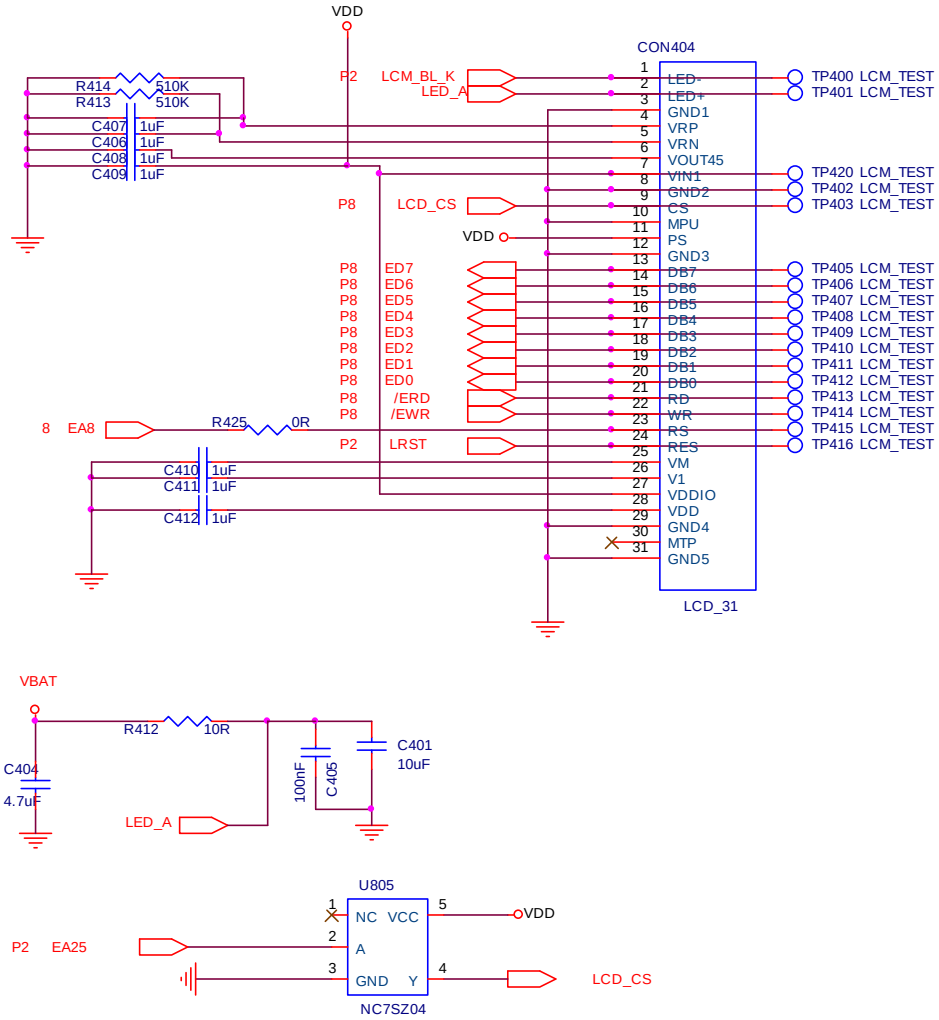
/ERD: External memory read strobe, active low

/EWR: External memory write strobe, active low

/ELB: External memory lower byte strobe

/EUB: External memory upper byte strobe

(2) LCM Interface



It’s a 8-bits parallel LCM, the main signal include:

VDD: 2.8V, power for LCM VDD and VIO;

GND: ground;

Vbat-→LED_A: power for LCM backlight LED

LCM_BL_K: LCM backlight LED control port; Low active;

LCD_CS: LCD chip select signal;

LRST: LCD reset signal;

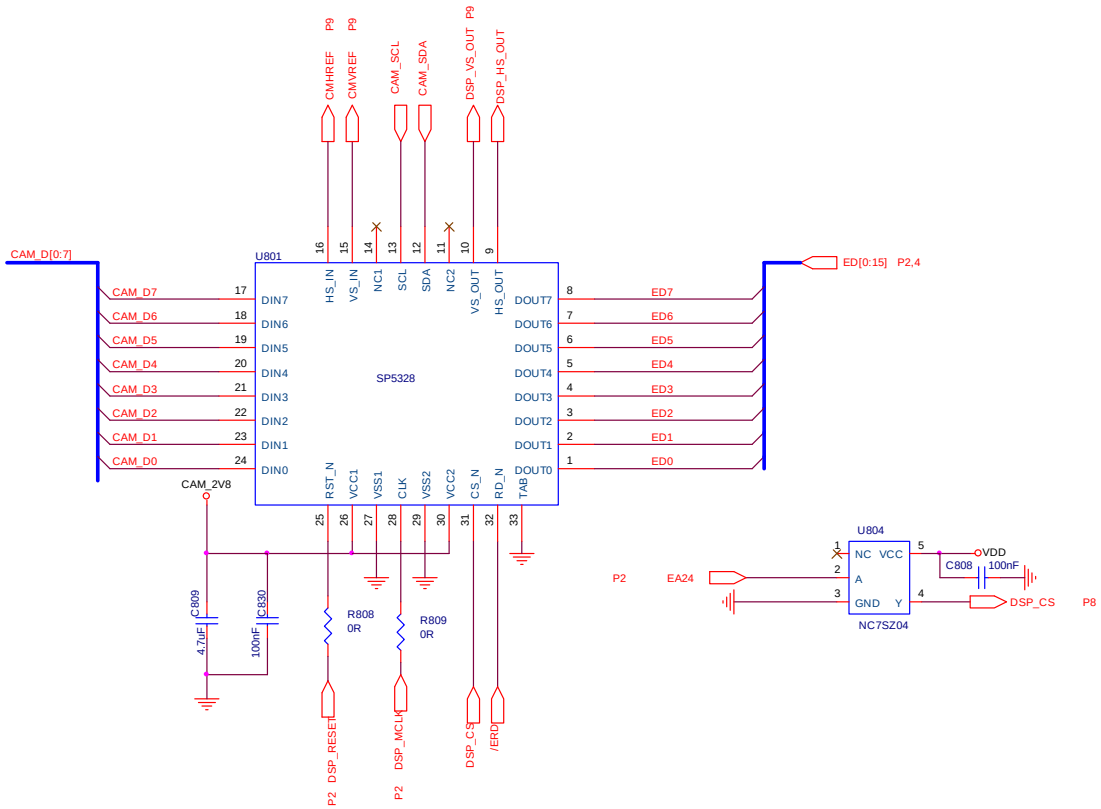
/ERD: read signal;

/EWR: write signal;

ED0-ED7: LCM data signal;

EA8: register select signal;

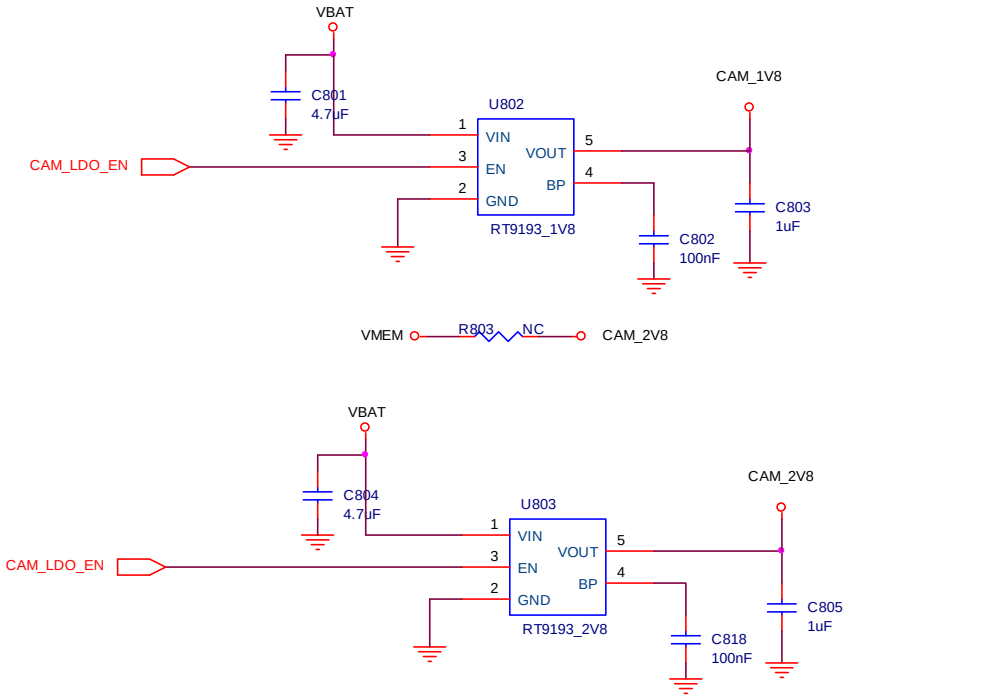
(3) DSP and Camera Module



U801: CMOS image sensor chip; SUPERPIX SP5328 is used to connect the CMOS Image Sensor(CIS) with External Memory Interface(EMI) of the Baseband chip U200. It allows the CPU to access the image data from the CIS in the way of likely accessing the SRAM.

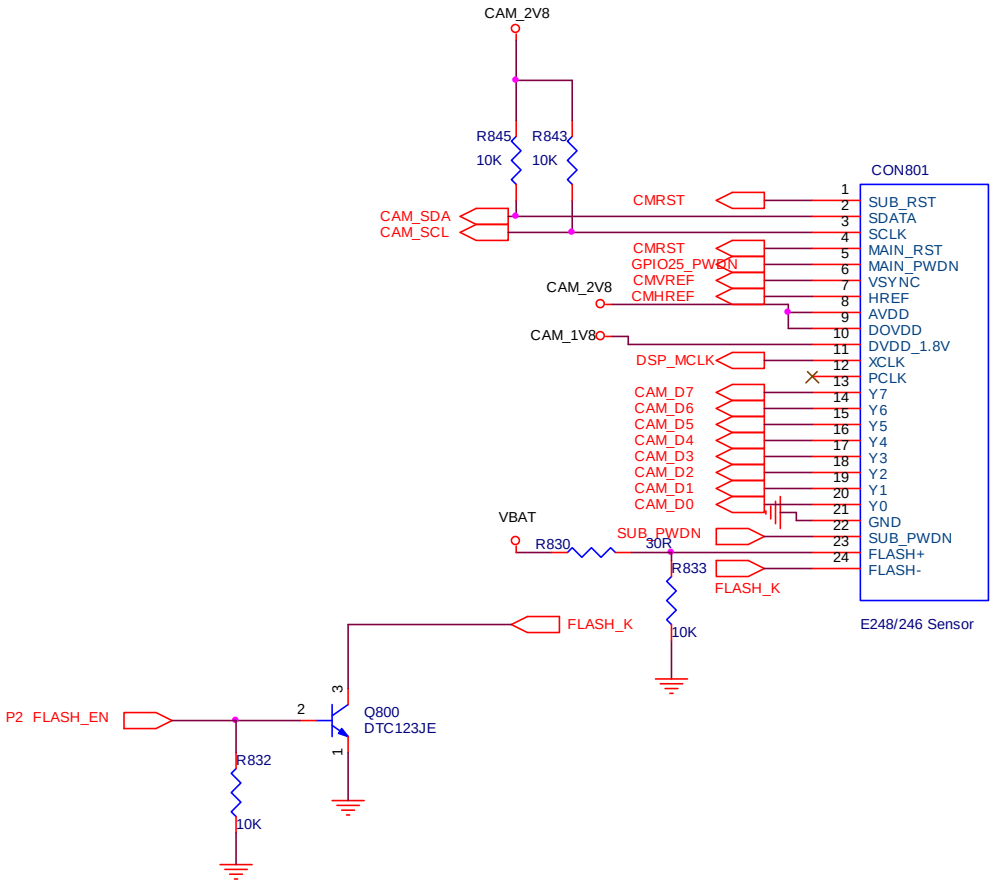
DSP general features:

- support external memory interface accessing;
- support CIS with the maximum resolution of VGA;
- Output RGB555, RGB444 and YUV422 format image;
- Resize the input image to any size below CIF;
- Advanced image signal processing to reduce the distortion;
- Serial interface to control the output image size and image format



U802: 1.8V LDO, power for camera sensor DVDD;

U803: 2.8V LDO, power for DSP and camera sensor;

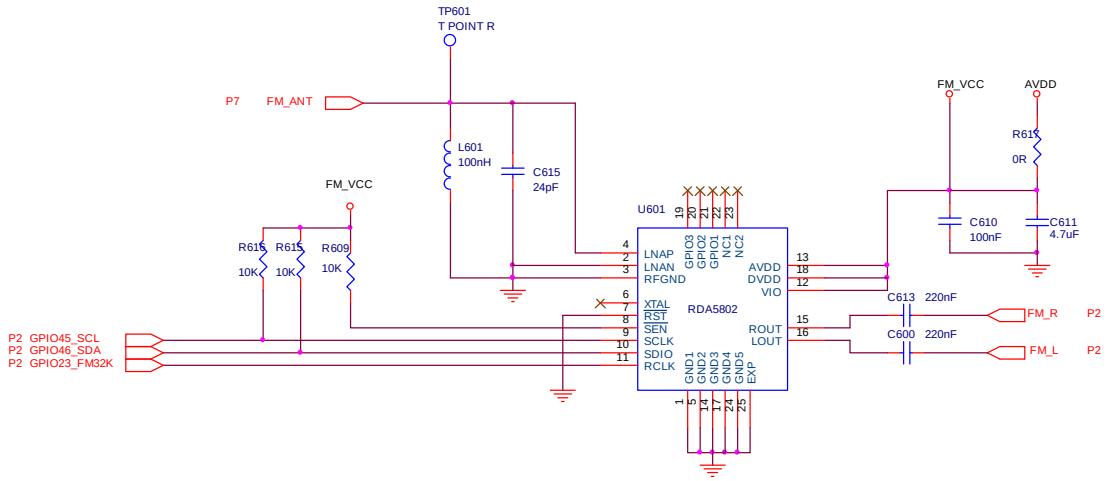


CON801 is the camera sensor interface;

CAM_SDA: I2C data bus between DSP and sensor;

CAM_SCL: I2C clock bus between DSP and sensor;
CMRST: camera sensor reset
GPIO25_PWDN: main sensor power down signal
CMVREF: output vertical sync
CMHREF: output horizontal sync
DSP_MCLK: external clock
CAM_D7-D0: image data bus
SUB_PWDN: sub sensor power down signal
FLASH_EN: Flash LED control signal， High active

（4）FM module



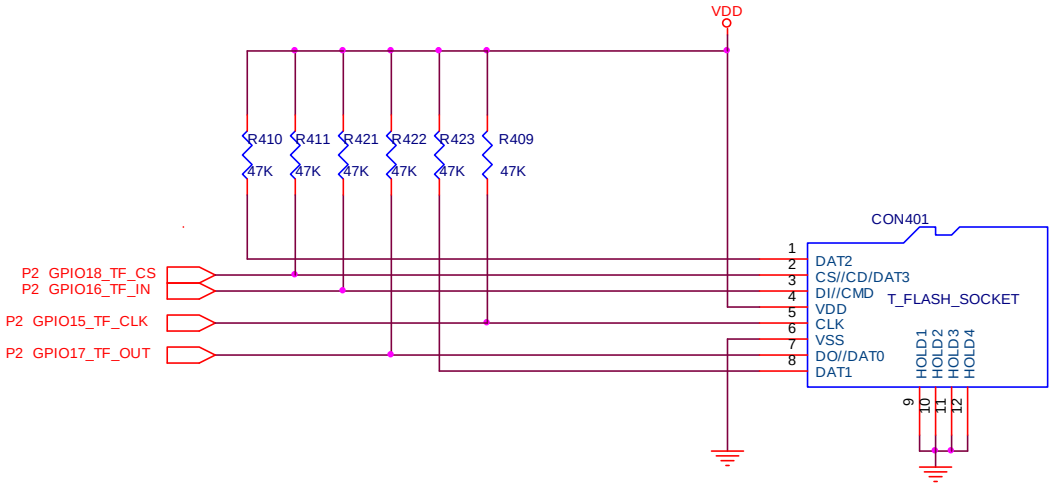
U602 is SINGLE-CHIP BROADCAST FM RADIO TUNER:RDA5802E.
The RDA5802 is a single-chip broadcast FM stereo radio tuner with fully integrated synthesizer, IF selectivity and MPX decoder. The tuner uses the CMOS process, support multi-interface and require the least external component.
The RDA5802 has a powerful low-IF digital audio processor, this make it have optimum sound quality with varying reception conditions.
The RDA5802 can be tuned to the worldwide frequency band.

Features:

* CMOS single-chip fully-integrated FMtuner
* Low power consumption
  - Ø Total current consumption lower than 17mA at 3.0V power supply
* Support worldwide frequency band
  - Ø 65 -108MHz
* Digital low-IF tuner
  - Ø Image-reject down-converter
  - Ø High performance A/D converter
  - Ø IF selectivity performed internally
* Fully integrated digital frequency synthesizer
  - Ø Fully integrated on-chipRF and IF VCO
  - Ø Fully integrated on-chip loop filter
* Autonomous search tuning

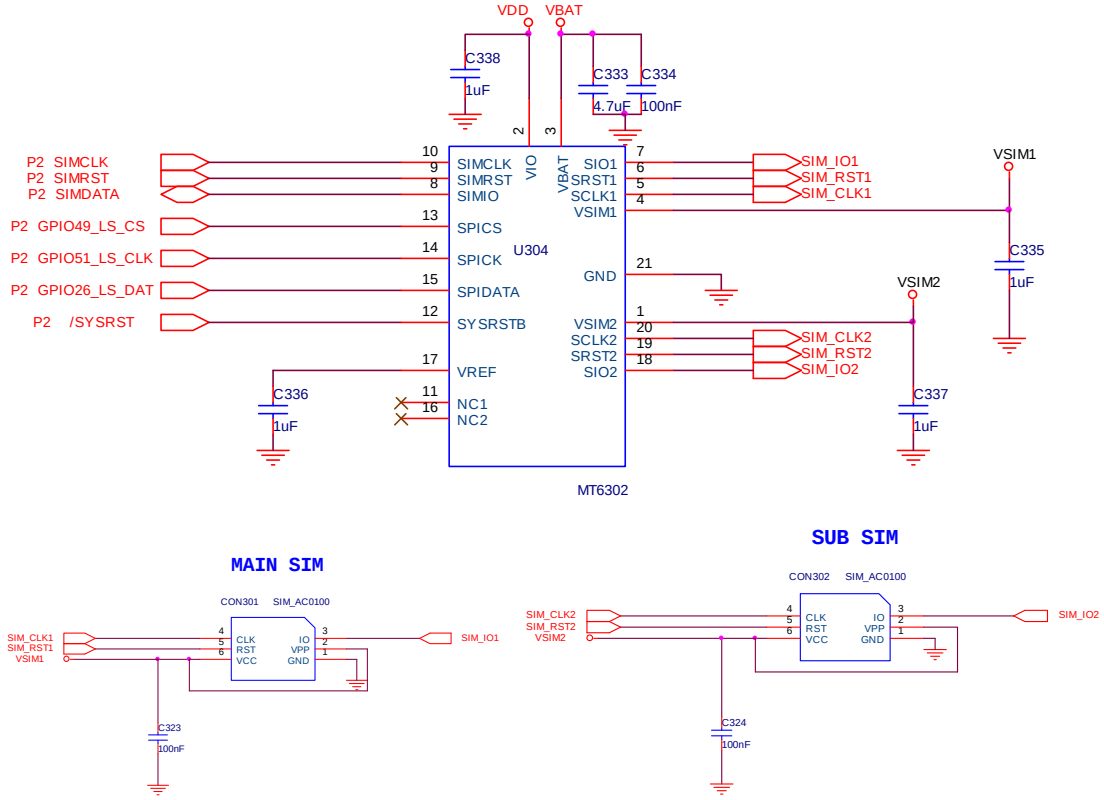
* Support 32.768KHz crystal oscillator
* Digital auto gain control (AGC)
* Digital adaptive noise cancellation
    Ø Mono/stereo switch
    Ø Softmute
    Ø High cut
* Programmable de-emphasis (50/75 ms)
* Receive signal strength indicator (RSSI)
* Bass boost
* volume control
* I2S digital output interface
* Line-level analog output voltage
* 32.768KHz 12M,24M,13M,26M,19.2M,38.4MHz Reference clock
* 2-wire and 3-wire serial control bus interface
* Directly support 32Ωresistance loading
* Integrated LDO regulator
    Ø 2.7 to 5.5 V operation voltage

(5)T-Flash



CON401 is the T-Flash card connector. VDD(2.8V)is the power. T-card is controlled by 4-wires SPI(CS/CLK/dataIN/dataOut) interface by baseband IC.

(6)Dual SIM



U304 is Dual SIM Card Controller,

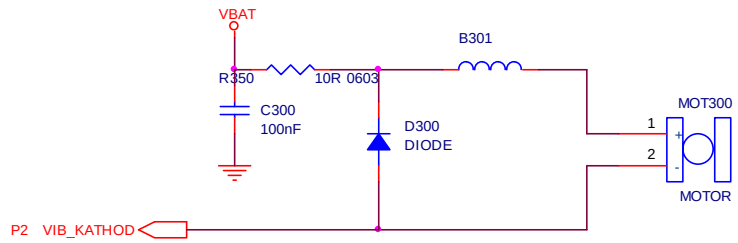
The MT6302 is a dual SIM card control chip optimized for GSM handsets, especially those based on the MediaTek MT62xx system solution. It supports both 1.8V and 3V SIM cards. A serial port interface (SPI) is used to control dual SIM channel individually.

Features

* Control and communication through a SPI interface with baseband processor.
* Independent 1.8V/3V VCC control for each SIM card
* Power management and control for dual SIM cards
*Independent clock stop mode (at high or low level) for each SIM card

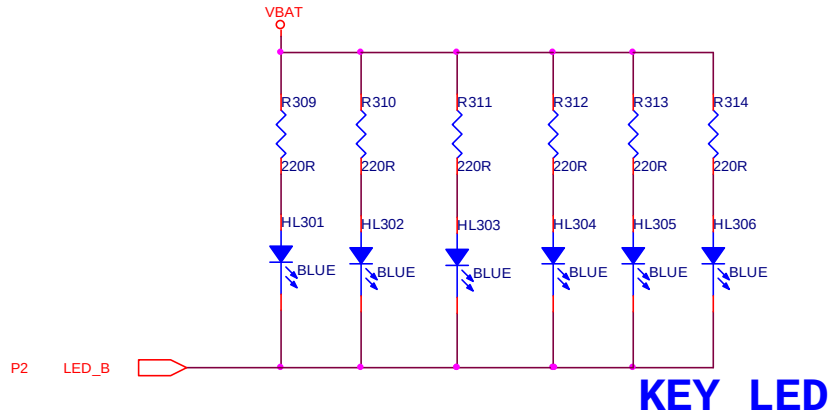
CON301/302 are SIM card connectors.

(7)Motor



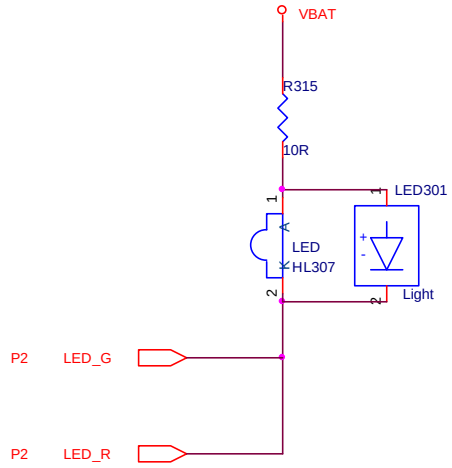
Motor is powered by Vbat and controlled by VIB_KATHOD.

(8)Key backlight



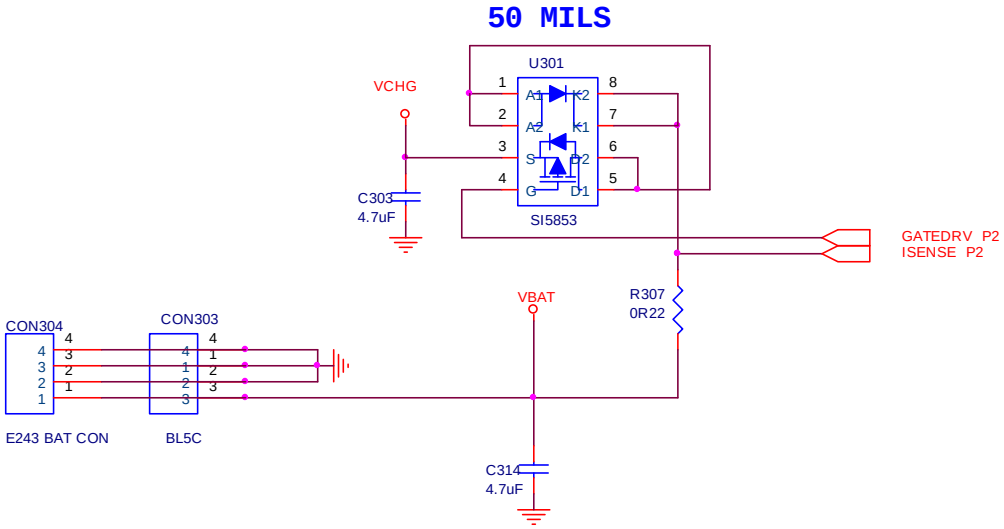
Key LEDs are powered by Vbat and controlled by LED_B.

(9) Torch



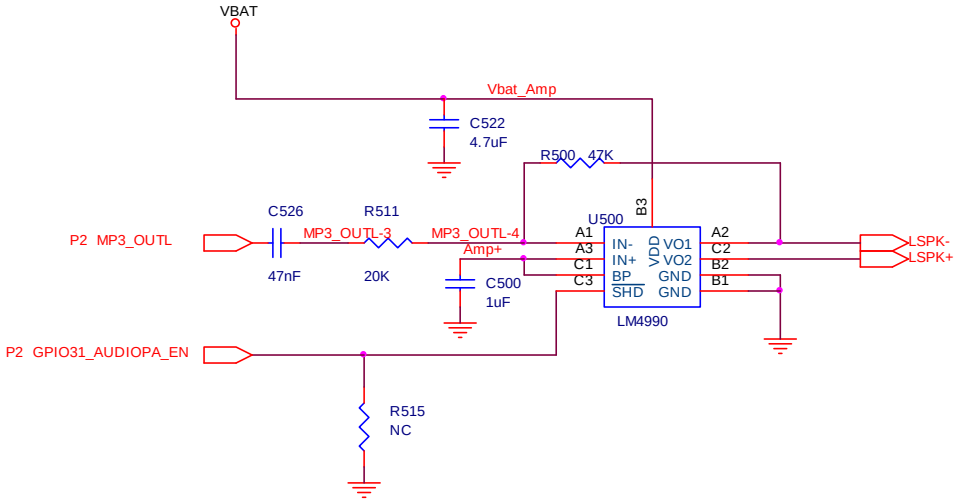
Torch Lamp is power by Vbat and controlled by LED_G / LED_R.

(10)charger and battary



CON303/304 are battery conectors. U301 is charge control P-MOS with diode. Vchg is supplied by external chaeger, GATED_RV is the control signal of P-MOS.

(11)audio PA



U500 is the audio amplifier. It's powered by Vbat.

GPIO31_AUDIOPA_EN: Enable signal.

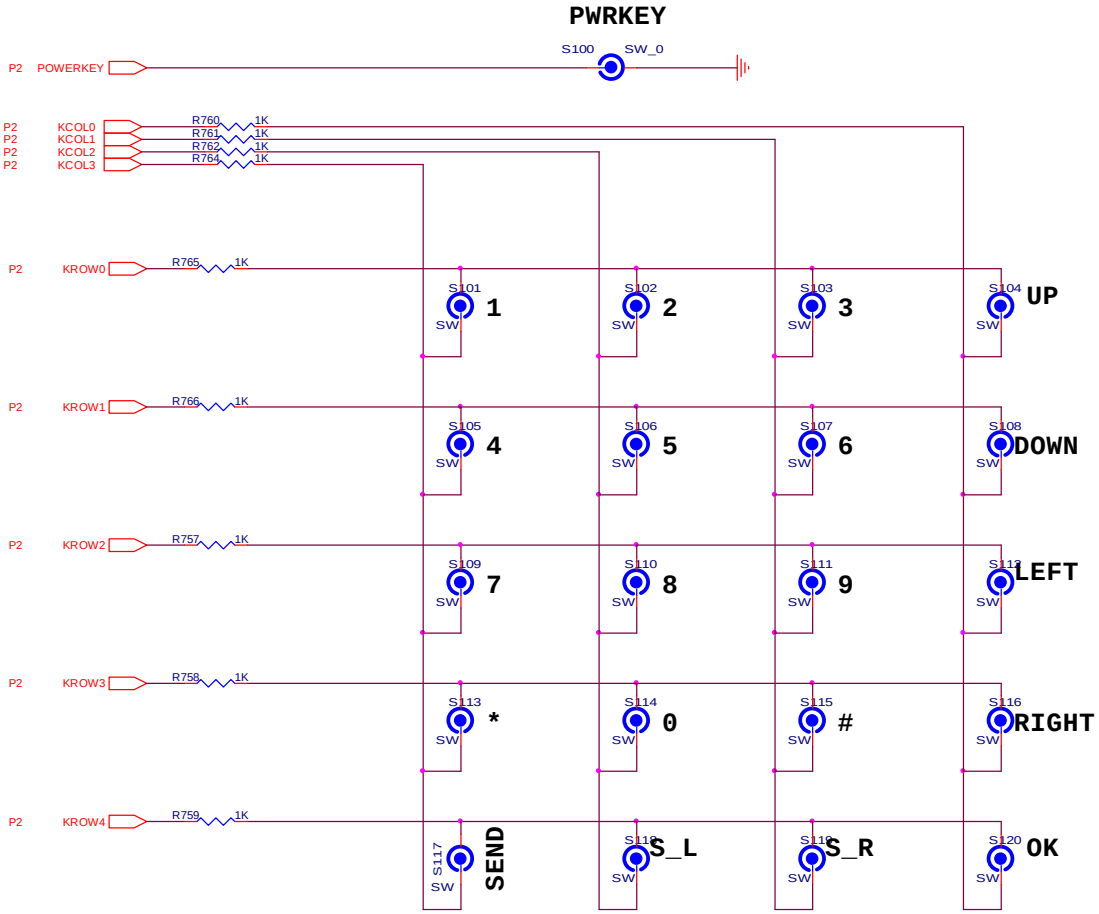
MP3_OUTL is the audio input signal;

C525: the input coupling capacitor

R500/R511: adjust the amplifier gain;

LSPK+/- are the out signal and used to driver the 8 ohm speaker.

(12) KeyPAD



S100: power on/off key

POWERKEY : Power key press input to baseband;

V600: 5-row ×4-column keypad controller with hardware scanner

For MT6223D: The keypad can be divided into two parts: one is the keypad interface including 6 columns and 5 rows with one dedicated power-key, as shown in Fig. 1 ; the other is the key detection block which provides key pressed, key released and de-bounce mechanisms. Each time the key is pressed or released, i.e. something different in the 5 x 6 matrix or power-key, the key detection block senses the change and recognizes if a key has been pressed or released. Whenever the key status changes

and is stable, a KEYPAD IRQ is issued. The MCU can then read the key(s) pressed directly in KP_HI_KEY, KP_MID_KEY and KP_LOW_KEY registers. To ensure that the key pressed information is not missed, the status register in keypad is not read-cleared by APB read command. The status register can only be changed by the key-pressed detection FSM.