FCC ID: YE6DAZZL8

Model: **YTRUG281**

Technical Description of Wireless Optical Mouse

The equipment under test (EUT) is the Mouse Unit (2.4GHz transceiver) of a wireless optical mouse system (mouse and dongle) operating in 2.402GHz - 2.480GHz using FSK technique. The Mouse Unit radio system has two parts: radio modem and microcontroller. The microcontroller scans keystrokes, wheel and sensor, then packs the data by adding preambles, frame information, and error checking bytes. The radio system employs 79 channels (the frequency range is 2.402-2.480GHz) in random. When the data validation has error, the system switches channel.

The Mouse Unit radio system will send sync packets after being powered on, and then search Dongle's responses. This is search mode. If any responses-packet is received, the Mouse Unit radio system will enter normal working mode. If the Mouse Unit radio system loses synchronization, it will enter sleep mode.

The Mouse Unit radio system is powered by two 1.5V "AAA". The power consumption of RF module is about 2.7mA. The total power consumption is about 9.5mA in normal working mode. It will enter sleep mode if no key is pressed or no motion after 30 second. The total power consumption is 100-200uA in sleep mode.

Modulation Type: FSK
Antenna Type: Internal, Integral antenna

The functions of main Components are mentioned as below.

1) U5 acts as MCU dealing with internal data.
2) U3 acts as RF transceiver module (2.402GHz-2.480GHz).
3) Y1 generates 12MHz clock to U3.
4) U6 acts as voltage regulator
5) U4 acts as Optical sensor.

MU2400

2.4GHz Low Data Rate RF Transceiver

Data Sheet

DATA SHEET

Version 1.5.0

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MuChip Co., Ltd

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MU2400 – 2.4GHz Low Data Rate RF Transceiver

General Description

The MU2400 is a single-chip FSK low data rate RF transceiver for the world wide 2.4 – 2.5GHz ISM band. The data rate of the MU2400 can be operated up to 1.6Mbps in buffer mode. The MU2400 uses the standard CMOS process to offer a complete FSK RF transceiver solution with small die size, low power consumption, minimum external parts and high reliability.

The MU2400 consists of a fully integrated frequency synthesizer, a power amplifier, a crystal oscillator, a demodulator, modulator, and Auto-ACK protocol engine. A reduced off-chip filter is realized by the low-IF architecture in RX chain. The MU2400 is programmable for frequency channels, and protocol setup easily through a 4-wire SPI interface.

Features

- Single-chip FSK transceiver
- Auto-ACK & Auto-retransmission
- Star-Network with 6 channels
- Address and CRC computation
- 1/1.6Mbps data rate
- 1 ~ 64 bytes payload length
- 64 bytes FIFO size
- 4-wire digital interface (SPI)
- Power supply range: 1.8 to 3.6V
- Battery low supply voltage detector
- Support 4 power modes: Active/Standby/Idle/Power Down
- Operation range: -40 ^{o}C to +85 ^{o}C
- Standard CMOS process
- 24-pin 4x4 QFN package
- On-chip VCO, PLL and PLL loop filter
- On chip channel filter

Applications

- Wireless mouse, keyboard, joystick
- Keyless entry
- Alarm and security system
- Home automation
- Surveillance
- Automotive
- Telemetry
- Industrial sensors
- Wireless data communication
- Toys

1. Pin Configuration

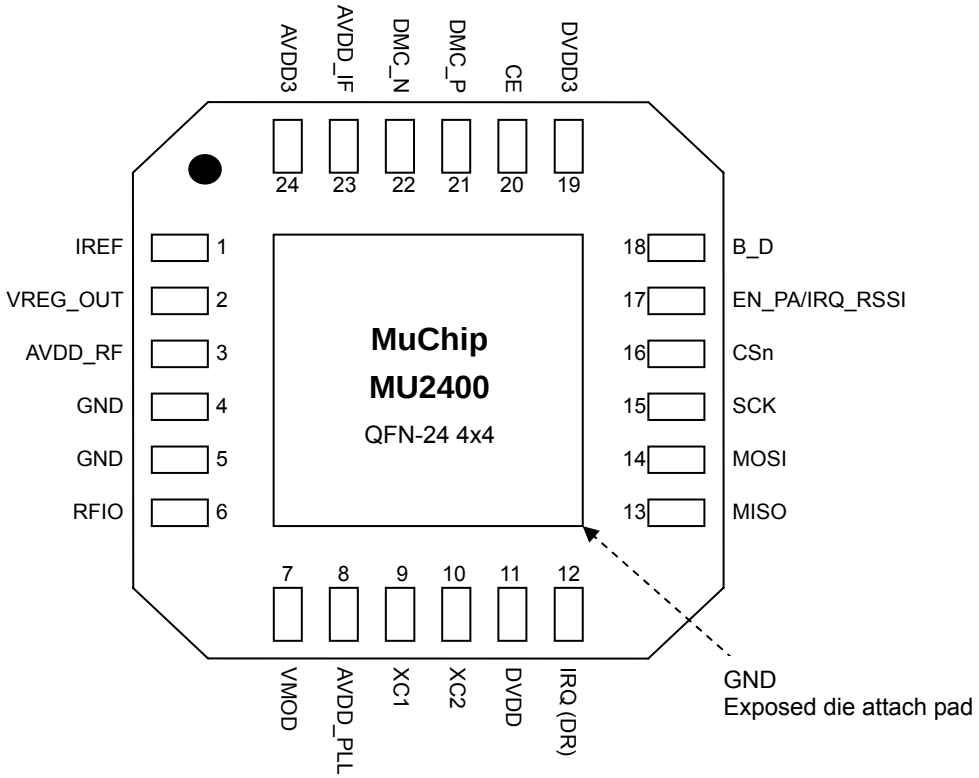


Figure 1: Pin Configuration

The exposed die attach pad must be connected to a solid ground plate because this is the main ground connection for the MU2400.

2. Pin Description

Pin	Name	Type	Description
1	IREF	Analog Input	Reference resistor pin, connect to an external resistor
2	VREG_OUT	Power	On-chip voltage regulator output
3	AVDD_RF	Power	RF power supply
4	GND	Ground	Connect to PCB ground
5	GND	Ground	Connect to PCB ground
6	RFIO	Analog I/O	RF input/output
7	VMOD	Analog I/O	Connect to external capacitor for filtering
8	AVDD_PLL	Power	PLL power supply
9	XC1	Analog I/O	Be configured as the two pin definitions: a. Crystal pin1 for external crystal b. For external clock signal, it connects to ground.
10	XC2	Analog I/O	Be configured as the two pin definitions: a. Crystal pin2 for external crystal b. For external clock signal, it's the input pin of external clock
11	DVDD	Power	Digital power supply
12	IRQ(DR)	Digital I/O	Be configured as the two operation modes: a. IRQ: Interrupt signal in buffer mode b. DR: data input/data output in direct mode
13	MISO	Digital Output	Be configured as the two operation modes: a. master input/slave output in SPI mode b. data output in buffer mode
14	MOSI	Digital Input	Be configured as the two operation modes: a. master output/slave input in SPI mode b. data input in buffer mode
15	SCK	Digital Input	SPI input clock
16	CSn	Digital Input	SPI selection / programming enable
17	EN_PA/ IRQ_RSSI	Digital Output	Be configured as the two output modes: 1. EN_PA: To control the external PA chip 2. IRQ_RSSI outputs high – To indicate the MCU to read the RSSI digital registers, RSSI is only valid during receiving signal. – Let MCU know whether the channel is occupied.

18	B_D	Digital Output	Battery detector output
19	DVDD3	Power	Digital I/O power supply
20	CE	Digital Input	Chip enable
21	DMC_P	Analog Output	Demodulator analog output, connecting to an external AC coupling capacitor
22	DMC_N	Analog Input	Demodulator analog input, connecting to an external AC coupling capacitor
23	AVDD_IF	Power	RX IF power supply, voltage regulator output
24	AVDD3	Power	Voltage regulator power supply
	Back side plate	GND	Ground

Table 1: Pin Function Description

3. Block Diagram

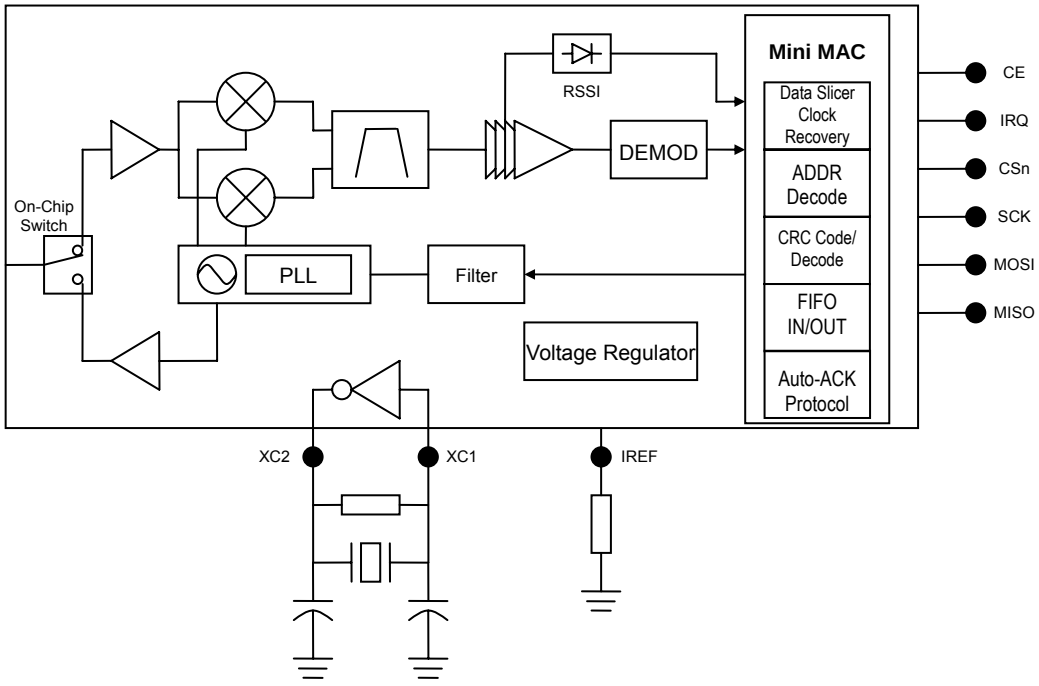


Figure 2: Block Diagram

10. Packet Handling Methods

The packet handler offered by the MU2400 makes it possible to be operated up to the high data rate without the requirement for a costly and high-speed microcontroller (MCU) for the data processing and clock recovery. The MU2400 can offer the application microcontroller a simple SPI compatible interface. The speed of the SPI input clock (SCK) in the MU2400 will be determined by the interface-speed microcontroller itself even the system is operated up to the maximal data rate, i.e. 1.6Mbps.

In RX Buffered Mode, IRQ notifies the MCU when a valid address and payload is received respectively. Then, the MCU can clock out the received payload from an MU2400 RX FIFO.

In TX Buffered Mode, the MU2400 digital part automatically generates preamble value and CRC value. The advantage is to reduce memory demand in the MCU resulting in a low cost MCU, as well as to speed up the software development time. The MU2400 has 64 bytes FIFO size. The MCU can access the FIFO or reset the FIFO at any time.

11. Auto-Acknowledgement (RX)

If auto acknowledgement is enabled and a valid packet with correct data pipe address and CRC is received, the RX device will enter the TX mode and send an acknowledgement packet to TX device. After the RX device has sent the acknowledgement packet to the TX device, normal operation in RX device will be resumed.

12. Auto Re-Transmission (TX)

An auto retransmission is available when auto acknowledgement is enabled. It is used at the TX device. It will be to state how many times the data in the data register will resend if data is not acknowledged. After each sending, the TX device will enter the RX mode and wait a specified time period for acknowledgement. When the ACK packet is received, the TX device will return to the normal transmit function. If there is no more unsent data in the TX FIFO, the TX device will go into the Standby mode.

If the acknowledgement is not received in the TX device, the TX device will transfer to TX mode and resend the data after a specified time period. Then, this action will be continued until acknowledgement is received in the TX device or a time out occurs because of the maximum number of resending is reached.

13. Star Network

An MU2400 configured as primary RX will be able to receive data through 6 different data pipes. A data pipe will have a unique address but share the same frequency channel. This means that six different MU2400 devices configured as primary TX can be communicated with one MU2400 device configured as RX, and the MU2400 configured as RX will be able to distinguish between six different MU2400 configured as primary TX. Besides, only one data pipe can receive a packet at a time.

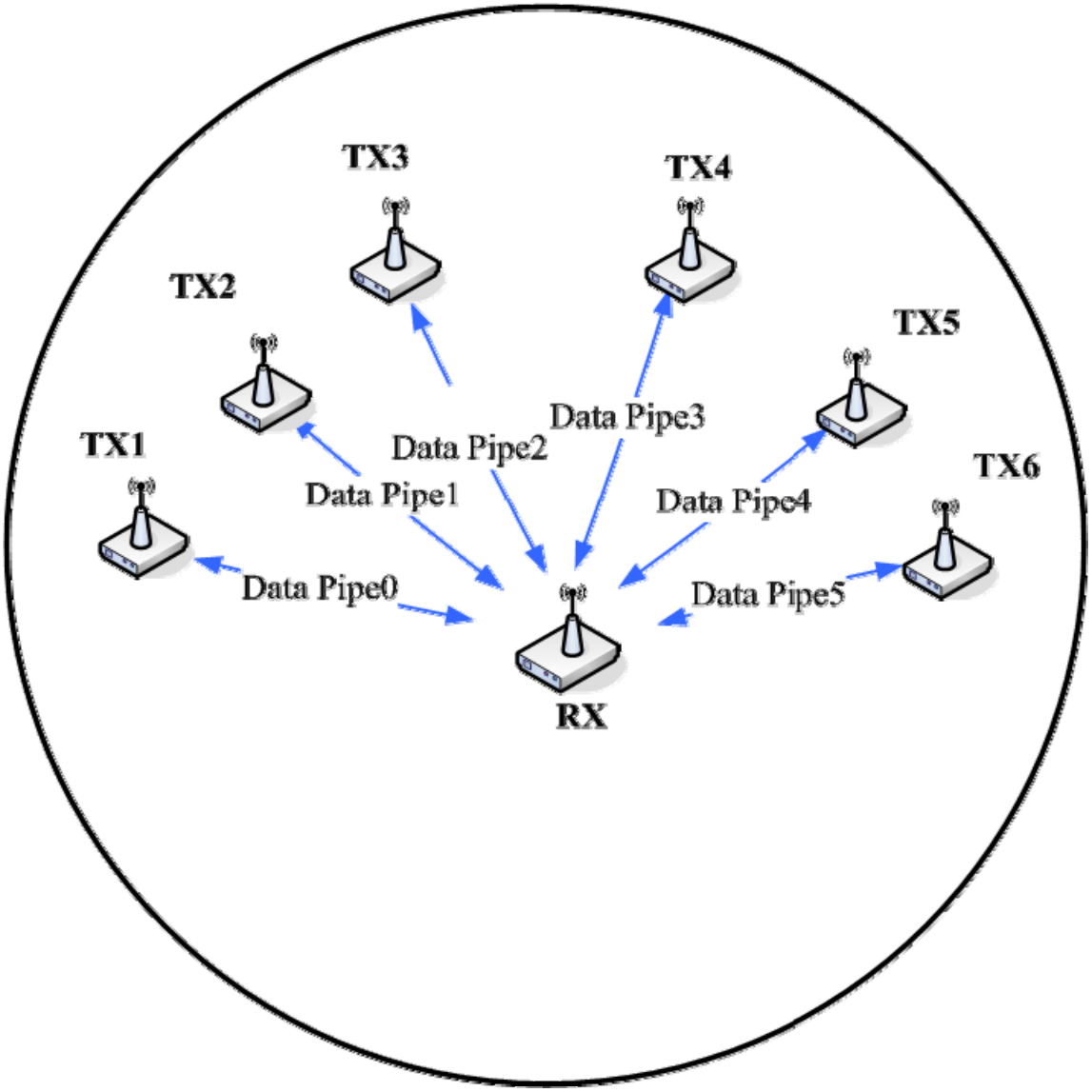


Figure 4: Star Network Configuration

The RX receives packet from more than one TX. To ensure that the ACK packet from the RX is transmitted to the correct TX, the RX takes the data pipe address where it received the packet and used it as the TX address when transmitting the ACK packet. On the TX device, the TXADR must be the same as the RXADR0. On the RX device, the RXADR0~RXADR5, defined as the data pipe address, must be unique. The ***Figure 6*** is an example of data pipe addressing for the TX and the RX.

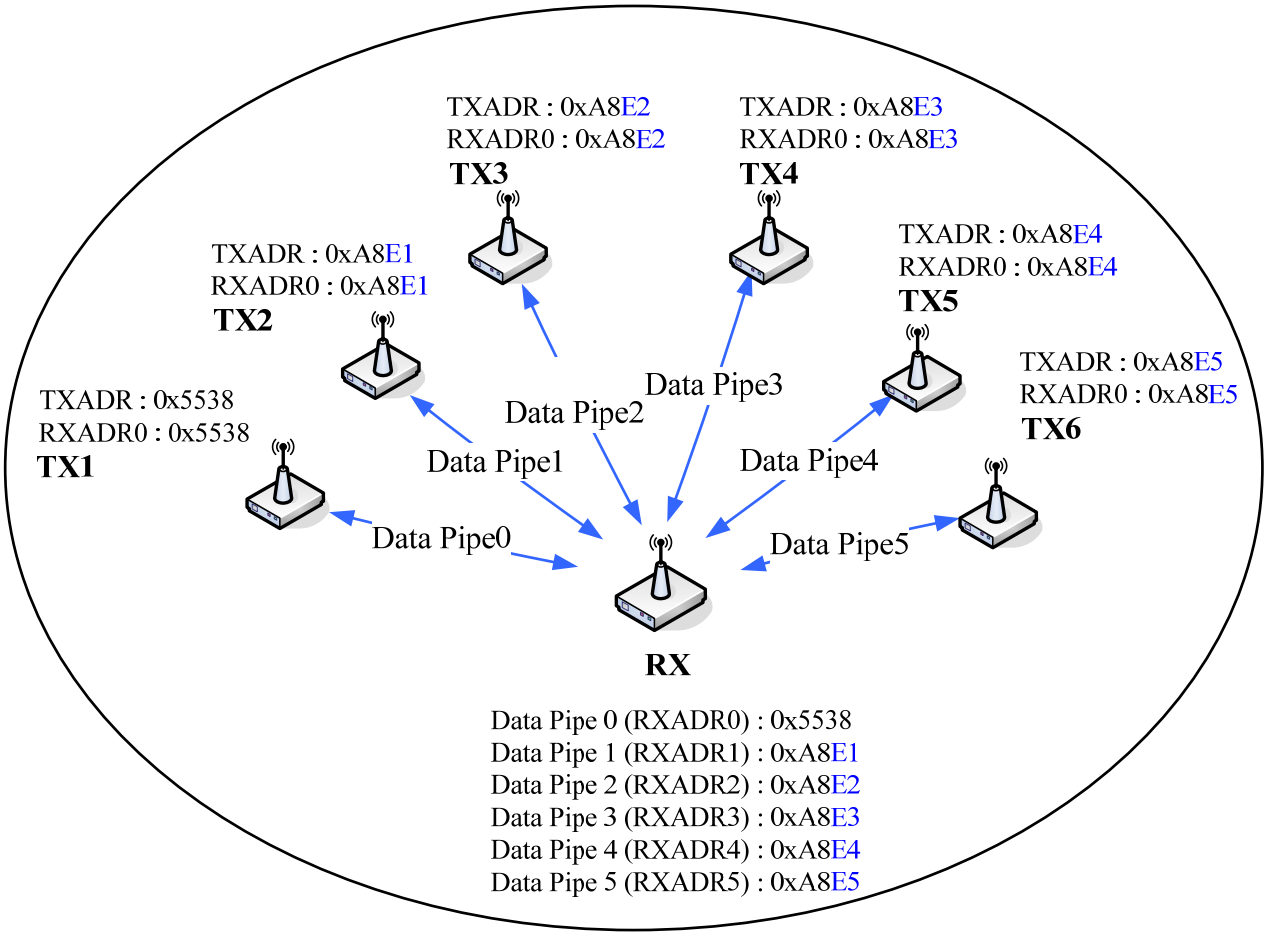


Figure 6: Example of data pipe addressing

18. Crystal Oscillator Description

There are two ways to provide the reference clock to the MU2400. One is to use the low-cost crystal of its frequency is 12/16/24MHz with maximum frequency tolerance +/-60ppm. The other is to use the external clock provided by MCU.

18.1. Using External Crystal Oscillator

The ***Figure 15*** shows the connection of crystal network between XC1 and XC2 pins. C1 and C2 capacitance are used to adjust different crystal loading. The MU2400 supports the low cost crystal of its frequency is 12/16/24MHz with maximum frequency tolerance +/- 60ppm. If crystal accuracy is larger than +/-40ppm, the users need to do the crystal frequency offset calibration. The ***Figure 16*** shows the detail calibration procedure. The ***Table 13*** shows the requirement of the crystal electrical specification.

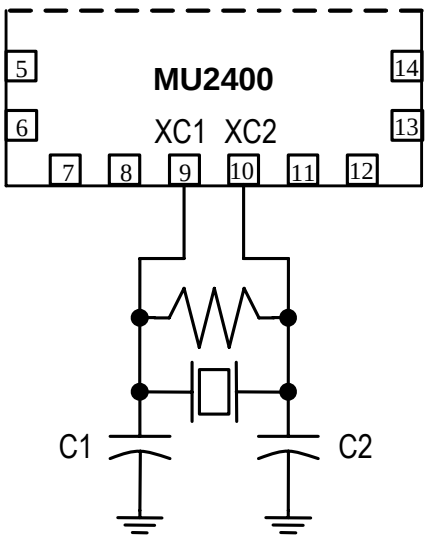


Figure 15: Crystal Network Connection for using external crystal oscillator

Frequency Tolerance	ESR	Co	CL
+/- 60ppm	60Ω	7pF Max.	22pF

Table 13: Requirement of Crystal Electrical Specification

18.3. Using External Clock provided by MCU

When using external clock provided by MCU to drive the crystal reference pin XC2 of the MU2400, some rules must be followed. First, the register R0x00[2] is set to Low. When MCU drives the MU2400 clock input pin, XC2, the value of load capacitance C_L is determined by the MCU only. The frequency accuracy of +/-40ppm is still required to get a functional radio link. The input signal should not have amplitudes exceeding any rail voltage, but this is tolerable within any DC voltage. To achieve low current consumption and also good SNR ratio when using an external clock from MCU, it is recommended to use an input signal larger than 0.4 V_{-peak}. The ***Figure 18*** shows the connection for using the external clock. When using an external clock provided by MCU, XC2 is the input pin, and XC1 is not used. Therefore, XC1 needs to connect to ground.

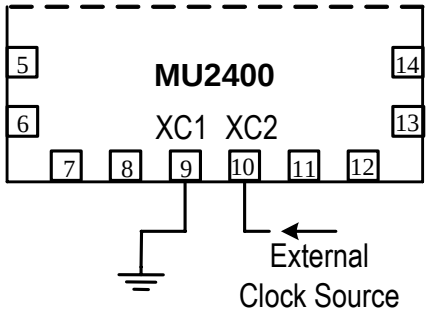


Figure 18: Connect to the external clock provided by MCU

24. Application Diagram

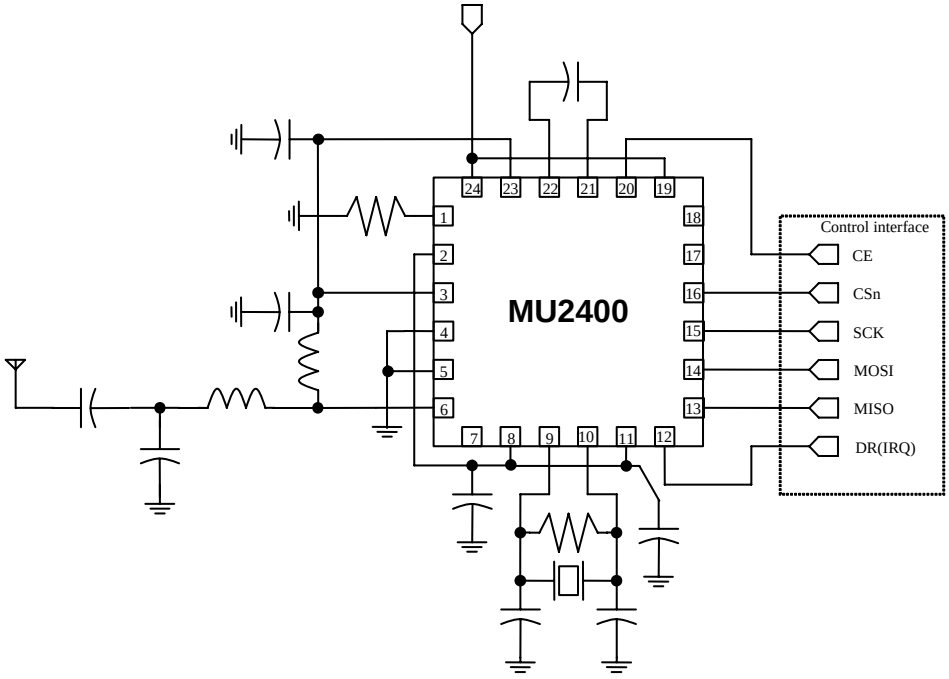


Figure 23: Recommended Application Circuit

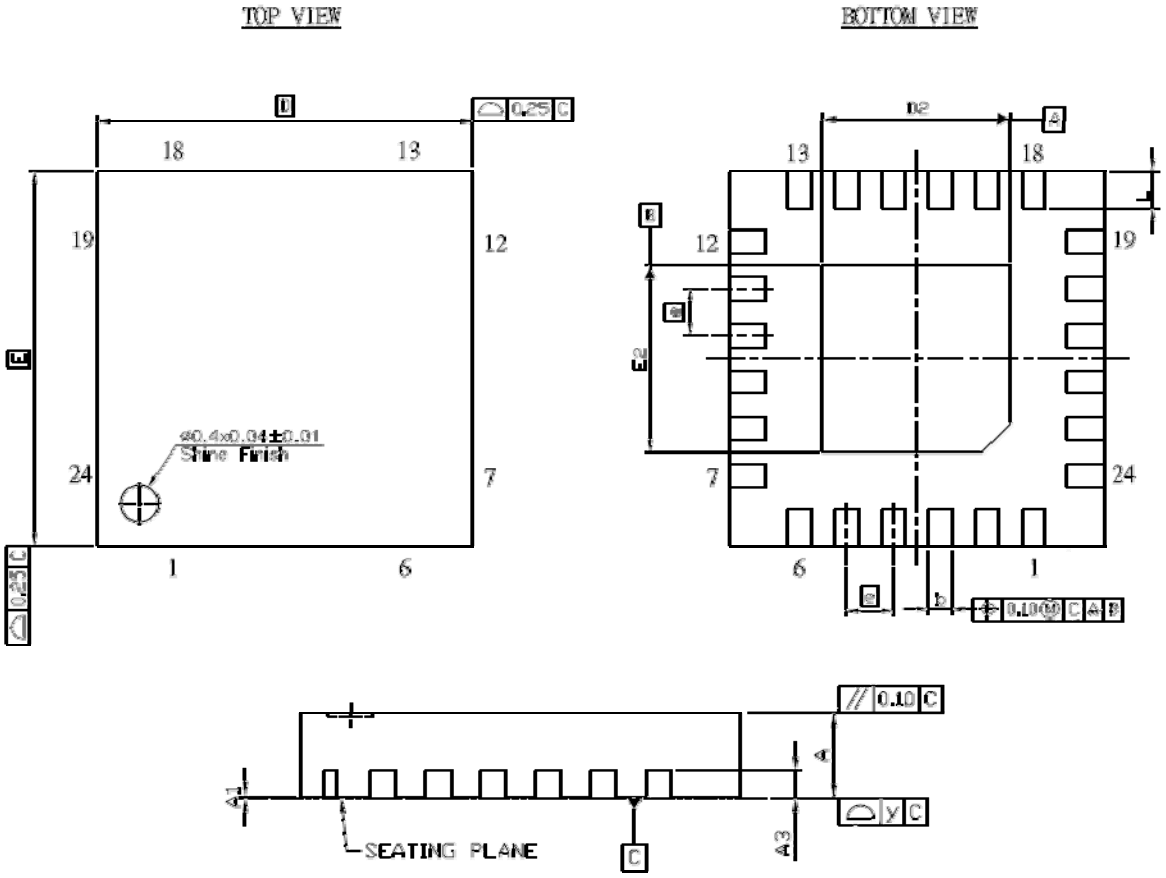
Only a few external components are required for using the MU2400. The reference application circuit is shown in ***Figure 23***. The detail recommended application design is referred to the MU2400 Application Note.

25. Ordering Information

Part No.	Package	Units Per Reel / Tray
MU2400	QFN24, Pb Free, Tape & Reel, -40°C ~ 85°C	3K
MU2400	QFN24, Pb Free, Tray, -40°C ~ 85°C	490 EA

Figure 24: Ordering Information

26. Package Information

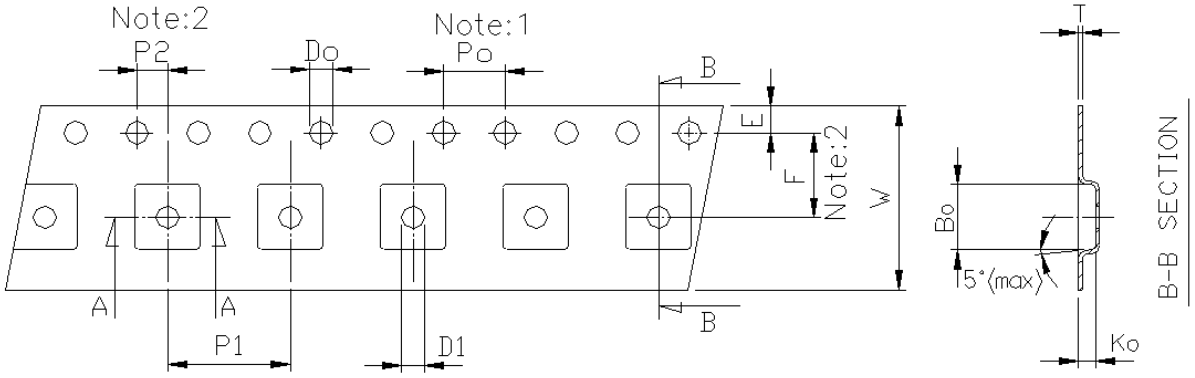


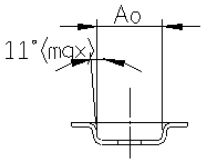
SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3		0.203 REF			8 REF	
b	0.18	0.25	0.30	7.09	9.84	11.81
D	3.90	4.00	4.10	153.5	157.5	161.4
D2	1.90	2.00	2.10	74.8	78.7	82.7
E	3.90	4.00	4.10	153.5	157.5	161.4
E2	1.90	2.00	2.10	74.8	78.7	82.7
e		0.50 BSC			19.69 BSC	
L	0.30	0.40	0.50	11.8	15.7	19.7
y		0.08			3.15	

Figure 25: Package Information

27. Tape Reel Information

QFN 4x4x0.8 Carrier Tape





A–A SECTION

Ao= 4.25± 0.10 mm

Bo= 4.25± 0.10 mm

Ko= 1.25± 0.10 mm

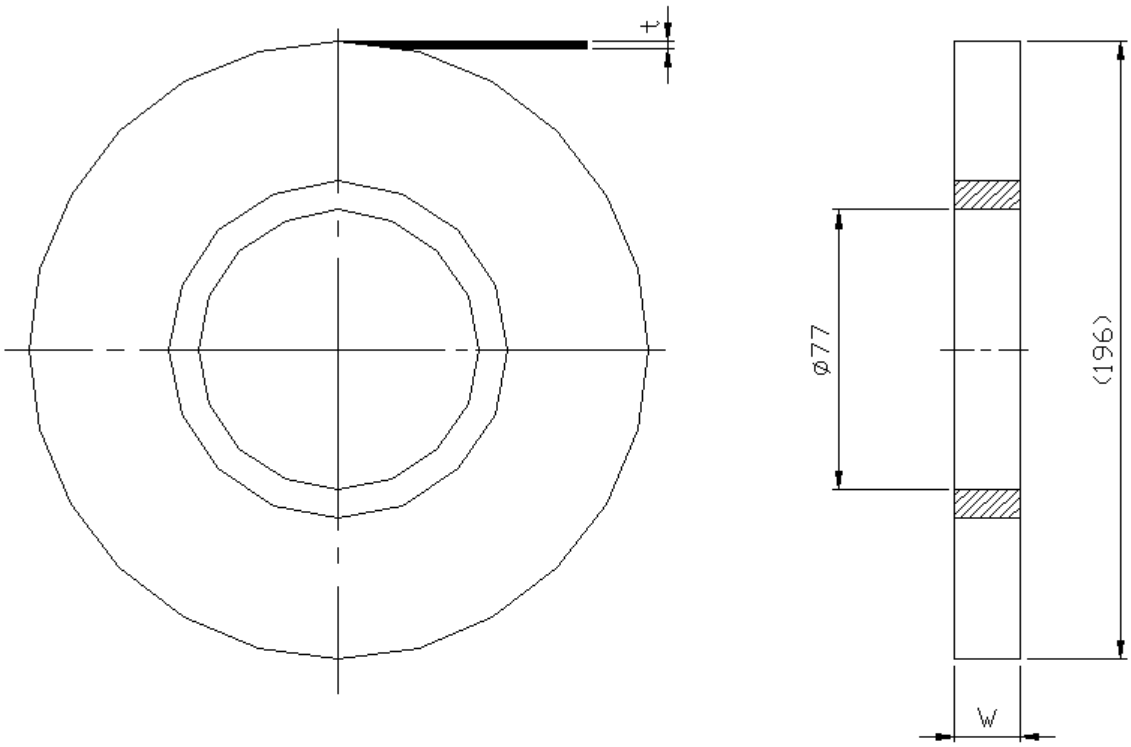
Unit: mm

Symbol	Spec.
K1	–
Po	4.0± 0.10
P1	8.0± 0.10
P2	2.0± 0.05
Do	1.55± 0.05
D1	1.50(MIN)
E	1.75± 0.10
F	5.50± 0.05
10Po	40.0± 0.10
W	12.0± 0.20
T	0.30± 0.05

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ± 0.1mm
2. Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
3. Ao & Bo measured on a place 0.3mm above the bottom of the pocket to top surface of the carrier.
4. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1mm per 100mm through a length of 250mm.

QFN 4x4x0.8 Cover Tape Dimension



Width(mm)	5.4±0.10	9.3±0.10	13.3±0.10	21.3±0.10
Length(M)	490	490	490	490
Thickness(um)	48±5	48±5	48±5	48±5

QFN 4x4x0.8 Reel Dimension