
802.15.4 Family of RF Modules
High Performance and Long Range

# DiZiC 802.15.4 DZ-ZB RF Modules

*Quickly add wireless capability with these high performance ZigBee compliant modules*

The DiZiC DZ-ZB 802.15.4 Modules allow you to quickly add wireless networking capabilities to your products. These ZigBee-compliant modules are ready-to-use, simple to operate, and available in a wide range of configurations. They are ideal for industrial sensors, consumer remote controls, home appliances, and more.

## Features

- STM32W108 ZigBee / IEEE 802.15.4 SoC
  - Complete System-on-Chip
  - 32-bit ARM® Cortex-M3 processor
  - 2.4 GHz IEEE 802.15.4 transceiver & lower MAC
  - Supports 16 channels
  - 128 kB flash, 8 kB SRAM memory
  - 128-bit AES encryption accelerator
  - Flexible ADC, SPI/UART/TWI serial communications, and general purpose timers
  - 24 highly configurable GPIO with Schmitt trigger inputs
  - Data rate up to 250 kbit/s
- Low power consumption, advanced management:
  - RX Current (w/ CPU): 27 mA
  - TX Current (w/ CPU, +3 dBm TX): 31 mA
  - Low deep sleep current with retained RAM and GPIO:
    400 nA/ 800 nA with/without sleep timer
  - Low-frequency internal RC oscillator for low-power sleep timing
  - High-frequency internal RC oscillator for fast (100 µsec) processor start-up from sleep
- Innovative network and processor debug:
  - Serial Wire/JTAG interface
  - Standard ARM debug capabilities: Flash Patch & Breakpoint; Data Watch-point & Trace; Instrumentation Trace Macrocell
- Exceptional RF Performance
  - Normal mode Link Budget up to 102 dB; configurable up to107 dB
  - -99 dBm normal RX sensitivity; configurable to -100 dBm (1%PER, 20 byte packet)
  - +3 dB normal mode output power; configurable up to +7 dBm
  - Robust WiFi and Bluetooth coexistence
- Application Flexibility:
  - Single voltage operation: 2.1 V to 3.6 V
  - Optional 32.768 kHz crystal for higher timer accuracy
  - Low external component count with single 24 MHz crystal
  - External power amplifier versions
- Peripherals
  - 24 GPIOs, SPI, USART, and I2C
  - 12-bit ADC with up to 6 inputs
  - 2x 16-bit timers
  - DMA controller
- Power Level Options:
  - standard power level (+7 dBm)
  - Or two RF Front End (PA and LNA, +20 dBm) versions.
- RF Output Options:
  - Chip antenna
  - U.FL connector
  - Single port 50 Ohm RF pad.
- ZigBee Software Stack Options:
  - EmberZNet PRO ZigBee stack
  - RF4CE stack
  - Low level PHY / MAC stack.
- EMI Options:
  - Standard version without shielding
  - Metal shielding protection

## Target Applications

- Smart Energy
- Building automation and control (HVAC)
- Home automation and control
- Security and monitoring
- AMR/AMI
- Logistic & Asset tracking
- Medical
- General ZigBee wireless sensor networking
- Active RFID
- Wireless hand-held terminals
- Industry telemetry /automatic data collection
- Temperature and humidity control systems
- Traffic and control for street lamp

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# 1 Product Approvals

The DZ-ZB-S-A has been designed to meet all national regulations for world-wide use.

## 1.1 FCC Approvals

The DZ-ZB-S-A with integrated Antenna has been tested to comply with **FCC CFR Part 15** (USA) The devices meet the requirements for modular transmitter approval as detailed in the **FCC public notice DA00.1407.transmitter**.

**FCC statement:**

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

**FCC ID: YCMDZZBSA**

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by DiZiC Co., Ltd. may void the user's authority to operate the equipment.

**[Paragraph Number] FCC Labelling Requirements**

When integrating the DZ-ZB-S-A into a product it must be ensured that the FCC labelling requirements are met. This includes a clearly visible label on the outside of the finished product specifying the DiZiC FCC identifier (**FCC ID: YCMDZZBSA**) as well as the FCC notice shown on the previous page. This exterior label can use wording such as "**Contains Transmitter Module FCC ID: YCMDZZBSA**" or "**Contains FCC ID: YCMDZZBSA**" although any similar wording that expresses the same meaning may be used. [Paragraph Number]

## 1.2 IC (Industry Canada) Approvals

The DiZiC DS-ZB-S-A with integrated Antenna has been tested to comply with IC.

**IC-ID: 9022A-DZZBSA**

The labelling requirements for Industry Canada are similar to those of the FCC. Again, a clearly visibly label must be placed on the outside of the finished product stating something like "**Contains Transmitter Module, IC: 9022A-DZZBSA**", although any similar wording that expresses the same meaning may be used.

The integrator is responsible for the final product to comply to IC ICES-003 and FCC Part 15, Sub. B - Unintentional Radiators.

## 1.3 European Certification (ETSI)

The DZ-ZB-S-A has been certified to the following standards:

- Radio: EN 300 328:V1.7.1
- EMC: EN 301 489-17:V2.1.1
- Safety: EN 60950-1:2005 (Ed. 2.0)

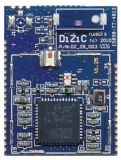
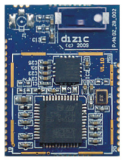
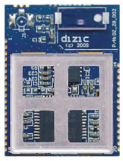
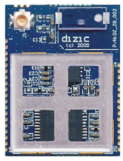
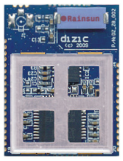
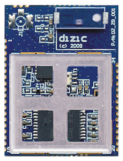
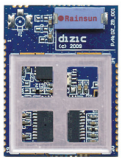
If the DZ-ZB-S-A module is incorporated into an OEM product, the OEM product manufacturer must ensure compliance of the final product to the European Harmonised EMC, and low voltage/

safety standards. A Declaration of Conformity must be issued for each of these standards and kept on file as described in Annex II of the R&TTE Directive. The final product must not exceed the specified power ratings, antenna specifications and installation requirements as specified in this user manual. If any of these specifications are exceeded in the final product then a submission must be made to a notified body for compliance testing to all of the required standards.

The 'CE' marking must be applied to a visible location on any OEM product. For more information please refer to http://ec.europa.eu/enterprise/faq/ce-mark.htm. Customers assume full responsibility for learning and meeting the required guidelines for each country in their distribution market.

# 2 Configurations

Four set of options are used to configure the *DZ-ZB Modules* based on user requirements: Output Options, Power Level Options, ZigBee Stack Options, and EMI Protection Options (not shown below).

| EMI Protection Option | Power Level Option | Output Option: 50 Ohm RF Pad | Output Option: U.FL Connector | Output Option: Embedded Antenna |
|---|---|---|---|---|
| Standard (No shielding) | Standard +7 dBm |  DZ_ZB_S-P-a-S |  DZ_ZB_S-U-a-S |  DZ_ZB_S-A-a-S |
| | Front End +20 dBm |  DZ_ZB_T-P-a-S |  DZ_ZB_T-U-a-S |  DZ_ZB_T-A-a-S |
| | Front End +20 dBm with Power Level Detector |  DZ_ZB_R-P-a-S |  DZ_ZB_R-U-a-S |  DZ_ZB_R-A-a-S |
| Enhanced Interference Protection | Standard +7 dBm |  DZ_ZB_S-P-a-M |  DZ_ZB_S-U-a-M |  DZ_ZB_S-A-a-M |
| | Front End +20 dBm |  DZ_ZB_T-P-a-M |  DZ_ZB_T-U-a-M |  DZ_ZB_T-A-a-M |
| | Front End +20 dBm with Power Level Detector |  DZ_ZB_R-P-a-M |  DZ_ZB_R-U-a-M |  DZ_ZB_R-A-a-M |

where “a” represents Stack Option, one of:
F -- RF4CE Stack
X -- Proprietary Stack
Z -- EmberZNet Pro Stack

*Figure 1: DZ-ZB module configurations*

## 2.1 Power Level Options: Codes [S] [R] or [T]

Three power level options are available, including a standard module without a power amplifier and two modules with power amplifiers sourced from two vendors.

*Table 1: Power level options*

| Selector | Option | Description |
|---|---|---|
| [S] | Standard + 7dBm | STM32W chip: System on Chip - where radio, microcontroller, program/user memory, RAM, ZigBee protocols stack are integrated in one chip. |
| [R] | Front End (PA and LNA) with RF output power level detector + 20 dBm | ADD DESCRIPTION |
| [T] | Front End (PA and LNA) + 20 dBm | ADD DESCRIPTION |

## 2.2 RF Output Options: Codes [A] [P] or [U]

Three RF output options are available, including an onboard antenna, an RF pad, and an U.FL connector.

*Table 2: Output Options*

| Selector | Option | Description |
|---|---|---|
| [A] | Embedded SMD Antenna | ADD DESCRIPTION |
| [P] | Single ended 50 Ω RF Pad | ADD DESCRIPTION |
| [U] | U.FL 50 Ω coaxial connector | ADD DESCRIPTION |

## 2.3 ZigBee Stack Options: Codes [F] [X] or [Z]

Three ZigBee stack options are available, including an RF4CE stack, a stack from Ember, and a proprietary stack. Programming instructions for each of the ZigBee stacks are included on the product CD.

*Table 3: ZigBee Stack Options*

| Selector | Option | Description |
|---|---|---|
| [F] | RF4CE stack | ADD DESCRIPTION |
| [X] | Proprietary stack | ADD DESCRIPTION |
| [Z] | EmberZnet PRO stack | ADD DESCRIPTION |

## 2.4 EMI Protection Options: [M] or [S]

A metal shield cap can be added to the module for EMI protection.

*Table 4: SEMI Protection Options*

| Selector | Option | Description |
|---|---|---|
| [M] | Metal shield cap | Enables enhanced level of electromagnetic immunity (EMI) protection. |
| [S] | Standard module | RF Module without metal shielding. |

## 2.5 Configuration Options Matrix

Table 5 below shows all the available options for the *DZ-ZB Module*.

*Table 5: DZ-ZB module options set*

| RF Output | | Output Power Level | | Software Stack | | EMI Protection | |
|---|---|---|---|---|---|---|---|
| Code | Description | Code | Description | Code | Description | Code | Description |
| A | Embedded SMD Antenna | S | Standard + 7dBm | F | RF4CE stack | M | Metal shield cap |
| P | Single ended 50 Ω RF Pad | R | Front End (PA and LNA) with RF output power level detector + 20 dBm | X | Proprietary stack | S | Standard module |
| U | U.FL 50 Ω coaxial connector | T | Front End (PA and LNA) + 20 dBm | Z | EmberZnet PRO stack | | |

With these options, a total of 54 configurations of the *DZ-ZB module* are possible. Table 6 provides a matrix of these configurations and the associated codes, which are used when ordering the module.

*Table 6: Configuration options matrix*

| | A | | | | | | P | | | | | | U | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | F | | X | | Z | | F | | X | | Z | | F | | X | | Z | |
| | M | S | M | S | M | S | M | S | M | S | M | S | M | S | M | S | M | S |
| S | ASFM | ASFS | ASXM | ASXS | AFZM | AFZS | PSFM | PSFS | PSXM | PSXS | PSZM | PSZS | USFM | USFS | USXM | USXS | USZM | USZS |
| R | ARFM | ARFS | ARXM | ARXS | ARZM | ARZS | PRFM | PRFS | PRXM | PRXS | PRZM | PRXS | URFM | URFS | URXM | URXS | URZM | URZS |
| T | ATFM | ATFS | ATXM | ATZM | ATXS | ATZS | AOFM | AOFS | AOXM | AOXS | AOZM | AOZS | UTFM | UTFS | UTXM | UTXS | UTZM | UTZS |

# 3 Block Diagram

The *DZ-ZB Module* is low-power, highly sensitivity IEEE 802.15.4 / ZigBee-compliant module. This multi-functional device is based on the *STMicroelectronics* STM32W108 fully integrated System-on-Chip[1] (STM32W108CBU6x version).

This STM32W108 SoC integrates a 2.4 GHz IEEE 802.15.4-compliant transceiver, a 32-bit ARM® Cortex™- M3 microprocessor, Flash and RAM memory, as well as peripherals for use by designers of ZigBee-based systems [2].

Figure 2 below shows a block diagram of the *DZ-ZB Module*.

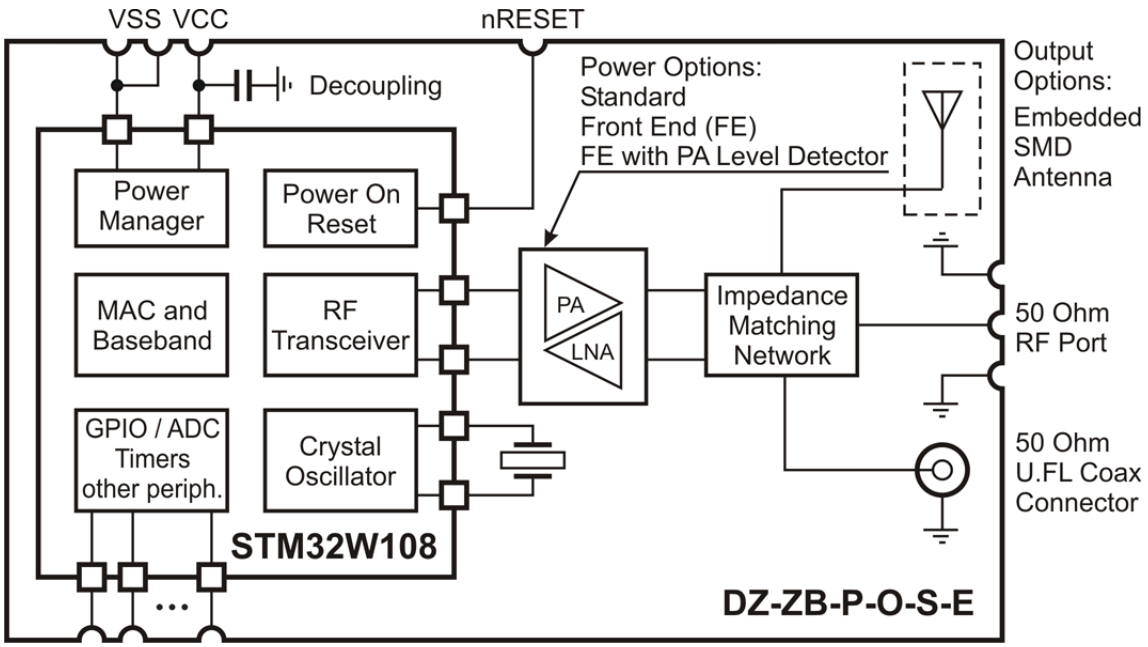



*Figure 2: Block diagram of DZ-ZB RF Modules*

# 4 Absolute Maximum Ratings

Stresses above the absolute maximum ratings listed in this section may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 4.1 Voltage Characteristics

*Table 7: Voltage characteristics*

| Ratings | Min. | Max. | Unit |
|---|---|---|---|
| Regulator input voltage (VDD_PADS) | -0.3 | +3.6 | V |
| RF Input Power (for max level for correct packet reception Receive characteristics) RX signal into a lossless balun | | 15 | dBm |
| Voltage on any GPIO (PA[7:0], PB[7:0], PC[7:0]), SWCLK, nRESET, VREG_OUT | -0.3 | VDD_PADS +0.3 | V |

## 4.2 Current Characteristics

*Table 8: Current characteristics*

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| IVDD | Total current into VDD/VDDA power lines (source) | 150 | mA |
| IVSS | Total current out of VSS ground lines (sink) | 150 | mA |
| IIO | Output current sunk by any I/O and control pin | 25 | mA |

## 4.3 Thermal Characteristics

*Table 9: Thermal characteristics*

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| TSTG | Storage temperature range | –40 to +140 | ℃ |
| TJ | Maximum junction temperature | 150 | ℃ |

# 5 Components

This section describes the key components of the *DZ-ZB Modules* including the STM32W108 SoC, the RF Front End with RF Output Power Level Detector, the RF Front End (FE), and the ZigBee stacks.

## 5.1 STM32W108 – System-on-Chip Transceiver

The STM32W108 is a fully integrated System-on-Chip that includes:

- 2.4 GHz, IEEE 802.15.4 compliant transceiver
- 32-bit ARM® Cortex™ -M3 microprocessor
- Flash and RAM memory
- Peripherals for use of designers of ZigBee-based systems.

Figure 3 below shows the block diagram of STM32W108.

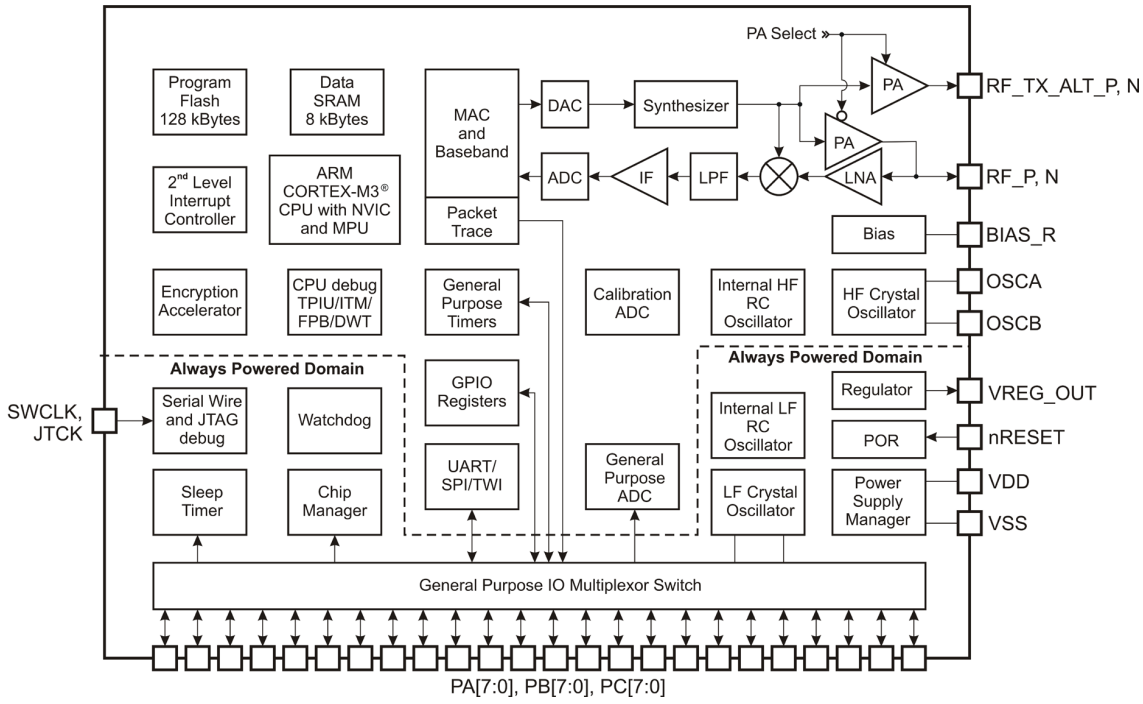



*Figure 3: Block diagram of System-on-Chip STM32W108*

### 5.2.1 IEEE 802.15.4 Compliant Transceiver

This SoC transceiver utilizes an efficient architecture that exceeds the dynamic range requirements imposed by the IEEE 802.15.4-2003 standard by over 15 dB. The integrated receive channel filtering allows for robust
co-existence with other communication standards in the 2.4 GHz spectrum such as IEEE 802.11 and Bluetooth. The integrated regulator, VCO, loop filter, and power amplifier keep the external component count low. An optional high performance radio mode (boost mode) is software-selectable to boost dynamic range.

### 5.3.2 Operation Modes

The integrated 32-bit ARM® Cortex™-M3 microprocessor is highly optimized for high performance, low power consumption, and efficient memory utilization. With its integrated MPU, the STM32W108 supports two different modes of operation: System mode and Application mode.

The networking stack software runs in System Mode with full access to all areas of the chip. Application code, however, runs in Application Mode with limited access to STM32W108 resources. This allows for the scheduling of events by the application developer while preventing modification of restricted areas of memory and registers. This architecture results in increased stability and reliability of deployed solutions.

### 5.4.3 Flash and RAM Memory

The STM32W108 has 128 Kbytes of embedded Flash memory and 8 Kbytes of integrated RAM for data and program storage. The STM32W108 HAL software employs an effective wear-levelling algorithm that optimizes the lifetime of the embedded Flash.

### 5.5.4 Integrated MAC Functions

To maintain the strict timing requirements imposed by ZigBee and IEEE 802.15.4-2003 standards, the STM32W108 IC integrates a number of MAC functions into the hardware. The MAC hardware handles automatic ACK transmission and reception, automatic back off delay, and clear channel assessment for transmission, as well as automatic filtering of received packets. A packet trace interface is also integrated in the MAC hardware allowing complete, non-intrusive capture of all packets to and from the STM32W108 IC.

### 5.6.5 Power Management

The STM32W108 IC offers a number of advanced power management features that enables long battery life. A high-frequency internal RC oscillator allows the processor core to begin code execution quickly upon waking. Various deep sleep modes are available with less than 1 µs power consumption while retaining RAM contents.

### 5.7.6 Peripherals

To support user-defined applications, on-chip peripherals include UART, SPI, TWI, ADC, general-purpose timers, and up to 24 GPIOs. Additionally, an integrated voltage regulator, power-on-reset circuit, and sleep timer are available.

### 5.8.7 Interfaces

The STM32W108 IC utilizes standard Serial Wire and JTAG interfaces for powerful software debugging and programming of the ARM Cortex-M3 core. The STM32W108 IC integrates the standard ARM system debug components including Flash Patch and Breakpoint (FPB), Data Watch-point and Trace (DWT), and Instrumentation Trace Macrocell (ITM).

## 5.9 + 20 dBm Front End (PA and LNA) with RF Output Power Level Detector

This optional *Front End* (FE) available with the DZ-ZB Module (code [R]) is a fully integrated, single-chip, single-die microwave IC which incorporates all the RF functionality needed for today's wireless communications. The architecture of this FE IC integrates the following all in a BiCMOS single-chip device:

- RF power Level (at PA output) detect circuit
- A Power Amplifier (PA) and a Low Noise Amplifier (LNA)
- TX and RX switching circuitry
- Associated matching network
- Harmonic filter

Combining superior performance, high sensitivity and efficiency, low noise, small form factor, and low cost, this FE is the perfect solution for applications requiring extended range and bandwidth and can result in a potential 10x range increase.

The block diagram of the module with the RF Front End is shown in figure 4 below:

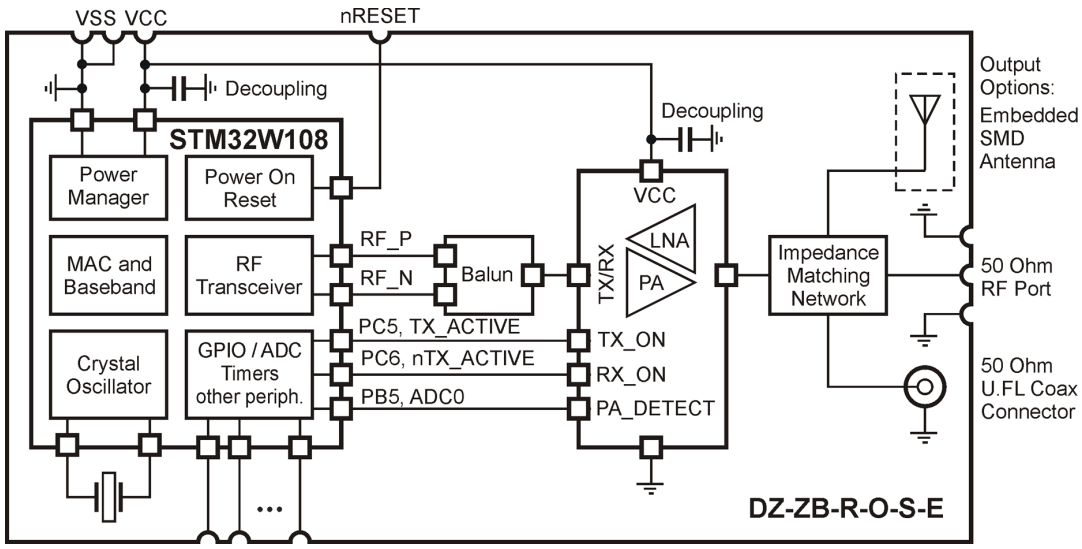



*Figure 4: Module block diagram with front end incorporating RF power level detector (Power level option "R")*

The table below summarizes the functional description of the signals controlling front end.

*Table 10: Functional description of the Front End signals*

| FE Signal name | Direction | Description | STM32W108 port name |
|---|---|---|---|
| TX_ON | Digital input to FE | When RX_ON = 1:<br>TX_ON = 1:Transmit Mode<br>TX_ON = 0: Receive Mode | PC5, TX_ACTIVE |
| RX_ON | Digital input to FE | RX_ON = 0: FE in shut down mode<br>RX_ON = 1: FE enabled<br>Transmit / Receive function is determined by TX_ON signal | PC6, nTX_ACTIVE |

*Table 10: Functional description of the Front End signals*

| FE Signal name | Direction | Description | STM32W108 port name |
|---|---|---|---|
| PA_DETECT | Analog output from FE | PA_DETECT voltage is proportional to generated RF power at FE output pin.<br>For RF output power between:<br>+5 dBm to +20 dBm<br>PA_DETECT voltage is between 20 mV<br>to 1200 mV respectively | PB5, ADC0 |

## 5.10 + 20 dBm RF FRONT END Front End (PA and LNA)

This optional RF Front End is a cost-effective and high performance IC for low-power and low-voltage 2.4-GHz wireless applications. It extends the range for all existing and future 2.4-GHz low-power RF transceivers, transmitters and System-on-Chip products. It increases the link budget by providing a power amplifier for increased output power, and an LNA with low noise figure for improved receiver sensitivity. This FE for high performance wireless applications consists of

- A 20 dBm Power Amplifier (PA) and a Low Noise Amplifier (LNA)
- RF switching circuitry
- RF impedance matching circuits
- Balun

The block diagram of the 20 dBm RF Front End is shown in figure 5 below.

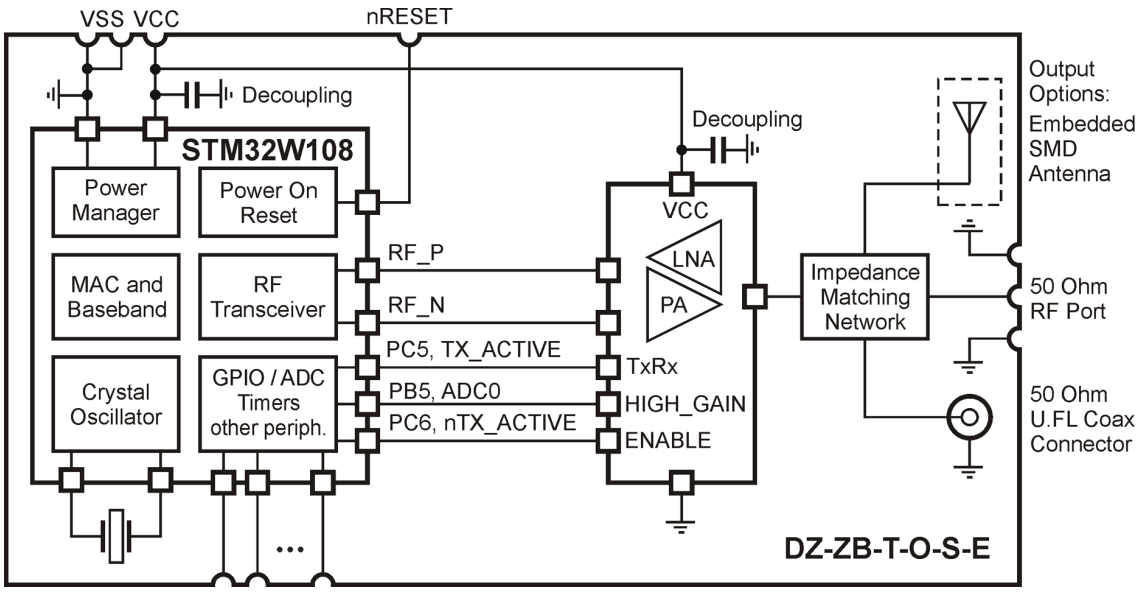



*Figure 5: Block diagram of the module with front end (Power level option "T")*

Table 11 below summarizes the functional description of the signals controlling front end.

*Table 11: Functional description of the Front End signals*

| FE Signal name | Direction | Description | STM32W108 port name |
|---|---|---|---|
| TxRx | Digital input to FE | When ENABLE = 1:<br>TxRx = 1: Transmit Mode<br>TxRx = 0: Receive Mode | PC5, TX_ACTIVE |
| HIGH_GAIN | Digital input to FE | Receive only (ENABLE = 1, TxRx = 0):<br>HIGH_GAIN = 1: LNA is in High Gain Mode.<br>LNA Gain = approx. 11dB<br>HIGH_GAIN = 0: LNA is in Low Gain Mode.<br>LNA Gain = approx. 1 dB | PB5, ADC0 |
| ENABLE | Digital input to FE | ENABLE = 1: FE Enabled ENABLE = 0: FE in power down mode | PC6, nTX_ACTIVE |

## 5.11 ZigBee Stacks

Three ZigBee stacks are available:

- RF4CE (Radio Frequency for Consumer Electronics) stack, which is used primarily for a wide range of remotely-controlled audio/visual consumer electronics products.
- Proprietary ZigBee stack, which is a robust ZigBee protocol software package for wireless control and monitoring applications.
- EmberZNet PRO stack, which is a complete ZigBee protocol software package containing all the elements required for robust and reliable mesh networking applications.

Figure 6 below shows the a block diagram of the three optional ZigBee stacks.

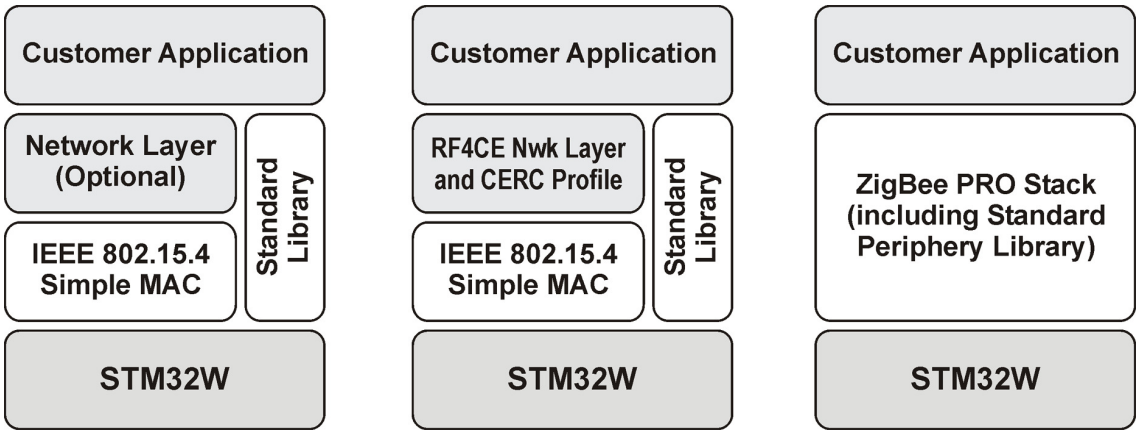



*Figure 6: Available stacks*

# 6 Electrical Characteristics

## 6.1 Parameter conditions

**Note:** Unless otherwise specified, all voltages are referenced as VSS.

### 6.2.1 Minimum and Maximum Values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation, and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3).

### 6.3.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25°C, VDD = 3.3 V (for the 2V VDD 3.6 V voltage range). They are given only as design guidelines and are not tested. Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

## 6.4 Operating Conditions

### 6.5.1 General Operating Conditions

*Table 12: General operating conditions*

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VDD_PADS | Regulator input voltage (VDD_PADS) | 2.1 | – | 3.6 | V |
| TOP | Operating temperature range | -40 | – | 85 | ℃ |

### 6.6.2 Electrostatic Discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

*Table 13: ESD absolute maximum ratings*

| Symbol | Ratings | Conditions | Class | Maximum value | Unit |
|---|---|---|---|---|---|
| VESD (HBM) | Electrostatic discharge voltage (Human Body Model) | TA = +25 ℃ conforming to JESD22-A114 | 2 | ±2000 | V |
| VESD (CDM) | Electrostatic discharge voltage (Charge Device Model) for non-RF pins | TA = +25 ℃ conforming to JESD22-C101 | II | ±400 | |
| | Electrostatic discharge voltage (Charge Device Model) for RF pins | | | ±225 | |
| MSL | Moisture sensitivity level | – | – | MSL3 | – |

### 6.7.3 DC Characteristics

*Table 14: DC electrical characteristics*

| Parameter | Conditions | Typical value for module (Power Level Option) | | | Unit |
|---|---|---|---|---|---|
| | | "S" Standard | "R" Front End | "T" Front End | |
| Regulator input voltage (VDD_PADS) | – | 2.0 - 3.6 | – | – | V |
| **Deep Sleep Current** | | | | | |
| Quiescent current, internal RC oscillator disabled | -40℃, VDD_PADS = 3.6 V | 0.4 | – | – | A |
| | +25℃, VDD_PADS = 3.6 V | 0.4 | 5.4 | 0.7 | A |
| | +85℃, VDD_PADS = 3.6 V | 0.6 | – | – | A |
| Quiescent current, including internal RC oscillator | -40℃, VDD_PADS = 3.6 V | 0.7 | – | – | A |
| | +25℃, VDD_PADS = 3.6 V | 0.8 | 5.8 | 1.1 | A |
| | +85℃, VDD_PADS = 3.6 V | 1.2 | – | – | A |
| Quiescent current, including 32.768 kHz oscillator | -40℃, VDD_PADS = 3.6V | 1.2 | – | – | A |
| | +25℃, VDD_PADS = 3.6 V | 1.3 | 6.3 | 1.6 | A |
| | +85℃, VDD_PADS = 3.6 V | 1.7 | – | – | A |
| Quiescent current, including internal RC oscillator and 32.768 kHz oscillator | -40℃, VDD_PADS = 3.6V | 1.4 | – | – | A |
| | +25℃, VDD_PADS = 3.6V | 1.5 | 6.5 | 1.8 | A |
| | +85℃, VDD_PADS = 3.6 V | 2 | – | – | A |
| Simulated deep sleep (debug mode) current | With no debugger activity | 200 | – | – | A |

*Table 14: DC electrical characteristics (Continued)*

| Parameter | Conditions | Typical value for module (Power Level Option) | | | Unit |
|---|---|---|---|---|---|
| | | "S" Standard | "R" Front End | "T" Front End | |
| **Reset current** | | | | | |
| Quiescent current, nRESET asserted | Typical at 25℃/3 V Max at 85℃/3.6 V | 1.2 | 1.2 | 1.2 | mA |
| **Processor and peripheral currents** | | | | | |
| ARM® Cortex-M3, RAM, and flash memory | 25℃, 1.8 V memory and 1.25 V core ARM® Cortex-M3 running at 12 MHz from crystal oscillator Radio and all peripherals off | 8.0 | 8.0 | 8.0 | mA |
| ARM® Cortex-M3, RAM, and flash memory | 25℃, 1.8 V memory and 1.25 V core ARM® Cortex-M3 running at 24 MHz from crystal oscillator Radio and all peripherals off | 9.0 | 9.0 | 9.0 | mA |
| ARM® Cortex-M3, RAM, and flash memory sleep current | 25℃, 1.8 V memory and 1.25 V core ARM® Cortex-M3 clocked at 12 MHz from the crystal oscillator Radio and all peripherals off | 4.0 | 4.0 | 4.0 | mA |
| ARM® Cortex-M3, RAM, and flash memory sleep current | 25℃, 1.8 V memory and 1.25 V core ARM® Cortex-M3 clocked at 6 MHz from the high frequency RC oscillator Radio and all peripherals off | 2.0 | 2.0 | 2.0 | mA |
| Serial controller current | For each controller at maximum data rate | 0.2 | 0.2 | 0.2 | mA |
| General purpose timer current | For each timer at maximum clock rate | 0.1 | 0.1 | 0.1 | mA |
| General purpose ADC current | At maximum sample rate, DMA enabled | 1.1 | 1.1 | 1.1 | mA |
| **RX current** | | | | | |
| Radio receiver, MAC, and baseband | ARM® Cortex-M3 sleeping | 20 | 27 | 24 | mA |
| Total RX current (Radio receiver, MAC and baseband, CPU + IRAM, and Flash memory) | VDD_PADS = 3,0 V, 25℃, ARM® Cortex-M3 running at 12 MHz | 27 | 34 | 31 | mA |
| VDD_PADS = 3,0 V, 25℃, ARM® Cortex-M3 running at 24 MHz | – | 28 | 35 | 32 | mA |

*Table 14: DC electrical characteristics (Continued)*

| Parameter | Conditions | Typical value for module (Power Level Option) | | | Unit |
|---|---|---|---|---|---|
| | | "S" Standard | "R" Front End | "T" Front End | |
| Boost mode total RX current (Radio receiver, MAC and baseband, CPU+ IRAM, and Flash memory ) | VDD_PADS = 3,0 V, 25°C, ARM® Cortex-M3 running at 12 MHz | 28 | 35 | 32 | mA |
| VDD_PADS = 3,0 V, 25°C, ARM® Cortex-M3 running at 24 MHz | – | 29 | 36 | 33 | mA |
| **TX current** | | | | | |
| Radio transmitter, MAC, and baseband | 25°C and 1.8 V core; max. power out (+3 dBm typical) ARM® Cortex-M3 sleeping | 26 | 136 | 138 | mA |
| Total TX current (Radio transmitter, MAC and baseband, CPU + IRAM, and Flash memory) | VDD_PADS = 3.0 V, 25°C; maximum power setting (+7dBm); running at 24 MHz | 40 | 150 | 152 | mA |
| | VDD_PADS = 3.0 V, 25°C; +3 dBm power setting; ARM® Cortex-M3 running at 24 MHz | 32 | 142 | 144 | mA |
| | VDD_PADS = 3.0 V, 25°C; 0dBm power setting; ARM® Cortex-M3 running at 24 MHz | 30 | 140 | 142 | mA |
| | VDD_PADS = 3.0 V, 25°C; minimum power setting; ARM® Cortex-M3 running at 24 MHz | 24 | 134 | 136 | mA |

## 6.8 RF Characteristic

### 6.9.1 Receiver Characteristics

*Table 15: Receiver characteristics*

| Parameter | Conditions | Typical value for module (Power Level Option) | | | Unit |
|---|---|---|---|---|---|
| | | [S] Standard | [R] Front End | [T] FrontEnd | |
| Frequency range | – | 2400 - 2500 | | | MHz |
| Sensitivity (boost mode) | 1% PER, 20 byte packet defined by IEEE 802.15.4-2003 | -100 | TBD | -105 | dBm |

*Table 15: Receiver characteristics*

| Parameter | Conditions | Typical value for module (Power Level Option) | | | Unit |
|---|---|---|---|---|---|
| | | [S] Standard | [R] Front End | [T] Front End | |
| Sensitivity | 1% PER, 20 byte packet defined by IEEE 802.15.4-2003 | -99 | TBD | -104 | dBm |
| Co-channel rejection | IEEE 802.15.4 signal at -82 dBm | -6 | – | – | dBc |
| Relative frequency error (2 x 40 ppm required by IEEE 802.15.4) | – | -120 …+120 | – | – | ppm |
| Relative timing error (2 x 40 ppm required by IEEE 802.15.4) | – | -120 …+120 | – | – | ppm |
| Linear RSSI range | As defined by IEEE 802.15.4 | 40 | – | – | dB |
| RSSI Range | – | -90 … -30 | – | – | dBm |

### 6.10.2 Transmitter Characteristics

*Table 16: Transmitter characteristics*

| Parameter | Conditions | Typical value for module (Power Level Option) | | | Unit |
|---|---|---|---|---|---|
| | | [S] Standard | [R] Front End | [T] Front End | |
| Maximum output power (boost mode) | At highest power setting | 7 | 20 | 20 | dBm |
| Maximum output power | At highest power setting | 3 | 20 | 20 | dBm |
| Minimum output power | At lowest power setting | -32 | -9 | -9 | dBm |
| Error vector magnitude | As defined by IEEE 802.15.4, which sets a 35% maximum | 5 … 15 | | | % |
| Carrier frequency error | – | -40 … +40 | | | ppm |
| PSD mask relative | 3.5 MHz away | -20 | – | – | dB |
| PSD mask absolute | 3.5 MHz away | -30 | – | – | dBm |

# 7 Mechanical Characteristics

## 7.1 Module Pad Diagram

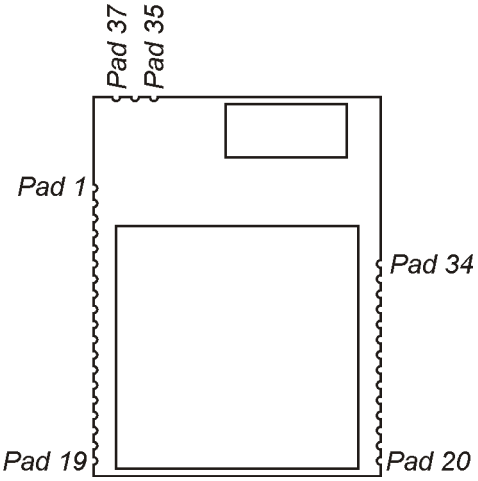



*Figure 7: Pad connection diagram for modules (top view)*

## 7.2 Module Pads

*Table 17: Pad description*

| Pad | Signal | Direction | Description |
|---|---|---|---|
| 1 | GND | Power | Ground supply pad. |
| 2 | GND | Power | Ground supply pad. |
| 3 | VCC | Power | Power supply pad. |
| 4 | VCC | Power | Power supply pad. |
| 5 | nRESET | I | Active low chip reset (internal pull-up). |
| 6 | PC5 | I/O | Digital I/O. |
| | TX_ACTIVE | O | Logic-level control for external Rx/Tx switch.<br>- The STM32W108 baseband controls TX_ACTIVE and drives it high (VDD_PADS) when in Tx mode.<br>- Select alternate output function with GPIO_PCCFGH[7:4]. |
| 7 | PC6 | I/O | Digital I/O. |
| | OSC32B | I/O | 32.768 kHz crystal oscillator.<br>- Select analogue function with GPIO_PCCFGH[11:8]. |
| | nTX_ACTIVE | O | Inverted TX_ACTIVE signal (see PC5).<br>- Select alternate output function with GPIO_PCCFGH[11:8]. |

*Table 17: Pad description (Continued)*

| Pad | Signal | Direction | Description |
|---|---|---|---|
| 8 | PC7 | I/O | Digital I/O. |
| | OSC32A | I/O | 32.768 kHz crystal oscillator.<br>- Select analogue function with GPIO_PCCFGH[15:12]. |
| | OSC32_EXT | I | Digital 32 kHz clock input source. |
| 9 | PA7 | I/O High current | Digital I/O Disable REG_EN with GPIO_DBGCFG[4]. |
| | TIM1CH4 | O | Timer 1 Channel 4 output.<br>Enable timer output with TIM1_CCER.<br>Select alternate output function with GPIO_PACFGH[15:12].<br>Disable REG_EN with GPIO_DBGCFG[4]. |
| | | I | Timer 1 Channel 4 input. Cannot be remapped. |
| | REG_EN | O | External regulator open drain output. (Enabled after reset). |
| 10 | PB3 | I/O | Digital I/O |
| | TIM2_CH3<br>*See also Pad 13* | O | Timer 2 channel 3 output.<br>Enable remap with TIM2_OR[6].<br>Enable timer output in TIM2_CCER.<br>Select alternate output function with GPIO_PBCFGL[15:12]. |
| | | I | Timer 2 channel 3 input Enable remap with TIM2_OR[6]. |
| | UART_CTS | I | UART CTS handshake of Serial Controller 1.<br>- Enable with SC1_UARTCFG[5].<br>- Select UART with SC1_MODE. |
| | SC1SCLK | O | SPI master clock of Serial Controller 1.<br>- Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[6] Enable master with SC1_SPICFG[4].<br>- Select SPI with SC1_MODE.<br>- Select alternate output function with GPIO_PBCFGL[15:12]. |
| | | I | SPI slave clock of Serial Controller 1.<br>Enable slave with SC1_SPICFG[4].<br>Select SPI with SC1_MODE. |

*Table 17: Pad description (Continued)*

| Pad | Signal | Direction | Description |
|---|---|---|---|
| 11 | PB4 | I/O | Digital I/O |
| | TIM2_CH4<br>*See also Pad 15* | O | Timer 2 channel 4 output...Enable remap with TIM2_OR[7].<br>- Enable timer output in TIM2_CCER.<br>- Select alternate output function with GPIO_PBCFGH[3:0]. |
| | | I | Timer 2 channel 4 input.<br>- Enable remap with TIM2_OR[7]. |
| | UART_RTS | O | UART RTS handshake of Serial Controller 1.<br>- Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[7].<br>- Enable with SC1_UARTCFG[5] Select UART with SC1_MODE.<br>- Select alternate output function with GPIO_PBCFGH[3:0]. |
| | SC1nSSEL | I | SPI slave select of Serial Controller 1.<br>- Enable slave with SC1_SPICFG[4].<br>- Select SPI with SC1_MODE. |
| 12 | PA0 | I/O | Digital I/O |
| | TIM2_CH1<br>*See also Pad 20* | O | Timer 2 channel 1 output.<br>- Disable remap with TIM2_OR[4].<br>- Enable timer output in TIM2_CCER.<br>- Select alternate output function with GPIO_PACFGL[3:0]. |
| | | I | Timer 2 channel 1 input...Disable remap with TIM2_OR[4]. |
| | SC2MOSI | O | SPI master data out of Serial Controller 2.<br>- Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[4].<br>- Enable master with SC2_SPICFG[4].<br>- Select SPI with SC2_MODE.<br>- Select alternate output function with GPIO_PACFGL[3:0]. |
| | | I | SPI slave data in of Serial Controller 2<br>- Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE |

*Table 17: Pad description (Continued)*

| Pad | Signal | Direction | Description |
|---|---|---|---|
| 13 | PA1 | I/O | Digital I/O |
| | TIM2_CH3<br>*See also Pad 10* | O | Timer 2 channel 3 output.<br>- Disable remap with TIM2_OR[6].<br>- Enable timer output in TIM2_CCER.<br>- Select alternate output function with GPIO_PACFGL[7:4]. |
| | | I | Timer 2 channel 3 input<br>- Disable remap with TIM2_OR[6] |
| | SC2SDA | I/O | TWI data of Serial Controller 2<br>- Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[6] Select TWI with SC2_MODE.<br>- Select alternate open-drain output function with GPIO_PACFGL[7:4]. |
| | SC2MISO | O | SPI slave data out of Serial Controller 2.<br>- Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[6].<br>- Enable slave with SC2_SPICFG[4].<br>- Select SPI with SC2_MODE.<br>- Select alternate output function with GPIO_PACFGL[7:4]. |
| | | I | SPI master data in of Serial Controller 2.<br>- Enable slave with SC2_SPICFG[4]. |
| 14 | GND | Power | Ground supply pad. |
| 15 | PA2 | I/O | Digital I/O. |
| | TIM2_CH4<br>*See also Pad 11* | O | Timer 2 channel 4 output.<br>- Disable remap with TIM2_OR[7].<br>- Enable timer output in TIM2_CCER.<br>- Select alternate output function with GPIO_PACFGL[11:8]. |
| | | I | Timer 2 channel 4 input<br>- Disable remap with TIM2_OR[7]. |
| | SC2SCL | I/O | TWI clock of Serial Controller 2.<br>- Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[7].<br>- Select TWI with SC2_MODE.<br>- Select alternate open-drain output function with GPIO_PACFGL[11:8]. |
| | SC2SCLK | O | SPI master clock of Serial Controller 2.<br>- Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[7].<br>- Enable master with SC2_SPICFG[4].<br>- Select SPI with SC2_MODE.<br>- Select alternate output function with GPIO_PACFGL[11:8]. |
| | | I | SPI slave clock of Serial Controller 2.<br>- Enable slave with SC2_SPICFG[4].<br>- Select SPI with SC2_MODE. |

*Table 17: Pad description (Continued)*

| Pad | Signal | Direction | Description |
|---|---|---|---|
| 16 | PA3 | I/O | Digital I/O. |
| | SC2nSSEL | I | SPI slave select of Serial Controller 2.<br>- Enable slave with SC2_SPICFG[4].<br>- Select SPI with SC2_MODE. |
| | TRACECLK<br>*See also Pad 27* | O | Synchronous CPU trace clock.<br>- Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[5].<br>- Enable trace interface in ARM core.<br>- Select alternate output function with GPIO_PACFGL[15:12]. |
| | TIM2_CH2<br>*See also Pad 21* | O | Timer 2 channel 2 output.<br>- Disable remap with TIM2_OR[5].<br>- Enable timer output in TIM2_CCER.<br>- Select alternate output function with GPIO_PACFGL[15:12]. |
| | | I | Timer 2 channel 2 input Disable remap with TIM2_OR[5]. |
| 17 | PA4 | I/O | Digital I/O. |
| | ADC4 | Analog | ADC Input 4<br>- Select analogue function with GPIO_PACFGH[3:0]. |
| | PTI_EN | O | Frame signal of Packet Trace Interface (PTI).<br>- Disable trace interface in ARM core.<br>- Select alternate output function with GPIO_PACFGH[3:0]. |
| | TRACEDATA2 | O | Synchronous CPU trace data bit 2<br>Select 4-wire synchronous trace interface in ARM core<br>Enable trace interface in ARM core<br>Select alternate output function with GPIO_PACFGH[3:0]. |
| 18 | PA5 | I/O | Digital I/O. |
| | ADC5 | Analog | ADC Inputs<br>- Select analog function with GPIO_PACFGH[7:4]. |
| | PTI_DATA | O | Data signal of Packet Trace Interface (PTI).<br>- Disable trace interface in ARM core.<br>- Select alternate output function with GPIO_PACFGH[7:4]. |
| | nBOOTMODE | I | Embedded serial boot-loader activation out of reset.<br>- Signal is active during and immediately after a reset on nRESET. |
| | TRACEDATA3 | O | Synchronous CPU trace data bit 3.<br>- Select 4-wire synchronous trace interface in ARM core.<br>- Enable trace interface in ARM core.<br>- Select alternate output function with GPIO_PACFGH[7:4]. |
| 19 | PA6 | I/O High current | Digital I/O. |
| | TIM1_CH3 | O | Timer 1 channel 3 output.<br>- Enable timer output in TIM1_CCER.<br>- Select alternate output function with GPIO_PACFGH[11:8]. |
| | | I | Timer 1 channel 3 input<br>- Cannot be remapped. |

*Table 17: Pad description (Continued)*

| Pad | Signal | Direction | Description |
|---|---|---|---|
| 20 | PB1 | I/O | Digital I/O. |
| | SC1MISO | O | SPI slave data out of Serial Controller 1.<br>Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4].<br>Select SPI with SC1_MODE.<br>Select slave with SC1_SPICR.<br>Select alternate output function with GPIO_PBCFGL[7:4]. |
| | SC1MOSI | O | SPI master data out of Serial Controller 1.<br>Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4]<br>Select SPI with SC1_MODE.<br>Select master with SC1_SPICR.<br>Select alternate output function with GPIO_PBCFGL[7:4]. |
| | SC1SDA | I/O | TWI data of Serial Controller 1.<br>- Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4].<br>- Select TWI with SC1_MODE.<br>- Select alternate open-drain output function with GPIO_PBCFGL[7:4]. |
| | SC1TXD | O | UART transmit data of Serial Controller 1.<br>- Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4].<br>- Select UART with SC1_MODE.<br>- Select alternate output function with GPIO_PBCFGL[7:4]. |
| | TIM2_CH1<br>*See also Pad 12* | O | Timer 2 channel 1 output.<br>- Enable remap with TIM2_OR[4].<br>- Enable timer output in TIM2_CCER.<br>- Select alternate output function with GPIO_PACFGL[7:4]. |
| | | I | Timer 2 channel 1 input.<br>- Disable remap with TIM2_OR[4]. |

*Table 17: Pad description (Continued)*

| Pad | Signal | Direction | Description |
|---|---|---|---|
| 21 | PB2 | I/O | Digital I/O |
| | SC1MISO | I | SPI master data in of Serial Controller 1.<br>- Select SPI with SC1_MODE.<br>- Select master with SC1_SPICR. |
| | SC1MOSI | I | SPI slave data in of Serial Controller 1.<br>- Select SPI with SC1_MODE.<br>- Select slave with SC1_SPICR. |
| | SC1SCL | I/O | TWI clock of Serial Controller 1.<br>- Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[5].<br>- Select TWI with SC1_MODE.<br>- Select alternate open-drain output function with GPIO_PBCFGL[11:8]. |
| | SC1RXD | I | UART receive data of Serial Controller 1.<br>- Select UART with SC1_MODE. |
| | TIM2_CH2<br>*See also Pad 16* | O | Timer 2 channel 2 output.<br>- Enable remap with TIM2_OR[5].<br>- Enable timer output in TIM2_CCER.<br>- Select alternate output function with GPIO_PBCFGL[11:8]. |
| | | I | Timer 2 channel 2 input.<br>- Enable remap with TIM2_OR[5]. |
| 22 | SWCLK | I/O | Serial Wire clock input/output with debugger.<br>- Selected when in Serial Wire mode (see JTMS description, Pad 26). |
| | JTCK | 1 | JTAG clock input from debugger.<br>- Selected when in JTAG mode (default mode, see JTMS description, Pad 26) Internal pull-down is enabled. |
| 23 | PC2 | I/O | Digital I/O.<br>- Enable with GPIO_DBGCFG[5]. |
| | JTDO | O | JTAG data out to debugger.<br>- Selected when in JTAG mode (default mode, see JTMS description, Pad 26). |
| | SWO | O | Serial Wire Output asynchronous trace output to debugger.<br>- Select asynchronous trace interface in ARM core.<br>- Enable trace interface in ARM core.<br>- Select alternate output function with GPIO_PCCFGL[11:8].<br>- Enable Serial Wire mode (see JTMS description, Pad 26).<br>- Internal pull-up is enabled. |
| 24 | PC3 | I/O | Digital I/O.<br>- Either enable with GPIO_DBGCFG[5], or enable Serial Wire mode (see JTMS description, Pad 26) |
| | JTDI | 1 | JTAG data in from debugger.<br>- Selected when in JTAG mode (default mode, see JTMS description, Pad 26).<br>- Internal pull-up is enabled. |

*Table 17: Pad description (Continued)*

| Pad | Signal | Direction | Description |
|---|---|---|---|
| 25 | GND | Power | Ground supply pad. |
| 26 | PC4 | I/O | Digital I/O.<br>- Enable with GPIO_DBGCFG[5]. |
| | JTMS | I | JTAG mode select from debugger.<br>- Selected when in JTAG mode (default mode).<br>- JTAG mode is enabled after power-up or by forcing nRESET low.<br>- Select Serial Wire mode using the ARM-defined protocol through a debugger.<br>- Internal pull-up is enabled. |
| | SWDIO | I/O | Serial Wire bidirectional data to/from debugger.<br>- Enable Serial Wire mode (see JTMS description)<br>- Select Serial Wire mode using the ARM-defined protocol through a debugger<br>- Internal pull-up is enabled. |
| 27 | PB0 | I/O | Digital I/O. |
| | VREF | Analog O | ADC reference output.<br>- Enable analog function with GPIO_PBCFGL[3:0]. |
| | VREF | Analog I | ADC reference input.<br>- Enable analog function with GPIO_PBCFGL[3:0].<br>- Enable reference output with an STM system function. |
| | IRQA | I | External interrupt source A. |
| | TRACECLK *See also Pad 16* | O | Synchronous CPU trace clock.<br>- Enable trace interface in ARM core.<br>- Select alternate output function with GPIO_PBCFGL[3:0]. |
| | TIM1CLK | I | Timer 1 external clock input. |
| | TIM2MSK | I | Timer 2 external clock mask input. |
| 28 | GND | Power | Ground supply pad. |
| 29 | PC1 | I/O | Digital I/O. |
| | ADC3 | Analog | ADC Inputs.<br>- Enable analog function with GPIO_PCCFGL[7:4] |
| | SWO *See also Pad 23* | O | Serial Wire Output asynchronous trace output to debugger.<br>- Select asynchronous trace interface in ARM core.<br>- Enable trace interface in ARM core.<br>- Select alternate output function with GPIO_PCCFGL[7:4]. |
| | TRACEDATA0 | O | Synchronous CPU trace data bit 0.<br>- Select 1-, 2- or 4-wire synchronous trace interface in ARM core.<br>- Enable trace interface in ARM core.<br>- Select alternate output function with GPIO_PCCFGL[7:4]. |

*Table 17: Pad description (Continued)*

| Pad | Signal | Direction | Description |
|---|---|---|---|
| 30 | PC0 | I/O High current | Digital I/O.<br>- Either enable with GPIO_DBGCFG[5], or enable Serial Wire mode (see JTMS description, Pad 26) and disable TRACEDATA1. |
| | JRST | I | JTAG reset input from debugger.<br>- Selected when in JTAG mode (default mode, see JTMS description) and TRACEDATA1 is disabled.<br>- Internal pull-up is enabled. |
| | IRQD1 | I | Default external interrupt source D |
| | TRACEDATA1 | O | Synchronous CPU trace data bit 1.<br>- Select 2- or 4-wire synchronous trace interface in ARM core.<br>- Enable trace interface in ARM core.<br>- Select alternate output function with GPIO_PCCFGL[3:0]. |
| 31 | PB7 | I/O High current | Digital I/O. |
| | ADC2 | Analog | ADC Input 2.<br>- Enable analog function with GPIO_PBCFGH[15:12]. |
| | IRQC1 | I | Default external interrupt source C. |
| | TIM1_CH2 | O | Timer 1 channel 2 output.<br>- Enable timer output in TIM1_CCER.<br>- Select alternate output function with GPIO_PBCFGH[15:12]. |
| | | I | Timer 1 channel 2 input.(Cannot be remapped). |
| 32 | PB6 | I/O High current | Digital I/O. |
| | ADC1 | Analog | ADC Input 1.<br>- Enable analog function with GPIO_PBCFGH[11:8]. |
| | IRQB | I | External interrupt source B. |
| | TIM1_CH1 | O | Timer 1 channel 1 output.<br>- Enable timer output in TIM1_CCER.<br>- Select alternate output function with GPIO_PBCFGH[11:8]. |
| | | I | Timer 1 channel 1 input. (Cannot be remapped). |
| 33 | PB5 | I/O | Digital I/O. |
| | ADC0 | Analog | ADC Input 0.<br>- Enable analog function with GPIO_PBCFGH[7:4]. |
| | TIM2CLK | I | Timer 2 external clock input. |
| | TIM1MSK | I | Timer 2 external clock mask input. |
| 34 | GND | Power | Ground supply pad. |
| 35 | GNDRF | RF Ground | Ground pad for RF port. |
| 36 | RF | Analog | RF port with 50 Ohm impedance. |

*Table 17: Pad description (Continued)*

| Pad | Signal | Direction | Description |
|---|---|---|---|
| 37 | GNDRF | RF Ground | Ground pad for RF port. |

## 7.3 Package Mechanical Dimensions

Module dimensions are 25 mm x 19 mm x 2 mm. Figures 8 and 9 below shows a detailed drawing of the package dimensions.

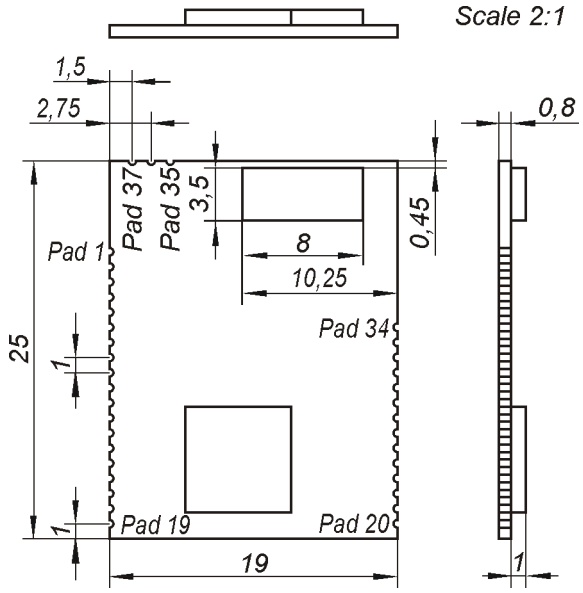



*Figure 8: Standard module dimensions without metal shielding*

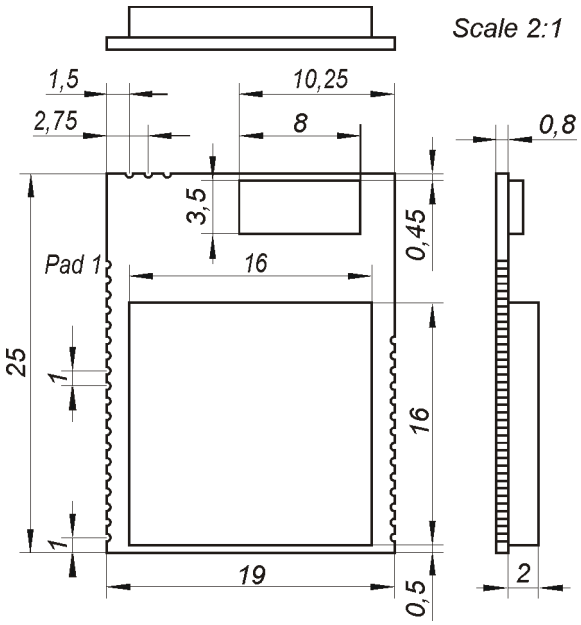



*Figure 9: Dimensions with metal shielding (Enhanced EMI protection)*

# 8 Soldering

## 8.1 Solder Temperature Profile

Figure 10 below shows the solder temperature profile for the DZ-ZB RF Module. This temperature profile is similar for other RoHS compliant packages, but manufacturing lines should be programmed with this profile in order to guarantee proper solder connection to the PCB.

**Note:** The module can be soldered only once.

### 8.2.1 Reflow Profile

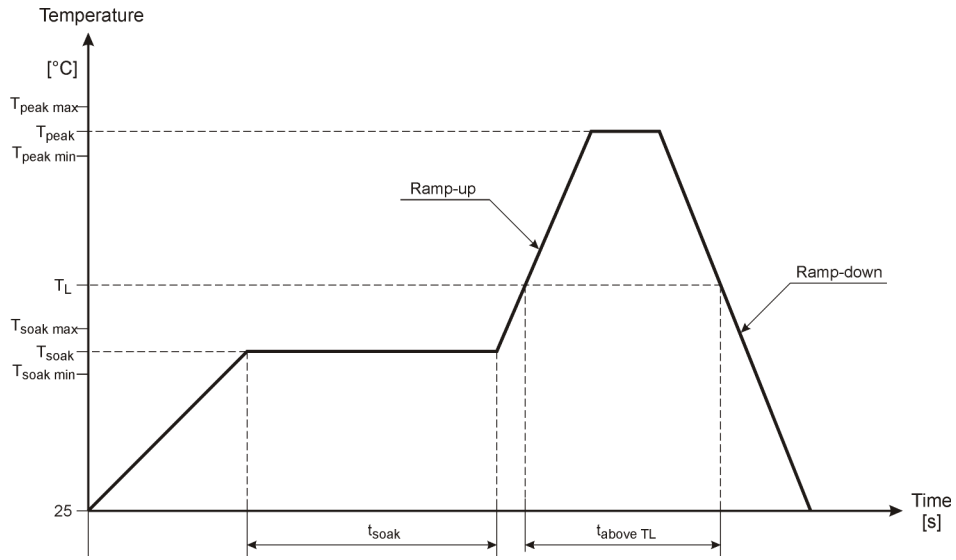



*Figure 10: Reflow profile*

## 8.3 Profile Parameters

Table 18 below describes the temperature profile parameters.

**Warning:** The module should be processed according to recommended temperature profile only once.

*Table 18: Solder Reflow Parameters*

| Parameter | Value |
|---|---|
| Average Ramp Up Rate (from $Tsoak_{max}$ to Tpeak) | 3℃ per second max |
| Average Ramp Up Rate (from 25℃ to $Tsoak_{min}$) | 2℃ to 4℃ per second max |
| Minimum Soak Temperature ($Tsoak_{mjn}$) | 150℃ |
| Maximum Soak Temperature ($Tsoak_{max}$) | 200℃ |
| TL | 220℃ |
| Time above TL | 30 to 60 seconds |
| Minimum Peak Temperature $Tpeak_{min}$ | 230℃ |
| Maximum Peak Temperature $Tpeak_{max}$ | 250℃ |

*Table 18: Solder Reflow Parameters*

| Parameter | Value |
|---|---|
| Ramp Down Rate | 6℃ per second max |

## 8.4 Recommended Footprint

Figure 11 below shows the recommended footprint for the module.

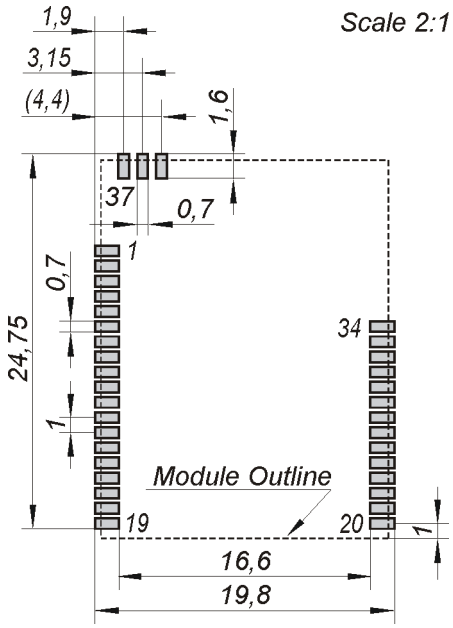



*Figure 11: Recommended footprint for modules (top view)*

With modules configured with output option “A”, that is, with the embedded SMD antenna, the presence of any conductive materials in proximity of the module’s antenna must be prevented. This requirement is valid also for copper traces, ground planes, wires, and connectors.

Figure 12 below shows the recommended “Copper-Keep-Out” area where the presence of any copper (and any conductive material as well) should be avoided.

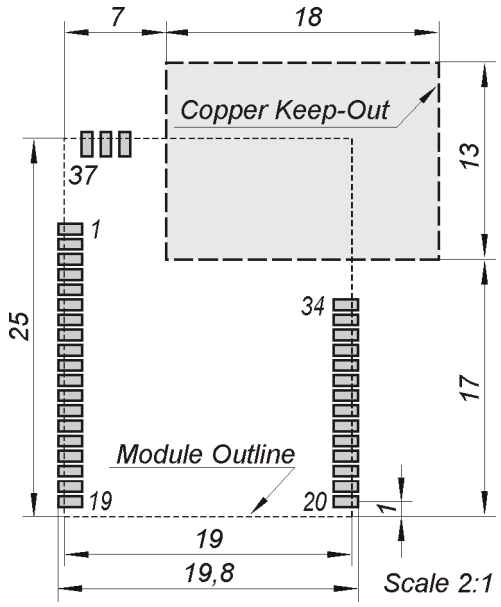



*Figure 12: Recommended "Copper-Keep-Out" Area (top view) – only for modules with Output Option "A"*

# 9 Ordering Information

When ordering DZ-ZB modules, the following code is used:

**DZ_ZB_ [P] [O] [S] [E]**

where:

**DZ** ..... **Manufactured by DiZiC**

**ZB** ..... **ZigBee Module**

**[P]** ..... **Power Level Options**

- S ..... Standard + 7dBm
- R ..... Front End with RF Output Power Level Detector + 20 dBm
- T ..... Front End + 20 dBm

**[O]** ..... **Output options:**

- A ..... Embedded SMD Antenna assembled on module
- P ..... Single ended 50 Ohm RF Pad
- U ..... 50 Ohm U.FL coaxial connector

**[S]** ..... **Stack options**

- F ..... RF4CE stack
- X ..... Proprietary stack
- Z ..... EmberZNet PRO stack

**[E]** ..... **Electromagnetic Interference (EMI) protection options:**

- S ..... Standard, without protective metal shielding
- M ..... Metal Shield, for enhanced EMI protection

# 10 Acronyms

This chapter defines a collection of terms that are commonly used when talking about networks in general or ZigBee in particular.

AC ..... Alternating Current
ACK ..... Acknowledge
ADC ..... Analogue-to-Digital Converter
API ..... Application Programming Interface
ARM ..... Advanced RISC Machines Ltd, now ARM Holdings
BiCMOS ..... Bipolar junction transistors combined with CMOS technology
BER ..... Bit Error Rate
CMOS ..... Complementary Metal–Oxide–Semiconductor
CPU ..... Central Processing Unit
CTS ..... Clear To Send
dB ..... decibel, logarithmic unit of measurement that expresses the magnitude of a physical quantity
dBm ..... Power ratio in decibels of the measured power referenced to one milliwatt (1 mW)
DC ..... Direct Current
DWT ..... Data Watch-point and Trace
EEPROM ..... Electrically Erasable Programmable Read-Only Memory
EMI ..... Electromagnetic Interference
ESD ..... Electrostatic Discharge
FE ..... Front End
FPB ..... Flash Patch and Breakpoint
GPIO ..... General Purpose Input/Output
HAL ..... Hardware Abstraction Layer
HBM ..... Human Body Model
HF ..... High Frequency
HVAC ..... Heating, Ventilating and Air Conditioning
I²C ..... Inter-Integrated Circuit bus
IEEE ..... Institute of Electrical and Electronics Engineers
IRQ ..... Interrupt Request
ISM ..... Industrial, Scientific and Medical radio band
ITM ..... Instrumentation Trace Macrocell
JTAG ..... Joint Test Action Group, digital interface for debugging of embedded device
LNA ..... Low Noise Amplifier
MAC ..... Media Access Control layer
MCU ..... Microcontroller Unit
MPU ..... Multi-core Processing Unit
PA ..... Power Amplifier

PC ..... Printed Circuit Board
PER ..... Package Error Ratio
PSD ..... Power Spectral Density
PTI ..... Packet Trace Interface
RAM ..... Random Access Memory
RF ..... Radio Frequency
RF4CE ..... Radio Frequency for Consumer Electronics consortium
RSSI ..... Received Signal Strength Indicator
RX ..... Receiver
SMD ..... Surface Mounted Device
SPI ..... Serial Peripheral Interface
STM ..... STMicroelectronics, an Italian-French electronics and semiconductor manufacturer
TWI ..... Two Wire Interface, a variant of I²C
TX ..... Transmitter
UART ..... Universal Asynchronous Receiver/Transmitter
U.FL ..... Miniature coaxial RF connector (up to 6 GHz) manufactured by Hirose Electric Group in Japan
VCO ..... Voltage Controlled Oscillator
ZigBee, ZigBee PRO ..... Wireless networking standards targeted at low-power applications
802.15.4 ..... The IEEE 802.15.4-2003 standard applicable to low-rate wireless Personal Area Network

# 11 References

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# DOCUMENT INFORMATION

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