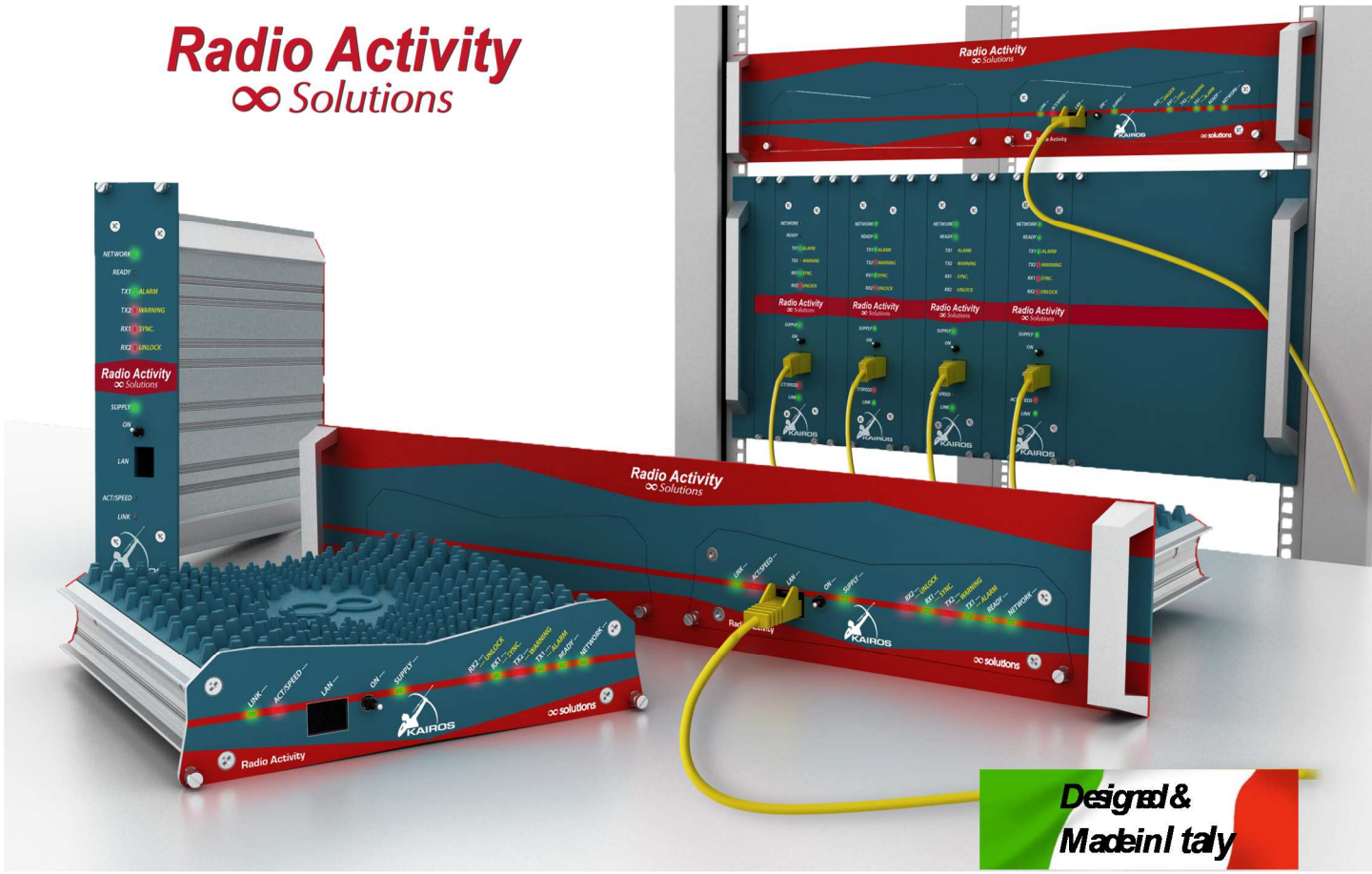

KAIROS KA-500 circuit description

Version 1.0

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Summary

KAIROS – KA-500 circuit description

1.1 CIRCUIT DESCRIPTION

1.1.1 Overview

The KA-500 is a UHF multi-protocol transceiver designed to operate in the frequency range of 450 to 527MHz.

1.1.2 Frequency Configuration

The receiver system is composed by two separate receivers matched to obtain a soft space diversity reception. Main and diversity receiver channels are completely independent and coherent (sharing the same local oscillators). This receiver uses a double conversion heterodyne system, with 45 MHz first IF and 1.5MHz digital conversion to base-band.

The transmit signal frequency is generated by the VCO / PLL and modulated by the signal from the DSP. It is then amplified and fed to the antenna.

The frequency selection is performed via the channel table, which can be edited in order to fix TX and RX frequency pair, with a step of 50Hz, in the tuning range of the equipment (450-527MHz). channel change can be performed in programming mode only, by remote connection, via dedicated SW.

Please be aware that the working frequency selection must be done in accordance with local Government permission rules.

1.1.3 Receiver System

1.1.3.1 Front-end circuit

The front-end circuit consist of former BPF, former LPF, RF Low Noise Amplifier (U30 and U14), and latter BPF. The BPF covers frequency range 450 to 527MHz.

The former BPF, former LPF, and latter BPF attenuate the unwanted signals and send only the necessary signal to the first mixer (MX1 and MX2).

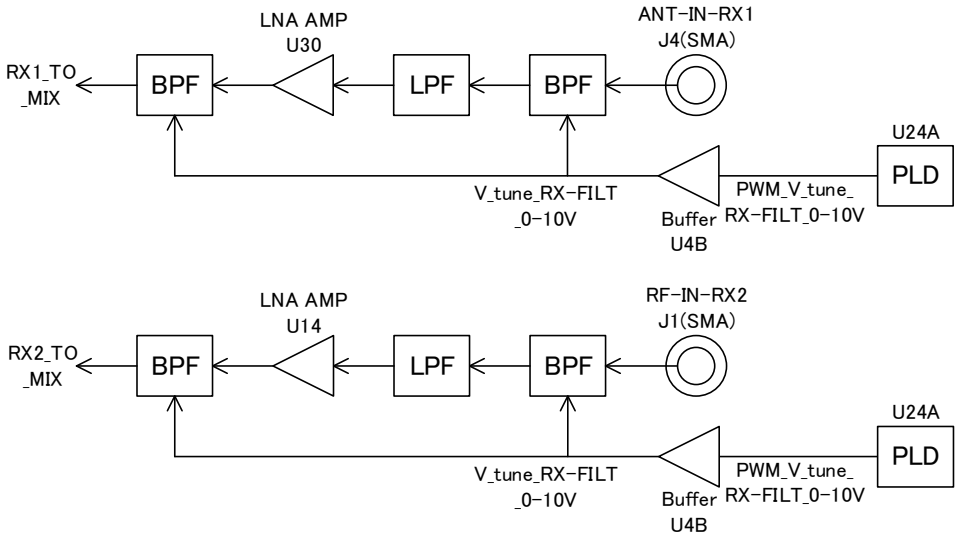


Fig1. Front-end circuit

1.1.3.2 First Mixer circuit

The filtered signal from the front-end circuit is heterodyned with the first local oscillator signal from the PLL frequency synthesizer circuit at the first mixer (MX1 and MX2) to become a 45 MHz first intermediate frequency (IF) signal.

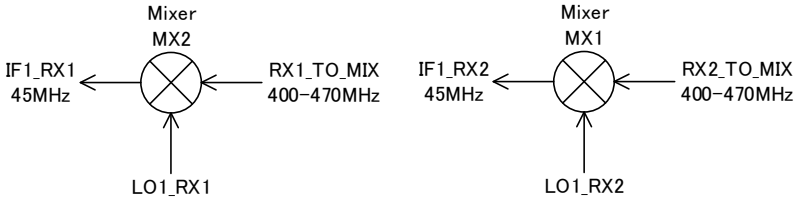


Fig. 2 1st-Mixer circuit

1.1.3.3 IF circuit

The first IF signal is amplified by the IF Post amplifier (U27 and U11) and passed through a monolithic crystal filter (Y5 and Y2) to reject adjacent channel signal. The filtered first IF signal is amplified by the IF amplifier (U28, U15, Q37, and Q27).

The IF signal is then fed into a Digitizing Subsystem IC (U26 and U16), that digitizes with a signal bandwidth ranging from 6.8kHz to 270kHz. This IC is consisted of a low noise amplifier, a mixer, a band-pass sigma-delta analog-to digital converter, and a decimation filter with programmable decimation factor. The signals from the receivers are sent in digital vector format to the DSP. These vectors represent the electromagnetic field vectors, as received from antennas, before any demodulation. By this way the DSP can sum, with the appropriate phases, the received signals to obtain a “soft diversity” reception. This corresponds to an electronic antennas alignment in order to receive the maximum available information along the incoming signal detection.

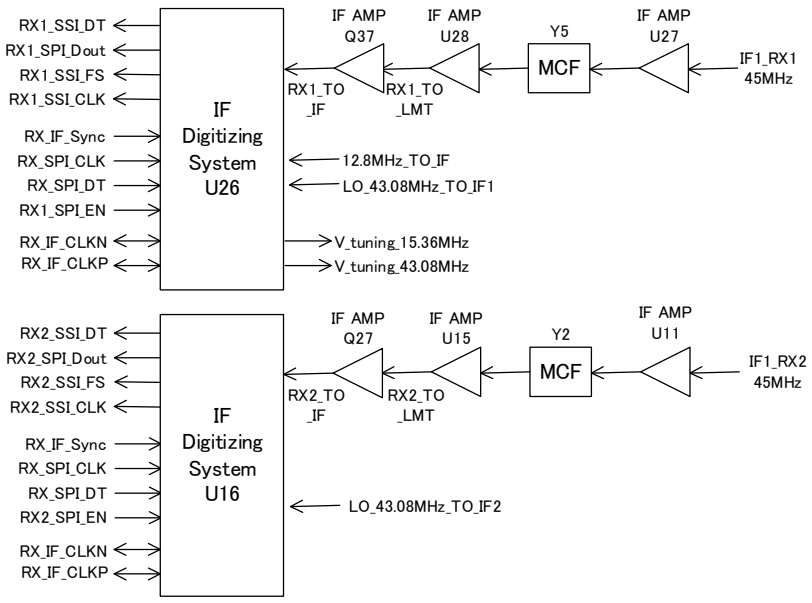


Fig. 3 IF Circuit

1.1.4 Transmit System

1.1.4.1 Drive and Final amplifier

The signal from TX VCO circuit is amplified by pre-drive amplifier (U37). The output of the pre-drive amplifier (U37) is amplified by the drive amplifier (Q57: MOS FET) and final amplifier (Q58: LDMOS) to 25W. The power amplifier works in C class and ensures a very high efficiency, lowering the needed power from supply system and lowering the thermal dissipation.

The output of the final amplifier (Q58) is the passed through the harmonic filter (LPF), the CM coupler circuit, and filter circuit to lower spurious emissions under required levels by existing regulations.

An internal TX/ RX switch can be enabled for simplex/ half duplex applications. This switch must be requested directly in phase of order of the equipment, due to isolation reasons, it I s not enable this function via SW.

1.1.4.2 CM coupler circuit

The CM coupler circuit is a line for detecting forward wave and reflected wave. Forward wave is detected and is converted into DC voltage by the detector IC (U39 and U42). If an abnormal antenna load is connected, reflected wave is detected and converted into DC voltage by the detector IC (U39 and U42).

1.1.4.3 APC circuit

The APC circuit always monitors the current flowing through drive amplifier(Q57) and final amplifier (Q58).

The power control circuit (Q55, Q56, and U40) acts in a closed loop and keeps constant the total power at MOSFET drain.

1.1.4.4 High temperature detector circuit

To prevent thermal destruction of drive amplifier (Q57) and final amplifier (Q58), this circuit reduces the APC control voltage when the temperature of drive amplifier (Q57) and final amplifier (Q58) rises.

A thermal sensor is hosted in the near proximity of the final MOS (Q58) stage for temperature monitoring. If the reflected power or the MOSFET (Q58) temperature exceeds protection threshold, regulation circuit will lower output power up to safe levels for transmitter.

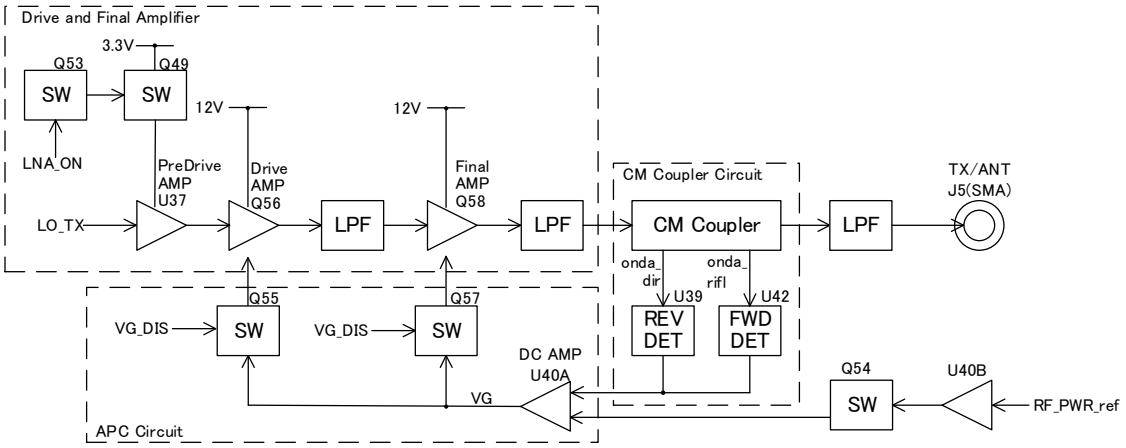


Fig. 4 Transmit system

1.1.5 PLL System

1.1.5.1 Receiver PLL circuit

The receiver PLL circuit consists of VCO (DV6, DV8, Q33 and Q34) and the PLL(U23).

1.1.5.1.1 RX VCO

RX VCO generates a first local signal. For the VCO oscillation frequency, the first local signal is 181MHz to 219MHz. The VCO oscillation frequency is determined by two systems of voltage control terminals “RX_Lo1_V_tune_fine_0-5V” and “RX_LO1_V_tune_coarse_0-10V”.

The voltage control terminals, “RX_Lo1_V_tune_fine_0-5V” is controlled by the PLL IC(U23).

The voltage control terminals, “RX_LO1_V_tune_coarse_0-10V” is controlled by the PLD(U24A) through DAC(U3A) circuit. The output frequency changes continuously according to the applied voltage.

The first local circuit consists of the VCO, the buffer amplifier(Q31), the RF amplifier(U22), the PLL IC(U23) and the active loop filters.

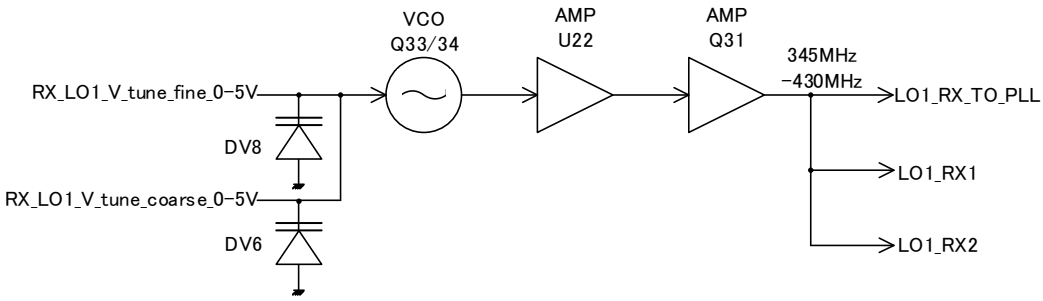
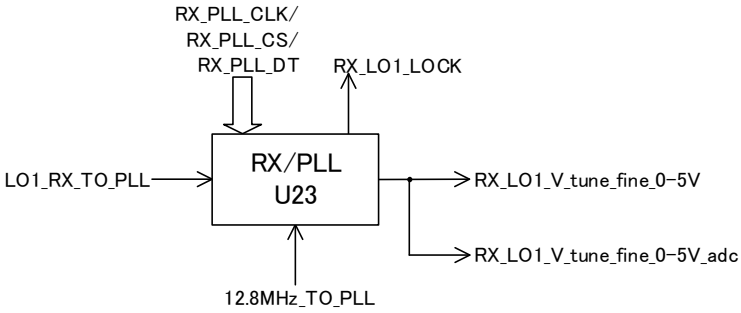


Fig. 5 RX VCO circuit

1.1.5.1.2 PLL IC

PLL IC (U23) compares the differences in phase of the VCO oscillation frequency (LO1_RX_TO

_PLL) and the reference frequency (12.8MHz_TO_PLL), returns the difference to the VCO "RX_Lo1_V_tune_fine_0-5V" terminal and realizes the "Phase Locked Loop" for the return control. This allows the VCO oscillation frequency to accurately match (lock) the desired



frequency.

Fig. 6 RX PLL circuit

1.1.5.2 Transmitter PLL circuit

The transmitter PLL circuit consists of the VCO (DV16, DV17, DV18, DV19, Q47 and Q49) and the PLL (U34). They produce the transmitter frequency signal.

1.1.5.2.1 TX VCO

TX VCO produces transmitter frequencies from 450MHz to 527MHz. The VCO oscillation frequencies is determined by two systems of voltage control terminals.

The voltage control terminals, "TX_LO_V_tune_fine_0-5V" and "TX_LO_V_tune_coarse_0-10V", are controlled by the PLL IC(U34) and MCU. The output frequency changes continuously according to applied voltage. For the modulation input terminal, "", the output frequency changes according to the applied voltage.

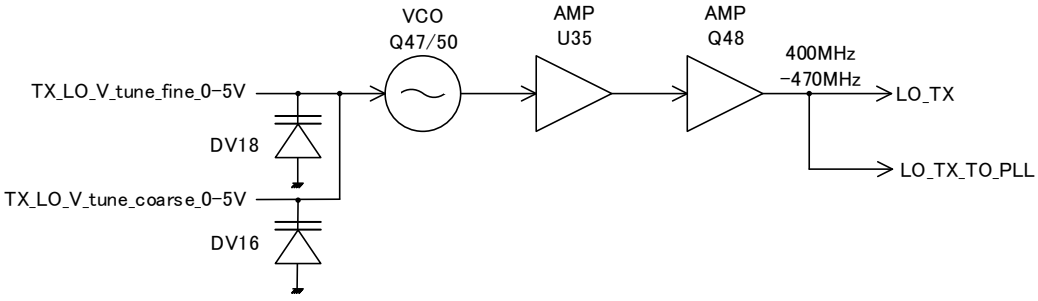


Fig. 7 TX VCO circuit

1.1.5.2.2 PLL IC

The PLL IC (U34) compares the differences in phases of the VCO oscillation frequency and the transmitter PLL reference signal (12.8MHz), returns the difference to the VCO “TX_LO_V_tune_

fine_0-5V” terminal and realizes the “Phase Locked Loop” for the return control. This allows the VCO oscillation frequency to accurately match (lock) the desired frequency.

The desired frequency is set for the PLL IC by the MCU through the 3-line serial bus. Whether the PLL IC is locked or not is monitored by the MCU through the “” signal line.

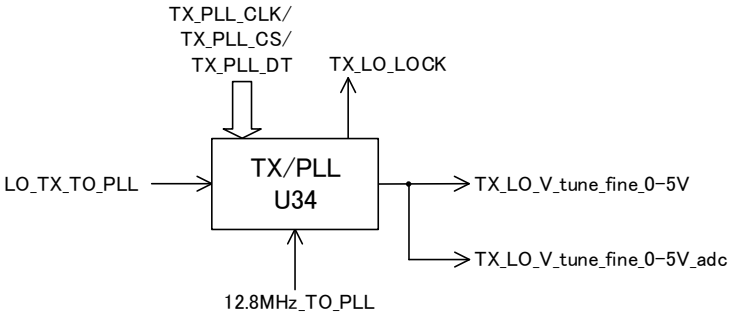


Fig. 8 TX PLL circuit

1.1.6 Control System

1.1.6.1 MCU circuit

The LINUX operative system is based on a powerful risk processor with 128M RAM and a 64M Flash disk. It manages an autosensing LAN ethernet 10/100 interface, supporting the Precision Time Protocol over IP (standard 1588v2).

The risk processor is equipped with 4 serial ports to manage GPS, AMBE Codec, external hosts and auxiliary devices; it is equipped also with a Real Time Clock with tampon battery.

1.1.6.2 DSP circuit

The core of system is this unit which via software performs every function of signal processing into radio station.

The DSP(U20) is a low power / high performances fixed point 80MIPS device, that can process contemporary up to 2 analog duplex signals ensuring 70dB of SNR, 2 digital receivers and 1 digital modulator.

Communication and control functions of the unit are ensured to the Risk processor (U32) which manages communications with external world and with other equipment modules. The DSP program is downloaded directly from the Risk at every start.

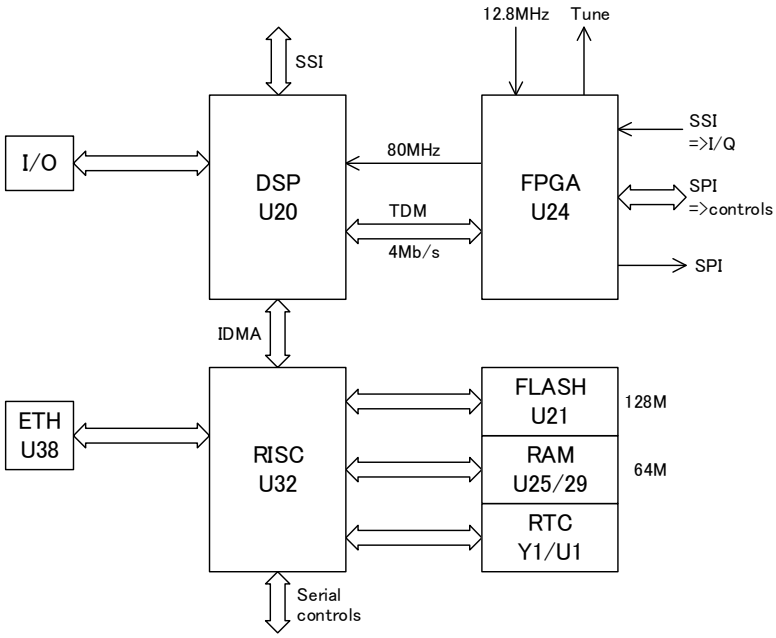


Fig. 9 Control System

1.1.7 Power supply circuit

The equipment is powered to Main connector (P7) by nominal 13.2V DC from battery with negative shorted to ground and with a maximum current absorption of 5A.

The on/off switch (Q21, Q22, Q23 and U8) is managed by the FPGA device (U24C) that surveys the power supply events. The FPGA memorize the last state and automatically powers on/off KAIROS according with the last state.

An I/O placed in the back of the equipment allows to switch off KAIROS from an external push-button.

The Power Supply subsystem protects the equipment from:

- Polarity inversion
- Over voltage: the equipment switches off when the power supply exceeds 15.6V. This may be useful in solar panel powered applications or in mobile applications.
- Under Voltage: equipment switches off when the power supply drops 10.8V. This saves an external lead acid battery that could be damaged from an excessive discarding.
- Current limiting: an internal short circuit does not destroy the equipment of fuse the power supply cable.
- Transient voltage: a double protection, one fast and resettable combined with another one relatively slow but able to absorb more energy, automatically stops transient in the power supply.
- Soft start/inrush current: when the equipment is connected to the power supply, this circuit limit the maximum current during the charging of the internal capacitors.

The Power Supply subsystem gives the following secondary voltages:

- 13.6V unregulated for the RF power amplifier
- 13.6V limited at 400mA for a general purpose external device
- 10V linear regulated for the Voltage Controlled Oscillators of RX and TX
- 5V switching regulated for low noise amplifier, PLL and some logics
- 3.3V switching regulated for DSP, FPGA, Risk processor, IF, Ethernet device and other logics
- 1.8V switching regulated for DSP and Risk processor

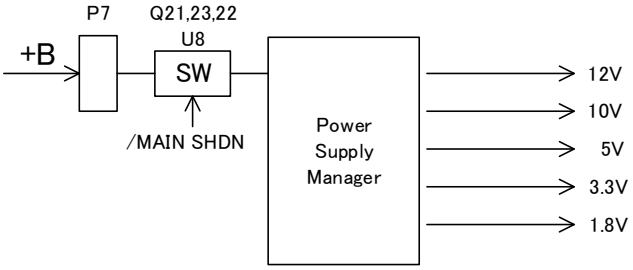


Fig. 10 Power Supply circuit