

FN990 Family

Hardware Design Guide

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1 APPLICABILITY TABLE

Table 1: Applicability Table

Products	HARDWARE VERSIONS	DESCRIPTIONS
FN990A40-HP	1.00	3G / 4G (20 Layer) / Sub-6 (BW: 200MHz), PC1.5 n41, n77, n78, n79 cellular module

Note: The applied MCP varies depending on the HW version.

- HW1.00 : MCP 4G+4G
- HW1.10 : MCP 8G+8G

2 INTRODUCTION

2.1 Scope

This document introduces the Dejero Labs Inc FN990 Family module and presents possible and recommended hardware solutions for the development of a product based on this module. All the features and solutions described in this document apply to all FN990 Family variants listed in the applicability table.

This document cannot include every hardware solution or every product that can be designed. Where the suggested hardware configurations are not to be considered mandatory, the information provided should be used as a guide and starting point for the proper development of the product with the Dejero Labs Inc FN990 Family module.

2.2 Audience

This document is intended for Dejero Labs Inc customers, especially system integrators, about to implement their applications using the Dejero Labs Inc FN990 Family module.

2.3 Contact Information, Support

For technical support and general questions, e-mail:

- info@Dejero.com

2.4 Conventions

Note: Provide advice and suggestions that may be useful when integrating the module.

Danger: This information MUST be followed, or catastrophic equipment failure or personal injury may occur.

ESD Risk: Notifies the user to take proper grounding precautions before handling the product.

Warning: Alerts the user on important steps about the module integration.

All dates are in ISO 8601 format, that is YYYY-MM-DD.

2.5 Terms and Conditions

Refer to <https://www.Dejero.com>.

2.6 Disclaimer

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3 GENERAL PRODUCT DESCRIPTION

3.1 Overview

The aim of this document is to present the possible and recommended hardware solutions useful for developing a product with the Dejero Labs Inc FN990 Family M.2 module.

FN990 Family is Telit's platform for the M.2 module for applications, such as M2M applications and industrial IoT device platforms, based on the following technologies:

- 5G sub-6 / 4G / 3G networks for data communication
- Designed for industrial-grade quality

Front-end for mobile products, offering mobile communication features to an external host CPU through its rich interfaces.

FN990 Family is available in hardware variants as listed in the APPLICABILITY TABLE.

The designated RF band set for each variant is detailed in Section Frequency Bands and CA / EN-DC Combinations

3.2 Frequency Bands and CA / EN-DC Combinations

Frequency Bands

Operating frequencies in 5G, LTE, and WCDMA modes conform to 3GPP specifications.

The table below lists the FN990 operating frequencies on 5G, LTE, and WCDMA modes.

5G NR Sub-6 Bands Supportive

Table 2: 5G NR Sub-6 Bands supportive

NR BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels	SCS (kHz)
n1 - 2100	FDD	1920 - 1980	2110 - 2170	Tx: 384000 - 396000 Rx: 422000 - 434000	15
n2 - 1900 PCS	FDD	1850 - 1910	1930 - 1990	Tx: 370000 - 382000 Rx: 386000 - 398000	15
n3 - 1800	FDD	1710 - 1785	1805 - 1880	Tx: 342000 - 357000 Rx: 361000 - 376000	15
n5 - 850	FDD	824 - 849	869 - 894	Tx: 164800 - 169800 Rx: 173800 - 178800	15
n7 - 2600	FDD	2500 - 2570	2620 - 2690	Tx: 500000 - 514000 Rx: 524000 - 538000	15
n8 - 900	FDD	880 - 915	925 - 960	Tx: 176000 - 183000 Rx: 185000 - 192000	15
n12 - 700 a	FDD	699 - 716	729 - 746	Tx: 139800 - 143200 Rx: 145800 - 149200	15
n13 - 700 c	FDD	777 - 787	746 - 756	Tx: 155400 - 157400 Rx: 149200 - 151200	15

NR BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels	SCS (kHz)
n14 - 700 PS	FDD	788 - 798	758 - 768	Tx: 157600 - 159600 Rx: 151600 - 153600	15
n18 - 800 Lower	FDD	815 - 830	860 - 875	Tx: 163000 - 166000 Rx: 172000 - 175000	15
n20 - 800	FDD	832 - 862	791 - 821	Tx: 166400 - 172400 Rx: 158200 - 164200	15
n25 - 1900+	FDD	1850 - 1915	1930 - 1995	Tx: 370000 - 383000 Rx: 386000 - 399000	15
n26 - 850+	FDD	814 - 849	859 - 894	Tx: 162800 - 169800 Rx: 171800 - 178800	15
n28 - 700 APT	FDD	703 - 748	758 - 803	Tx: 140600 - 149600 Rx: 151600 - 160600	15
n29 - 700d	SDL	-	717 - 728	Rx: 143400 - 145600	15
n30 - WCS	FDD	2305 - 2315	2350 - 2360	Tx: 461000 - 463000 Rx: 470000 - 472000	15
n38 - 2600	TDD	2570 - 2620		T/Rx: 514000 - 524000	30
n40 - 2300	TDD	2300 - 2400		T/Rx: 460000 - 480000	30
n41 - 2600+	TDD	2496 - 2690		T/Rx: 499200 - 537996	30
n48 - 3600	TDD	3550 - 3700		T/Rx: 636668 - 646666	30
n66 - AWS-3	FDD	1710 - 1780	2110 - 2200	Tx: 342000 - 356000 Rx: 422000 - 440000	15
n71 - 600	FDD	663 - 698	617 - 652	Tx: 132600 - 139600 Rx: 123400 - 130400	15
n75 - 1500+	SDL	-	1432 - 1517	Rx: 286400 - 303400	-
n76 - 1500-	SDL	-	1427 - 1432	Rx: 285400 - 286400	-
n77 - 3700	TDD	3300 - 4200		T/Rx: 620000 - 680000	30
n78 - 3500	TDD	3300 - 3800		T/Rx: 620000 - 653332	30
n79 - 4700	TDD	4400 - 5000		T/Rx: 693334 - 733332	30

LTE Bands supportive

Table 3: LTE Bands supportive

E-UTRA BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels
B1 - 2100	FDD	1920 - 1980	2110 - 2170	Tx: 18000 - 18599 Rx: 0 - 599
B2 - 1900 PCS	FDD	1850 - 1910	1930 - 1990	Tx: 18600 - 19199 Rx: 600 - 1199
B3 - 1800+	FDD	1710 - 1785	1805 - 1880	Tx: 19200 - 19949 Rx: 1200 - 1949
B4 - AWS-1	FDD	1710 - 1755	2110 - 2155	Tx: 19950 - 20399 Rx: 1950 - 2399
B5 - 850	FDD	824 - 849	869 - 894	Tx: 20400 - 20649 Rx: 2400 - 2649
B7 - 2600	FDD	2500 - 2570	2620 - 2690	Tx: 20750 - 21449 Rx: 2750 - 3449
B8 - 900 GSM	FDD	880 - 915	925 - 960	Tx: 21450 - 21799 Rx: 3450 - 3799
B12 - 700 a	FDD	699 - 716	729 - 746	Tx: 23010 - 23179 Rx: 5010 - 5179
B13 - 700 c	FDD	777 - 787	746 - 756	Tx: 23180 - 23279 Rx: 5180 - 5279
B14 - 700 PS	FDD	788 - 798	758 - 768	Tx: 23280 - 23379 Rx: 5280 - 5379
B17 - 700 b	FDD	704 - 716	734 - 746	Tx: 23730 - 23849 Rx: 5730 - 5849
B18 - 800 Lower	FDD	815 - 830	860 - 875	Tx: 23850 - 23999 Rx: 5850 - 5999
B19 - 800 Upper	FDD	830 - 845	875 - 890	Tx: 24000 - 24149 Rx: 6000 - 6149
B20 - 800 DD	FDD	832 - 862	791 - 821	Tx: 24150 - 24449 Rx: 6150 - 6449
B25 - 1900+	FDD	1850 - 1915	1930 - 1995	Tx: 26040 - 26689 Rx: 8040 - 8689
B26 - 850+	FDD	814 - 849	859 - 894	Tx: 26690 - 27039 Rx: 8690 - 9039
B28 - 700 APT	FDD	703 - 748	758 - 803	Tx: 27210 - 27659 Rx: 9210 - 9659
B29 - 700 d	SDL	-	717 - 728	Rx: 9660 - 9769
B30 - 2300 WCS	FDD	2305 - 2315	2350 - 2360	Tx: 27660 - 27759 Rx: 9770 - 9869

E-UTRA BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels
B32 - 1500 L	SDL	-	1452 - 1496	Rx: 9920 - 10359
B34 - 2000	TDD	2010 - 2025		
B38 - 2600	TDD	2570 - 2620		
B39 - 1900+	TDD	1880 - 1920		
B40 - 2300	TDD	2300 - 2400		
B41 - 2600+	TDD	2496 - 2690		
B42 - 3500	TDD	3400 - 3600		
B43 - 3700	TDD	3600 - 3800		
B46 - 5200	SDL	5150 - 5925		
B48 - 3600	TDD	3550 - 3700		
B66 - AWS-3	FDD	1710 - 1780	2110 - 2200	Tx: 131972 - 132671 Rx: 66436 - 67335
B71 - 600	FDD	663 - 698	617 - 652	Tx: 133122 - 133471 Rx: 68586 - 68935

WCDMA Bands supportive

Table 4: WCDMA Bands supportive

UTRA BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels
B1 - 2100	FDD	1920 - 1980	2110 - 2170	Tx: 9612 - 9888 Rx: 10562 - 10838
B2 - 1900 PCS	FDD	1850 - 1910	1930 - 1990	Tx: 9262 - 9538 Rx: 9662 - 9938
B4 - AWS-1	FDD	1710 - 1755	2110 - 2155	Tx: 1312 - 1513 Rx: 1537 - 1738
B5 - 850	FDD	824 - 849	869 - 894	Tx: 4132 - 4233 Rx: 4357 - 4458
B6 - 850 Japan	FDD	830 - 840	875 - 885	Tx: 4162 - 4188 Rx: 4387 - 4413
B8 - 900 GSM	FDD	880 - 915	925 - 960	Tx: 2712 - 2863 Rx: 2937 - 3088
B19 - 800 Japan	FDD	830 - 845	875 - 890	Tx: 312 - 363 Rx: 712 - 763

CA / MIMO / EN-DC

The FN990 Family supports 2CA, 3CA, 4CA, 5CA, 6CA, and 7CA for LTE CA combinations and EN-DC for NR FR1 configuration.

Note: Please refer to the FN990 Family CA / EN-DC list, for a detailed list of CA and EN-DC combinations.

3.3 Target Market

The FN990 Family can be used for telematics applications where tamper-resistance, confidentiality, integrity, and authenticity of end-user information are required, for example:

- Industrial equipment
- Home network
- Internet connectivity

3.4 Main Features

The FN990 Family of industrial-grade cellular modules features 5G Sub-6, LTE, and multi-RAT modules together with an on-chip powerful application processor and a rich set of interfaces.

The main functions and features are listed below:

Table 5: Main Features

Function	Features
Physical	M.2 Type 3052-S3-B
Cellular technology	FN990A40 5G: FR1(Sub 6G), Rel 16 NSA up to: 4.1Gbps on DL, 0.55Gbps on UL SA up to: 4.1Gbps on DL, 0.9Gbps on UL 4G: CAT. 20 (2Gbps) on DL, CAT. 18 (211Mbps) on UL, Rel 16 3G: HSPA+ Rel9 up to 42/5.7Mbps in DL/UL
Supported Bands	5G: n1/n2/n3/n5/n7/n8/n12/n13/n14/n18/n20/n25/n26/n28/n29(SDL)/n30/n38/n40/n41/n48/n66/n71/n75(SDL)/n76(SDL)/n77/n78/n79 4G: B1/B2(B25)/B3/B4(B66)/B26(B5,B18,B19)/B7/B8/B12(B17)/B13/B14/B20/B28/B29(SDL)/B30/ B32(SDL)/B34/B38/B39/B40/B41/B42/B43/B46(SDL)/B48/B71 3G: B1/B2/B4/B5(B6,B19)/B8
1Tx / 4Rx (4x4 DL MIMO)	5G: n1/n2/n3/n7/n25/n30/n38/n40/n41/n48/n66/n75/n77/n78/n79 4G: B1/B2/B3/B4/B7/B25/B30/B32/B34/B38/B39/B40/B41/B42/B43/B48/B66

Function	Features
2Tx (2x2 UL MIMO) / 4Rx (4x4 DL MIMO)	5G: n38/n41/n48/n77/n78/n79
1Tx / 1Rx (2 nd Rx Diversity)	4G: all operating bands 3G: all operating bands
GNSS	Upper L-band: GPS/Glonass/Beidou/Galileo
USIM port – Dual Voltage	Two SIM support (UIM2 can be assigned as optional eSIM) Class B and Class C support
Application processor	Application processor to run customer application code 32-bit ARM s-A7 up to 1.8 GHz running the Linux operating system 4Gbit NAND Flash + 4Gbit LPDDR4 2133 MHz MCP is supported (HW1.00) 8Gbit NAND Flash + 8Gbit LPDDR4 2133 MHz MCP is supported (HW1.10)
Main Interfaces	PCIe Gen3 x 1-lane USB 3.1 Gen 2 Peripheral Ports – GPIOs
Antenna connection	4 x MHF-4 type Cellular/GNSS antenna connectors 1 x MHF-4 type Dedicated GNSS antenna connector
Form factor	M.2 Form factor (30 * 52 * 2.25 mm), accommodating the multiple RF bands
Environment and quality requirements	The device is designed and qualified by Dejero Labs Inc to satisfy environmental and quality requirements.
Single supply module	The module internally generates all its required internal supply voltages.
RTC	Real-time clock is supported.
Operating temperature	Range -40 degC to +85 degC (conditions as defined in Section 2.8.1, Temperature Range)
Operating Humidity	≤95%, non-condensing

Configurations Pins

The FN990 modems can be configured as USB 3.1 Gen 2 or PCIe devices. The primary host interface can be set using the four pins listed in the table below.

Table 6: Configurations Pins

Pin	Signal	State	Interface Type
21	CONFIG_0	GND	PCIe or USB 3.1 Gen 2 Port Configuration 2 (Applicable to WWAN only)
69	CONFIG_1	GND	
75	CONFIG_2	NC	
1	CONFIG_3	NC	

Note: On the host side, each of the CONFIG_0 to CONFIG_3 signals must be equipped with a pull-up resistor. Based on the state of the configuration pins on

the Add-in Card, being tied to GND or left No Connect (NC), the detected pins will create a 4-bit logic state that requires decoding.

Used by an Add-in Card where USB 3.1 Gen1 is present on the connector and PCIe is No Connect.

Only a single lane of PCIe is available in these configurations.

For more details, please refer to the PCI Express M.2 Specification document.

3.5 Block Diagram

The figure below shows an overview of the internal architecture of the FN990 Family module.

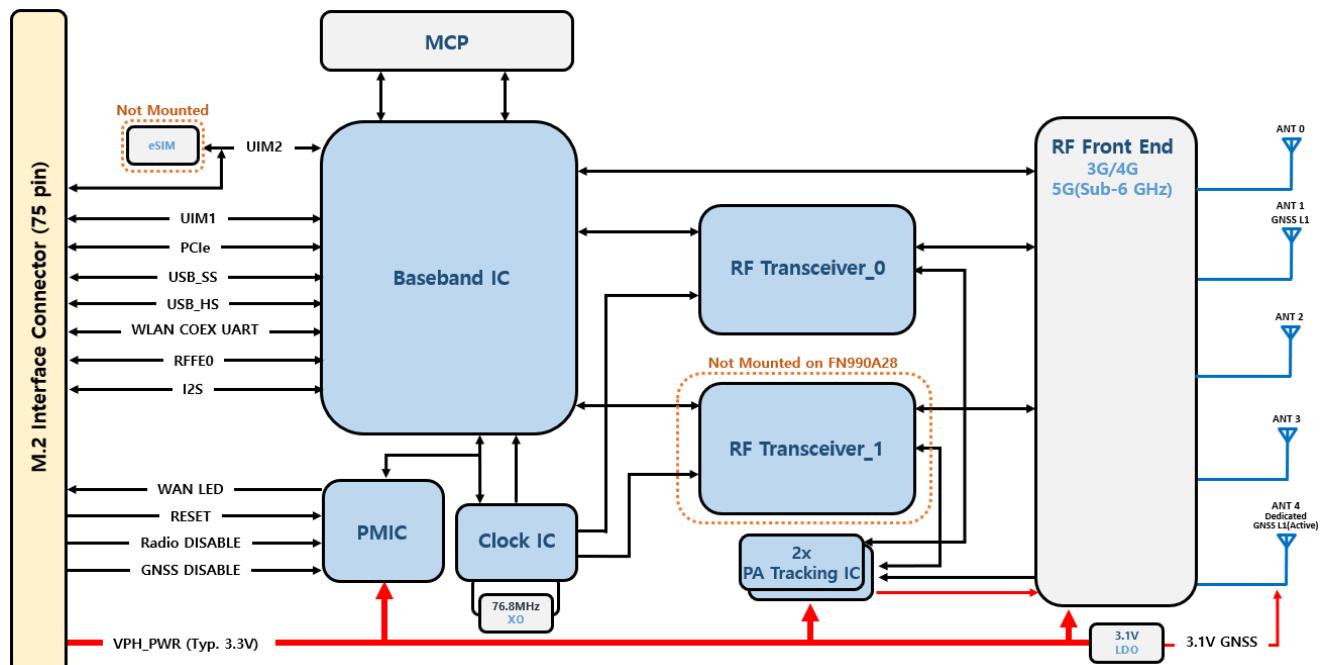


Figure 1: FN990 Family Block Diagram

3.6 RF Performance

The RF performance in 5G, LTE, and WCDMA modes conforms to the 3GPP specifications.

Conducted Transmit Output Power

TX power follows the measurement conditions and specifications defined in 3GPP.

Table 7: Conducted Transmit Output Power

Band	Power class	RF Power (dBm) Nominal*
5G NR Sub-6 n1, n2, n3, n5, n7, n8, n12, n13, n14, n18, n20, n25, n26, n28, n30, n38, n40, n41, n48**, n66, n71, n77, n78, n79	3 (0.2W)	23
5G NR Sub-6 n41, n77, n78, n79 Supports Power Class 2	2 (0.4W)	26

Band	Power class	RF Power (dBm) Nominal*
5G NR Sub-6 n41, n77, n78, n79 UL MIMO Supports Power Class 1.5***	1.5 (0.8W)	29
LTE All Bands B1, B2, B3, B4, B5, B7, B8, B12, B13, B14, B17, B18, B19, B20, B25, B26, B28, B30, B34, B38, B39, B40, B41, B42**, B43**, B48**, B66, B71	3 (0.2W)	23
LTE B41 Supports Power Class 2	2 (0.4W)	26
3G WCDMA B1, B2, B4, B5, B6, B8, B19	3 (0.2W)	23

* Max output power tolerance according to 3GPP TS 38.521-1, 3GPP TS 36.521-1 and 3GPP TS 34.121-1 or better

** These bands may show lower power due to country-type approvals constraints

*** one same NR band has two PC2 Tx paths and UL MIMO capability.

Conducted Receiver Sensitivity

The Sensitivity of the receiver follows the measurement conditions and specifications defined in 3GPP.

Table 8: 3GPP Compliance for Conducted Receiver Sensitivity

Technology	3GPP Compliance
5G NR Sub-6	Throughput >95%
4G LTE	Throughput >95%
3G WCDMA	BER <0.1% 12.2 Kbps

Table 9: Typical Conducted Receiver Sensitivity - NR Bands

NR Band	Typical Conducted Rx Sensitivity (dBm) *						
	SCS (kHz)	BW (MHz)	ANT0	ANT1	ANT2	ANT3	Combined
NR FDD n1	15	20	-95	-94	-96	-95	-100
NR FDD n2	15	20	-95	-94	-95	-95	-100
NR FDD n3	15	20	-94	-94	-96	-95	-100
NR FDD n5	15	20	-96	NA	-98	NA	-99
NR FDD n7	15	20	-93	-94	-94	-95	-99
NR FDD n8	15	20	-96	NA	-98	NA	-99
NR FDD n12	15	15	-98	NA	-98	NA	-100
NR FDD n13	15	10	-99	NA	-100	NA	-102
NR FDD n14	15	10	-99	NA	-100	NA	-102
NR FDD n18	15	15	-98	NA	-98	NA	-100

NR Band	Typical Conducted Rx Sensitivity (dBm) *						
NR FDD n20	15	20	-96	NA	-98	NA	-100
NR FDD n25	15	20	-94	-94	-95	-95	-100
NR FDD n26	15	20	-96	NA	-98	NA	-99
NR FDD n28	15	20	-96	NA	-98	NA	-100
NR FDD n29	15	10	-96	NA	-98	NA	-100
NR FDD n30	15	10	-96	-96	-98	-98	-102
NR TDD n38	30	20	-95	-94	-94	-94	-99
NR TDD n40	30	80	-88	-88	-88	-89	-93
NR TDD n41	30	100	-88	-86	-87	-87	-92
NR TDD n48	30	40	-91	-91	-93	-92	-97
NR FDD n66	15	20	-94	-94	-95	-97	-99
NR FDD n71	15	20	-97	NA	-98	NA	-100
NR SDL n75	30	30	-92	-93	-92	-92	-97
NR SDL n76	30	5	-94	-97	-97	97	-100
NR TDD n77	30	100	-88	-89	-87	-87	-93
NR TDD n78	30	100	-88	-88	-87	-87	-93
NR TDD n79	30	100	-85	-90	-89	-88	-93

*3.3 Voltage / Room temperature

Table 10: Typical Conducted Receiver Sensitivity - LTE Bands

E-UTRA Band	Typical Conducted Rx Sensitivity (dBm) *				
	ANT0	ANT1	ANT2	ANT3	Combined
LTE FDD B1	-97	-96.5	-96.5	-96.5	-103
LTE FDD B2	-97	-96	-96	-96	-103
LTE FDD B3	-97	-96	-96	-96	-103
LTE FDD B4	-97	-96	-96	-96	-103
LTE FDD B5	-99	NA	-99	NA	-102
LTE FDD B7	-97	-96	-96	-96	-103
LTE FDD B8	-99	NA	-99	NA	-102
LTE FDD B12	-99	NA	-99	NA	-102
LTE FDD B13	-99	NA	-99	NA	-102
LTE FDD B14	-99	NA	-99	NA	-102
LTE FDD B17	-99	NA	-99	NA	-102
LTE FDD B18	-99	NA	-99	NA	-102

E-UTRA Band	Typical Conducted Rx Sensitivity (dBm) *				
LTE FDD B19	-99	NA	-99	NA	-102
LTE FDD B20	-99	NA	-99	NA	-102
LTE FDD B25	-97	-96	-96	-96	-103
LTE FDD B26	-99	NA	-99	NA	-102
LTE FDD B28	-99	NA	-99	NA	-102
LTE SDL B29	-99	NA	-99	NA	-101
LTE FDD B30	-96	-95	-95	-95	-102
LTE SDL B32	-97	-97	-97	-97	-101
LTE TDD B34	-96.5	NA	-98	NA	-100
LTE TDD B38	-97	-96.5	-96.5	-96.5	-103
LTE TDD B39	-97	-97	-97	-97	-103
LTE TDD B40	-96.5	-96.5	-96.5	-96.5	-103
LTE TDD B41	-96	-96	-96	-96	-102
LTE TDD B42	-97	-96	-96	-96	-102
LTE TDD B43	-97	-96	-96	-96	-102
LTE SDL B46	-90	NA	-88.5	NA	-91
LTE TDD B48	-97	-96	-96	-96	-103
LTE FDD B66	-97	-96	-96	-96	-103
LTE FDD B71	-99	NA	-99	NA	-102

*3.3 Voltage / Room temperature

Table 11: Typical Conducted Receiver Sensitivity - WCDMA Bands

UTRA Band	Typical Conducted Rx Sensitivity (dBm) *				
	ANT0	ANT1	ANT2	ANT3	Combined
WCDMA FDD B1	-110	NA	-109	NA	NA
WCDMA FDD B2	-110	NA	-110	NA	NA
WCDMA FDD B4	-110	NA	-109	NA	NA
WCDMA FDD B5	-110	NA	-110	NA	NA
WCDMA FDD B6	-110	NA	-110	NA	NA
WCDMA FDD B8	-110	NA	-110	NA	NA
WCDMA FDD B19	-110	NA	-110	NA	NA

*3.3 Voltage / Room temperature

Note: The sensitivity level has a deviation of approximately +/- <2dB, device, and channel because the level shows a typical value.

The sensitivity level of the NR bands has a deviation of approximately +/- <3dB depending on the EN-DC combinations, but the combined sensitivity performance meets the 3GPP requirements.

LTE level is measured at BW 10 MHz except Band 46

B46 BW = 20 MHz

3.7 Mechanical Specifications

Dimensions

The overall dimensions of FN990 Family modems are:

- Length: 52 mm
- Width: 30 mm
- Thickness: 2.25 mm

Weight

- The nominal weight of the FN990A40 is 8.2 grams.

3.8 Environmental Requirements

Temperature Range

Table 12: Temperature Range

Mode	Temperature	Note
Operating Temperature Range	-20°C ~ +55°C	This range is defined by 3GPP (the global standard for wireless mobile communication). Dejero Labs Inc guarantees that its modules comply with all 3GPP requirements and that it has the full functionality of the
	-40°C ~ +85°C	module in this range. Dejero guarantees full cellular functionality within this range. However, there may be slight deviations from the 3GPP specification in receiver performance or maximum output power. Despite this, all functionalities, including call connections, SMS, USB communication, and UART activation, will be maintained, and any degradation will not result in malfunctions. GNSS functionality may be affected at temperatures below -30°C.
Storage and non-operating Temperature Range	-40°C ~ +85°C	

Note: RED compliance from -30°C to +75°C

Warning: The application processor temperature which is in the FN990 Family must be kept below 95°C for the best performance. Depending on the various

application, a heat sink, thermal pad, or, other cooling systems may be required to properly dissipate the heat.

A large solder-resist opening area is located on the bottom side of the module. Adding a TIM on that area with a heatsink is one of the best ways to dissipate the heat well. The temperature can be read via AT commands. For more details, please refer to the SW user guide or thermal design guideline.

RoHS Compliance

As a part of the Dejero Labs Inc corporate policy of environmental protection, the FN990 Family products comply with the RoHS (Restriction of Hazardous Substances) directive of the European Union (EU directive 2011/65/EU).

4 PINS ALLOCATION

4.1 Pin-out

Table 13: FN990 Family Pin-out Information

Pin	Signal	I/O	Function	Type	Comment
USB Communication Port					
7	USB_HS_DP	I/O	USB 2.0 Data Plus	Analog	
9	USB_HS_DM	I/O	USB 2.0 Data Minus	Analog	
29	USB_SS_TX_M	O	USB 3.1 super-speed transmit – Minus	Analog	
31	USB_SS_TX_P	O	USB 3.1 super-speed transmit – Plus	Analog	
35	USB_SS_RX_M	I	USB 3.1 super-speed receive – Minus	Analog	
37	USB_SS_RX_P	I	USB 3.1 super-speed receive – Plus	Analog	
PCIe Communication Port					
41	PCIE_TX0_M	O	PCIe transmit 0 – Minus	Analog	
43	PCIE_TX0_P	O	PCIe transmit 0 – Plus	Analog	
47	PCIE_RX0_M	I	PCIe receive 0 – Minus	Analog	
49	PCIE_RX0_P	I	PCIe receive 0 – Plus	Analog	
53	PCIE_REFCLK_M	I	PCIe differential reference clock – Minus	Analog	
55	PCIE_REFCLK_P	I	PCIe differential reference clock – Plus	Analog	
50	PCIE_RESET_N	I	Functional reset to PCIe bus	VPH_PWR	Internal 10K PU
52	PCIE_CLKREQ_N	O	PCIe reference clock request signal	VPH_PWR	Internal 10k PU
54	PCIE_WAKE_N	O	PCIe wake-up	VPH_PWR	Internal 10k PU
SIM Card Interface 1					
36	UIM1_VCC	O	Supply output for an external UIM1 card	1.8V / 2.95V	Power
34	UIM1_DATA	I/O	Data connection with an external UIM1 card	1.8V / 2.95V	Internal 20k PU
32	UIM1_CLK	O	Clock output to an external UIM1 card	1.8V / 2.95V	

Pin	Signal	I/O	Function	Type	Comment
30	UIM1_RESET_N	O	Reset output to an external UIM1 card	1.8V / 2.95V	
66	UIM1_PRESENT	I	UIM1 Card Present Detect	1.8V	Internal 100k PU Active HIGH
SIM Card Interface 2					
48	UIM2_VCC	O	Supply output for an external UIM2 card	1.8V / 2.95V	Power
42	UIM2_DATA	I/O	Data connection with an external UIM2 card	1.8V / 2.95V	Internal 20k PU
44	UIM2_CLK	O	Clock output to an external UIM2 card	1.8V / 2.95V	
46	UIM2_RESET_N	O	Reset output to an external UIM2 card	1.8V / 2.95V	
40	UIM2_PRESENT	I	UIM2 Card Present Detect	1.8V	Internal 100k PU Active HIGH
Miscellaneous Functions					
6	FULL_CARD_POWER_OFF_N	I	Module On/Off	1.8V / VPH_PWR	Internal 47k PD
8	W_DISABLE_N	I	RF disable	VPH_PWR	Internal 100k PU
10	LED_N	O	LED control		Open Drain
23	WAKE_ON_WAN_N	O	Wake Host	1.8V	Default PU
65	VREG_L6B_1P8	O	Reference Voltage	1.8V	Power
67	SYS_RESIN_N	I	Reset Input	1.8V	Internal 100k PU
68	TGPIO_01	I/O	General Purpose I/O Can be I2S_CLK	1.8V	
25	TGPIO_02	I/O	General Purpose I/O Can be DPR	1.8V	
62	TGPIO_03	I/O	General Purpose I/O	1.8V	
64	TGPIO_04	I/O	General Purpose I/O	1.8V	
20	USB_PCIE_SWITCH	I	Switch Host Interface	1.8V	Internal 10k PU
22	TGPIO_06	I/O	General Purpose I/O Can be I2S_DIN	1.8V	
24	TGPIO_07	I/O	General Purpose I/O Can be I2S_DOUT	1.8V	
28	TGPIO_08	I/O	General Purpose I/O Can be I2S_WS	1.8V	

Pin	Signal	I/O	Function	Type	Comment
56	I2C_SDA	I/O	I2C Data Can be GPIO_09	1.8V	Internal 2.2k PU
58	I2C_SCL	I/O	I2C Clock Can be GPIO_10	1.8V	Internal 2.2k PU
38	1PPS	O	1PPS/TSN	1.8V	
26	W_DISABLE2_N	I	GNSS disable	VPH_PWR	Internal 100k PU
MIPI Control					
61	RFFE0_DATA	I/O	Data	1.8V	
63	RFFE0_CLK	O	Clock	1.8V	
Power Supply					
2	VPH_PWR	I	Power supply	Power	
4	VPH_PWR	I	Power supply	Power	
70	VPH_PWR	I	Power supply	Power	
72	VPH_PWR	I	Power supply	Power	
74	VPH_PWR	I	Power supply	Power	
GROUND					
3	GND	-	Ground	Ground	
5	GND	-	Ground	Ground	
11	GND	-	Ground	Ground	
27	GND	-	Ground	Ground	
33	GND	-	Ground	Ground	
39	GND	-	Ground	Ground	
45	GND	-	Ground	Ground	
51	GND	-	Ground	Ground	
57	GND	-	Ground	Ground	
71	GND	-	Ground	Ground	
73	GND	-	Ground	Ground	

Pin	Signal	I/O	Function	Type	Comment
Config					
21	CONFIG_0	-		Ground	
69	CONFIG_1	-		Ground	
75	CONFIG_2	-		Floating	
1	CONFIG_3	-		Floating	
Reserved for Future Use					
59	RFU				
60	RFU				

Warning: Reserved pins must not be connected.

4.2 FN990 Family Signals That Must be Connected

The below table specifies the FN990 Family signals that must be connected for debugging purposes, even if not used by the end application:

Table 14: Mandatory Signals

Pin	Signal	Notes
2, 4, 70, 72, 74	VPH_PWR	
3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73	GND	
6	FULL_CARD_POWER_OFF_N	
7	USB_D+	If not used, connect to a test point or a USB connector
9	USB_D-	If not used, connect to a test point or a USB connector

4.3 Pin Layout

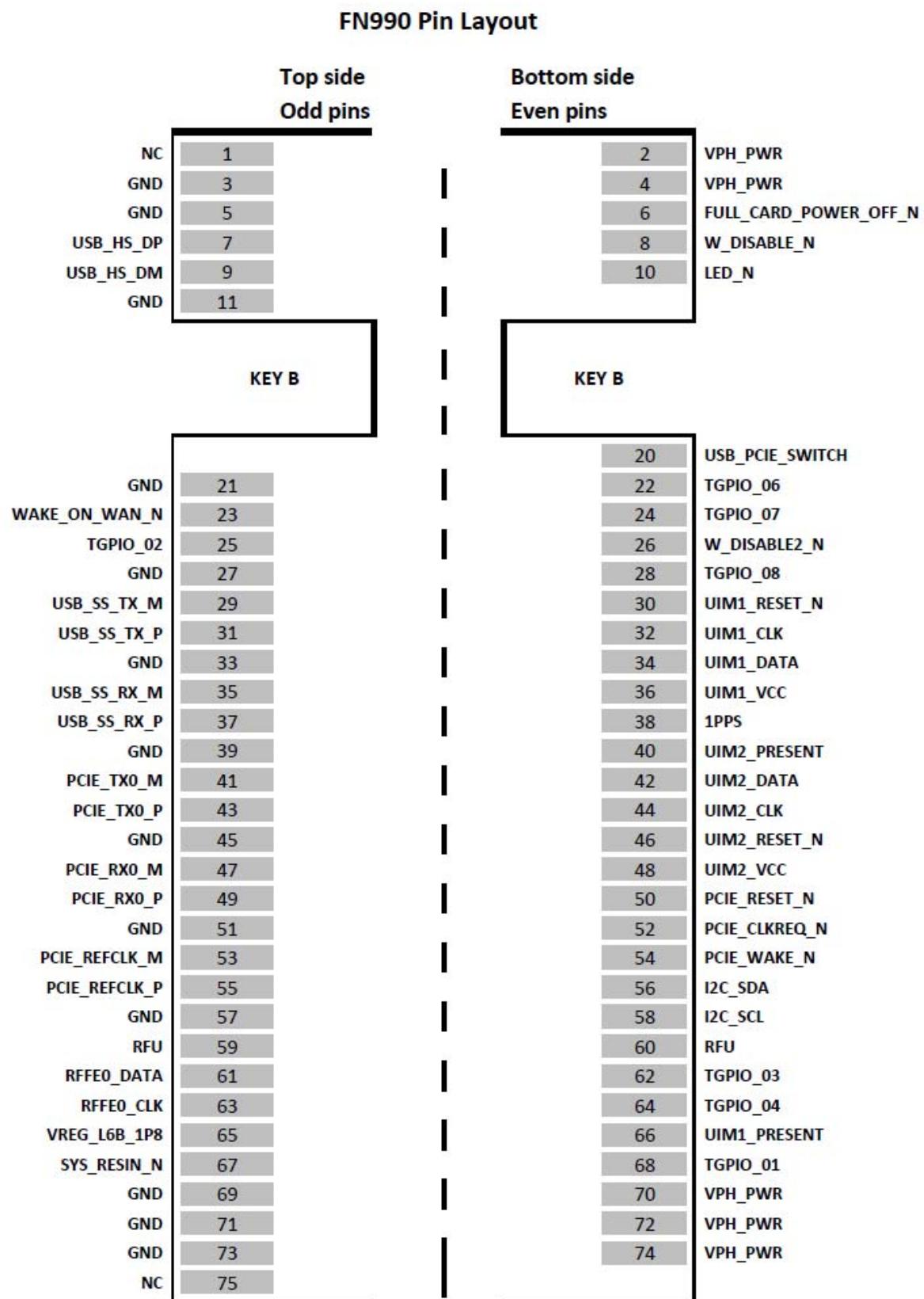


Figure 2: FN990 Family Pinout

The power supply circuitry and board layout are very important areas of the whole product design, with a critical impact on the overall product performance. Please follow carefully the following requirements and guidelines to ensure a reliable and stable design.

5.1 Power Supply Requirements

The FN990 Family power requirements are as follows:

Table 15: Power Supply Requirements

Power Supply	Value
Nominal Supply Voltage	3.3V
Supply Voltage Range	3.135 V – 4.4 V
Maximum ripple on the module input supply	30 mV
Peak current consumption	3.3 V @ 4 A

5.2 Power Consumption

Table 16: FN990 Family Current Consumption

Mode	Average [Typ.]	Mode Description
IDLE Mode		
CFUN=1	35mA	No call connection USB is connected to a host
Airplane Mode (PSMWDISACFG=1, W_DISABLE_N: Low)		
CFUN=4	< 3mA	Tx and Rx are disabled; the module is not registered on the network (Airplane mode) USB is disconnected
Standby Mode (PSMWDISACFG=1, W_DISABLE_N: Low)		
CFUN=1	< 5mA	Module cycles between wake and sleep USB is disconnected
Operative Mode (WCDMA)		
WCDMA Voice	850mA	WCDMA B1 voice call (Tx=23dBm)
WCDMA HSPA	650mA	WCDAM data call (DC-HSDPA up to 42Mbps, Max throughput)
Operative Mode (LTE)		
Single-mode (1DL/1UL SISO)	1000mA	Non-CA, B3 BW 10MHz, 1 RB, 23dBm, QPSK DL / QPSK UL
7DLCA (4x4,2x2MIMO) with 1UL(SISO)	1450mA	CA_1A-3C-7C-20A-38A, Full RB, 256QAM DL/ 256QAM UL (1500Mbps DL / 103Mbps UL)
5DLCA (4x4MIMO) with 1UL(SISO)	1150mA	CA_1A-3C-7C, Full RB, 256QAM DL/ 256QAM UL (2Gbps DL / 103Mbps UL)
Operative Mode (NR-FR1)		
NSA mode	900 mA	EN-DC_1A (1DL/UL SISO) -n78A (1DL/1UL SISO)
		LTE: BW 20MHz, 1 RB, QPSK DL / QPSK UL, 23dBm

Mode	Average [Typ.]	Mode Description
1CC+1FR1		FR1: BW 100MHz, Inner RB 137(Number)@64(Position), QPSK DL / QPSK UL, 23 dBm
NSA mode 6CC+1FR1	2000mA	EN-DC_1A (DL2x2/1UL SISO) -3C (DL4x4) -7C (DL4x4) -28A (DL2x2) -n78A (1DL 4x4MIMO/1UL SISO/60M)
		LTE: BW 20MHz, Full RB, 256QAM DL / 256QAM UL (2Gbps DL / 103Mbps UL)
		FR1: BW100MHz, Full RB, 256QAM DL / 256QAM UL (1.6Gbps DL/118Mbps)
SA mode 1FR1	380mA	FR1(n78A): BW100MHz, Full RB, 256QAM DL / 256QAM UL (1.89Gbps DL/1.25Mbps)
SA mode 2FR1	730mA	FR1(CA_n78A_n78A): BW200MHz, Full RB, 256QAM DL / 256QAM UL (3.8Gbps DL/1.25Mbps)

* Loop-back mode in call equipment

* 3.3 voltage/room temperature

Note: Worst/best-case current consumption values depend on mobile network configuration – not under module control.

5.3 General Design Rule

The principal guidelines for the Power Supply Design include three different design steps:

- Electrical design
- Thermal design
- PCB layout

Electrical Design Guidelines

The electrical design of the power supply is highly dependent on the power source from which the power is drained.

+5v Source Power Supply Design Guidelines

- The desired power supply voltage output is 3.3V. Being the difference between the input source and the desired output moderate, a linear regulator can be used. A switching power supply is preferred to reduce power dissipation.
- When using a linear regulator, a proper heat sink must be provided to dissipate the power generated.
- A low ESR bypass capacitor of adequate capacity must be provided to cut the current absorption peaks close to the FN990 Family module. A 100 μ F tantalum capacitor is usually suitable on VPH_PWR.
- Make sure that the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode must be inserted close to the modem power input to protect the FN990 Family module from power polarity inversion.

Thermal Design Guidelines

This section provides thermal design guidelines useful for developing a product with a Dejero Labs Inc FN990 modem.

Proper thermal protection design protects against human or component damage under worst-case conditions.

Furthermore, it reduces the probability of failure and does not adversely affect the use of the module, and greatly extends the operation time with maximum performance.

For more details, please refer to the thermal design guidelines.

Note: FN990 Family supports different RATs: 3G, 4G, and 5G Sub-6.

Based on the Radio Access Technology, the FN990 modem might exhibit high current consumption, thus proper thermal designs are essential to dissipate heat well.

Note: There is a large solder-resist opening area on the bottom side of the module. Adding a TIM on that area with the solder-resist opening area is highly recommended to ensure proper heat dissipation.

The modem temperature value can be read via AT command.

Note: For optimal RF performance, thermal dissipation, and mechanical stability, the FN990 must be connected to the ground and metal chassis of the host board.

It is recommended that between the shield cover of the module and the heatsink or the metal chassis of the host device use a TIM for better heat dissipation..

Power Supply PCB Layout Guidelines

As described in the electrical design guidelines, a low ESR capacitor should be connected to the power supply output to reduce current peaks. A protection diode on the modem power supply input should be connected to protect the FN990 from spikes and polarity inversion.

Placement of these components is crucial for correct operation: a misplaced component can badly affect power supply performance:

- The bypass low ESR capacitor must be placed close to the FN990 power input pins or - if the power supply is of a switching type - it can be placed close to the inductor to reduce ripple, as long as the PCB trace from the capacitor to FN990 is wide enough to avoid significant voltage drop even during the 4A current peaks.
- The protection diode must be placed close to the modem connector.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure that no voltage drops occur during the 4A current peaks.

- The PCB traces connecting the FN990 and bypass capacitor must be wide enough to avoid voltage drops even when 4A current absorption peaks occur. These traces should be kept as short as possible.
- The PCB traces connecting the switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode as close as possible to the power switching IC (only for the switching power supplies). This is done to reduce the radiated field (noise) at the switching frequency (usually 100-500 kHz).
- Use a good common ground plane.
- Place the power supply on the board to ensure that the high current return paths in the ground plane do not overlap any noise-sensitive circuitry, such as microphone amplifier/buffer or earphone amplifier.
- The power supply input cables must be kept separate from noise-sensitive lines, such as microphone/earphone cables.

5.4 RTC

The RTC within the FN990 Family module does not have a dedicated RTC supply pin. The RTC block is supplied by the VPH_PWR supply.

If the VPH_PWR power is removed, RTC is not maintained so if it is necessary to maintain an internal RTC, VPH_PWR must be supplied continuously.

5.5 Reference Voltage

The 1.8V regulated power supply output is supplied as the reference voltage to a host board. This output is active when the module is turned ON and turns OFF when the module is shut down.

The table below lists the reference voltage of the FN990 Family modules.

Table 17: FN990 Family Reference Voltage

Pin	Signal	I/O	Function	Type	Comment
65	VREG_L6B_1P8	O	Reference Voltage	Power	1.8V

5.6 Internal LDO for GNSS Bias

The LDO for GNSS bias is applied inside the FN990 Family model.

The voltage supply is generated internally by the FN990 (LDO) and is fed to GNSS active antenna.

The table below lists the LDO for GNSS bias of FN990 Family modules.

Table 18: LDO for GNSS bias of FN990 Family

Symbol	Parameter	Min	Typ	Max	Unit
$V_{GNSS\ DC\ bias}$	Voltage of internal LDO for GNSS bias	2.9	3.1	3.15	[V]
$I_{GNSS\ DC\ bias}$	Current of internal LDO for GNSS bias	-	-	100	[mA]

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings – Not Optional

Warning: A deviation from the value ranges listed below could damage the FN990 module.

Table 19: Absolute Maximum Ratings - Not Optional

Symbol	Parameter	Min	Max	Unit
VPH_PWR	Battery supply voltage on pin VPH_PWR	-0.3	+4.7	[V]

6.2 Recommended Operating Conditions

Table 20: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T _{amb}	Ambient temperature	-40	+25	+85	[degC]
VPH_PWR	Battery supply voltage on pin VPH_PWR	3.135	3.3	4.4	[V]
I _{VPH_PWR}	Peak current on pin VPH_PWR	-	-	4	[A]

7 DIGITAL SECTION

7.1 Logic Levels

Unless otherwise specified, all FN990 Family interface circuits are 1.8V CMOS logic.

Only USIM interfaces are capable of dual voltage I/O.

The following tables show the logic level specifications used in the FN990 interface circuits. The data specified in the tables below are valid throughout all drive strengths and the whole temperature range.

Warning: Do not connect FN990 digital logic signal directly to the application digital logic signals with a voltage higher than 2.134V for 1.8V CMOS signals.

1.8V Pins – Absolute Maximum Ratings

Table 21: Absolute Maximum Ratings - Not Functional

Parameter	Min	Max
Input level on any digital pin when on	-	+2.134 V
Input voltage on analog pins when on	-	+2.134 V

1.8V Standard GPIOs

Table 22: Operating Range - Interface Levels (1.8V CMOS)

Parameter	Min	Max	Unit	Comment
V_{IH}	Input high level	1.26	2.1	[V]
V_{IL}	Input low level	-0.3	0.54	[V]
V_{OH}	Output high level	1.35	1.8	[V]
V_{OL}	Output low level	0	0.45	[V]

1.8V UIM1/UIM2 Pins

Table 23: Operating Range - UIM Pins Working at 1.8V

Parameter	Min	Max	Unit	Comment
V_{IH}	Input high level	1.17	2.1	[V]
V_{IL}	Input low level	-0.3	0.63	[V]
V_{OH}	Output high level	1.35	1.8	[V]
V_{OL}	Output low level	0	0.45	[V]

2.95V Pins – Absolute Maximum Ratings

Table 24: Absolute Maximum Ratings - Not Functional

Parameter	Min	Max
Input level on any digital pin when on	-	+3.344 V
Input voltage on analog pins when on	-	+3.344 V

2.95V Sim Card Pins

Table 25: Operating Range - UIM Pins Working at 2.95V

Parameter	Min	Max	Unit	Comment
V_{IH}	Input high level	1.843	3.25	[V]
V_{IL}	Input low level	-0.3	0.73	[V]
V_{OH}	Output high level	2.21	2.95	[V]
V_{OL}	Output low level	0	0.368	[V]

VPH_PWR Level I/O Pins

Table 26: Operating Range - I/O Pins Working at VPH_PWR

Parameter	Min	Max	Unit
V_{IH}	Input high level	$0.65 \times VPH_PWR$	-
V_{IL}	Input low level	-	$0.35 \times VPH_PWR$
V_{OH}	Output high level	$0.8 \times VPH_PWR$	VPH_PWR
V_{OL}	Output low level	0	$0.2 \times VPH_PWR$

7.2 Power ON/OFF/RESET

The following tables show the description of power control pins.

Table 27: Power Interface Signals

Pin	Signal	I/O	Function	Type	Comment
6	FULL_CARD_POW ER_OFF_N	I	Module On/Off	1.8V VPH_PWR	/ Internal 47k PD
67	SYS_RESET_N	I	Reset Input	1.8V	Internal 100k PU
65	VREG_L6B_1P8	O	Reference Voltage	1.8V	Power
*	BOOT_OK Shutdown Indicator	/O	Power ON/OFF Status Check	1.8V	* Can be assigned to GPIO

Power On

To turn on the FN990 data card, the FULL_CARD_POWER_OFF_N pin must be asserted high.

Note: To turn on the FN990 module, the SYS_RESIN_N pin must not be asserted low. If asserted low for more than one second, the FN990 modem will be reset. Power on can be triggered by the SYS_RESIN_N pin (low level) as well. Even so, please control the FN990 ON/OFF status using the FULL_CARD_POWER_OFF_N pin.

Initialization and Activation State

After turning on the FN990 module, the device is not yet fully functional because the software boot and initialization process takes some time to complete. For this reason, it is not recommended to start communicating with the FN990 module during the initialization phase.

The AT command interface is accessible via USB or PCIe port. In general, as shown in the figure below, the FN990 modems become fully operational (in the Activation state) at least 50 seconds after the FULL_CARD_POWER_OFF_N is asserted.

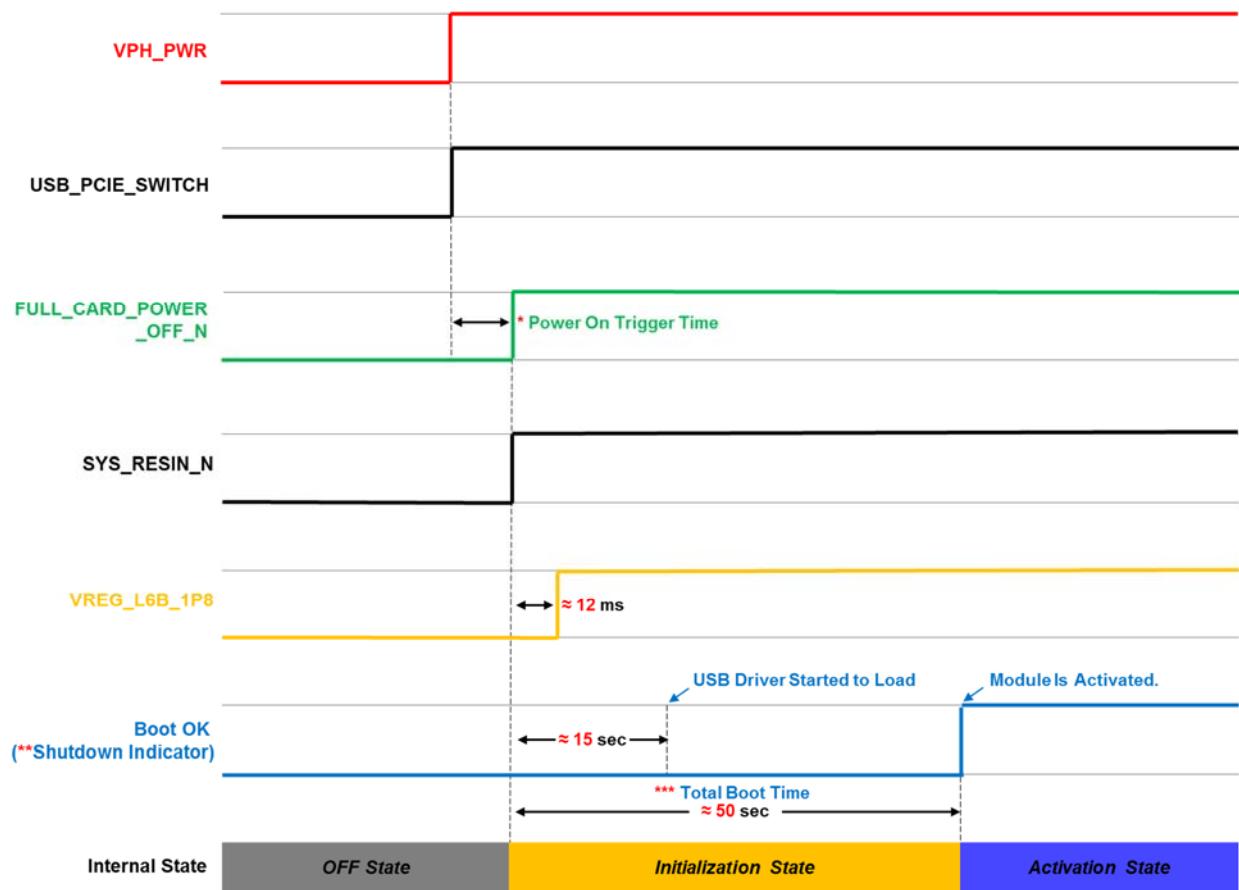


Figure 3: FN990 Family Power ON Sequence - USB mode (USB_PCIE_SWITCH: High, Default)

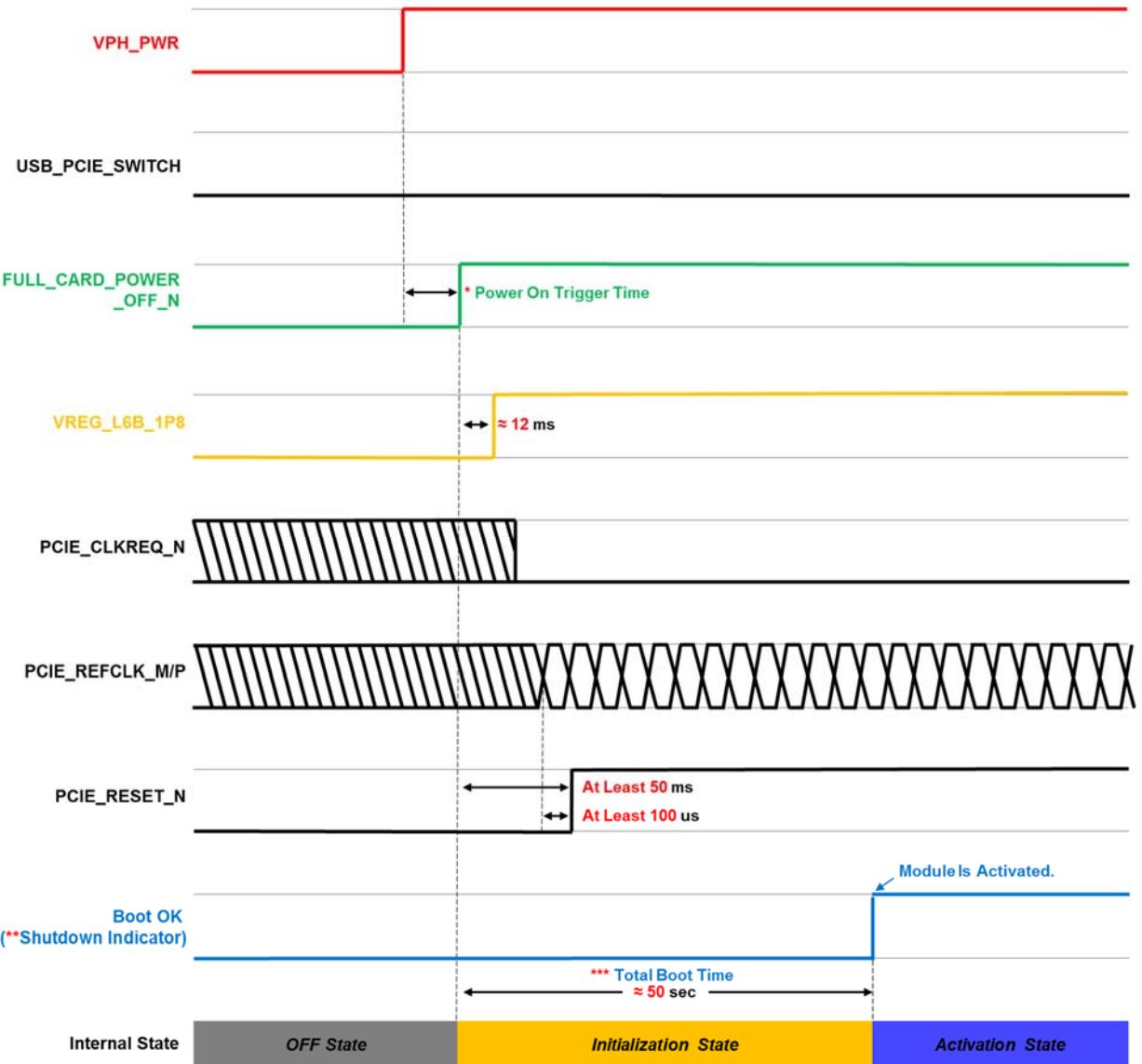


Figure 4: FN990 Family Power ON Sequence – PCIe EP mode (USB_PCIE_SWITCH: Low)

Note: To verify if the FN990 Family has powered up properly, please follow the indications below:

* Power on trigger time is the interval between **VPH_PWR** to **FULL_CARD_POWER_OFF_N**: this could be null (0 ms) if the customer application requires turning on the module automatically.

** Monitoring **BOOT_OK** (Shutdown indicator) pin. When the status translates to high, the module boot-up process is complete. To use **BOOT_OK** (Shutdown indicator), the shutdown indication function must be enabled through the **AT#SHDNIND** command. (please refer to the AT Reference Guide document)

*** The stated total boot time is an approximate measure of the latest SW and HW configuration. The boot time may be lengthened or shortened depending on the module configuration, firmware, or hardware version.

Note: Active low signals are labeled with a name ending with “_N”.

Note: To avoid a back-powering effect, it is recommended to prevent any HIGH logic level signals from being applied to the digital pins of the module when it is powered OFF or during an ON/OFF transition.

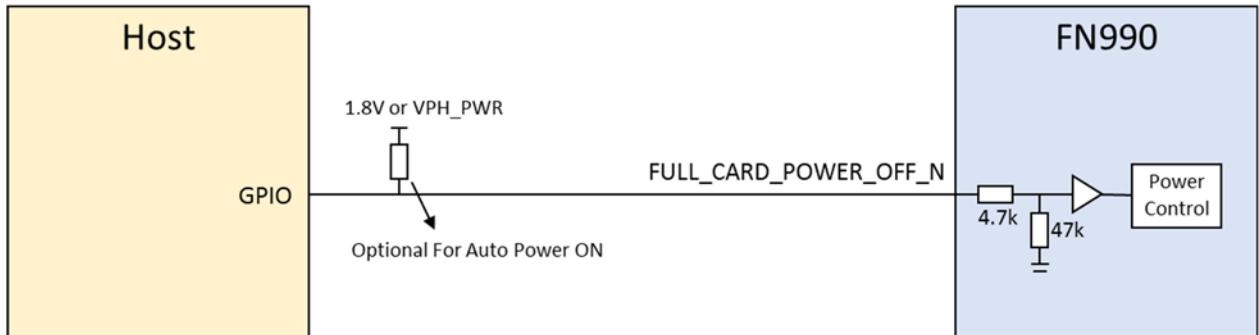


Figure 5: Example Circuit for ON/OFF by FULL_CARD_POWER_N

Power Off

Power off of the device can be done in two different ways:

- Graceful shutdown by FULL_CARD_POWER_OFF_N
- Fast shutdown by GPIO triggered

Graceful Shutdown

To shutdown the FN990 Family module safely, the host can use the graceful shutdown function.

The graceful shutdown can be triggered by:

- FULL_CARD_POWER_OFF_N

Graceful Shutdown by FULL_CARD_POWER_N

To gracefully shutdown the FN990, FULL_CARD_POWER_OFF_N should be asserted to Low.

Once FULL_CARD_POWER_N is asserted to Low, the FN990 enters the finalization state, terminates active processes, and prepares to turn off safely.

As shown in the diagram below, VREG_L6B_1P8 will indicate when the module is ready to be turned off.

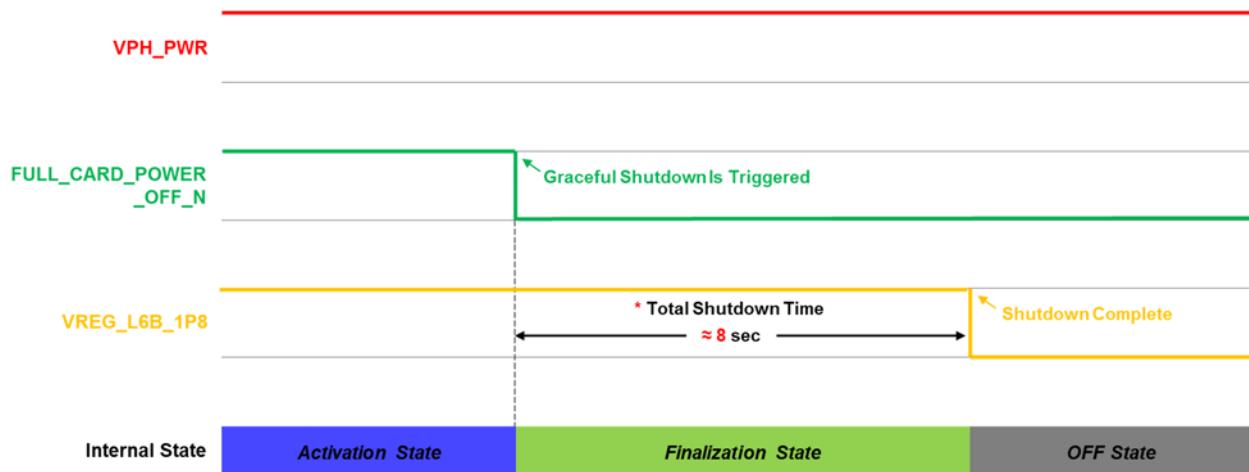


Figure 6: Graceful Shutdown by FULL_CARD_POWER_N

Note: Graceful Shutdown triggered by FULL_CARD_POWER_OFF_N is only effective after the module boots up completely.

* The stated total shutdown time is an approximate measure of the latest SW and HW combination. The shutdown time may be lengthened or shortened depending on the SW configuration, SW, or HW version.

Fast Shutdown

For quicker FN990 module shutdown, the host application can use the fast shutdown function, which can be triggered by:

- GPIO (+ optional shutdown indicator)

Fast Shutdown by GPIO

To leverage the fast shutdown feature, one of the GPIO lines should be assigned as Fast Shutdown Trigger using the AT commands.

Once the fast shutdown trigger senses a High to Low transition, the fast shutdown is started: the FN990 enters a finalization state, terminates active processes, and prepares to turn off safely. As shown in the figure below, when the module is ready to be turned off, it will be indicated via VREG_L6B_1P8.

Please refer to the AT User Guide for more details on how to enable the shutdown indicator and fast shutdown trigger.

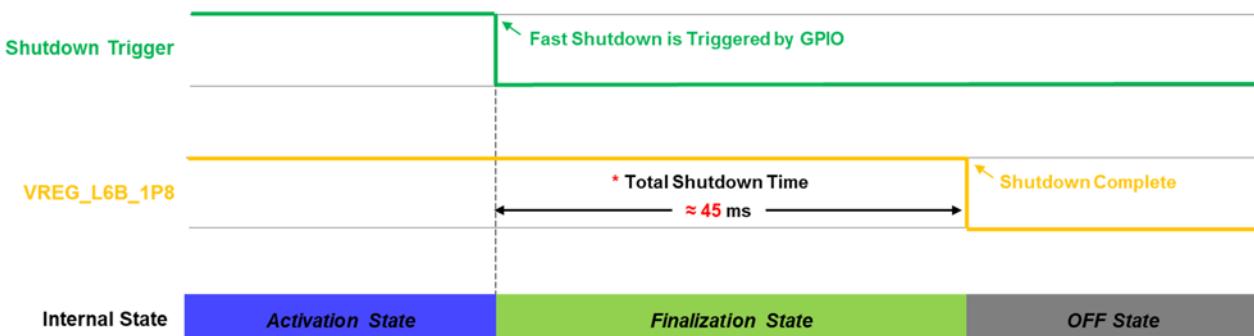


Figure 7: Fast Shutdown by GPIO

Note: Using a fast shutdown without a shutdown indicator function, the FULL_CARD_POWER_N pin should be controlled to prevent the FN990 from rebooting.

For more information, please refer to the AT commands reference guide and SW user guide document.

* The stated total shutdown time is an approximate measure of the latest SW and HW combination. The shutdown time may be lengthened or shortened depending on the SW configuration, SW, or HW version.

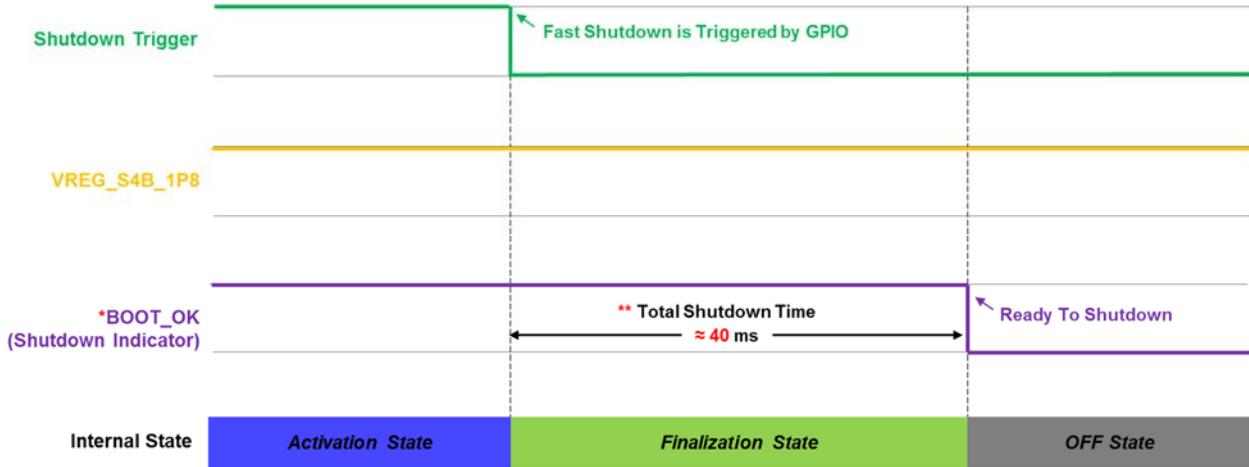


Figure 8: Fast Shutdown by GPIO (*SHDNIND Enable, Optional)

Note: *Shutdown Indicator is an optional function and is disabled by default. The host can verify the module entered the OFF state by monitoring the shutdown indicator pin status. To turn on the module after using a fast shutdown with a shutdown indicator function, it should be re-powered or rebooted.

For more information, please refer to AT Commands Reference Guide and SW User Guide document.

Note: Fast shutdown function is disabled by default. To use the fast shutdown function, please refer to the AT Commands Reference Guide and SW User Guide document.

Warning: If the VPH_PWR is to be kept at a high status, the module will reboot. (Not applicable to the Shutdown Indicator function).

Warning: Failure to follow recommended shut-down procedures might damage the device and consequently void the warranty.

Reset

Device reset can be achieved as follows:

- Unconditional reset using the SYS_RESIN_N

Unconditional Hardware Reset

To unconditionally restart the FN990 Family module, the SYS_RESIN_N pin must be asserted low for more than 1 second and then released.

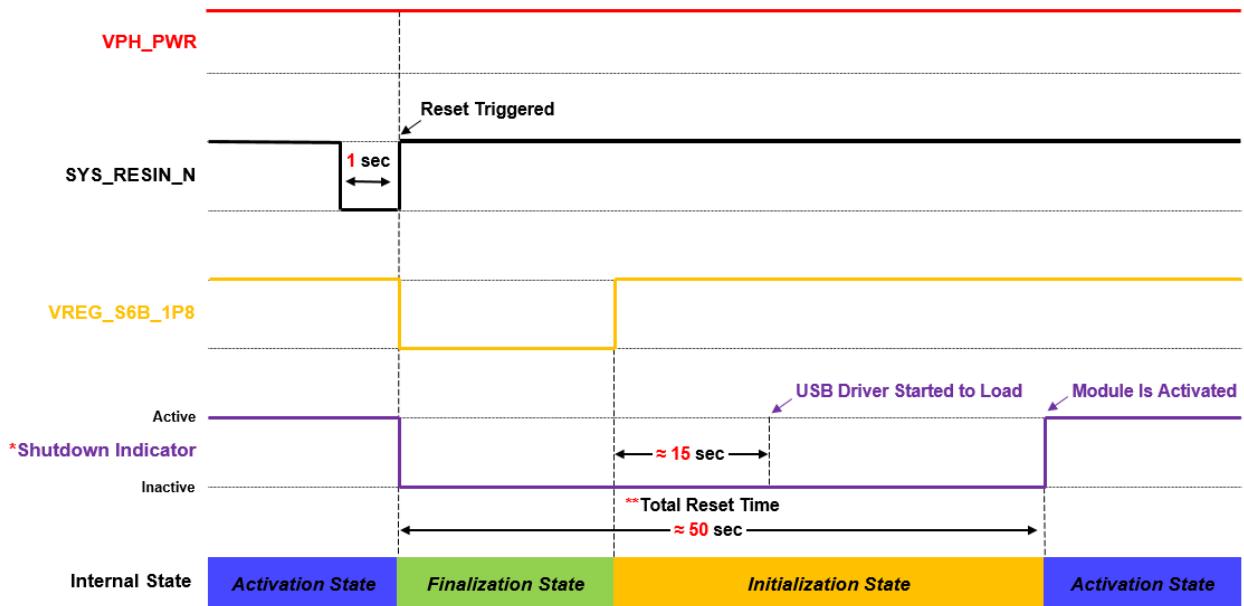


Figure 9: Unconditional Hardware Reset by [SYS_RESET_N](#)

Note: *Shutdown Indicator is an optional function. If SHDIND is enabled, it can verify the status via the SHDIND function.

Please refer to the AT commands user guide document.

** The stated total reset time is an approximate measure of the latest SW and HW combination. The shutdown time may be lengthened or shortened depending on the SW configuration, SW, or HW version.

Note: Unconditional hardware reset must be used only as an emergency procedure, and not as a normal power-off operation.

Note: Do not use any pull-up resistor on the RESET_N line or any totem pole digital output. Using a pull-up resistor may cause latch-up problems on the FN990 Family power regulator and improper functioning on the module.

The RESET_N line must be connected only in an open-collector configuration.

The below figure shows a simple circuit for this action.

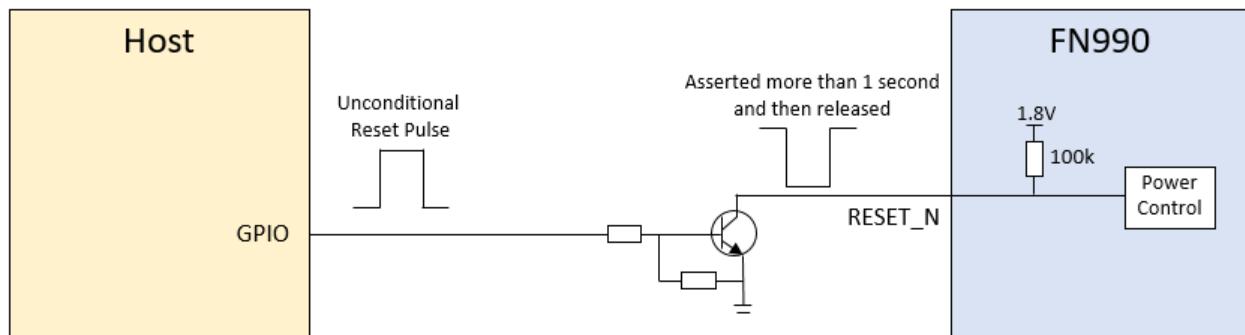


Figure 10: Example Circuit for [RESET](#) by [SYSTEM_RESET_N](#)

7.3 Communication Ports

The below table summarizes all the hardware interfaces of the FN990 Family module.

Table 28: FN990 Family Hardware Interfaces

Interface	Description
PCIe	Peripheral Component Interconnect Express Gen 3.0
USB	USB 3.1 Gen 2 interface
USIM	x2 dual voltage each (1.8V / 2.95V)
eSIM	Embedded SIM (optional)
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
Control Interfaces	W_DISABLE_N, WAKE_ON_WAN_N, LED, DPR
Antenna ports	x4 Cellular, 1 for GNSS

Host Interface

Note: FN990 M.2 data card supports USB 3.1 Gen 2 and PCIe Gen 3 respectively.

Host Interface Switch Function

This section describes the host interface switch functions.

Note: The meaning of the name USB/PCIe switch implies which interface provides the main function.

Please refer to the 1VV0301750, FN990 Family Software User Guide, regarding each function.

Table 29: Host Interface Switch Pin

Pin	Signal	I/O	Function	Type	Comment
20	USB_PCIE_SWITCH	I	Switch Host Interface	1.8V	Internal PU 10k

Table 30: USB/PCIe Switch Pin

USB/PCIe Switch	Mode	USB	PCIe EP	PCIe RC
High (Default)	USB	Available	Not support	Available**
Low	PCIe	Available*	Available	Not support

FN990 Family M.2 Card determines the host interface by checking the status of the USB_PCIE_SWITCH pin at the beginning of the power-on sequences.

*** Note:** When using PCIe EP, PCIe RC cannot be used, and basic functions such as mobile data and AT commands are provided through PCIe EP, while USB is provided only for debugging and specific purpose.

For more details, please refer to the 1VV0301750, FN990 Family Software User Guide.

* *Note: FN990 Family supports the following devices as EP for data interface:

- Marvell AQC107 Ethernet Controller
- Realtek RTL8125 Ethernet Controller

Please consult Dejero Labs Inc if a different EP device is used as a data interface since the EP device kernel driver needs to be modified to use the FN990 network hardware accelerator.

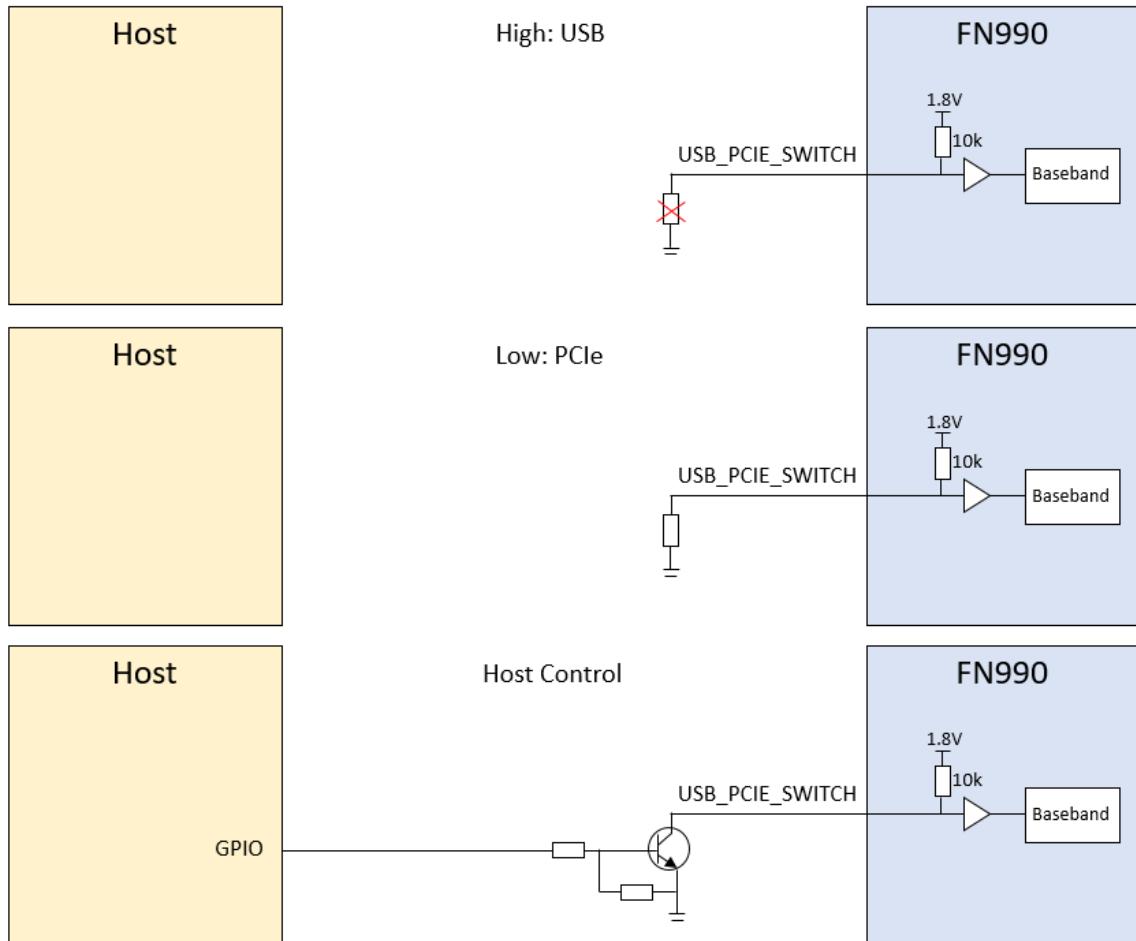


Figure 11: Example Circuit for HOST Interface Switch Function

PCIe Interface

The FN990 Family module includes a PCIe interface. PCIe needs AC coupling series capacitors on the TX lines in both directions. To interface PCIe with the application board that controls the modem, 0.22 uF capacitors should be installed on PCIE_RX_P/M lines of the FN990. The series capacitors are already placed on PCIE_TX_P/M lines inside the FN990.

Internally, the VPH_PWR level 10k pull-up resistor is already mounted on PCIE_WAKE_N, PCIE_CLKREQ_N, and PCIE_RESET_N.

The suggested PCIe interface connection is shown in the diagram below:

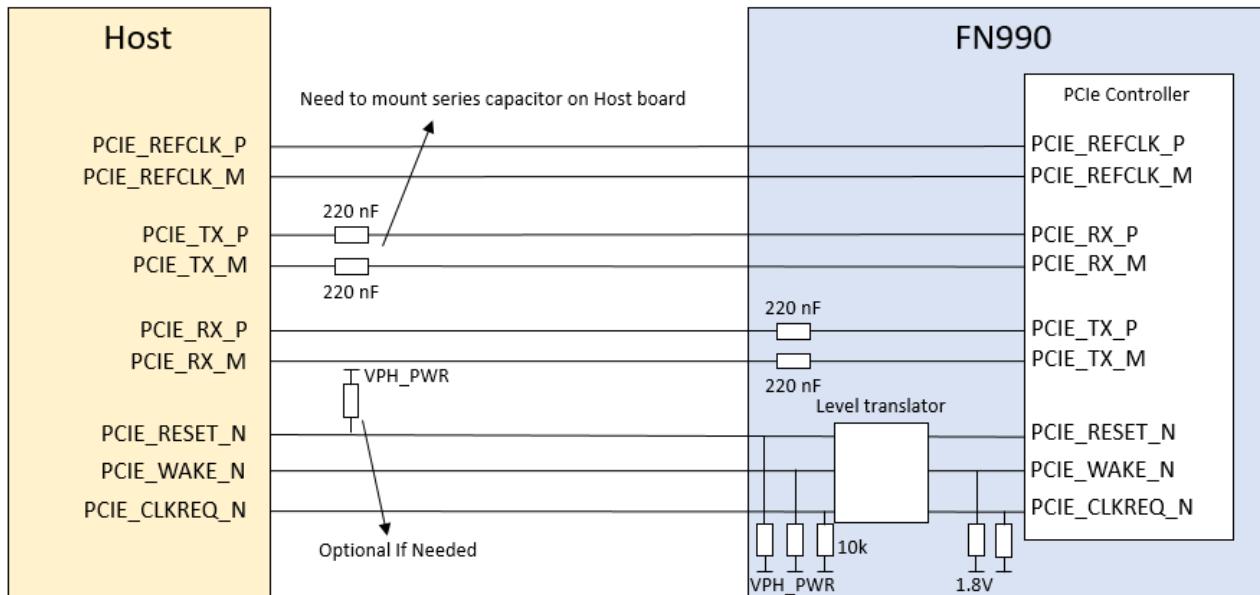


Figure 12: Connection for PCIe Interface

Note: FN990 Family supports PCIe root complex (RC) mode.

Depending on the EP device such as NIC or something else, may require a suitable value of pull-up resistor on the PCIE_RESET_N line.

Customers interested in using PCIe RC mode can contact Dejero Labs Inc Technical Support at:

- info@Dejero.com

Note: The PCIe signals traces must be routed carefully: minimize trace lengths, number of vias, and capacitive loading. The impedance value should be as close as possible to the 85 Ohm differential.

Table 31: PCIe Interface Signals

Pin	Signal	I/O	Function	Type	Comment
41	PCIE_TX0_M	O	PCIe transmit 0 – Minus	Analog	
43	PCIE_TX0_P	O	PCIe transmit 0 – Plus	Analog	
47	PCIE_RX0_M	I	PCIe receive 0 – Minus	Analog	
49	PCIE_RX0_P	I	PCIe receive 0 – Plus	Analog	
53	PCIE_REFCLK_M	I	PCIe differential reference clock – Minus	Analog	
55	PCIE_REFCLK_P	I	PCIe differential reference clock – Plus	Analog	
50	PCIE_RESET_N	I	Functional reset to PCIe bus	VPH_PWR	Internal 10k PU
52	PCIE_CLKREQ_N	O	PCIe reference clock request signal	VPH_PWR	Internal 10k PU

Pin	Signal	I/O	Function	Type	Comment
54	PCIE_WAKE_N	O	PCIe wake-up	VPH_PWR	Internal 10k PU

Note: PCIE_RESET_N operates as digital input in PCIe end point mode and open drain in PCIe root complex mode. PCIE_CLKREQ_N and PCIE_WAKE_N operate as an open drain in PCIe end point mode, and digital input in PCIe root complex mode.

The default of the FN990 Family is end point mode.

Note: Consider placing a low-capacitance ESD protection component to protect the FN990 against ESD spikes.

Warning: FN990 data cards are not designed or intended to support Hot-Swap or Hot-Plug connection. Performing Hot-Swap or Hot-Plug may pose a danger to the FN990 Family module, to the host device, and to the person handling the device.

PCIe Layout Guidelines

The below guidelines will provide general guidelines for the PCIe interface to improve signal integrity.

- All other sensitive/high-speed signals and circuits must be protected from PCIe corruption.
- PCIe signals must be protected from noisy signals (clocks, SMPS, and so forth).
- Pay extra attention to crosstalk, ISI, and intralane skew and impedance discontinuities.
- PCIe Tx AC coupling capacitors are better placed close to the source or receiver side to keep good SI of the route on the PCB.
- To maintain impedance balance, maintain positive and negative traces as balanced as possible in terms of the signal and its return path.
- Trace length matching between the reference clock, Tx, and Rx pairs is not required.
- External capacitors also should keep differential traces. Ensure not to stagger the capacitors. This can affect the differential integrity of the design and can create EMI.

Table 32: PCIe Routing Constraints

Type of guidance	Guideline	Requirement
General	Data rate	8 Gbps*
	Insertion loss at 4 GHz (dB)	-10 dB
	Impedance	85 ohms differential
	Bus length	285 mm**
Length matching	Intra pair match	< 0.7mm
Spacing	To all other signals	> 4 x line width
	Tx lane to Rx lane	> 4 x line width

Type of guidance	Guideline	Requirement
Component	AC capacitance	220 nF

*Actual throughput at the system level could be lower due to overheads.

**PCIe trace length in FN990 Family: about 15 mm.

USB 3.1 Interface

The FN990 Family modules include super-speed USB 3.1 Gen 2 with high-speed USB 2.0 backward compatibility. It complies with the Universal Serial Bus Specification, revision 3.1, and can be used for control and data transfers as well as for diagnostic monitoring and firmware update.

The USB port is typically the main interface between the FN990 Family module and application hardware. USB 3.1 needs AC coupling series capacitors on the TX lines in both directions.

To interface USB 3.1 with the application board controlling the modem, it is necessary to install a 220 nF capacitor on the USB_SS_RX_P/M lines of the FN990 Family. The series capacitors are already placed on USB_SS_TX_P/M lines inside the FN990 module.

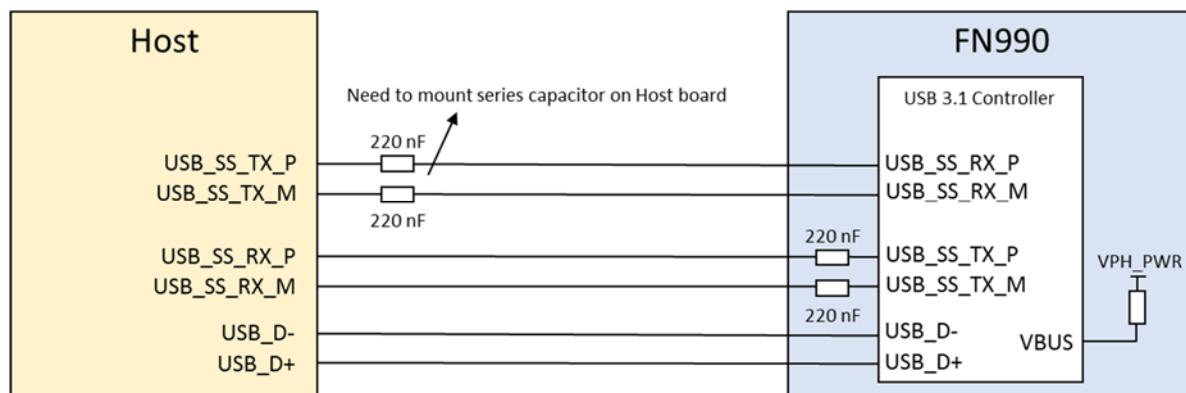


Figure 13: Connection for USB Interface

Note: The USB signal traces must be carefully routed: minimize trace lengths, number of vias, and capacitive loading. The impedance value should be as close as possible to the 85 Ohm differential.

Table 33: USB Interface Signals

Pin	Signal	I/O	Function	Type	Comment
7	USB_HS_DP	I/O	USB 2.0 Data Plus	Analog	
9	USB_HS_DM	I/O	USB 2.0 Data Minus	Analog	
29	USB_SS_RX_M	O	USB 3.1 super-speed receive – Minus	Analog	
31	USB_SS_RX_P	O	USB 3.1 super-speed receive – Plus	Analog	
35	USB_SS_TX_M	I	USB 3.1 super-speed transmit – Minus	Analog	
37	USB_SS_TX_P	I	USB 3.1 super-speed transmit – Plus	Analog	

Note: Consider placing a low-capacitance ESD protection component to protect FN990 Family against ESD strikes.

USB OTG Feature

FN990 family supports USB On-The-Go (OTG) function.

Note: Since the FN990 family does not support a USB_ID pin, a TPGIO pin should be set as the purpose of USB_ID using the #OTGCFG command. The module will be in host mode if the TGPIO pin is connected to the ground. External 5 V power is required on an application board to supply 5 V power to the OTG device because the FN990 family does not supply power for the OTG device.

USB Layout Guidelines

- If third-party components are required for signal improvement, place them closer to the USB connector.
- There are relatively fast edge rates, so must be routed away from sensitive circuits and signals (RF, audio, and XO).
- Maintain good isolation between the USB connector and RF antennas (especially 2.4 GHz).
- Route the RF signals operating at a 2.4 GHz frequency with the highest isolation possible from USB_SS_TX/RX traces.
- USB SS Tx AC coupling capacitors are better placed close to the source or the ESD/connector side to keep good SI of the main route on the PCB.
- Route differential pairs in the inner layers with a solid GND reference to have good impedance control and to minimize discontinuities.
- Keep isolation between the Tx pair, Rx pair, and DP/DM to avoid crosstalk.
- The SS-USB Tx and Rx differential pair maximum length is recommended to be less than 136 mm.
- For USB 2.0 signal, the maximum trace length should be less than 234 mm.

Table 34:USB Routing Constraints

Type of guidance	Guideline	Requirement	
		USB 3.1 Gen 2	USB 2.0
General	Data rate	10 Gbps	480Mbps
	Insertion loss at 5 GHz (dB)	-7 dB	N/A
	Impedance	85 ohms differential	
	Bus length	136 mm	234 mm
Length matching	Intra pair match	< 0.7mm	< 2mm
Spacing	To all other signals	> 4 x line width	> 3 x line width
	Tx lane to Rx lane	> 4 x line width	N/A
Component	AC capacitance	220 nF	N/A

SIM Interface

The FN990 modem family supports an external SIM interface. (1.8 V or 2.95 V)

Note: UIM2 can be assigned as an optional eSIM. In that case, UIM2 can't be used as an external SIM interface.

Table 35: SIM Interface Signals

Pin	Signal	I/O	Function	Type	Comment
SIM Card Interface 1					
36	UIM1_VCC	O	Supply output for an external UIM1 card	1.8V / 2.95V	Power
34	UIM1_DATA	I/O	Data connection with an external UIM1 card	1.8V / 2.95V	Internal 20k PU
32	UIM1_CLK	O	Clock output to an external UIM1 card	1.8V / 2.95V	
30	UIM1_RESET_N	O	Reset output to an external UIM1 card	1.8V / 2.95V	
66	UIM1_PRESENT	I	UIM1 Card Present Detect	1.8V	Internal 100k PU Active High*
SIM Card Interface 2					
48	UIM2_VCC	O	Supply output for an external UIM2 card	1.8V / 2.95V	Power
42	UIM2_DATA	I/O	Data connection with an external UIM2 card	1.8V / 2.95V	Internal 20k PU
44	UIM2_CLK	O	Clock output to an external UIM2 card	1.8V / 2.95V	
46	UIM2_RESET_N	O	Reset output to an external UIM2 card	1.8V / 2.95V	
40	UIM2_PRESENT	I	UIM2 Card Present Detect	1.8V	Internal 100k PU Active High*

Note: * From xx3 official SW, the default UIM_PRESENT pin setting has been changed from low to high to comply with the M.2 specification standard.

Pin settings can be changed through AT#SIMINCFG, please refer to the AT commands reference guide for details.

If you have any special requirements, please contact Technical Support or Sales.

SIM Schematic Example

The diagram below shows in particular how the SIM part of the application interface should be designed.

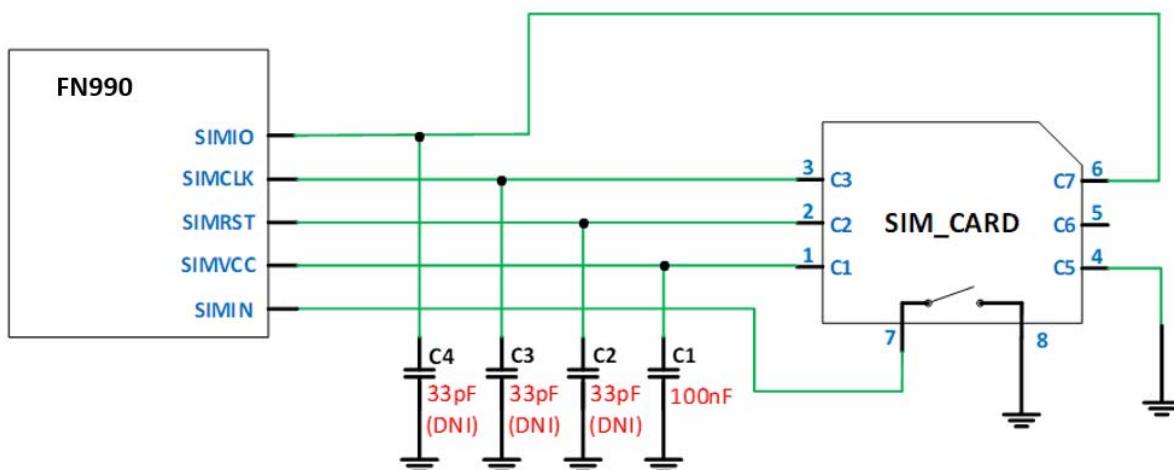


Figure 14: SIM Schematic Example

Note: FN990 Family modems contain an internal pull-up resistor on SIMIO. It is not necessary to install an external pull-up resistor.

eSIM Interface

FN990 modems include pads for an optional embedded SIM (WLCSP package).

Customers interested in using an embedded SIM mounted on the FN990 can contact Dejero Labs Inc Technical Support at:

- TS-EMEA@Dejero Labs Inc.com
- TS-AMERICAS@Dejero Labs Inc.com
- TS-APAC@Dejero Labs Inc.com

I2C – Inter-integrated Circuit

The FN990 Family supports an I2C interface: the table below lists the I2C signals of the modem.

Table 36: I2C Signal

Pin	Signal	I/O	Function	Type	Comment
56	I2C_SDA	I/O	I2C Data Can be GPIO_09	1.8V	Internal 2.2k PU
58	I2C_SCL	I/O	I2C Clock Can be GPIO_10	1.8V	Internal 2.2k PU

Control Interface

Table 37: Control Interface Pins

Pin	Signal	I/O	Function	Type	Comment
8	W_DISABLE_N	I	WLAN disable	VPH_PWR	Internal 100k PU
26	W_DISABLE2_N	I	GNSS disable	VPH_PWR	Internal 100k PU
10	LED_N	O	LED control		Open Drain
23	WAKE_ON_WAN_N	O	Wake Host	1.8V	Default PU
25	GPIO_02	I/O	General Purpose Can be DPR	I/O 1.8V	

WLAN/GNSS Disable

The W_DISABLE_N signal is provided to disable the WLAN/GNSS function:

- W_DISABLE_N

Low: Airplane mode

High or Floating: Normal operation

- W_DISABLE2_N

Low: GNSS Disable

High or Floating: Normal operation

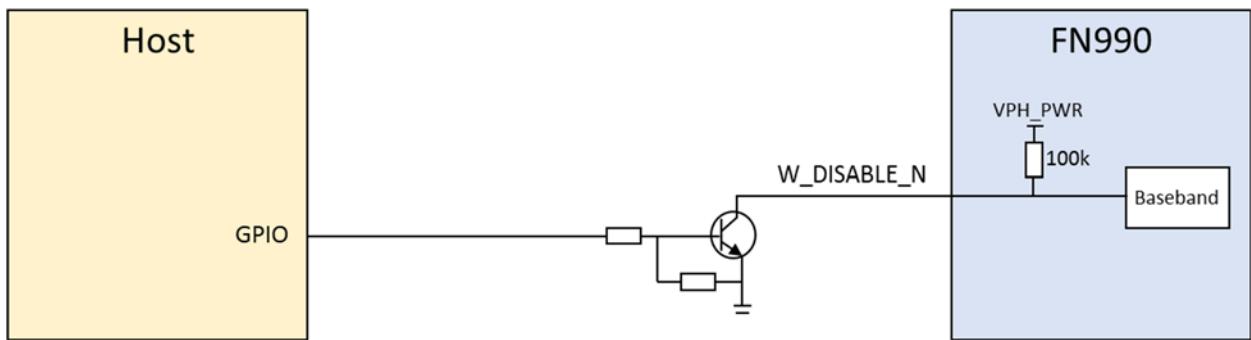


Figure 15: Example Circuit for WLAN/GNSS Disable Function

Please refer to the AT commands guide for setting the WLAN/GNSS disable function.

LED

The LED signal drives the LED output. The recommended LED connection is the following:

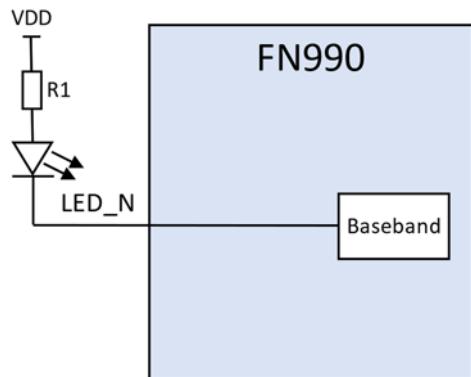


Figure 16: Recommended LED Connection

R1 and VDD determine the LED brightness and forward current.

When VDD is 3.3V and LED's forward voltage is 2.0V, the recommended R1 value ranges from 66 to 250 Ohm.

However, the resistor value must be calculated considering the LED specifications. It is recommended to use VDD below the VPH_PWR level.

Note: If the LED function is enabled and a LED is connected to the LED_N pin, current consumption may be slightly increased. And current sinking mode (up to 10mA) can be supported.

Wake Host

WAKE_ON_WAN_N is an active low signal and is used to wake the Host when specific events occur.

- SMS
- Network de-registration
- Voice Call

Please refer to the AT commands guide for setting the Wake function.

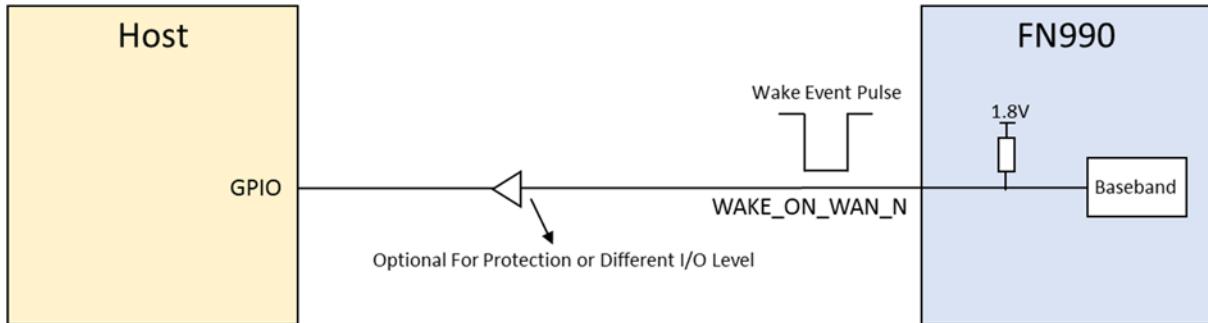


Figure 17: Recommended LED Connection

DPR

This signal is input directly to the FN990 module from a suitable SAR sensor. Then FN990 Family module will reduce output tx power.

DPR function is not available yet: specific implementation will be determined on customer request.

For further information on the DPR function on the FN990 modem family, please contact Dejero Labs Inc Technical Support at:

- TS-EMEA@Dejero Labs Inc.com
- TS-AMERICAS@Dejero Labs Inc.com
- TS-APAC@Dejero Labs Inc.com

7.4 General Purpose I/O

The general-purpose I/O pins can be configured to act in four different ways:

- Input
- Output
- Fast shutdown
- Dedicate function (Customer requirement)

Input pins can only report digital values (high or low) present on the pin at the read time.

Output pins can only be set or the pin level can be queried.

Table 38: General Purpose I/O

Pin	Signal	I/O	Function	Type	Comment
General Purpose I/O					
68	TGPIO_01	I/O	General Purpose I/O Can be I2S_CLK	1.8V	
25	TGPIO_02	I/O	General Purpose I/O Can be DPR	1.8V	
62	TGPIO_03	I/O	General Purpose I/O	1.8V	
64	TGPIO_04	I/O	General Purpose I/O	1.8V	
22	TGPIO_06	I/O	General Purpose I/O Can be I2S_DIN	1.8V	
24	TGPIO_07	I/O	General Purpose I/O Can be I2S_DOUT	1.8V	
28	TGPIO_08	I/O	General Purpose I/O	1.8V	

Pin	Signal	I/O	Function	Type	Comment
			Can be I2S_WS		
56	I2C_SDA	I/O	I2C Data Can be GPIO_09	1.8V	Internal 2.2k PU
58	I2C_SCL	I/O	I2C Clock Can be GPIO_10	1.8V	Internal 2.2k PU

Using a GPIO as INPUT

GPIO pins, when used as inputs, can be tied to a digital output of another device and report its status, provided the device interface levels are compatible with the GPIO 1.8V CMOS levels.

If a digital output of a device is tied to GPIO input, the pin has interface levels different than 1.8V CMOS. It can be buffered with an open collector transistor with a 47K ohm pull-up resistor to 1.8V.

Using a GPIO as OUTPUT

GPIO pins, when used as output, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pins have a push-pull output, and therefore the pull-up resistor can be omitted.

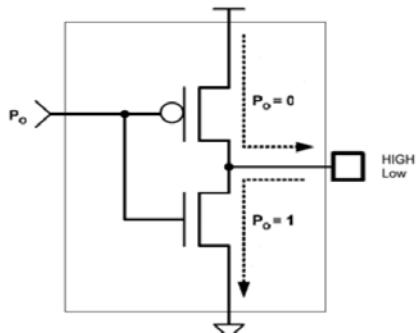


Figure 18: GPIO Output Pin Equivalent Circuit

8 RF Section

8.1 Antenna Interface

The antenna connection is one of the most important aspects of the whole application design as it strongly affects the overall radio performance. Hence, please read and follow the requirements and the guidelines as carefully as possible.

FN990 family modules provide four MHF-4 type RF connectors covering the 5G FR1/LTE/WCDMA bands including GNSS and one MHF-4 type RF connector dedicated to GNSS.

Warning: When connecting cellular and GNSS antennas to the module, pay special attention not to damage RF connectors.

Antenna Configuration

Please refer to the picture below for the connector position.

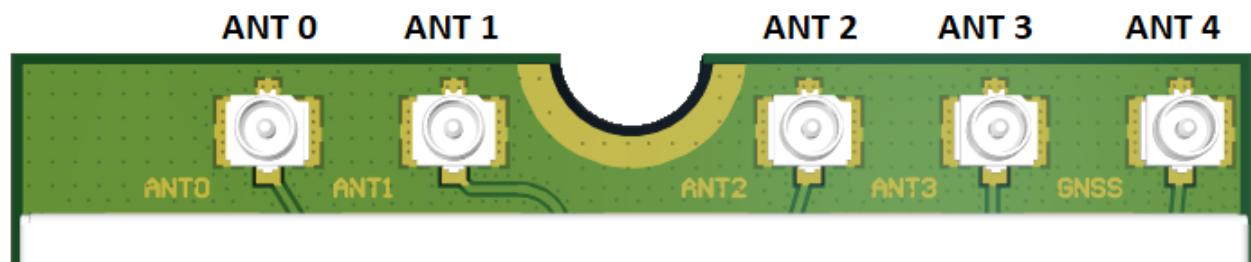


Figure 19: Antenna Configuration

Refer to the following antenna configuration assigned.

Table 39: Antenna Configuration

Antenna port	Technology	Tx	Rx	GNSS
ANT 0	WCDMA	B1, B2, B4, B5, B6, B8, B19	B1, B2, B4, B5, B6, B8, B19	-
	LTE	B1, B2, B3, B4, B5, B7, B8, B12, B13, B14, B17, B18, B19, B20, B25, B26, B28, B30, B34, B38, B39, B40, B41, B66, B71	B1, B2, B3, B4, B5, B7, B8, B12, B13, B14, B17, B18, B19, B20, B25, B26, B28, B29(SDL), B30, B32(SDL), B34, B38, B39, B40, B41, B42, B43, B46(SDL), B48, B66, B71	
	5G NR FR1	n1, n2, n3, n5, n7, n8, n12, n13, n14, n18, n20, n25, n26, n28, n29(SDL), n30, n38, n40, n41, n48, n66, n71, n75(SDL), n76(SDL), n77, n78, n79	n1, n2, n3, n5, n7, n8, n12, n13, n14, n18, n20, n25, n26, n28, n29(SDL), n30, n38, n40, n41, n48, n66, n71, n75(SDL), n76(SDL), n77, n78, n79	
ANT 1	WCDMA	-	-	GPS L1, Galileo E1, Beidou B1, Glonass G1
	LTE	-	B1, B2, B3, B4, B7, B25, B30, B32(SDL), B34, B38, B39, B40, B41, B42, B43, B48, B66	

Antenna port	Technology	Tx	Rx	GNSS
	5G NR FR1	n48, n77, n78, n79	n1, n2, n3, n7, n25, n30, n38, n40, n41, n48, n66, n75(SDL), n76(SDL), n77, n78, n79	
ANT 2	WCDMA	-	B1, B2, B4, B5, B6, B8, B19	-
	LTE	-	B1, B2, B3, B4, B5, B7, B8, B12, B13, B14, B17, B18, B19, B20, B25, B26, B28, B29(SDL), B30, B32(SDL), B34, B38, B39, B40, B41, B42, B43, B46(SDL), B48, B66, B71	
	5G NR FR1	n38, n41	n1, n2, n3, n5, n7, n8, n12, n13, n14, n18, n20, n25, n26, n28, n29(SDL), n30, n38, n40, n41, n48, n66, n71, n75(SDL), n76(SDL), n77, n78, n79	
ANT 3	WCDMA	-	-	-
	LTE	B42, B43, B48	B1, B2, B3, B4, B7, B25, B30, B32(SDL), B34, B38, B39, B40, B41, B42, B43, B48, B66	
	5G NR FR1	n48, n77, n78, n79	n1, n2, n3, n7, n25, n30, n38, n40, n41, n48, n66, n75(SDL), n76(SDL), n77, n78, n79	
ANT 4	GNSS	-	-	GPS L1, Galileo E1, Beidou B1, Glonass G1

Please refer to the tables below for the antenna port on each supported band:

Table 40: 5G NR Sub-6 bands for Antenna Configuration

NR Band				
	ANT0	ANT1	ANT2	ANT3
NR FDD n1	PRx/Tx0	MIMO1	DRx	MIMO2
NR FDD n2	PRx/Tx0	MIMO1	DRx	MIMO2
NR FDD n3	PRx/Tx0	MIMO1	DRx	MIMO2
NR FDD n5	PRx/Tx0	NA	DRx	NA
NR FDD n7	PRx/Tx0	MIMO1	DRx	MIMO2
NR FDD n8	PRx/Tx0	NA	DRx	NA
NR FDD n12	PRx/Tx0	NA	DRx	NA
NR FDD n13	PRx/Tx0	NA	DRx	NA
NR FDD n14	PRx/Tx0	NA	DRx	NA
NR FDD n18	PRx/Tx0	NA	DRx	NA
NR FDD n20	PRx/Tx0	NA	DRx	NA

NR Band				
NR FDD n25	PRx/Tx0	MIMO1	DRx	MIMO2
NR FDD n26	PRx/Tx0	NA	DRx	NA
NR FDD n28	PRx/Tx0	NA	DRx	NA
NR SDL n29	PRx	NA	DRx	NA
NR FDD n30	PRx/Tx0	MIMO1	DRx	MIMO2
NR TDD n38	DRx/Tx1	MIMO1	PRx/Tx0	MIMO2
NR TDD n40	PRx/Tx0	MIMO1	DRx	MIMO2
NR TDD n41	DRx/Tx1	MIMO1	PRx/Tx0	MIMO2
NR TDD n48	DRx	MIMO2/Tx1	MIMO1	PRx/Tx0
NR FDD n66	PRx/Tx0	MIMO1	DRx	MIMO2
NR FDD n71	PRx/Tx0	NA	DRx	NA
NR SDL n75	PRx	MIMO1	DRx	MIMO2
NR SDL n76	PRx	MIMO1	DRx	MIMO2
NR TDD n77	DRx	MIMO2/Tx1	MIMO1	PRx/Tx0
NR TDD n78	DRx	MIMO2/Tx1	MIMO1	PRx/Tx0
NR TDD n79	DRx	MIMO2/Tx1	MIMO1	PRx/Tx0

Table 41: LTE for Antenna Configuration

E-UTRA Band				
	ANT0	ANT1	ANT2	ANT3
LTE FDD B1	PRx/Tx0	MIMO1	DRx	MIMO2
LTE FDD B2	PRx/Tx0	MIMO1	DRx	MIMO2
LTE FDD B3	PRx/Tx0	MIMO1	DRx	MIMO2
LTE FDD B4	PRx/Tx0	MIMO1	DRx	MIMO2
LTE FDD B5	PRx/Tx0	NA	DRx	NA
LTE FDD B7	PRx/Tx0	MIMO1	DRx	MIMO2
LTE FDD B8	PRx/Tx0	NA	DRx	NA
LTE FDD B12	PRx/Tx0	NA	DRx	NA
LTE FDD B13	PRx/Tx0	NA	DRx	NA
LTE FDD B14	PRx/Tx0	NA	DRx	NA
LTE FDD B17	PRx/Tx0	NA	DRx	NA
LTE FDD B18	PRx/Tx0	NA	DRx	NA
LTE FDD B19	PRx/Tx0	NA	DRx	NA
LTE FDD B20	PRx/Tx0	NA	DRx	NA

E-UTRA Band				
LTE FDD B25	PRx/Tx0	MIMO1	DRx	MIMO2
LTE FDD B26	PRx/Tx0	NA	DRx	NA
LTE FDD B28	PRx/Tx0	NA	DRx	NA
LTE SDL B29	PRx	NA	DRx	NA
LTE FDD B30	PRx/Tx0	MIMO1	DRx	MIMO2
LTE SDL B32	PRx	MIMO1	DRx	MIMO2
LTE TDD B34	PRx/Tx0	MIMO1	DRx	MIMO2
LTE TDD B38	PRx/Tx0	MIMO1	DRx	MIMO2
LTE TDD B39	PRx/Tx0	MIMO1	DRx	MIMO2
LTE TDD B40	PRx/Tx0	MIMO1	DRx	MIMO2
LTE TDD B41	PRx/Tx0	MIMO1	DRx	MIMO2
LTE TDD B42	DRx	MIMO2	MIMO1	PRx/Tx0
LTE TDD B43	DRx	MIMO2	MIMO1	PRx/Tx0
LTE SDL B46	PRx	NA	DRx	NA
LTE TDD B48	DRx	MIMO2	MIMO1	PRx/Tx0
LTE FDD B66	PRx/Tx0	MIMO1	DRx	MIMO2
LTE FDD B71	PRx/Tx0	NA	DRx	NA

Table 42: WCDMA for Antenna Configuration

UTRA Band				
	ANT0	ANT1	ANT2	ANT3
WCDMA FDD B1	PRx/Tx0	NA	DRx	NA
WCDMA FDD B2	PRx/Tx0	NA	DRx	NA
WCDMA FDD B4	PRx/Tx0	NA	DRx	NA
WCDMA FDD B5	PRx/Tx0	NA	DRx	NA
WCDMA FDD B6	PRx/Tx0	NA	DRx	NA
WCDMA FDD B8	PRx/Tx0	NA	DRx	NA
WCDMA FDD B19	PRx/Tx0	NA	DRx	NA

8.2 Antenna Connector

The FN990 Family is equipped with a set of 50Ω RF MHF-4 Receptacles from I-PEX 20449-001E.

For more information about mating connectors, please consult <https://www.i-pex.com>

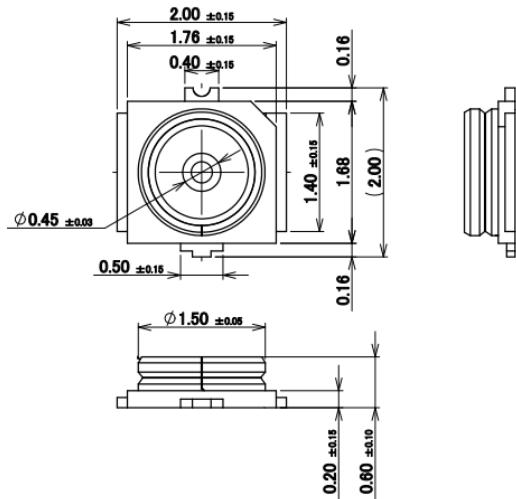
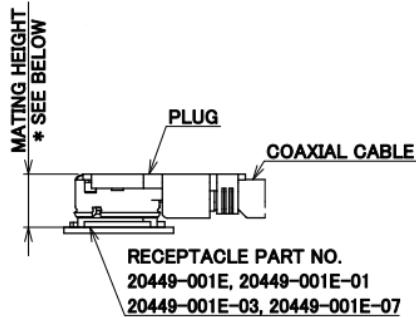


Figure 20: MHF-4 RF connector



*** MATING HEIGHT**
**1.2 MAX. WITH 20611-001R, 20572-001R-08,
 20448-004R-081, 20448-001R-081E**
1.4 MAX. WITH 20565-001R-**
1.7 MAX. WITH 20632-001R-37

MATING CONDITION
WITH MHF 4/MHF 4L PLUG

Figure 21: MHF-4 Receptacle

8.3 Antenna Requirements

Antennas for FN990 Family modules must meet the requirements listed in the table below.

WCDMA/LTE/5G Sub-6 Antenna Requirements

Table 43: WCDMA / LTE / 5G Sub-6 Antenna Requirements

Item	Value
Frequency range	Depending on the frequency band(s) provided by the network operator, the customer must use the most suitable antenna for that/those band(s). The bands supported by the FN990 Family are provided in Section 2.2 Frequency Bands and CA / EN-DC Combinations
Impedance	50 Ohm
Input power	> 24 dBm average power in WCDMA & LTE & 5G Sub-6
VSWR absolute max	<= 10:1

Item	Value
VSWR recommended	<= 2:1

8.4 Antenna Cable

Connecting cables between the module and LTE/Sub-6 antenna must have a 50 Ohm impedance.

If the impedance of the module does not match, RF performance is significantly reduced.

Table 44: Minimize Antenna Cable Recommendations

Item	Value
Impedance	50 Ohm
Max cable loss	Less than 0.5 dB
Avoid coupling with other signals.	

Warning: Impedance of antenna connector and RF cable must be matched to 50 Ohm: mismatch will affect RF performance; especially high insertion loss of RF cable will cause Tx power and Rx sensitivity degradation.

Warning: The FN990 should be located away from noise sources: RF cables and antennas should be installed away from noise sources such as SMPS, USB/PCIe interfaces, etc.

Antenna Installation Guidelines

- Each antenna must be installed with 20dB isolation.
- Install the antenna in a location with access to the network radio signal.
- The Antenna must not be installed inside metal cases.
- The Antenna must be installed according to the antenna manufacturer instructions.
- Antenna integration should optimize Radiation Efficiency. Efficiency values > 50% are recommended on all frequency bands.
- Antenna integration should not perturb the radiation pattern described in the Antenna manufacturer documentation.
- It is preferable to get an omnidirectional radiation pattern.
- To meet the related EIRP limitations, antenna gain must not exceed the values indicated in regulatory requirements, where applicable. The Typical antenna Gain in most M2M applications does not exceed 2dBi.
- If the device antenna is located farther than 20 cm from the human body and there are no co-located transmitters, then the Dejero Labs Inc FCC/IC approvals can be re-used by the end product.
- If the device antenna is located closer than 20 cm from the human body or there are co-located transmitters, then additional FCC/IC testing may be required for the end product (Dejero Labs Inc FCC/IC approvals cannot be reused).

Note: GNSS receive path uses either the dedicated GNSS connector or the shared Secondary AUX antenna connector.

8.5 GNSS Receiver

The FN990 Family integrates a GNSS receiver that can be used either in Standalone or in A-GPS (assisted GPS) mode.

FN990 modems support active GNSS antennas.

Table 45: GNSS Receiver

Item	Value
Frequency range	Wide-band GNSS: 1559 – 1606 MHz recommended GPS: 2.046 MHz BW NB GPS (centered on 1575.42 MHz) Glonass (GLO): ~ 8.3 MHz BW (1597.05 ~ 1606 MHz) BeiDou (BDS): 4.092 MHz BW (1559.05 ~ 1563.14 MHz) Galileo (GAL): 4.092 MHz BW (centered on 1575.42 MHz)
Passive Antenna Gain	1.5 dBi < Gain < 3dBi ¹
Impedance	50 Ohm
External Amplification Gain	7.5 dB < Gain < 26 dB for nominal performance ^{2,3} 1.5 dB < Gain < 7.5 dB for nominal performance ^{4,5}
Supply Voltage	3.1 V

Note:

¹ Configured as AT\$GPSANTPORT= 1 or 2 (Internal LNA Active in either configuration)

² Configured as AT\$GPSANTPORT= 3 (Internal LNA bypassed)

³ Must not exceed 26 dB

⁴ Configured as AT\$GPSANTPORT= 4 (Internal LNA active)

⁵ Must not exceed 7.5 dB

Total gain applied at FN990 RF input connector (Passive Antenna gain + External LNA gain-losses)

GNSS RF Front-End Design

The FN990 Family contains an integrated LNA and front-end SAW filter.

This allows the module to operate properly with a passive GNSS antenna. If the antenna cannot be located near the FN990, then an active antenna (that is, an antenna with a built-in low noise amplifier) can be used with an external dedicated power supply circuit.

GNSS receive path uses either the dedicated GNSS connector #4 or the shared antenna connector #1.

Note: Please refer to the FN990 Family AT Commands Reference Guide, 80691ST11097A for detailed information about GNSS operating modes and GNSS antenna selection.

8.6 GNSS Characteristics

The below table specifies the GNSS characteristics and expected performance:

Table 46: GNSS Characteristics

Parameters		Typical Measurement	Notes
Sensitivity	Tracking Sensitivity	-161 dBm	Standalone or MS-based
	Acquisition	-148 dBm	
	Cold Start	-146 dBm	
TTFF	Hot	1 sec	Open Sky, mean TTFF
	Warm	27 sec	Open Sky, mean TTFF
	Cold	28 sec	Open Sky, mean TTFF
Min update rate		1Hz	
CEP		<2m	Open sky conditions. Standalone

9 MECHANICAL DESIGN

9.1 General

The FN990 Family module was designed to be compliant with a standard lead-free SMT process.

9.2 Finishing & Dimensions

The FN990 Family module's overall dimensions are:

- Length: 52.00 mm
- Width: 30.00 mm
- Thickness: 2.25 mm

9.3 Drawing

This figure shows the mechanical dimensions of the FN990 Family module.

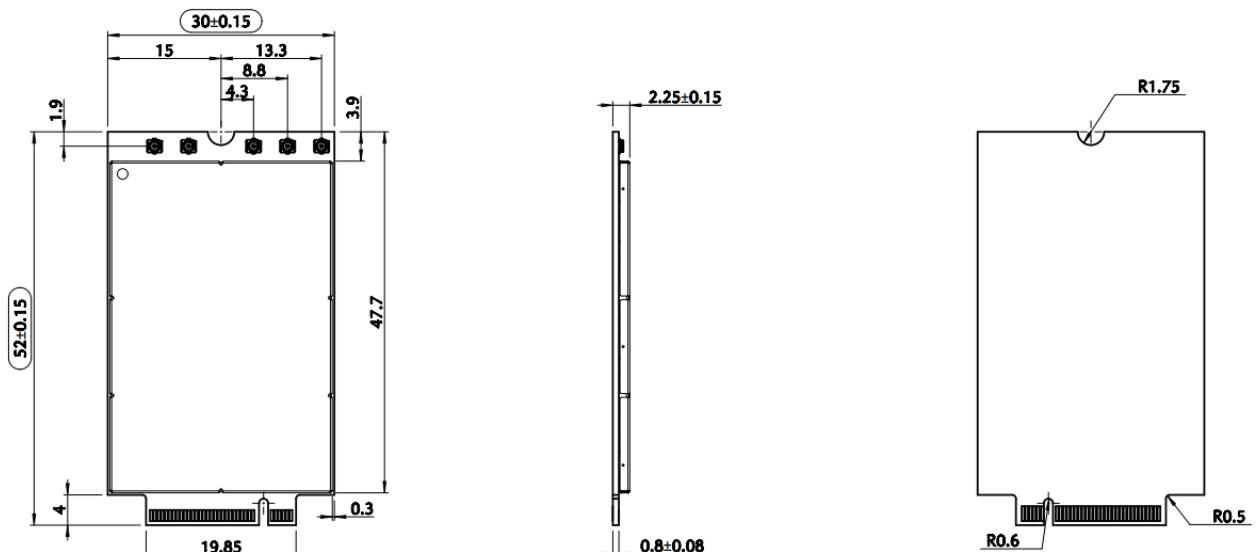


Figure 22: FN990 Family Module Mechanical Dimensions

9.4 Solder Resist Opening Area and Keepout Area

The figure below shows the solder resist opening area and keep-out area location on the FN990 bottom side.

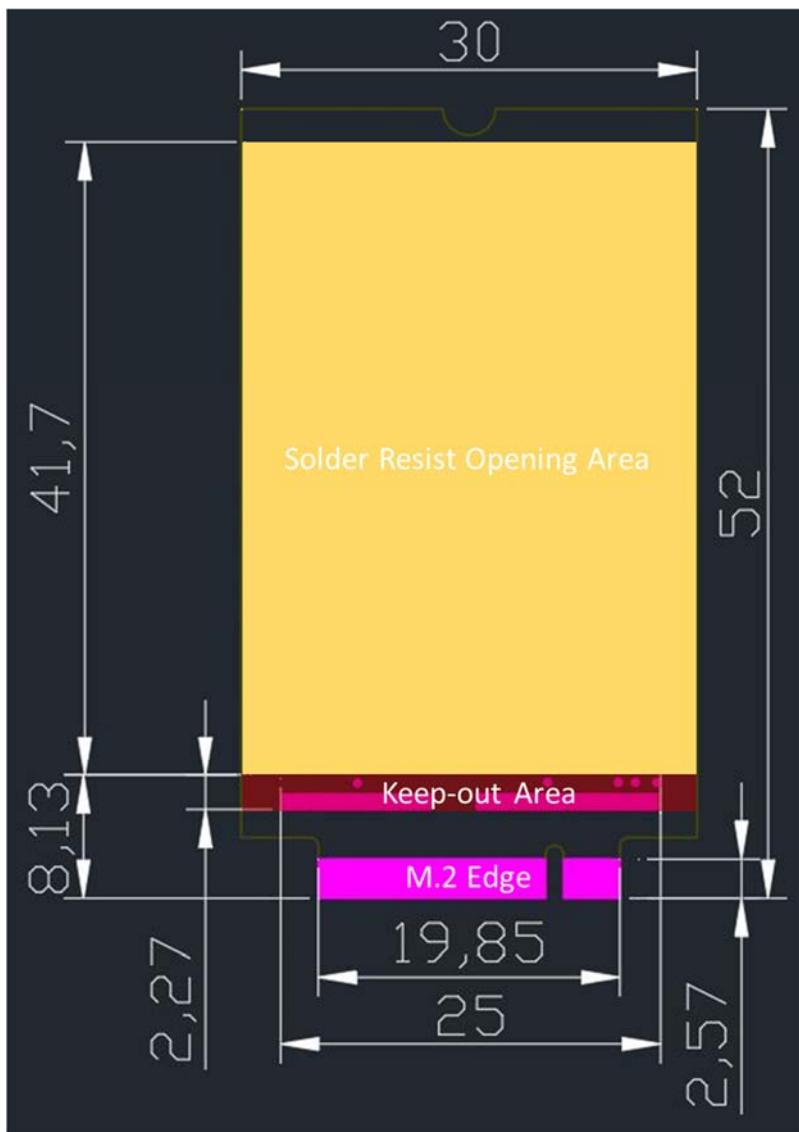


Figure 23: Solder Resist Opening Area and Keep Out Area on Bottom Side

To guarantee the performance and longevity of the end product, the heat generated by the FN990 module must be dissipated.

A large solder-resist opening area (30*41.7 mm) is provided on the bottom of the FN990 modems for better heat dissipation. The addition of a TIM on the back of the FN990 Family is the most important factor from the thermal dissipation point of view.

The recommended TIM size is 29 x 38 x 1.5 mm.

Note: For more information on thermal design, refer to the FN990 Family Thermal Design Guide.

Warning: The keep-out area (30*2.27 mm) on the bottom side is only for debugging purposes. Please do not use this area for hardware design.

10 Application Guide

10.1 Debug the FN990 Family Module in Production

To test and debug the FN990 Family module integration, it is strongly recommended to add test pins on the host PCB for the following purposes:

- Checking the connection between the FN990 Family itself and the application
- Testing the performance of the module by connecting it to an external computer

Depending on the customer application these test pins include, but are not limited to, the following signals:

- FULL_CARD_POWER_N, SYS_RESET_N, W_DISABLE_N, PCIE_WAKE_N
- VPH_PWR, GND
- VREG_L6B_1P8
- USB_D +/-
- USB_SS_TX/RX_M/P
- PCIE_TX/RX_M/P

10.2 Bypass Capacitor on Power Supplies

When a sudden voltage step is asserted to or a cut from the power supplies, the step transition causes effects such as overshoot and undershoot. This abrupt voltage transition can affect the device causing it to fail or to malfunction.

Bypass capacitors are needed to alleviate this behavior, which can appear differently depending on the various applications. Integrators must pay special attention to this issue when they design their application board.

The power lines length and width must be considered carefully, and the capacitors value must be selected accordingly.

The capacitor will also prevent power supply ripple and the switching noise caused in TDMA systems, such as GSM.

Most important, a suitable bypass capacitor must be mounted on the following lines on the application board:

- VPH_PWR

Recommended value:

- 100 uF for VPH_PWR

It must be considered that the capacitance mainly depends on the application board.

Generally, additional capacitance is required when the power line is longer.

Furthermore, if the fast power-down function is used, an additional bypass capacitor should be mounted on the application board.

EMC Recommendations

EMC protection on all FN990 pins should be designed on the application side according to the customer's requirement.

ESD rating on all pins of FN990 Family:

Human Body Model (HBM): +/- 1000 V

Charged Device Model (CDM): +/- 250 V

All antenna pins up to +/- 4 kV

ESD Risk: Do not touch without proper electrostatic protective equipment. The product must be handled with care, avoiding any contact with the pins because electrostatic discharge may damage the product itself.

11 Packaging

11.1 Tray

The FN990 Family modules are packaged on trays of 15 pieces each. These trays can be used in SMT processes for pick & place handling.

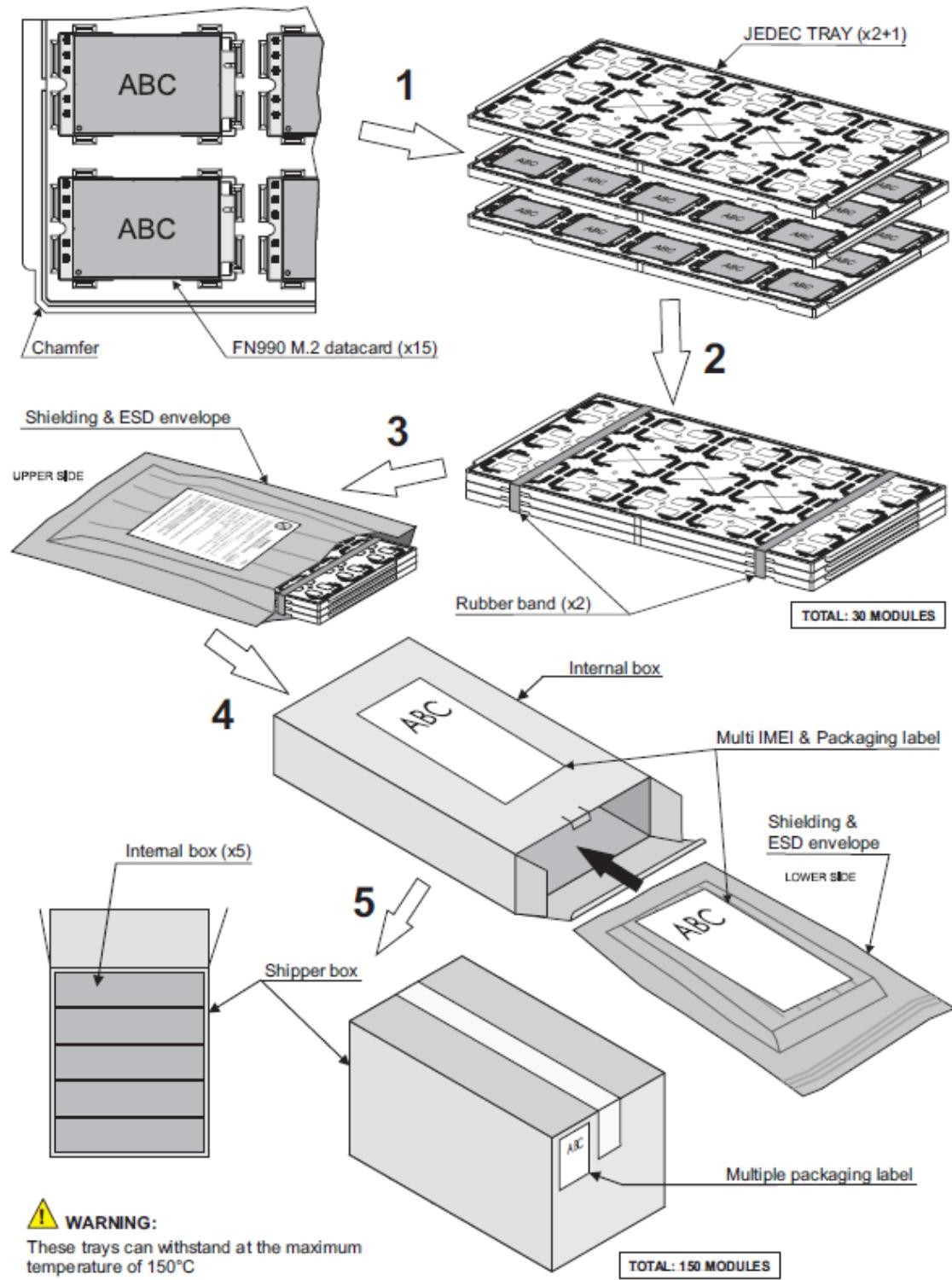


Figure 24: Tray Packaging

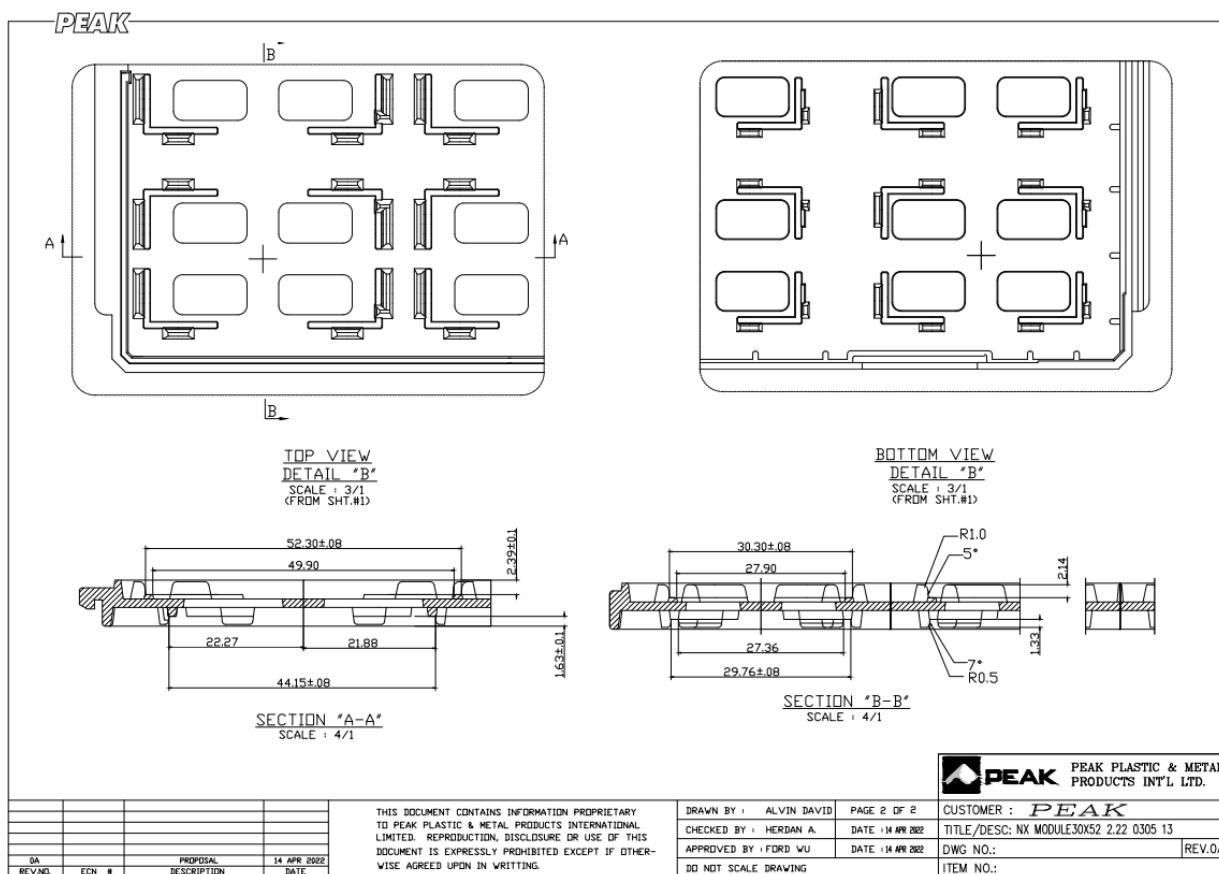
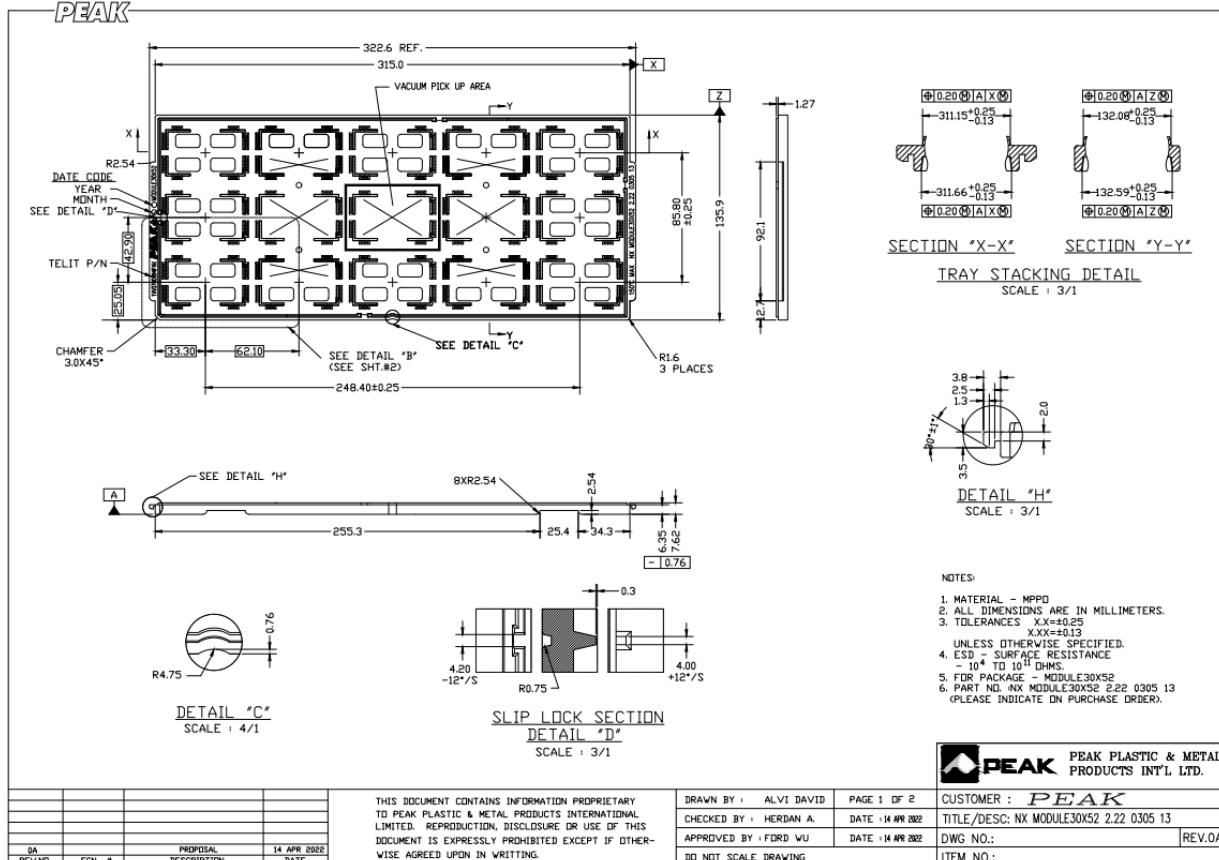


Figure 25: Tray Construction

12 CONFORMITY ASSESSMENT ISSUES

12.1 Approvals Compliance Summary

Table 47: Americas Approvals Compliance Summary

Region	Americas		
Country & Type Approval	BR ANATEL	CA ISED	US FCC
FN990A40-HP		●	●

Table 48: APAC Approvals Compliance Summary

Region	APAC				
Country & Type Approval	AU RCM	CN CCC	JP JRL / JTBL	KR KC	TW NCC
FN990A40-HP			●		

Table 49: EMEA Approvals Compliance Summary

Region	EMEA	
Country & Type Approval	EU RED	UK UKCA
FN990A40-HP	●	●

- The equipment is compliant
- Type approval is in progress
- The equipment is not compliant

12.2 Americas Approvals

USA FCC

FCC Certificates

The FCC Grants can be found here: <https://www.fcc.gov/oet/ea/fccid>

Applicable FCC Rules

Table 50: Applicable FCC Rules

Model	Applicable FCC Rules
FN990A40-HP	47 CFR Part 2, 15, 22, 24, 27, 90, 96

FCC Regulatory Notices

Modification Statement

Dejero Labs Inc has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Wireless Notice

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment and meets the FCC radio frequency (RF) Exposure Guidelines. This transmitter must not be co-located or operate in conjunction with any other antenna or transmitter. The antenna should be installed and operated with a minimum distance of 20 cm between the radiator and your body

FCC Class B digital device notice

This equipment has been tested and found to comply with the limits for a Class B digital device, according to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used per the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by taking one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.

- Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Information for the OEMs and Integrators

The following statement must be included with all versions of this document supplied to an OEM or integrator but should not be distributed to the end user.

1. This device is intended for OEM integrators only.
2. Please see the full Grant of Equipment document for other restrictions

Manual Information to the End User

The OEM integrator should be aware not to provide information to the end-user on how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warming as shown in this manual

Information on test modes and additional testing requirement

The module has been evaluated in mobile stand-alone conditions. For operational conditions other than a stand-alone modular transmitter in a host (multiple, simultaneously transmitting modules or other transmitters in a host), additional testing may be required (collocation, retesting...). If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements of FCC Part 2.1093.

Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only authorized by the FCC for the specific rule parts (for example, FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed. The end product with an embedded module may also need to pass the FCC Part 15 unintentional emission testing requirements and be properly authorized per FCC Part 15.

FCC Antenna info

This radio transmitter has been approved by FCC to operate with the antenna types listed below with the maximum allowable gain indicated. Antenna types not included in this list, with a gain greater than the maximum gain indicated for that type, are strictly prohibited from use with this device.

Table 51: FCC Antenna Type

Model	Antenna Type
FN990A40-HP	Omnidirectional Monopole Antenna

Table 52: Max Antenna Gain for FCC in dBi – WCDMA bands

Max Gain for FCC (dBi)			
UMTS	Max Gain to meet FCC ERP/EIPP and MPE limit	Max Gain to consider the same Frequency with LTE	Max gain allowed
B2	8.5	5.9	5.9
B4	5.5	5.5	5.5
B5	9.9	3.5	3.5

Table 53: Max Antenna Gain for FCC in dBi – LTE bands

Max Gain for FCC (dBi)			
LTE	Max Gain to meet FCC ERP/EIRP and MPE limit	Max Gain to consider EN-DC Active	Max gain allowed
B2	9.0	5.9	5.9
B4	6.0	5.5	5.5
B5	10.4	3.5	3.5
B7	9.0	3.8	3.8
B12	9.7	3.6	3.6
B13	10.2	3.9	3.9
B14	10.2	3.9	3.9
B17	9.7	3.6	3.6
B25	9.0	5.9	5.9
B26	10.4	3.5	3.5
B30	1.0	1.0	1.0
B38	9.0	3.8	3.8
B41	6.5	3.8	3.8
B42	0.5	0.5	0.5
B43	0.5	0.5	0.5
B48	0.5	0.5	0.5

B66	6.0	5.5	5.5
B71	9.5	2.9	2.9

Table 54: Max Antenna Gain for FCC in dBi – NR bands

Max Gain for FCC (dBi)			
NR	Max Gain to meet FCC ERP/EIRP and MPE limit	Max Gain to consider EN-DC Active	Max gain allowed
n2	8.5	5.9	5.9
n5	9.9	3.5	3.5
n7	8.5	3.8	3.8
n12	9.7	3.6	3.6
n13	10.2	3.9	3.9
n14	10.2	3.9	3.9
n25	8.5	5.9	5.9
n26	10.4	3.5	3.5
n30	1.0	1.0	1.0
n38	8.0	3.8	3.8
n41	5.5	3.8	3.8
n41 – PC1.5	4.0	2.3	2.3
n48	0.5	0.5	0.5
n66	5.5	5.5	5.5
n71	9.0	2.9	2.9
n77	2.5	2.5	2.5
n77 – PC1.5	1.0	1.0	1.0
n78	2.5	2.5	2.5
n78 – PC1.5	1.0	1.0	1.0

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Labelling requirements for the host device

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise, the host device must be labelled to display the FCC ID of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as in the below table.

Table 55: Host device FCC Label

Model	Host device FCC label
FN990A40-HP	Contains FCC ID: Y99FN990A40HP

Canada ISED

ISED Database

The products ISED certified can be found here:

Les produits certifiés ISED peuvent être trouvés ici :

[https://sms-
sgs.ic.gc.ca/equipmentSearch/searchRadioEquipments?execution=e1s1&lang=en](https://sms-sgs.ic.gc.ca/equipmentSearch/searchRadioEquipments?execution=e1s1&lang=en)

Applicable ISED Rules / Liste des Règles ISDE Applicables

Table 56: Applicable ISED rules / Règles ISDE applicables

Model	Applicable ISED rules / Règles ISDE applicables
FN990A40-HP	RSS: 102 Issue 5, 130 Issue 2, 132 Issue 4, 133 Issue 6, 139 Issue 4, 140 Issue 1, 192 Issue 5, 195 Issue 2, 199 Issue 4, Gen Issue 5 ICES: 003 Issue 7

ISED Regulatory Notices / Avis réglementaires d'ISDE

Modification Statement / Déclaration de modification

Dejero Labs Inc has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Dejero Labs Inc n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.

Interference Statement / Déclaration d'interférence

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2)

this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux applicables RSS standards d'Industrie Canada. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Radio Exposure Notice / Avis d'exposition radio

This device complies with ISED radiation exposure limits set forth for an uncontrolled environment and meets the RSS-102 of the ISED radio frequency (RF) Exposure rules. Antenna gain must be less than the values reported in the table below:

Le présent appareil est conforme à l'exposition aux radiations FCC / ISED définies pour un environnement non contrôlé et répond aux directives d'exposition de la fréquence de la FCC radiofréquence (RF) et RSS-102 de la fréquence radio (RF) ISED règles d'exposition. Gain de l'antenne doit être ci-dessous:

Table 57: ISED Antenna Type

Modèle	Type d'Antenne
FN990A40-HP	Antenne monopôle omnidirectionnelle

Table 58: Max antenna gain for ISED in dBi / Gain d'antenne max pour ISED en dBi – WCDMA bands

Gain maximum pour ISED (dBi) / Gain maximum pour ISDE (dBi)			
UMTS	Max Gain to meet IC ERP/EIPP and MPE limit	Max Gain to consider the same Frequency with LTE	Max gain allowed
B2	8.5	5.9	5.9
B4	5.5	5.5	5.5
B5	6.6	3.5	3.5

Table 59: Max antenna gain for ISED in dBi / Gain d'antenne max pour ISED en dBi – LTE bands

Gain maximum pour ISED (dBi) / Gain maximum pour ISDE (dBi)			
LTE	Max Gain to meet IC ERP/EIRP and MPE limit	Max Gain to consider EN-DC Active	Max gain allowed
B2	9.0	5.9	5.9
B4	6.0	5.5	5.5
B5	7.1	3.5	3.5

Gain maximum pour ISED (dBi) / Gain maximum pour ISDE (dBi)			
B7	9.0	3.8	3.8
B12	6.6	3.6	3.6
B13	6.9	3.9	3.9
B14	7.0	3.9	3.9
B17	6.7	3.6	3.6
B25	9.0	5.9	5.9
B26	7.1	3.5	3.5
B30	1.0	1.0	1.0
B38	9.0	3.8	3.8
B41	6.5	3.8	3.8
B42	6.0	6.0	6.0
B43	6.0	6.0	6.0
B48	6.5	6.5	6.5
B66	6.0	5.5	5.5
B71	6.5	2.9	2.9

Table 60: Max antenna gain for ISED in dBi / Gain d'antenne max pour ISED en dBi

Gain maximum pour ISED (dBi) / Gain maximum pour ISDE (dBi)			
NR	Max Gain to meet IC ERP/EIRP and MPE limit	Max Gain to consider EN-DC Active	Max gain allowed
n2	8.5	5.9	5.9
n5	6.6	3.5	3.5
n7	8.5	3.8	3.8
n12	6.6	3.6	3.6
n13	6.9	3.9	3.9
n14	7.0	3.9	3.9
n25	8.5	5.9	5.9
n26	7.1	3.5	3.5

n30	1.0	1.0	1.0
n38	8.0	3.8	3.8
n41	5.5	3.8	3.8
n41 - PC1.5	4.0	2.3	2.3
n48	7.5	7.5	7.5
n66	5.5	5.5	5.5
n71	6.0	2.9	2.9
n77	3.0	3.0	3.0
n77 - PC1.5	1.0	1.0	1.0
n78	3.0	3.0	3.0
n78 - PC1.5	1.0	1.0	1.0

NR bands

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.

This equipment must be installed and operated in accordance with provided instructions and the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-users and installers must be provided with antenna installation instructions and consider removing the no-collocation statement.

Cet équipement doit être installé et utilisé conformément aux instructions fournies et la ou les antennes utilisées pour cet émetteur doivent être installées pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doivent pas être co-localisées ou fonctionner en conjonction avec toute autre antenne ou émetteur. Les utilisateurs finaux et les installateurs doivent recevoir les instructions d'installation de l'antenne et envisager de supprimer la déclaration de non-collocation.

Information on test modes and additional testing requirement / Informations sur les modes de test et exigences de test supplémentaires

The module has been evaluated in mobile stand-alone conditions. For operational conditions other than a stand-alone modular transmitter in a host (multiple, simultaneously transmitting modules or other transmitters in a host), additional testing may be required (collocation, retesting...) If this module is intended for use in a portable

device, you are responsible for separate approval to satisfy the SAR requirements IC RSS-102.

Le module a été évalué dans des conditions mobiles autonomes. Pour des conditions de fonctionnement autres qu'un émetteur modulaire autonome dans un hôte (plusieurs modules transmettant simultanément ou d'autres émetteurs dans un hôte), des tests supplémentaires peuvent être nécessaires (colocalisation, retest...) Si ce module est destiné à être utilisé dans un appareil portable, vous êtes responsable de l'approbation séparée pour satisfaire aux exigences SAR IC RSS-102.

Labelling requirements for the host device / Exigences d'étiquetage pour le périphérique hôte

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise, the host device must be labelled to display the IC of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as in the following table.

L'appareil hôte doit être étiqueté comme il faut pour permettre l'identification des modules qui s'y trouvent. L'étiquette de certification du module donné doit être posée sur l'appareil hôte à un endroit bien en vue en tout temps. En l'absence d'étiquette, l'appareil hôte doit porter une étiquette donnant le IC du module, précédé des mots « Contient un module d'émission », du mot « Contient » ou d'une formulation similaire exprimant le même sens, comme en tableau suivant.

Table 61: Host device IC label / Étiquette IC du dispositif hôte

Model / HVIN	Host device IC label / Étiquette IC du dispositif hôte
FN990A40-HP	Contains IC: 12762A-FN990A40HP

CAN ICES-3 (B) / NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

12.3 APAC Approvals

Japan JATE/TELEC

Dejero Labs Inc strongly recommends to customers, deploying the module to Japan, the usage of AT#FWSWITCH command to select the right Japanese carrier profile. The carrier profile has been designed to enable the right 5G NR, LTE, and WCDMA bands and also the required carrier settings.

JRL/JTBL Regulatory Notices

Antenna info

According to Japan regulatory rule, module certification is valid only with the specific antennas registered to and approved by Japan Radio Law (JRL) certified body in relation to module certification. Customers who are going to use modules under JRL are responsible to contact Dejero Labs Inc technical support or sales to get the list of these antennas.

12.4 EMEA Approvals

EU RED

EU Declaration of Conformity

In accordance with the above Approval Compliance Summary table, where applicable (green ball), hereby, Dejero Labs Inc Communications S.p.A declares that the equipment is in compliance with the Directive 2014/53/EU.

The full text of the EU declaration of conformity is available at the following internet address: <https://www.Dejero Labs Inc.com/red>

Text of 2014/53/EU Directive (RED) requirements can be found here:

<https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32014L0053>

RED Antennas

This radio transmitter has been approved under RED to operate with the antenna types listed below with the maximum permissible gain indicated. The usage of a different antenna in the final hosting device may need a new assessment of host conformity to RED.

Table 62: RED Antenna Type

Model	Antenna Type
FN990A40-HP	Omnidirectional Monopole Antenna

Table 63: Max Antenna Gain for RED in dBi – WCDMA bands

Max Gain for RED (dBi)			
UMTS	Ant Gain to meet CE MPE limit	Max Gain to consider same Frequency with LTE	Max gain allowed
B1	11.84	8.7	8.7

B8	8.45	5.3	5.3
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Table 64: Max Antenna Gain for RED in dBi – LTE bands

Max Gain for RED (dBi)			
LTE	Ant Gain to meet CE MPE limit	Max Gain to consider EN-DC Active	Max gain allowed
B1	12.84	8.7	8.7
B3	12.33	9.2	9.2
B7	13.01	9.9	9.9
B8	9.45	5.3	5.3
B20	9.20	6.0	6.0
B28	8.47	5.3	5.3
B34	13.01	9.9	9.9
B38	13.01	6.9	6.9
B40	13.01	7.0	7.0
B41	10.01	6.9	6.9
B42	13.01	9.9	9.9
B43	13.01	9.9	9.9

Table 65: Max Antenna Gain for RED in dBi – NR bands

Max Gain for RED (dBi)			
NR	Ant Gain to meet CE MPE limit	Max Gain to consider EN-DC Active	Max gain allowed
n1	12.84	8.7	8.7
n3	12.33	9.2	9.2
n7	13.01	9.9	9.9
n8	9.45	5.3	5.3
n20	9.20	6.0	6.0
n28	8.47	5.3	5.3
n38	13.01	6.9	6.9
n40	13.01	7.0	7.0

Max Gain for RED (dBi)			
n41	10.01	6.9	6.9
n41 – PC1.5	8.01	4.9	4.9
n77	10.01	7.0	7.0
n77 – PC1.5	8.01	5.0	5.0
n78	10.01	7.0	7.0
n78 – PC1.5	8.01	5.0	5.0

12.5 RoHS, REACH, and WEEE Info

RoHS Info

Any requests on information related to RoHS certifications can be addressed to info@Dejero.com.

REACH Info

Any requests on information related to REACH certifications can be addressed to info@Dejero.com.

WEEE Info



This symbol means that according to local laws and regulations your product and/or its battery shall be disposed of separately from household waste. When this product reaches its end of life, take it to a collection point designated by local authorities. Proper recycling of your product will protect human health and the environment.

Table 66: Acronyms and Abbreviations

Acronym	Definition
CA	Carrier aggregation
CLK	Clock
CMOS	Complementary Metal – Oxide Semiconductor
DTE	Data Terminal Equipment
EN-DC	E-UTRA – NR Dual Connectivity
ESR	Equivalent Series Resistance
E-UTRA	Evolved UMTS Terrestrial Radio Access
FDD	Frequency Division Duplex
GPIO	General Purpose Input Output
HS	High Speed
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input Output
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
LTE	Long Term Evolution
NR	New Radio
PCB	Printed Circuit Board
PCIE	Peripheral Component Interconnect Express
RTC	Real-Time Clock
SDL	Supplementary Down Link
SIM	Subscriber Identification Module
SOC	System-on-Chip
SMPS	Switching Mode Power Supply
TDD	Time Division Duplex
TTSC	Dejero Labs Inc Technical Support Center
UART	Universal Asynchronous Receiver Transmitter
UMTS	Universal Mobile Telecommunication System
USB	Universal Serial Bus
VNA	Vector Network Analyzer
VSWR	Voltage Standing Wave Radio
WDMA	Wideband Code Division Multiple Access
CA	Carrier aggregation
CLK	Clock
CMOS	Complementary Metal – Oxide Semiconductor
DTE	Data Terminal Equipment

Acronym	Definition
EN-DC	E-UTRA – NR Dual Connectivity
ESR	Equivalent Series Resistance