FCC ID: Y7J5565B01

Technical Description:

The equipment under test (EUT) is a transceiver for a Bluetooth wireless Optical Mouse with Calculator/numeric keypad device. The EUT is energized by two AAA size batteries. The EUT can be connected with both “PC” and Macintosh hardware for use across various different computer models via Bluetooth protocol; it can be used as a wireless Calculator/numeric keypad for data entry.

Operating Frequency Band: 2402MHz ~ 2480MHz
Channel spacing: 1MHz
Total number of channel: 79
Sensitively: down to –84dBm
Spread Spectrum: FHSS
Modulation Method: GFSK

The functions of main ICs are mentioned as below;

1) BP2042S is a Bluetooth Module, including the BCM2042 and M24C128. BCM2042 acts as a Bluetooth Chip performs Bluetooth function, M24C128 acts as EEPROM (external memory).

2) IC1 acts as MCU for system.
3) U7 acts as Mouse Sensor.

Data Sheet

BCM2042

Single-Chip Bluetooth Transceiver for Wireless Input Devices

GENERAL DESCRIPTION

The Broadcom BCM2042 is a Bluetooth® 2.0 compliant, stand-alone baseband processor with an integrated 2.4-GHz Transceiver. The device is ideal for use in wireless input devices including keyboards, mice, joysticks, and game controllers. Built-in firmware adheres to the Bluetooth Human Interface Device (HID) profile.

The BCM2042 radio has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4-GHz unlicensed ISM band. It is fully compliant with Bluetooth radio specification V2.0.

The single-chip bluetooth transceiver is a monolithic component implemented in a standard digital CMOS process, and requires minimal external components to make a fully compliant Bluetooth device. The BCM2042 is available in three package options: an 88-pin BGA, a 100-pin BGA, and a 120-pin BGA.

APPLICATIONS

- Wireless keyboards
- Wireless pointing devices: mice, trackballs
- Game controllers
- Joysticks
- Point of sale (POS) input devices
- Remote controls and remote sensors

FEATURES

- Integrated switching regulator to support external sensor to reduce external BOM cost.
- Bluetooth specification version 2.0 compatible.
- Bluetooth HID profile version 1.0 compliant.
- Supports AFH
- Excellent receiver sensitivity
- On-chip ROM eliminates dedicated flash memory chip, significantly lowering system bill-of-materials.
- On-chip support for common keyboard and mouse interfaces eliminates external processor.
- Programmable key-scan matrix interface, up to 8x20 key-scanning matrix.
- 3-axis quadrature signal decoder.
- On-chip support for Serial Peripheral Interface (SPI). Applicable to master mode only.
- Broadcom Serial Communications Interface (compatible with I²C™ slaves).
- Programmable output power control meets Class 2 or Class 3 requirements.
- Class-1 operation support with external PA and T/R switch.
- Integrated 8051 microprocessor core.
- On-chip Power On Reset (POR).
- On-chip software control power management unit.
- Three package types available:
  - 120-pin BGA package—9 mm x 10 mm
  - 100-pin BGA package—9 mm x 9 mm
  - 88-pin BGA package—9 mm x 8 mm

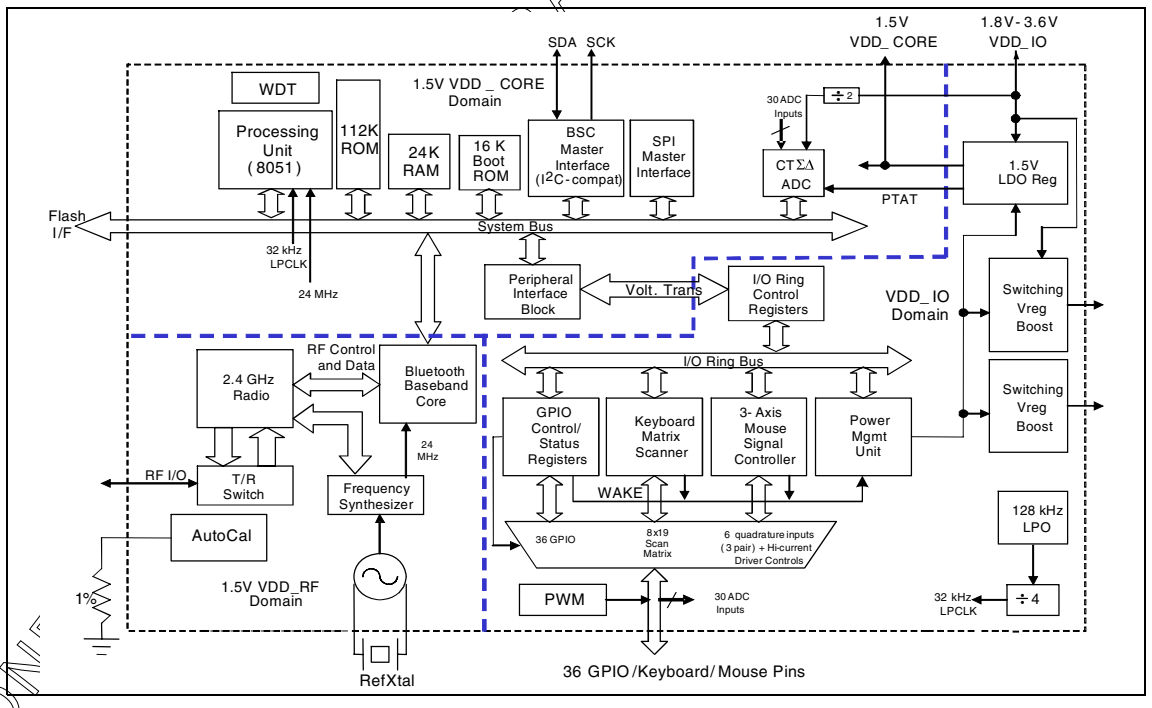

Figure 1: Functional Block Diagram

REVISION HISTORY

Revision	*Date*	*Change Description*
MCS2042-DS04-R	2/4/09	**Updated:** • "On-Chip Switching Regulators" on page 16 • Table 4, "Maximum Electrical Rating," on page 29 • Table 5, "Power Supply," on page 30
MCS2042-DS03-R	12/3/08	**Updated:** • Table 4, "Maximum Electrical Rating," on page 29. • Table 7, "Typical Current Consumption," on page 30. • Table 16, "Ordering Information," on page 40.
MCS2042-DS02-R	01/14/08	**Added:** • New 100-pin BGA to the following sections: • Cover page General Description and Features paragraphs • Table 2 on page 20 (new pin descriptions) • Table 3 on page 22 (new GPIO pin descriptions) • Figure 13 on page 28 (new ball pin diagram) • Figure 20 on page 38 (new mechanical drawing) **Updated:** • Table 4 on page 29 (with modified electrical characteristics) • Table 5 on page 29 • Table 16 on page 40 (with new ordering information) • Figure 2 on page 2 (by removing the undesired background grid) • Figure 6 on page 14 (by removing unsdesired background grid and sharpening figure text) • "Examples" on page 18

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Revision	*Date*	*Change Description*
MCS2042-DS01-R	12/07/07	**Updated:** • Figure 1, “Functional Block Diagram,” on page i • “Examples” on page 18 • Figure 8, “SW1 Used As Boost, SW2 Not Used,” on page 18 • Figure 9, “SW1 Not Used, SW2 Used As Buck,” on page 19 • Table 1, “Pin Description,” on page 20 • Table 3, “Maximum Electrical Rating,” on page 28 • Table 4, “Power Supply,” on page 28 • Table 6, “Typical Current Consumption,” on page 29 • Table 15, “Ordering Information,” on page 38
MCS2042-DS00-R	08/16/07	Initial release

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Section 1: Functional Description

INTEGRATED RADIO TRANSCEIVER

The BCM2042 has an integrated radio transceiver that has been optimized for use in 2.4-GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4-GHz unlicensed ISM band. It is fully compliant with Bluetooth Radio Specification v1.2 and meets or exceeds the requirements to provide the highest communication link quality of service.

TRANSMITTER PATH

The BCM2042 features a fully integrated zero IF transmitter. The baseband transmit data is digitally GFSK modulated in the modem block and up-converted to the 2.4-GHz ISM band in the transmitter path, which contains signal filters, an I/Q up-converter, an output power amplifier (PA), and RF filters.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Power Amplifier

The fully integrated PA provides a maximum output signal level of +4 dBm using a highly linearized, temperature compensated design. This gives the user greater flexibility in the type of front end matching and filtering to use with the BCM2042. Due to the linear nature of the PA combined with some integrated filtering, no external filters are required for meeting Bluetooth and regulatory harmonic and spurious requirements.

RECEIVER PATH

The receiver path uses a low IF scheme to down-convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high order on-chip channel filtering to ensure reliable operation in the noisy 2.4-GHz ISM band. The front end topology with built-in out-of-band attenuation enables the BCM2042 to be used in most applications with no off chip filtering.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the BCM2042 provides an Receiver Signal Strength Indicator (RSSI) signal to the baseband so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/sec) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The BCM2042 uses an internal RF and IF loop filter, which only requires one external capacitor.

Calibration

The BCM2042 radio transceiver features an automated calibration scheme that is fully self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration, which accounts for process and temperature variations, optimizes the performance of all major circuit blocks within the radio. The gain and phase of all relevant filter blocks, amplifier blocks, and matching circuits are calibrated. Calibration occurs in the background during normal operation and during LO frequency hop setting times.

Internal Regulator

To reduce the external BOM, the BCM2042 has an integrated 1.5V Low Dropout (LDO) regulator to provide power to the digital and RF circuits. This regulator operates from a 1.7V to 3.6V input supply with less than 50 mV of maximum dropout voltage at full load.

A ferrite bead may be needed between the digital and RF supply pins to isolate noise coupling and suppress the noise into the RF circuits. For optimal performance, it is best to include a low-pass filter between the digital and RF supply pins; a pi filter circuit with two shunt caps and one 0603 ferrite bead will suffice. Figure 2 illustrates a sample LDO filter.

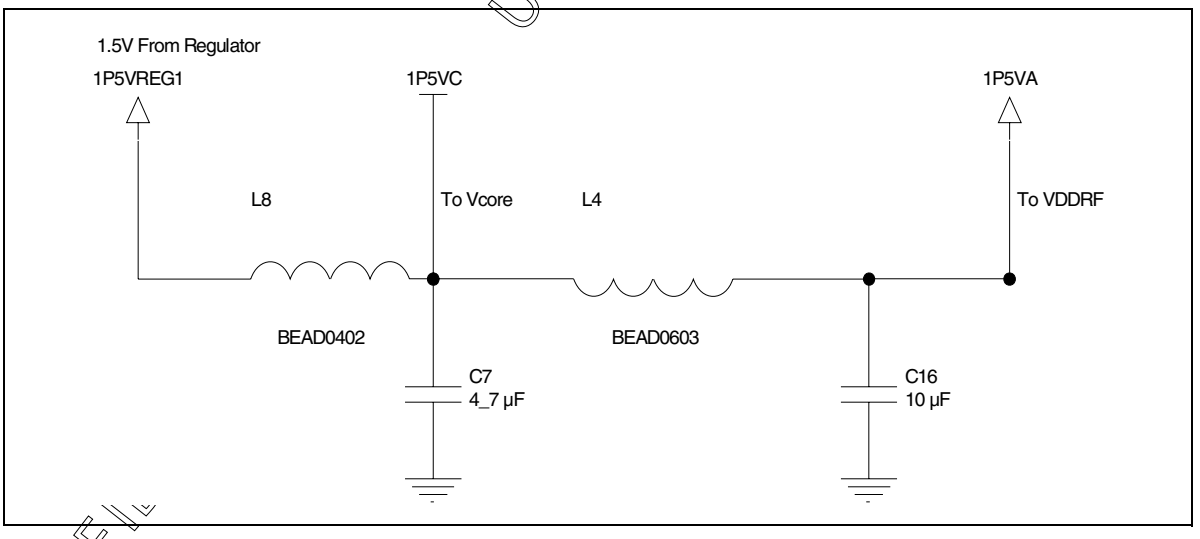


Figure 2: LDO Filter

MICROPROCESSOR UNIT

The Microprocessor Unit (µPU) runs software from the Link Control (LC) layer, up to the Host Controller Interface (HCI). The microprocessor is an enhanced performance 8051 microcontroller. The µPU also consists of one UART port, 2 KB of internal register RAM, 24 KB of internal SRAM, 112 KB of application ROM, and 16K of boot-ROM.

An external EEROM up to 32 KB in size may be connected to customize the operation of the BCM2042 for a particular application. The EEPROM may also contain patch-code to modify application behavior, or to fix any bugs which may exist in the ROM code.

The 8051 core is object code compatible with the industry standard 8051 microcontroller.

EXTERNAL MEMORY INTERFACE (120-PIN PACKAGE ONLY)

The memory interface (available only on the 120-pin package) allows 8051 microcontroller accesses to two types of 8-bit wide external memory: Flash memory and SRAM. The interface can access 128 KB (1 Mbit) of external Flash memory, 128 KB of external SRAM with no bank switching required, or access 256 KB (2 Mbit) of Flash without access to SRAM.

When using external Flash, 32 KB of the Flash may be used to contain configuration and patch-code, eliminating the need for an external EEPROM. When using a 256 KB (2 Mbit) or larger Flash, over-the-air firmware updates can be supported.

BLUETOOTH BASEBAND CORE

The Bluetooth Baseband Core (BBC) implements all of the time critical functions required for high performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules Asynchronous Connectionless Link TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Receive Functions: Symbol timing recovery, data de-framing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data de-whitening.
- Transmit Functions: Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening.

FREQUENCY HOPPING GENERATOR

The frequency hopping sequence generator selects the correct hopping channel number depending on the Link Controller state, Bluetooth clock, and the device address.

ENCRYPTION

The encryption key and the encryption engine are implemented using dedicated hardware to reduce software complexity and provide minimal intervention from the processor.

LINK CONTROL LAYER

The Link Control Layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the Link Control Unit (LCU). This layer consists of the Command Controller that takes commands from the software, and other controllers that are activated or configured by the Command Controller to perform the Link Control tasks. Each task performs a different state in the Bluetooth Link Controller. STANDBY and CONNECTION are the two major states. In addition, there are seven substates:

- PAGE
- PAGE SCAN
- INQUIRY
- INQUIRY SCAN
- PARK
- SNIFF
- HOLD

ADAPTIVE FREQUENCY HOPPING

The BCM2042 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency hop map.

FAST CONNECTION

The BCM2042 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 1.2 page and inquiry procedures and are designed to be forward compatible to Bluetooth version 1.2 extension fast connection mode.

BROADCOM SERIAL COMMUNICATIONS INTERFACE

The BCM2042 provides a 2-pin master Broadcom Serial Communications (BSC) interface which can be used to retrieve configuration information from an external EEPROM, or to communicate with peripherals such as track-ball or touch-pad modules, and motion tracking ICs used in mice. The BSC interface is compatible with I^2C slave devices. The BSC does not support multi-master capability or flexible wait-state insertion by either master or slave devices.

Listed below are the transfer clock rates supported by the BSC:

- 100 kHz
- 400 kHz
- 800 kHz[1]
- 1 MHz[2]

Listed below are the transfers supported by the BSC:

- Read (up to 8 bytes can be read)
- Write (up to 8 bytes can be written)
- Read-then-Write (up to 8 bytes can be read and up to 8 bytes can be written)
- Write-then-Read (up to 8 bytes can be written and up to 8 bytes can be read)

Transfers are performed under hardware control, requiring minimal setup and supervision by firmware.

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins which are tolerant to inputs as high as 3.6V. Pull-up resistors external to the BCM2042 are required on both SCL and SDA for proper operation.

CLOCK FREQUENCIES

The BCM2042 is set with crystal frequency of 24 MHz. This default frequency may be modified by an external EEPROM or Flash. On boot-up the clock frequency is read from the EEPROM or Flash, and used to initiate device operation.

EXTERNAL CLOCK CONNECTION

The external clock signal may be connected to the XTAL IN pin on the BCM2042. If the external clock signal is connected to the XTAL IN pin, it is recommended that a 1000 pF DC blocking capacitor is used in series with the XTAL IN pin. Figure 3 illustrates the proper external clock connection. The amplitude of the external clock signal should be greater than 700mV p-p, but should not exceed VDD_RF.

Note: Any external clock used with the BCM2042 must be accurate to ± 20 ppm.

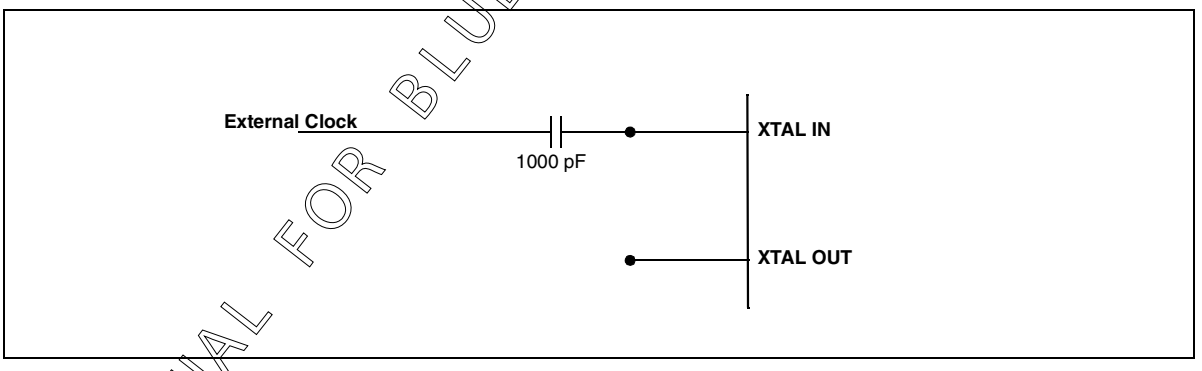


Figure 3: Recommended External Clock Connection

1. Not a standard I²C-compatible speed.
2. Compatibility with high-speed I²C-compatible devices is not guaranteed.

CRYSTAL OSCILLATOR

The crystal oscillator requires a crystal with an accuracy of ±20 ppm as defined by the Bluetooth specification. The crystal requires two external tuning capacitors. Refer to Figure 4 for the recommended configuration for crystals that present a 12 pF load. Refer to Figure 5 for the recommended configuration for crystals that present a 10 pF load. Refer to Table 1 for the recommended Crystal Oscillator specification.

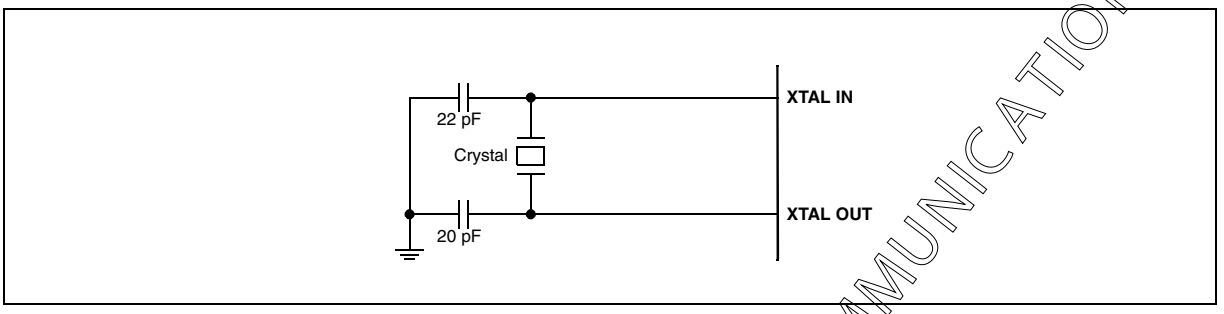


Figure 4: Recommended Oscillator Configuration – 12 pF Load Crystal

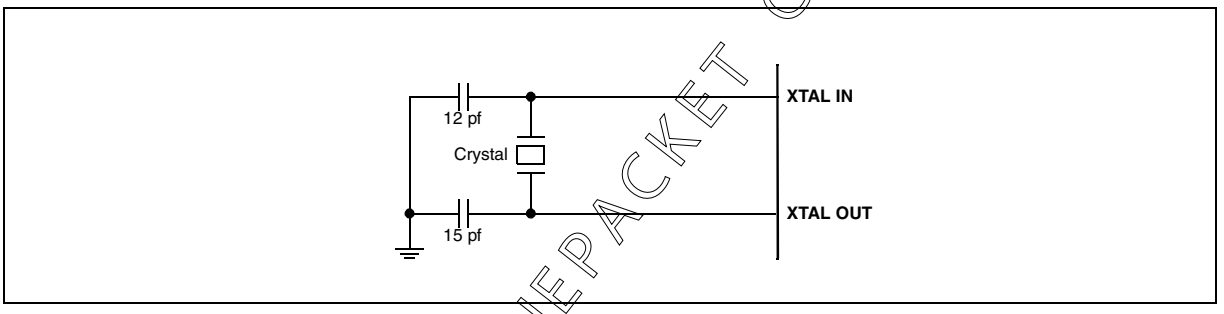


Figure 5: Recommended Oscillator Configuration – 10 pF Load Crystal

Table 1: Recommended Crystal Oscillator Specification

Parameter	*Value*
Tolerance	(+25°C) 10 ppm
Temperature stability	10 ppm
Operating temperature range	–20°C to +60°C
ESR	100Ω
Drive level	10 µW (100 µW max.)
Storage temperature	–40°C to +85°C

GPIO PORT

The BCM2042 has a total of 36 General Purpose I/Os (GPIOs) in 88-pin, 100-pin, and 120-pin packages. All I/O are 3.3V tolerant, CMOS, push-pull, programmable pull-ups/pull-downs, programmable Schmitt trigger, programmable slew rate, and programmable drive strength. The GPIOs are grouped into five different ports.

The following describes the functions of each port.

PORT 0

P0[7:0] consists of eight pins. Each pin is bidirectional, and has 2 mA push-pull capability. All pins can be programmed to wake on change. Each pin can be individually configured as key-scan row input KSI[7:0]. The P0[7:2] can be configured as mouse quadrature inputs.

P0[1:0] can be programmed as input channels for the BCM2042 on-chip Analog-to-Digital Converter (ADC).

PORT 1

P1[7:0] consists of eight pins. Each pin is bidirectional, and has 2 mA push-pull capability. Each pin can be individually configured as key-scan column output (KSO).

P1[7:0] can be programmed as input channels for the BCM2042 on-chip ADC.

PORT 2

P2[7:0] consists of eight pins. Each pin is bidirectional, and has 2 mA push-pull capability. Each pin can be individually configured as KSO.

P2[5:4] are pulled down at reset, and can be reprogrammed by firmware post initialization.

P2[6:7] are pulled up at reset, and can be reprogrammed by firmware post initialization.

P2[7:0] can be programmed as input channels for the BCM2042 on-chip ADC.

PORT 3

P3[5:0] consists of six pins.

P3[1:0] each pin is open-drain bidirectional, and provides 2 mA push-pull capability. Each pin can be individually configured as KSO. Each pin will default to output LOW at reset if TMC=1, and can be reprogrammed by firmware post-initialization.

P3[3:2] can also be individually configured as key-scan column output.

P3[5:2] each pin is bidirectional, and provides 16 mA push-pull capability. Each pin can be configured as optics control for mouse quadrature signals. Each pin can also be configured as PWM control output signals.

P3[4:5] are pulled up at reset, and can be reprogrammed by firmware post initialization.

P3[4] for Class I applications, this GPIO can be programmed to control the external power amplifier ramping time.

P3[5:4] can be programmed as input channels for the BCM2042 on-chip ADC.

PORT 4

P4[5:0] each pin is bidirectional with 2 mA drive capability. Each pin can be configured as alternate mouse quadrature input. They can also be configured as quadrature input pair (e.g., scroll wheel or volume knob on keyboard).

P4[0] can be use for external regulator control if TMC=1: high for enable, low for disable at reset, and can be reprogrammed by firmware post initialization

P4[0] for Class I applications, this pin is programmed to enable/disable external power amplifier and T/R switch for receive mode.

P4[1] this pin is pulled down at reset. For Class I applications, it is programmed to control the external T/R switch for transmit mode.

P4[4] is pulled up at reset.

P4[5] is pulled down at reset.

P4[5:0] can be programmed as input channels for the BCM2042 on-chip ADC.

KEYBOARD SCANNER

The Keyboard Scanner is designed to autonomously sample keys and store them into buffer registers without the need for the host microcontroller to intervene.

The scanner has the following features:

- Ability to turn off its clock if no keys pressed
- Sequential scanning of up to 160 keys in an 8 x 20 matrix
- Programmable number of columns from 1 to 20
- Programmable number of rows from 1 to 8
- 16-byte key-code buffer (can be augmented by firmware)
- 128-kHz clock—allows scanning of full 152-key matrix in about 1.2 ms
- N-key roll-over with selective 2-key lockout if ghost is detected
- Keys are buffered until host microcontroller has a chance to read it, or until overflow occurs
- Hardware debouncing and noise/glitch filtering
- Low power consumption. Single-digit µA-level sleep current

THEORY OF OPERATION

The key-scan block is controlled by a state machine with the following states:

Idle

The state machine begins in the idle state. In this state, all column outputs are driven high. If any key is pressed, a transition occurs on one of the row inputs. This transition causes the 128-kHz clock to be enabled (if it is not already enabled by another peripheral), and the state machine to enter the scan state. Also in this state, an 8-bit row-hit register and an 8-bit key-index counter is reset to 0.

Scan

In the scan state, a row counter counts from 0 up to a programmable number of rows minus 1. Once the last row is reached, the row counter is reset and the column counter is incremented. This cycle repeats until the row counter and column counters are both at their respective terminal count values. At the point, the state machine moves into the Scan-End state.

As the keys are being scanned, the key-index counter is incremented. This value is the value compared to the modifier key-codes stored, or in the key-code buffer if the key is not a modifier key. It can be used by the microprocessor as an index into a look-up table of usage codes.

Also, as the n-th row is scanned, the row-hit register is ORed with the current 8-bit row input values if the current column contains 2 or more row hits. During the scan of any column, if a key is detected at the current row, and the row-hit register indicates that a hit was detected in that same row on a previous column, then a ghost condition may have occurred, and a bit in a status register is set to indicate this.

Scan-End

In this state, it is determined if any keys were detected while in the Scan State. If so, the state machine returns to the Scan state. If not, the state machine returns to the Idle state, and the 128-kHz clock request signal is made inactive.

The microcontroller can poll the key status register.

Outputs:

KSO[19:0]—Key scanning outputs (Columns). Use GPIO ports: P3[3:0]; P2[7:0]; P1[7:0] 20 ports total; programmable.

KEYDET—Key press detected (connected to system power management unit to wake system from deep sleep if enabled).

Inputs:

KSI[7:0]—Key scanning inputs (Rows). Use GPIO ports: P0[7:0]; programmable.

Control Registers:

MODKEYn[7:0]—Key index of n-th modifier key, where n = 0 to 7.

RCTC[7:0]—Row and column terminal counts. Default: 0x00.

- RCTC[2:0] = Number of rows to scan minus 1.
- RCTC[7:3] = Number of columns to scan minus 1 (Only 0 to 19 valid).

KSCTRL0[7:0]—Control register for key scanning block 0.

- KSCTRL0[0]—Setting this bit enables the key-scan block. If it is cleared, the key-scan block does not operate, and will never enable the 128-kHz clock
- KSCTRL0[1]—Freeze keyscan clock for FW reading the H/W status. The typical latency for freeze is 2.5 cycle of the 128-kHz clock ~ 19.5 us.
  Note: the clock in the keyscan module in BCM2042 is not stopped when the freeze bit is set.
- KSCTRL0[2]—This bit enables ghost detection for keyscan.
- KSCTRL0[3]—This bit enables the keyscan block to wake the system if key is detected.

KSCTRL1[7:0]—Control register for key scanning block 1.

- KSCTRL1[7]ksi_drv_high—When in keyboard application, this bit enables the KSI rows to be outputs and driven high to accelerate pull-up resistor effect for avoiding false key detection because of column ll.
- KSCTRL1[6]pull_high—Used to pull the columns high after each column scan to alleviate slow rise-time due to a large key matrix capacitance; default is off.
- KSCTRL1[5:4]rc_ext[1:0]—Programmable idle duration between column scans. For example, when rc_ext[1:0] = 1, it provides one clock cycle idle time of no column scan. This is to alleviate the problem of slow RC delay on some of the keyboard designs. The valid values for rc_ext are 1, 2, and 3 (default)
- KSCTRL1[0]kysclk_stayon—The keyscan clock will stay on when set, otherwise, the clock will be gated off of the Multi-Interface Agent when no activity is pending.

Status Registers

KSTAT[7:0]—Status Register.

- KSTAT[0]clkrc_freezed—Firmware needs to poll this bit when trying to access or read the internal registers. When this bit is high, the freeze (bit 1 of the ksctl_adr register) is successful. Read access may proceed, otherwise, firmware has to wait and poll this bit until it is high. This is readable by the uP.
- KSTAT[2]keyfifo_set—Indicates that the there is an event recorded in the key event FIFO. Due to the possibility of simultaneous accesses by both the firmware and hardware, the value of this register needs to be confirmed with multiple reads.
- KSTAT[3]FIFO overflow—The 16-bytes key event FIFO overflows; more than 16 keys are pressed during the current scan interval.
- KSTAT[4]ghost_det—Ghost condition is detected. A marker 0xF5 is inserted in the event FIFO when ghost is detected; bit 2 of the ksctl register has to be enabled.

MOUSE QUADRATURE SIGNAL DECODER

The Mouse signal decoder is designed to autonomously sample two quadrature signals commonly generated by opto-mechanical mouse apparatus.

The decoder has the following features:

- Three pairs of inputs for X, Y, and Z (typical scroll wheel) axis signals, and two options:
  - For X axis you can chose P0_2 or P4_0 as X0 and P0_3 or P4_1 as X1.
  - For Y axis you can chose P0_4 or P4_2 as Y0 and P0_5 or P4_3 as Y1.
  - For Z axis you can chose P0_6 or P4_4 as Y0 and P0_7 or P4_5 as Y1.
- Control of up to four external high current GPIOs to power external optoelectronics:
  - Turn-on and turn-off time can be staggered for each HC-GPIO, to avoid simultaneous switching of high currents, and to avoid having multiple high-current devices on at the same time.
  - Sample time can be staggered for each axis.
  - Sense of the control signal can be active-high or active-low.
  - Control signal may be configured to be tri-stated for off condition, or driven high or low, as appropriate.

THEORY OF OPERATION

The mouse decoder block has at its core a 16-bit counter. As long as the mouse decoder is enabled, this counter continuously counts until it matches a terminal count set in the SCANPH and SCANPL registers, at which point it resets to 0 and repeats the cycle. The values of the other control registers control the point during the scan cycle at which certain events take place, including the toggling of GPIO signals or the sampling of the count values.

The GPIO signals may be used to control such items as LEDs, external ICs which may emulate quadrature signals, photodiodes and photodetectors.

Outputs:

QHCO[3:0]—four high current (up to 16 mA each @ 3V) general purpose I/O pins P3[5:2]

MOTDET—Motion detected (connected to system power management unit to wake system from deep sleep if enabled)

Inputs:

QDX[1:0] = quadrature inputs for X axis

QDY[1:0] = quadrature inputs for Y axis

QDZ[1:0] = quadrature inputs for Z axis

Control Registers:

QCTRL[7:0]—Quadrature decoder control

- QCTRL[0]—Setting this bit enables the quadrature block. If it is cleared, the quadrature block does not operate, and the 128-kHz clock is never enabled.

- QCTRL[7]—Setting this bit enables the quadrature block to wake the system if motion is detected on any of the three axes.

SCANPL[7:0] and SCANPH[15:8]—Length of scan period in units of 128-kHz clock cycles.

- Scan period can be adjusted from 0 to 655.350 ms. Example values:
  - 51 for BUSY mode (400 µs)
  - 128 for IDLE mode (1 ms)
  - 12,800 for SUSPEND mode (100 ms)
- OPTCNT[7:0]—controls register for the optical control signals
- OPTCNT[1:0]—controls optical control signal 0
  - 00 = Signal is active high, with tri-state when off (emulates open-source)
  - 01 = Signal is active high
  - 10 = Signal is active low, with tri-state when off (emulates open-drain)
  - 11 = Signal is active low
- OPTCNT[3:2] = as above, for optical control signal 1
- OPTCNT[5:4] = as above, for optical control signal 2
- OPTCNT[7:6] = as above, for optical control signal 3

OPTONTn[7:0]—n-th optical on-time control, where n is 0 to 3.

- This register controls the time in units of 128-kHz clock cycles for which one of the high-current GPIOs is left on during the sampling of the a mouse signal, relative to the start of a scan period.

OPTOFFTn[7:0]—n-th optical off-time control, where n is 0 to 3.

- This register controls the time in units of 128-kHz clock cycles for which one of the high-current GPIOs is left off during the sampling of the a mouse signal, relative to the start of a scan period.

SAMPTn[7:0]—n-th sample time control, where n is 0 to 2.

- This register controls the time at which a sample is taken for the n-th axis. This time is specified in units of 128-kHz clock cycles relative to the start of the scan period.

Status Registers:

QSTAT[7:0]—Status register for quadrature block.

- QSTAT[0]—This bit goes high some time after KSCTRL[0] is set, and when the key-scan block has frozen the data in the KEYCODE and MODSTAT registers.

QDXn[7:0] = Magnitude of X axis count for n-th quadrature block, where n = 0 to 2

QDYn[7:0] = Magnitude of Y axis count for n-th quadrature block, where n = 0 to 2

QDZn[7:0] = Magnitude of Z axis count for n-th quadrature block, where n = 0 to 2

- QFLAG[7:0] = sign and overflow bits for the three axes
- QFLAG[0] = sign bit for X axis
- QFLAG[1] = overflow for X axis
- QFLAG[2] = sign bit for Y axis
- QFLAG[3] = overflow for Y axis
- QFLAG[4] = sign bit for Z axis
- QFLAG[5] = overflow for Z axis

PULSE-WIDTH MODULATION

The BCM2042 has four internal 10-bit Pulse-Width Modulation (PWM) control signal outputs which can be used via GPIO Port 3[5:2]. When a 10-bit PWM counter value is bigger than the value defined in the PWM register, a logic 1 will be generated and be exclusive, or with the GPIO output status bit and output to port. Below are the control registers for each of the four ports.

- PWM1_ADR[7:0]: This is the lowest 8 bits of the 10-bit PWM control register for Port3_2.
- PWM2_ADR[7:0]: This is the lowest 8 bits of the 10-bit PWM control register for Port3_3.
- PWM3_ADR[7:0]: This is the lowest 8 bits of the 10-bit PWM control register for Port3_4.
- PWM4_ADR[7:0]: This is the lowest 8 bits of the 10-bit PWM control register for Port3_5.

PWM_MSB_ADR: Contains the highest 2 bits for each of the four 10-bit PWM control registers:

- PWM_MSB_ADR[7:6]: The highest 2 bits of the 10-bit PWM control register for Port3_5.
- PWM_MSB_ADR[5:4]: The highest 2 bits of the 10-bit PWM control register for Port3_4.
- PWM_MSB_ADR[3:2]: The highest 2 bits of the 10-bit PWM control register for Port3_3.
- PWM_MSB_ADR[1:0]: The highest 2 bits of the 10-bit PWM control register for Port3_2.

SERIAL PERIPHERAL INTERFACE

The BCM2042 has one SPI inside the chip with three-pin support for both full-duplex and half-duplex modes. In order to support more flexibility for user applications, the BCM2042 has two optional output ports that can be configured. The BCM2042 SPI acts as a Master device which supports 1.8V/3.3V SPI slave devices. Please note that 5V SPI slave is not supported by our interface.

INTERFACE

- SPI Clock: P4_2 or P2_6 (If choosing P4_2, then MOSI/MISO will be Port 4)
- MOSI (Master out slave in): P4_3 or P2_7 (if in half-duplex mode, only this pin)
- MISO (Master In slave out): P4_4 or P2_5 (only in full-duplex mode)

CONTROL REGISTER

spi_cntl_adr[7:0] SPI Control Register:

- spi_cntl_adr[1:0]spi_en[1:0]—SPI Enable. Setting this field to 01, 10, or 11 initiates an 8-bit serial transfer. At the end of the transfer, the SPI hardware module automatically clears both bits. Settings of 01 and 10 initiate half-duplex transfers. For these transfers, a three-pin SPI interface is used, in which both MOSI and MISO data are transferred on the MOSI pin. A setting of 01 causes the SPI hardware module to shift in 8 bits from the MOSI pin in half-duplex mode. A setting of 10 causes the SPI hardware module to shift out 8 bits on the MOSI pin. A setting of 11 initiates a full-duplex transfer using four SPI pins. 8 bits of data are shifted in from the MISO pin, and 8 bits are shifted out on the MOSI pin.
- spi_cntl_adr[2] spi_oeb_ovr—SPI Output Enable Override. The output enable for the MOSI bidirectional pin is controlled automatically by the SPI hardware, unless the **spi_oeb_ovr** bit is set. Under automatic control, the output enable is driven low (pin is an output) whenever the **spi_en[1]** bit is set. Otherwise, the MOSI pin is tri-stated. If the **spi_oeb_ovr** bit is set, the hardware ignores the output enable from the automatic control logic, and instead takes the

output enable directly from the **spi_oeb** bit. By default, the **spi_oeb_ovr bit** is set, meaning that software is given control of the output enable after reset.

- spi_cntl_adr[3] spi_oeb—The output enable (active low) for the MOSI pin. This bit is valid only when the **spi_oeb_ovr** bit is set. By default, the **spi_oeb_ovr** bit and the **spi_oeb** bit are both set after reset. Thus, software is given control of the output enable by default, and the pin is configured as an input after reset.
- spi_cntl_adr[5:4] spi_mode[1:0]—The SPI Mode. The timing of the four modes are shown in Figure 6. The SS (chip select) signal, while part of the SPI interface, is not controlled by the hardware.

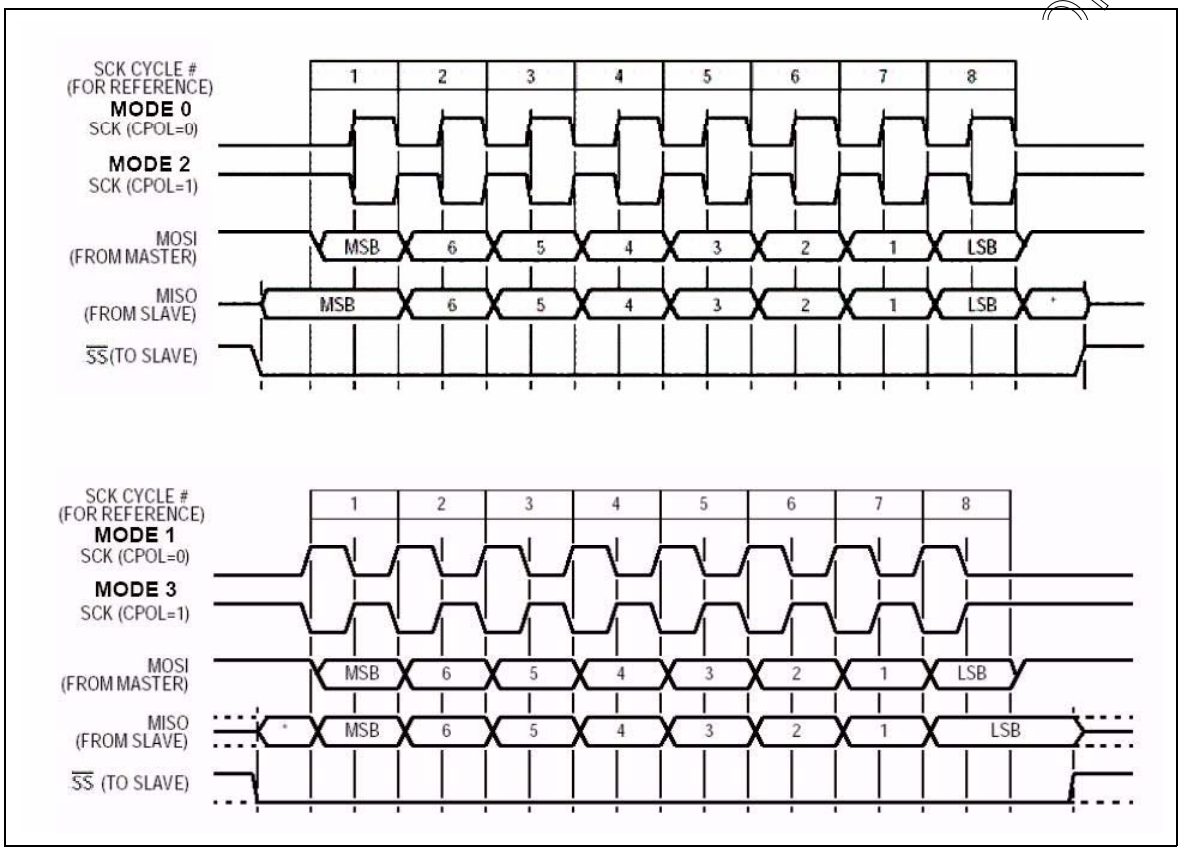


Figure 6: SPI Mode

SPI Port Select Register

- SPI_PORT_SEL_ADR[7:1] – reserved
- SPI_PORT_SEL_ADR[0] – spi_port_sel Select port 4 (set to 1) or port 2 for SPI interface:
  - SPI Clock – P42/P26
  - MOSI – P43/P27 (used for MISO when in half-duplex mode)
  - MISO – P44/P25

128-kHz Oscillator

The peripheral blocks of the BCM2042 are to all run from a single 128-kHz low-power RC oscillator. The oscillator can be turned on at the request of any of the peripherals. If the peripheral is not enabled, it shall not assert its clock request line.

The keyboard scanner is a special case in that it may drop its clock request line even when enabled, and then reassert the clock request line if a keypress is detected.

Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers, or packet handling in the baseband core. The following sections are power management functions provided by the BCM2042.

RF Power Management

The BBC generates power down control signals for the transmit path, receive path, phase-locked loop (PLL), and power amplifier to the 2.4-GHz transceiver. The transceiver then processes the power down functions accordingly.

Host Controller Power Management

Power is automatically managed by the firmware, and it does so based on input device activity. Some major power saving tasks that are controlled by firmware include:

- Disable on-chip regulators when in deep sleep mode
- Power-down on-chip ROM when in sleep mode or deep sleep mode
- Power-down external memory when in sleep mode

BBC Power Management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth specified low-power connection modes: Sniff, Hold, and Park. While in these low-power connection modes, the BCM2042 runs on the Low Power Oscillator and wakes up after a pre-defined time period.

The BCM2042 automatically adjusts its power consumption based on user activity. The following four power modes are supported:

- Busy mode
- Idle mode
- Suspend mode
- Power Down mode

The BCM2042 transitions to the next lower state after a programmable period of user inactivity. Busy mode is immediately entered when user activity resumes.

Power Down allows the device to be turned off while the host, and any other devices in the system, remain operational. When the BCM2042 is not needed in the system, VDD_RF, VDD_MEM, and VDD_CORE are shut down while VDD_IO is left powered. This allows the BCM2042 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

ON-CHIP SWITCHING REGULATORS

The BCM2042 has two on-chip switching regulators:

- SW1–a boost regulator for 2.7V to 3.3V to support external sensor and flash.
- SW2–a buck regulator that can be configured to 1.8V to support the on-chip LDO, which in turn supports the BCM2042 1.5V core and radio.

Both regulators support a two-cells-in-series input of 1.8V to 3.6V if the load is less than 50 mA. For loads of up to 200 mA and a switching regulator duty cycle of 75%, the regulators support two-cells-in-series with inputs of 1.8V to 3.2V.

The regulators provide the following features:

- Burst mode for low quiescent current
- PWM mode for clean supply voltage in active mode
- Low battery voltage lock-out
- Spread spectrum clocking for low RF interference
- High switching speed of 2 MHz
- Programmable switching frequency
- Over current protection
- Low power down current (<1 μA)
- Dual output:
  - 1.5V to 1.8V
  - 2.7V to 3.3V
- By-pass mode (This is firmware controlled, and can save more power while the input voltage is nearly equal to the output voltage or in a battery low condition)

THEORY OF OPERATION

For more description, see Figure 7.

- VFB1 = VFB2 = 1.1V ± 6% (This pin is the feedback pin for switching regulator)
- Voutput1 (3P0V_1) = VFB1 * (1+R1/R2)
- Voutput2 (1P8V_1) = VFB2 * (1+R3/R4)

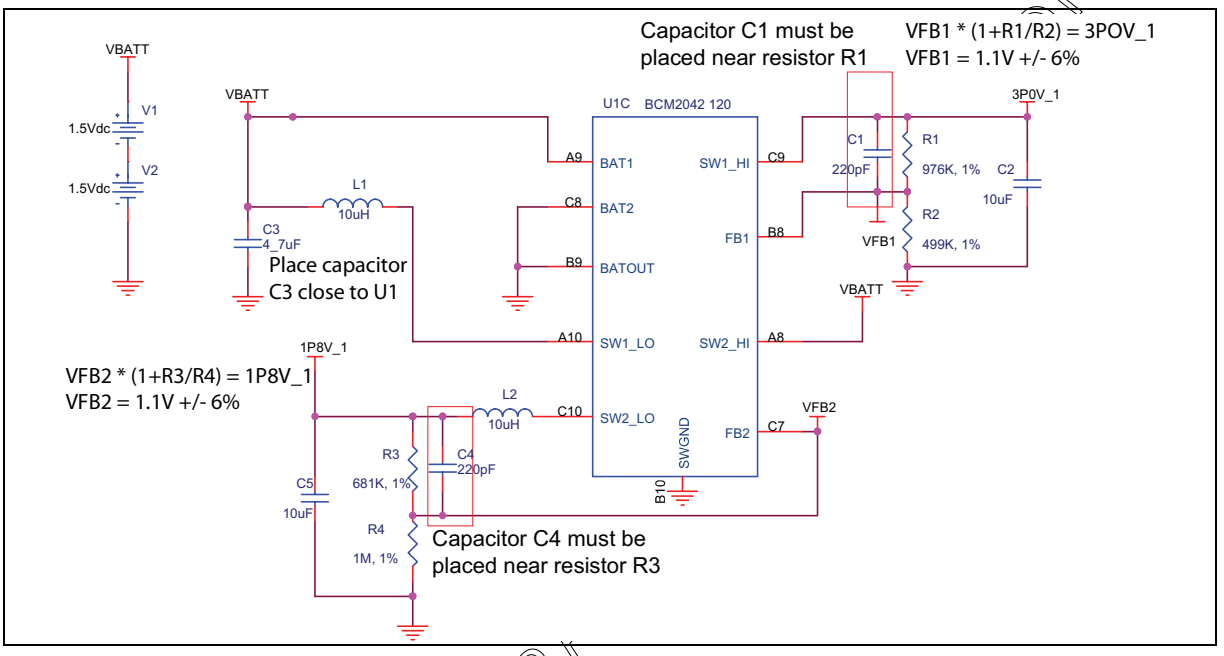


Figure 7: Two Cell in Series Configuration

EXAMPLES

Both SW1 and SW2 can work alone. Listed below are the most useful configurations.

1. SW1 is used as a boost, and SW2 is used as a buck (see Figure 7). In this condition, SW2 works in BUCK mode to step down the input voltage to 1.8V. Battery selection pin BAT1 is tied to VBATT while BAT2 and BATOUT are tied to GND. This mode is most often used with two alkaline cells in series (AA or AAA).

2 SW1 is used as a boost, and SW2 is not used (see Figure 8). Take the two cells in series as a reference. Be sure to leave three pins (SW2_HI, SW2_LO, and FB2) floating. This mode might be used when a regulated 1.8V for internal LDO, an output from pin VREG1, is available. Examples include:

- A single cell Alkaline battery feeding an external boost regulator producing 1.8V.
- Two alkaline cells in series feeding an external buck regulator or LDO producing 1.8V.
- A regulated power 1.8V supply.

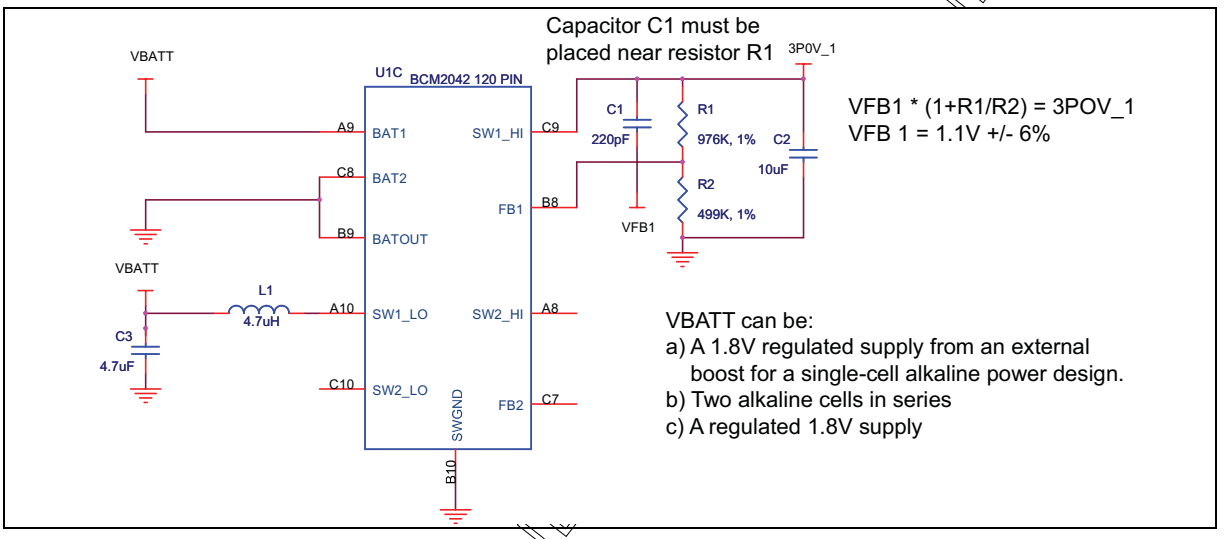


Figure 8: SW1 Used As Boost, SW2 Not Used

3. SW1 is not used, SW2 is used as buck (see Figure 9). This configuration is suitable for use in systems with a regulated 2.7V to 3.3V supply, such as a lithium-ion or lithium-polymer rechargeable battery, together with a 3.3V pre-regulator. Examples include:

- A single cell feeding an external boost regulator producing 2.7V~3.3V.
- Two cells in series feeding an external boost regulator producing 2.7V~3.3V.
- A regulated 2.7V to 3.3V supply, including LDO or buck regulator output by a Lithium-ion or Lithium-polymer battery-powered design.

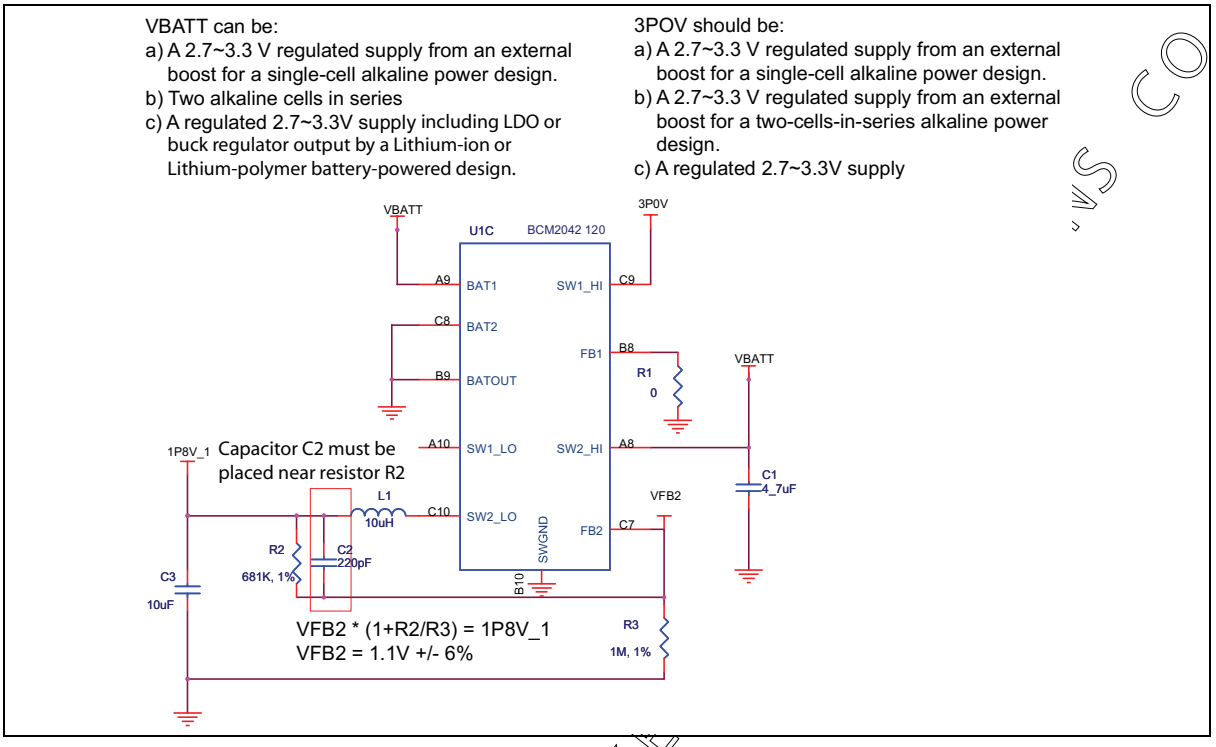


Figure 9: SW1 Not Used, SW2 Used As Buck

4 Switchers disabled: the switching regulator is controlled by firmware (see Figure 10). The battery selection pin BAT1 is connected to VBATT. BAT2, BATOUT, and FB1 are connected to GND. SW1_HI is connected to VBATT. SW1_LO, SW2_HI, SW2_LO, and FB2 are not connected.

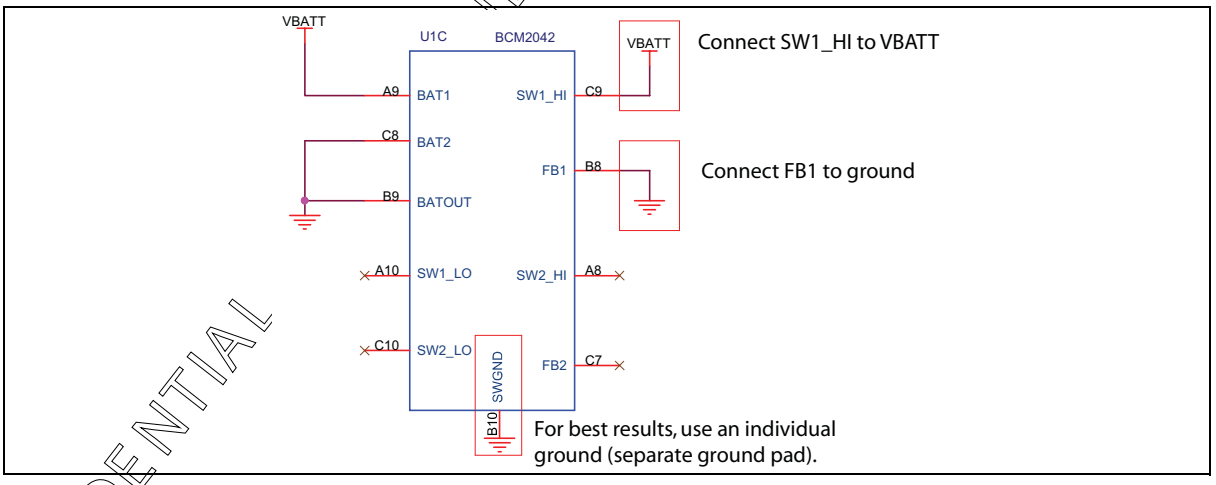


Figure 10: Switchers Disabled

Section 2: Pin Assignments

Table 2: Pin Description

Pin Number						
120-pin BGA (9x10)	*88-pin BGA (9x8)*	*100-pin BGA (9x9)*	*Pin Name*	*I/O*	*Power Domain*	*Description*
Radio I/O						
D1	D1	D1	RF_IOP	I/O	VDD_RF	RF I/O port, positive – connect to GND.
G4	G4	K3	RES	O	VDD_RF	External calibration resistor – connect to 150K, 1% to GND.
E1	E1	E1	RF_ION	I/O	VDD_RF	RF I/O port, negative – connect to antenna.
F3	F3	F3	TST1	I	VDD_RF	RF test point: connect to GND.
Clock Generator and Crystal Interface						
H2	H2	H2	VCTRIFP	O	VDD_RF	IF-VCO tuning supply – connect 470 pF, 5% to GND.
J3	J3	K2	XTAL_IN	I	VDD_RF	Crystal reference input – high impedance.
J2	J2	K1	XTAL_OUT	O	VDD_RF	Crystal reference output – low impedance.
Core						
L1	NA	NA	uP_ADDR0	O	VDD_MEM	Address bit 0 for external memory
K3	NA	NA	uP_ADDR1	O	VDD_MEM	Address bit 1 for external memory
L2	NA	NA	uP_ADDR2	O	VDD_MEM	Address bit 2 for external memory
M1	NA	NA	uP_ADDR3	O	VDD_MEM	Address bit 3 for external memory
M2	NA	NA	uP_ADDR4	O	VDD_MEM	Address bit 4 for external memory
M3	NA	NA	uP_ADDR5	O	VDD_MEM	Address bit 5 for external memory
L3	NA	NA	uP_ADDR6	O	VDD_MEM	Address bit 6 for external memory
L4	NA	NA	uP_ADDR7	O	VDD_MEM	Address bit 7 for external memory
M4	NA	NA	uP_ADDR8	O	VDD_MEM	Address bit 8 for external memory
K4	NA	NA	uP_ADDR9	O	VDD_MEM	Address bit 9 for external memory
J5	NA	NA	uP_ADDR10	O	VDD_MEM	Address bit 10 for external memory
L5	NA	NA	uP_ADDR11	O	VDD_MEM	Address bit 11 for external memory
M5	NA	NA	uP_ADDR12	O	VDD_MEM	Address bit 12 for external memory
K5	NA	NA	uP_ADDR13	O	VDD_MEM	Address bit 13 for external memory
J6	NA	NA	uP_ADDR14	O	VDD_MEM	Address bit 14 for external memory
K6	NA	NA	uP_ADDR15	O	VDD_MEM	Address bit 15 for external memory
M6	NA	NA	uP_ADDR16	O	VDD_MEM	Address bit 16 for external memory
M8	NA	NA	uP_DATA0	I/O	VDD_MEM	Data bit 0 for external memory
K8	NA	NA	uP_DATA1	I/O	VDD_MEM	Data bit 1 for external memory
M9	NA	NA	uP_DATA2	I/O	VDD_MEM	Data bit 2 for external memory
K9	NA	NA	uP_DATA3	I/O	VDD_MEM	Data bit 3 for external memory
M10	NA	NA	uP_DATA4	I/O	VDD_MEM	Data bit 4 for external memory
L10	NA	NA	uP_DATA5	I/O	VDD_MEM	Data bit 5 for external memory
L9	NA	NA	uP_DATA6	I/O	VDD_MEM	Data bit 6 for external memory
K10	NA	NA	uP_DATA7	I/O	VDD_MEM	Data bit 7 for external memory

Table 2: Pin Description (Cont.)

Pin Number			Pin Name	I/O	Power Domain	Description
120-pin BGA (9x10)	88-pin BGA (9x8)	100-pin BGA (9x9)				
K7	NA	NA	uP_CS0	O	VDD_MEM	External memory chip select – active low signal. Select external code space in flash memory.
L6	NA	NA	uP_CS1	O	VDD_MEM	External memory chip select – active low signal. Select external SRAM. Also can be function as uP_ADDR17 when using 4 Mbit flash memory.
M7	NA	NA	$\overline{\text{uP\_WRN}}$	O	VDD_MEM	External Memory write strobe – active low.
L7	NA	NA	$\overline{\text{uP\_RDN}}$	O	VDD_MEM	External Memory read strobe – active low.
H6	H6	K10	SDA	I/O	VDD_MEM	Broadcom Serial Control Data (I^2C compatible).
H5	H5	K9	SCL	I/O	VDD_MEM	Broadcom Serial Control Clock (I^2C compatible).
J10	J10	K7	uP_TX	O	VDD_MEM	Debug UART Transmit port.
J9	J9	K6	uP_RX	I	VDD_MEM	Debug UART Receiver port – after power on reset, if: UP_RX = 1, Boot-ROM waits for download of firmware through debug serial port. UP_RX = 0, Boot-ROM launches firmware image in the external Flash or internal ROM.
K1	NA	NA	XBOOT_N	I	VDD_MEM	External Boot ROM selection: 0 = Boot from external ROM. 1 = Boot from internal ROM.
H8	H8	J8	$\overline{\text{RESET\_N}}$	I	VDD_IO	Active low system reset – contains a weak pull up. Contains an internal POR hardware inside. No external reset monitor needed.
B3	B3	H8	TMC	I	VDD_IO	Test mode selection clock – contains a weak pull down.
Digital I/O and Core Power Supplies						
D6, D7, E7	D6, D7, E7	A7, B7, K8	VDD_IO	–	NA	Power supply for the GPIOs.
L8	NA	NA	VDD_MEM	–	NA	Digital I/O power supply. Power supply for external flash memory.
C4, J4, J7	C4, J4, J7	A2, J5, K5	VDD_CORE	–	NA	Baseband core power supply.
Switching Regulator Supplies						
A9	A9	B9	BAT1	I	NA	Battery cell positive terminal.
C8	C8	C9	BAT2	I	NA	Mode detection: ground this pin.
B9	B9	D9	BATOUT	O	NA	Ground this pin for 2-cell in serial mode.
A10	A10	D10	SW1_LO	I	NA	Switching regulator #1 inductor terminal.
C9	C9	A8	SW1_HI	O	NA	Switching regulator #1 output. 3V output. Output range from 2.7V to 3.3V. Adjustable (Ask your Broadcom Sales Representative for a copy of the *BCM2042 Application Note* covering the details of configuring the switching regulators for the above battery supplies.)
B8	B8	B8	FB1	I	NA	Switching regulator #1 external feedback.
C10	C10	A10	SW2_LO	I	NA	Switching regulator #2 inductor terminal.
A8	A8	B10	SW2_HI	O	NA	Switching regulator #2 output. If in two cells in series mode, the output pin will be the SW2_LO output range from 1.5V to 1.8V. Adjustable.

Table 2: Pin Description (Cont.)

Pin Number			Pin Name	I/O	Power Domain	Description
120-pin BGA (9x10)	88-pin BGA (9x8)	100-pin BGA (9x9)				
C7	C7	A9	FB2	I	NA	Switching regulator #2 external feedback.
B10	B10	C10,C8	SWGND	O	NA	Switching regulator ground.
RF Power Supplies						
F1, B2, C2, D2, E2, K2, G3, H3, D4, H4, E6, F6, F7, J8	F1, B2, C2, D2, E2, G3, H3, D4, H4, E6, F6, F7, J8	F1, B2, C2, D2, E2, J2, D3, E3, G3, H3, J3, E4, F4, E5, F5, E6, F6, G6, C7, D7, E7, F7, D8, E9, E10	GND	–	NA	Ground connection.
A2	A2	A1	VREG1	–	NA	Output for LDO.
A1	A1	NA	VREG2	–	NA	NA
B1, C1, G1, H1, J1, F2, G2	B1, C1, G1, H1, J1, F2, G2	B1, C1, G1, H1, J1, F2, G2	VDD_RF	–	NA	1.5V RF power supply.
A3	A3	A3	VDD_R3V	–	NA	On-chip LDOs input.

Table 3: GPIO Pin Descriptions

Pin Number			Pin Name	Default Direction	POR State	Alternative Function Description
120-pin BGA (9x10)	88-pin BGA (9x8)	100-pin BGA (9x9)				
F10	F10	G10	P0_0	input	floating	GPIO: P0_0 Keyboard Scan Input (ROW): KSI0 A/D CONVERTER Input
G7	G7	H7	P0_1	input	floating	GPIO: P0_1 Keyboard Scan Input (ROW): KSI1 A/D CONVERTER Input
G8	G8	G9	P0_2	input	floating	GPIO: P0_2 Keyboard Scan Input (ROW): KSI2 Quadrature: QDX0
H7	H7	J7	P0_3	input	floating	GPIO: P0_3 Keyboard Scan Input (ROW): KSI3 Quadrature: QDX1
G9	G9	H9	P0_4	input	floating	GPIO: P0_4 Keyboard Scan Input (ROW): KSI4 Quadrature: QDY0
G10	G10	H10	P0_5	input	floating	GPIO: P0_5 Keyboard Scan Input (ROW): KSI5 Quadrature: QDY1

Table 3: GPIO Pin Descriptions (Cont.)

Pin Number			Pin Name	Default Direction	POR State	Alternative Function Description
120-pin BGA (9x10)	88-pin BGA (9x8)	100-pin BGA (9x9)				
H9	H9	J9	P0_6	input	floating	GPIO: P0_6 Keyboard Scan Input (ROW): KSI6 Quadrature: QDZ0
H10	H10	J10	P0_7	input	floating	GPIO: P0_7 Keyboard Scan Input (ROW): KSI7 Quadrature: QDZ1
F4	F4	C3	P1_0	input	floating	GPIO: P1_0 Keyboard Scan Output (Column): KSO0 A/D CONVERTER Input
E4	E4	B3	P1_1	input	floating	GPIO: P1_1 Keyboard Scan Output (Column): KSO1 A/D CONVERTER Input
A4	A4	A4	P1_2	input	floating	GPIO: P1_2 Keyboard Scan Output (Column): KSO2 A/D CONVERTER Input
A5	A5	A5	P1_3	input	floating	GPIO: P1_3 Keyboard Scan Output (Column): KSO3 A/D CONVERTER Input
B4	B4	B4	P1_4	input	floating	GPIO: P1_4 Keyboard Scan Output (Column): KSO4 A/D CONVERTER Input
E8	E8	A6	P1_5	input	floating	GPIO: P1_5 Keyboard Scan Output (Column): KSO5 A/D CONVERTER Input
D8	D8	B6	P1_6	input	floating	GPIO: P1_6 Keyboard Scan Output (Column): KSO6 A/D CONVERTER Input
C6	C6	C6	P1_7	input	floating	GPIO: P1_7 Keyboard Scan Output (Column): KSO7 A/D CONVERTER Input
B5	B5	B5	P2_0	input	floating	GPIO: P2_0 Keyboard Scan Output (Column): KSO8 A/D CONVERTER Input
C5	C5	C5	P2_1	input	floating	GPIO: P2_1 Keyboard Scan Output (Column): KSO9 A/D CONVERTER Input
D9	D9	F8	P2_2	input	floating	GPIO: P2_2 Keyboard Scan Output (Column): KSO10 A/D CONVERTER Input
E9	E9	G8	P2_3	input	floating	GPIO: P2_3 Keyboard Scan Output (Column): KSO11 A/D CONVERTER Input

Table 3: GPIO Pin Descriptions (Cont.)

Pin Number			Pin Name	Default Direction	POR State	Alternative Function Description
120-pin BGA (9x10)	88-pin BGA (9x8)	100-pin BGA (9x9)				
D10	D10	F10	P2_4	input	PD	GPIO: P2_4 Keyboard Scan Output (Column): KSO12 A/D CONVERTER Input
F8	F8	F9	P2_5	input	PD	GPIO: P2_5 Keyboard Scan Output (Column): KSO13 A/D CONVERTER Input SPI: MISO
G5	G5	K4	P2_6	input	PU	GPIO: P2_6 Keyboard Scan Output (Column): KSO14 Auxiliary Clock output: ACLK0 A/D CONVERTER Input SPI: SPI_CLK
G6	G6	J6	P2_7	input	PU	GPIO: P2_7 Keyboard Scan Output (Column): KSO15 Auxiliary Clock output: ACLK1 A/D CONVERTER Input SPI: MOSI
F9	F9	G7	P3_0	output**	low**	GPIO: P3_0 Keyboard Scan Output (Column): KSO16
E10	E10	H6	P3_1	output**	low**	GPIO: P3_1 Keyboard Scan Output (Column): KSO17
A6	A6	C4	P3_2	input	floating	GPIO: P3_2 (Can do PWM output) Keyboard Scan Output: KSO18 Optical Control Output: QOC0
B6	B6	D5	P3_3	input	floating	GPIO: P3_3 (Can do PWM output) Keyboard Scan Output (Column): KSO19 Optical Control Output: QOC1
A7	A7	D6	P3_4	input	PU	GPIO: P3_4 (Can do PWM output) Optical Control Output: QOC2 A/D CONVERTER Input Infrared Channel External PA Ramp control: PA_Ramp
B7	B7	E8	P3_5	input	PU	GPIO: P3_5 (Can do PWM output) Optical Control Output: QOC03 A/D CONVERTER Input Infrared Channel
E5	E5	D4	P4_0	output**	high**	GPIO: P4_0 Quadrature: QDX0 External Regulator En: VREG_EN A/D CONVERTER Input External T/R switch control: RX_PU

Table 3: GPIO Pin Descriptions (Cont.)

Pin Number			Pin Name	Default Direction	POR State	Alternative Function Description
120-pin BGA (9x10)	88-pin BGA (9x8)	100-pin BGA (9x9)				
D5	D5	G5	P4_1	input	PD	GPIO: P4_1 Quadrature: QDX1 A/D CONVERTER Input External T/R switch control: TX_PU
F5	F5	H5	P4_2	input	floating	GPIO: P4_2 Quadrature: QDY0 A/D CONVERTER Input SPI: SPI_CLK Battery Detect pin in Default FW
C3	C3	G4	P4_3	input	floating	GPIO: P4_3 Quadrature: QDY1 A/D CONVERTER Input SPI: MOSI
D3	D3	H4	P4_4	input	PU	GPIO: P4_4 Quadrature: QDZ0 A/D CONVERTER Input SPI: MISO
E3	E3	J4	P4_5	input	PD	GPIO: P4_5 Quadrature: QDZ1 A/D CONVERTER Input
**Only if TMC is high. Will be default floating and input pin while TMC tied to GND						

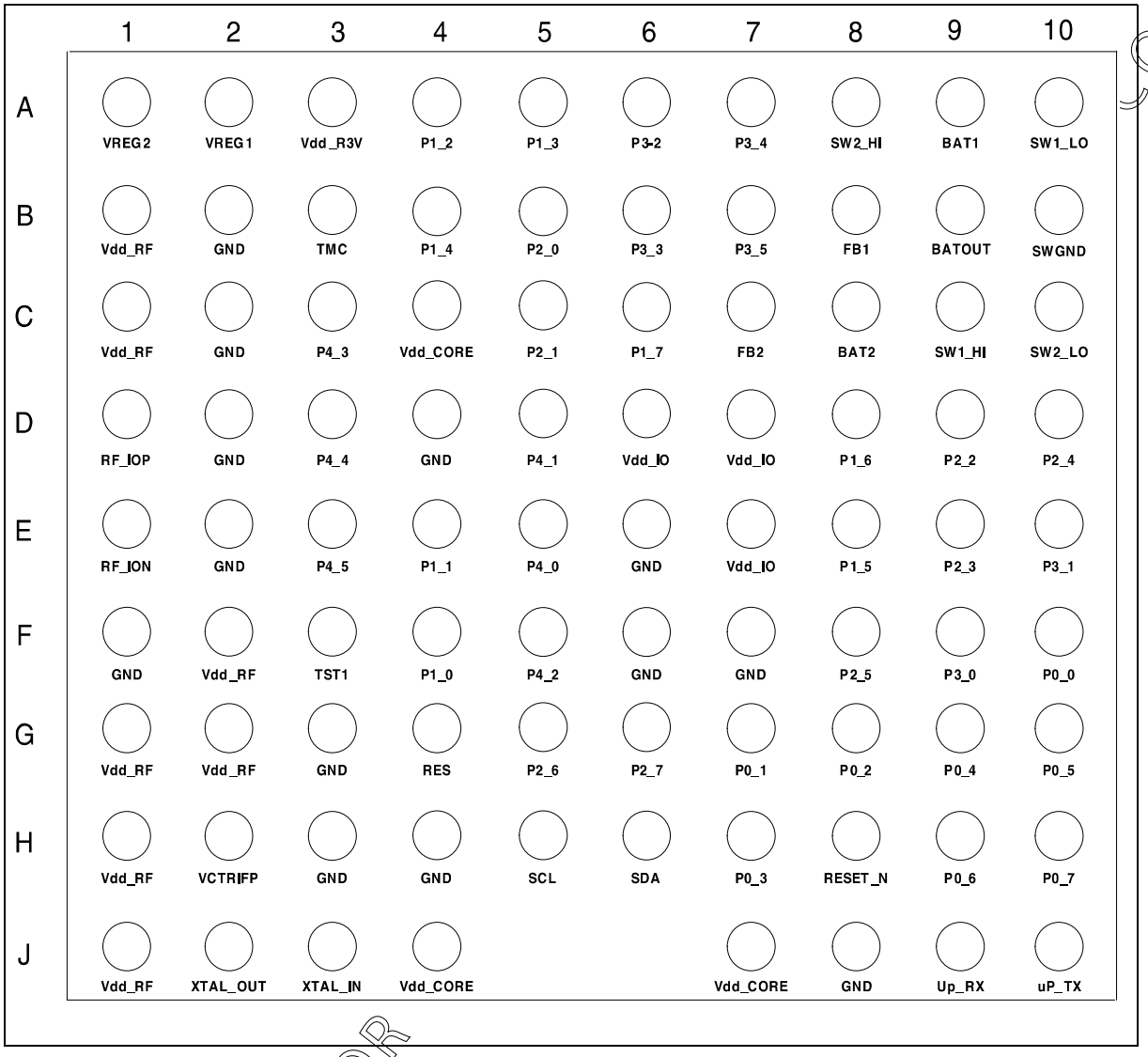


Figure 11: 88-Ball Pin Diagram

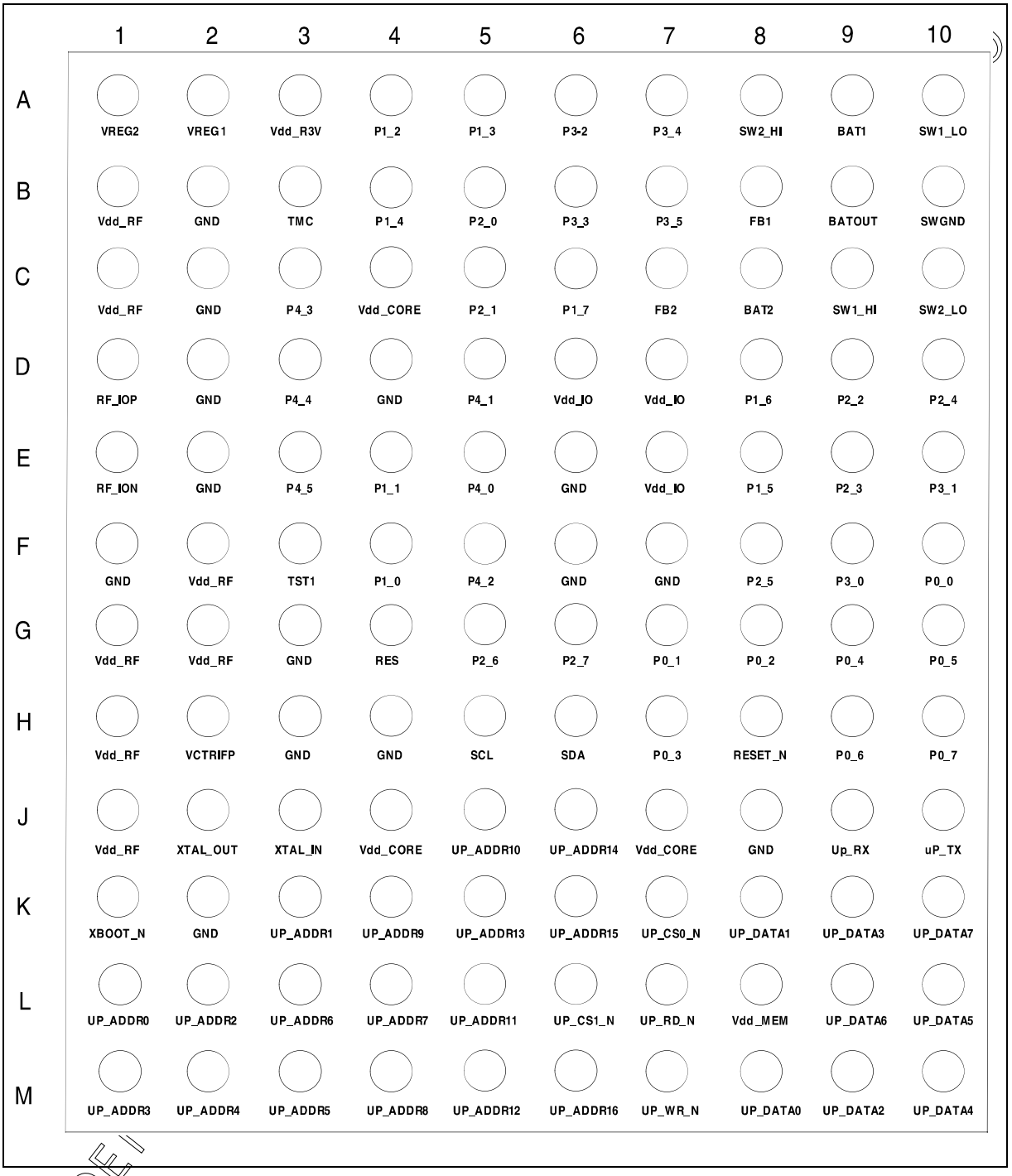


Figure 12: 120-Ball Pin Diagram

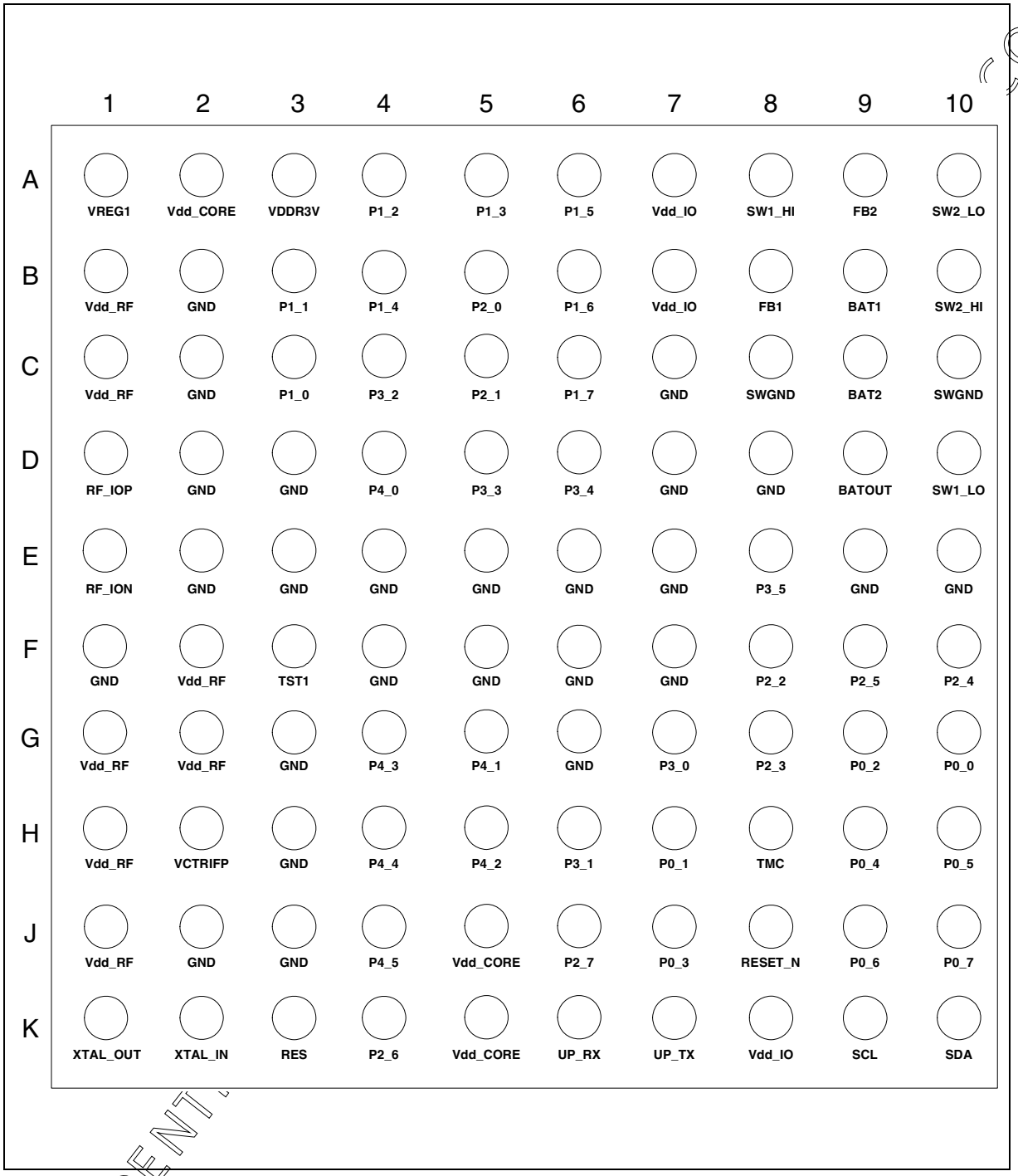


Figure 13: 100-Ball Pin Diagram

Section 3: Specifications

ELECTRICAL CHARACTERISTICS

Table 4 shows the maximum electrical rating for voltages referenced to V_{DD} pin.

Table 4: Maximum Electrical Rating

Rating	*Symbol*	*Value*	*Unit*
DC supply voltage for RF (VDD_RF)	–	1.65	V
DC supply voltage for Core (VDD_CORE)	–	1.65	V
DC supply voltage for I/O (VDD_IO or VDD_R3V)	–	4.1	V
DC supply voltage for Switching Regulator (2 cells in series)	–	–	
Steady State (< 200 mA load/95% duty cycle)	–	3.1	V
Steady State (< 200 mA load/75% duty cycle)	–	3.2	V
Steady State (< 50 mA load)	–	3.63	V
Less than 20 µs (where width measured 0.2V below peak)	–	4.5	V
Less than 10 ns (where width measured 0.2V below peak)	–	6.5	V
Voltage on the switching regulator #1 output pin	SW1_HI	3.63	V
Voltage on the switching regulator #2 output pin	SW2_LO	2.2 [a]	V
Voltage on input or output pin	–	V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage temperature range	Tstg	–40 to 125	°C

a. 2.2V~1.98V occurs when switcher 2 is in Bypass mode per the default application configuration.

Table 5 shows the power supply characteristics for the range T_J = 0 to 125°C.

Table 5: Power Supply

Parameter	*Min.*[1]	*Typical*	*Max.*[1]	*Unit*
DC supply voltage for RF (VDD_RF)	1.4	1.5	1.65	V
DC supply voltage for Core (VDD_CORE)	1.35	1.5	1.65	V
DC Supply voltage for VDD_IO	1.8	–	3.6	V
DC supply voltage for VDD_MEM or VDD_R3V	1.71	1.8	3.63	V
DC supply voltage for switching regulator (< 200 mA load/95% duty cycle)	1.8	–	3.1	V
DC supply voltage for switching regulator (< 200 mA load/75% duty cycle)	1.8	–	3.2	V
DC supply voltage for switching regulator (<50mA load)	1.8	–	3.6	V
Voltage on the switching regulator #1 output pin SW1_HI	2.7	3	3.3	V
Voltage on the switching regulator #2 output pin SW2_LO[2]	1.65	1.8	1.98	V
DC supply voltage for turning on switching regulators (BAT1)	1.4		3.63	V
Supply noise for VDD_RF[3,4]	–		150	µV rms

1. Overall performance degrades beyond Min and Max supply voltages.
2. When in SW2 only mode: make sure the power supply for this signal follows this spec.
3. Noise frequency fn: 100 kHz ~ 1 MHz.
4. Noise ripple: less than 50mV, as recommended. Supply sources other than the internal LDO, an output from pin VREG1, are not recommended.

Table 6 shows the digital level characteristics for (V_{SS} = 0 V), (T_A = 0 to 70°C).

Table 6: Digital Level

Characteristics	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
Input low voltage (3.3V I/O supply)	V_{IL}	–	–	0.8	V
Input high voltage (3.3V I/O supply)	V_{IH}	2.0	–	–	V
Input low voltage (1.8V I/O supply)	V_{IL}	–	–	0.6	V
Input high voltage (1.8V I/O supply)	V_{IH}	1.1	–	–	V
Output low voltage	V_{OL}	–	–	0.4	V
Output high voltage	V_{OH}	V_{DD} – 0.4	–	–	V
Input low current	I_{IL}	–	15	–	µA
Input high current	I_{IH}	–	15	–	µA
Output low current (3.3V I/O supply)	I_{OL}	–	–	2.0	mA
Output high current (3.3V I/O supply)	I_{OH}	–	–	2.0	mA
Input capacitance	C_{IN}	–	0.12	–	pF

Table 7: Typical Current Consumption

Operational Mode	*Minimum*	*Typical*	*Maximum*	*Unit*
Transmit[a]	–	39	–	mA
Receive[b]	–	29	–	mA
DM1 (TX mode)	–	28	–	mA
DM1 (RX mode)	–	25	–	mA
Sniff mode, 10 ms	–	5.4	–	mA
Sniff mode, 60 ms	–	0.75	–	mA
Sniff mode, 100 ms	–	0.46	–	mA
Sniff mode, 1.28 s	–	0.07	–	mA
Sleep (disconnected or Inter-Sniff, state preserved)	–	36	–	µA

Note: The current consumption data was measured at room temperature (25°C) directly on the VDD_IO, VDD_CORE, and VDD_RF rails and then added together; it should be 30 µA plus for each internal switcher, when used. Refer to the release note inside the firmware development kit (FDK) package posted on DocSafe, or contact Broadcom for accurate numbers if any customized application is used.

a. Max current when transmitter and baseband are both operating, 100% on.
b. Max current when receiver and baseband are both operating, 100% on.

RF SPECIFICATIONS

Table 8: Receiver RF Specifications (VDD_RF = 1.5V, T = 25°C)

Parameter	Minimum	Typical [3]	Maximum	Unit
Receiver Section				
Frequency range	2402	–	2480	MHz
Overall Rx sensitivity[1]	–	–85	–80	dBm
Input IP3	–	–10	–	dBm
Maximum input	–20	–10	–	dBm
Input impedance	–	50	–	Ω
Input impedance for RF_IO:	–	|S11| < –10 dB	–	–
Interference Performance				
Co-Channel interference, $C/I_{co\text{-}channel}$	–	9	11 [2]	dB
Adjacent (1 MHz) interference, $C/I_{1\ MHz}$	–	–5	0	dB
Adjacent (2 MHz) interference, $C/I_{2\ MHz}$	–	–35	–30	dB
Adjacent (≥3 MHz) interference, $C/I_{\geq 3\ MHz}$	–	–43	–40	dB
Image frequency interference, C/I_{Image}	–	–20	–9 [2]	dB
Adjacent (1 MHz) interference to in-band image frequency, $C/I_{Image\pm 1\ MHz}$	–	–35	–20 [2]	dB

1. The receiver sensitivity is measured at a BER of 0.1% on the device interface.
2. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 1.2 specification.
3. Typical operating conditions are 1.8V operating voltage and 25°C ambient temperature.

Table 9: Transmitter RF Specifications (VDD_RF = 1.5V, T = 25°C)

Parameter	Minimum	Typical	Maximum	Unit
Transmitter Section				
Frequency range	2402	–	2480	MHz
Output power—at max power setting[3]	–2	0	4	dBm
Output power—at minimum power setting[3]	–26	–	–18	dBm
Output power step size	–	2	–	dB
Output impedance [3]	–	50	–	Ω
Output impedance for RF_IO:	–	|S11| < –10 dB	–	–
In-Band Spurious Emission				
± 500 kHz	–	–	–20	dBc
20 dB bandwidth	–	900	1000	kHz
|M–N| = 2	–	–	–20 [1]	dBm
|M–N| ≥ 3	–	–	–40 [1]	dBm
Out-of-Band Spurious Emission				
30 MHz – 1 GHz	–	–	–36 [1,2]	dBm
1 GHz – 12.75 GHz	–	–	–30 [1,2]	dBm
1.8 GHz – 1.9 GHz	–	–	–47 [1]	dBm
5.15 GHz – 5.3 GHz	–	–	–47 [1]	dBm
LO Performance				
Lock time	–	180	–	µs
Initial carrier frequency tolerance	–	±25	±75	kHz
Frequency drift	–			
DH1 packet		±20	±25	kHz
DH3 packet		±20	±40	kHz
DH5 packet	–	±20	±40	kHz
Drift rate	–	10	20	kHz/50 µs
Frequency deviation	–			
00001111 sequence in payload[4]	140	–	175	kHz
10101010 sequence in payload[5]	115	–	–	kHz
Channel spacing	–	1	–	MHz

1. Maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 1.2 specification.
2. The spurious emissions during Idle Mode are the same as specified in Table 1: Receiver RF Specifications.
3. The RF characteristics are measured at the chip interface.
4. Average deviation in payload.
5. Max deviation in payload, for 99.9% of all frequency deviations.

TIMING AND AC CHARACTERISTICS

All tables in this section include a column for Reference Number. The Reference Number correlates to a specific number in Figure 14 on page 34 through Figure 17 on page 36. Use the numbers listed in this column to interpret the following timing diagrams.

MICROCONTROLLER TIMING SPECIFICATIONS

Table 10 through Table 14 shows the microcomputer timing specifications for (V_{DD} = 3.3V, V_{SS} = 0V, T_A = 0 to 70 °C).

Table 10: Microcontroller Timing Specifications

Reference Number	Characteristics	Minimum	Typical	Maximum	Unit
1	Host controller system clock (SCLK)	–	41.67		ns
2	Low power clock (LPCLK)	–	32	–	kHz
3	Address valid (UP_ADDR[16:0])	4xSCLK–5	–	–	ns
4	Address valid to UP_CSx_N	TBD	–	–	ns
8	Address valid to UP_RD_N	SCLK–21		–	ns
7	Address valid to UP_WR_N	SCLK–21	–	–	ns
9	UP_CSx_N valid	TBD	–	–	ns

Table 11: Program Memory Read Timing Specifications

Reference Number	Characteristics	Minimum	Typical	Maximum	Unit
10	UP_RD_N valid	2xSCLK–5	–	–	ns
11	Data setup to UP_RD_N invalid	19	–	–	ns
12	Data hold from UP_RD_N invalid	0	–	–	ns

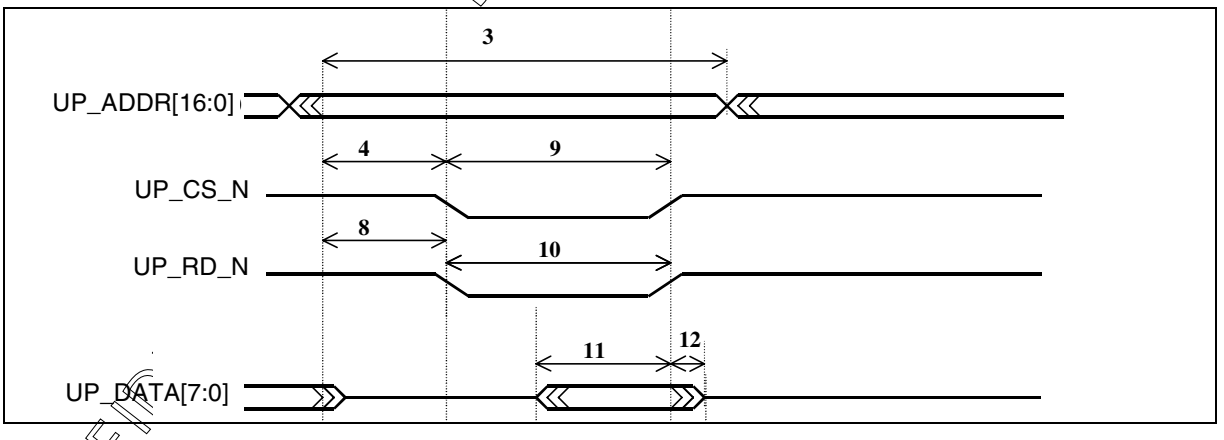


Figure 14: Program Memory Read Timing

Table 12: Program Memory Write Timing Specifications

Reference Number	Characteristics	Minimum	Typical	Maximum	Unit
13	UP_WR_N valid	2xSCLK–5	–	–	ns
14	Address valid to data valid	SCLK+1	–	–	ns
15	Data hold from UP_WR_N invalid	0	–	–	ns

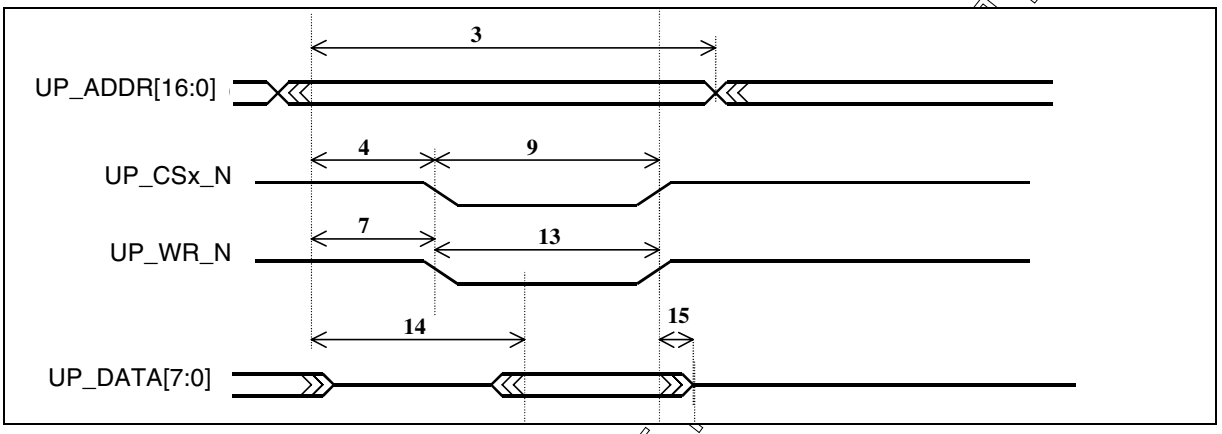


Figure 15: Program Memory Write Timing

Table 13: Data Memory Read Timing Specifications

Reference Number	Characteristics	Minimum	Typical	Maximum	Unit
16	UP_RD_N valid	2xSCLK–5	–	–	ns
18	Data setup to UP_RD_N invalid	19	–	–	ns
19	Data hold from UP_RD_N invalid	0	–	–	ns

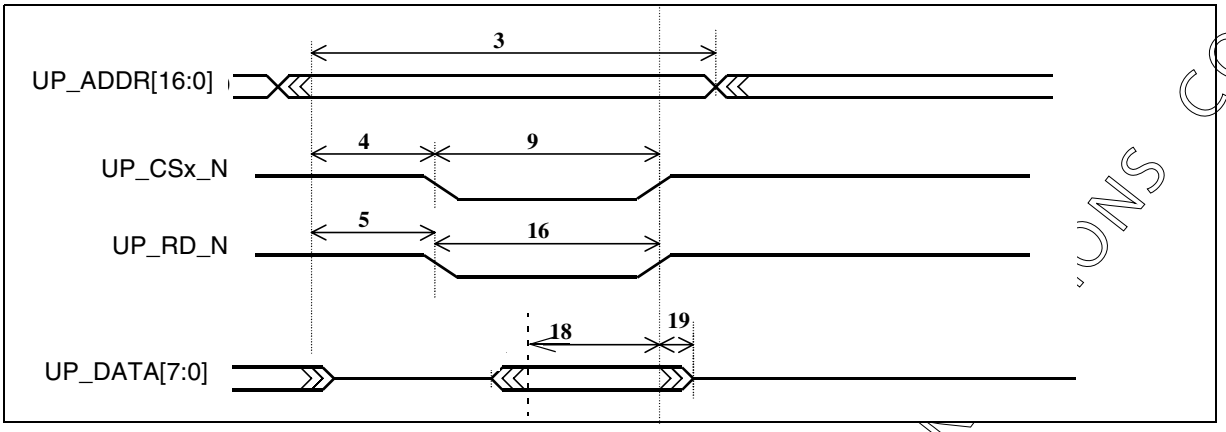


Figure 16: Data Memory Read Timing

Table 14: Data Memory Write Timing Specifications

Reference Number	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
20	UP_WR_N valid	2xSCLK–5	–	–	ns
21	Address valid to data valid	SCLK+1	–	–	ns
22	Data hold from UP_WR_N invalid	0	–	–	ns

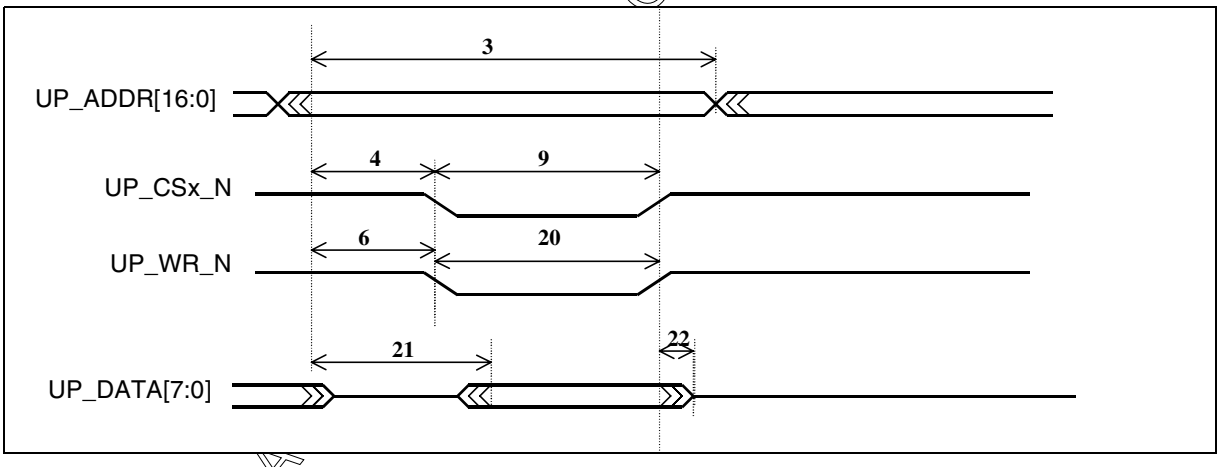


Figure 17: Data Memory Write Timing

Section 4: Mechanical Information

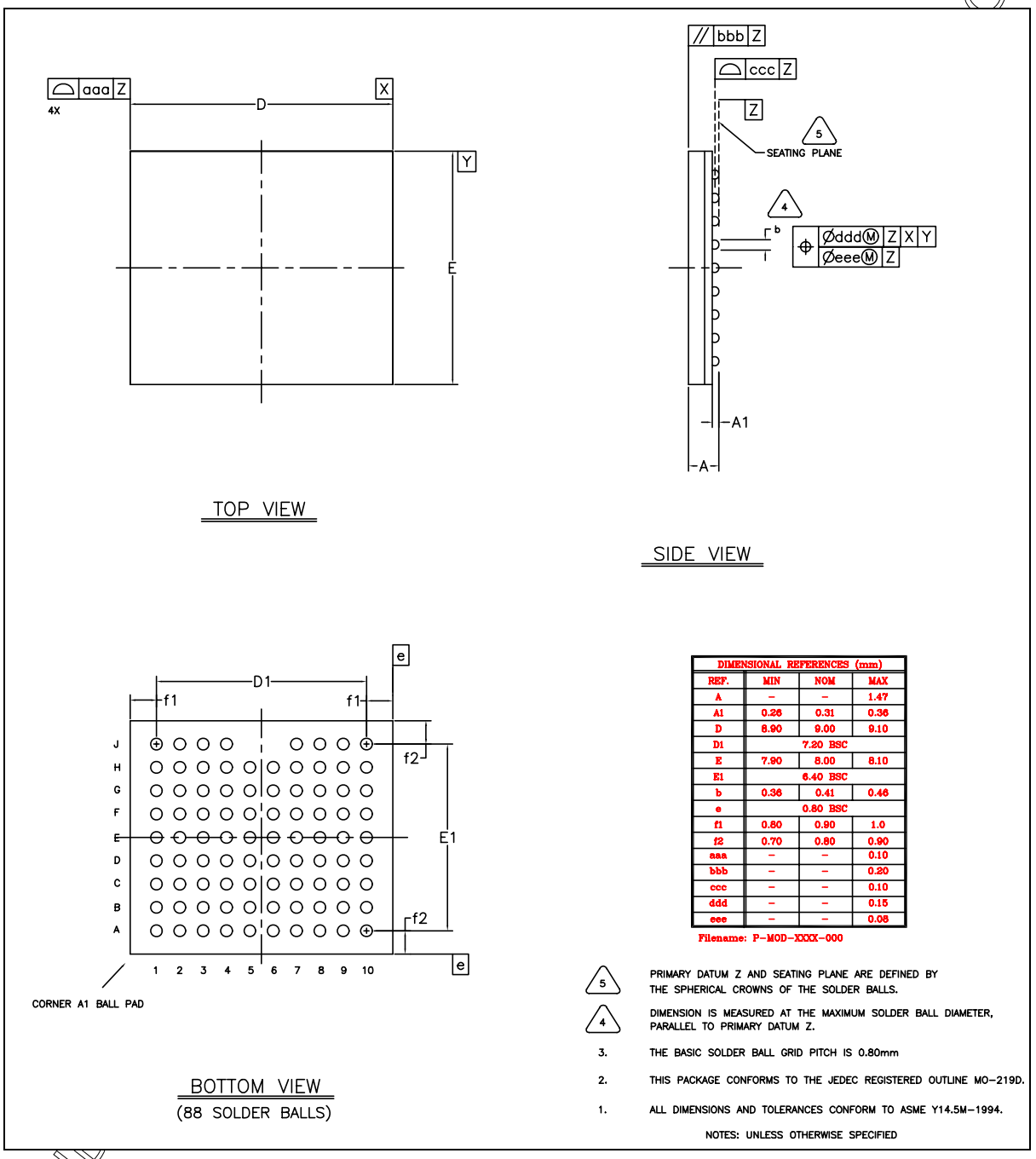
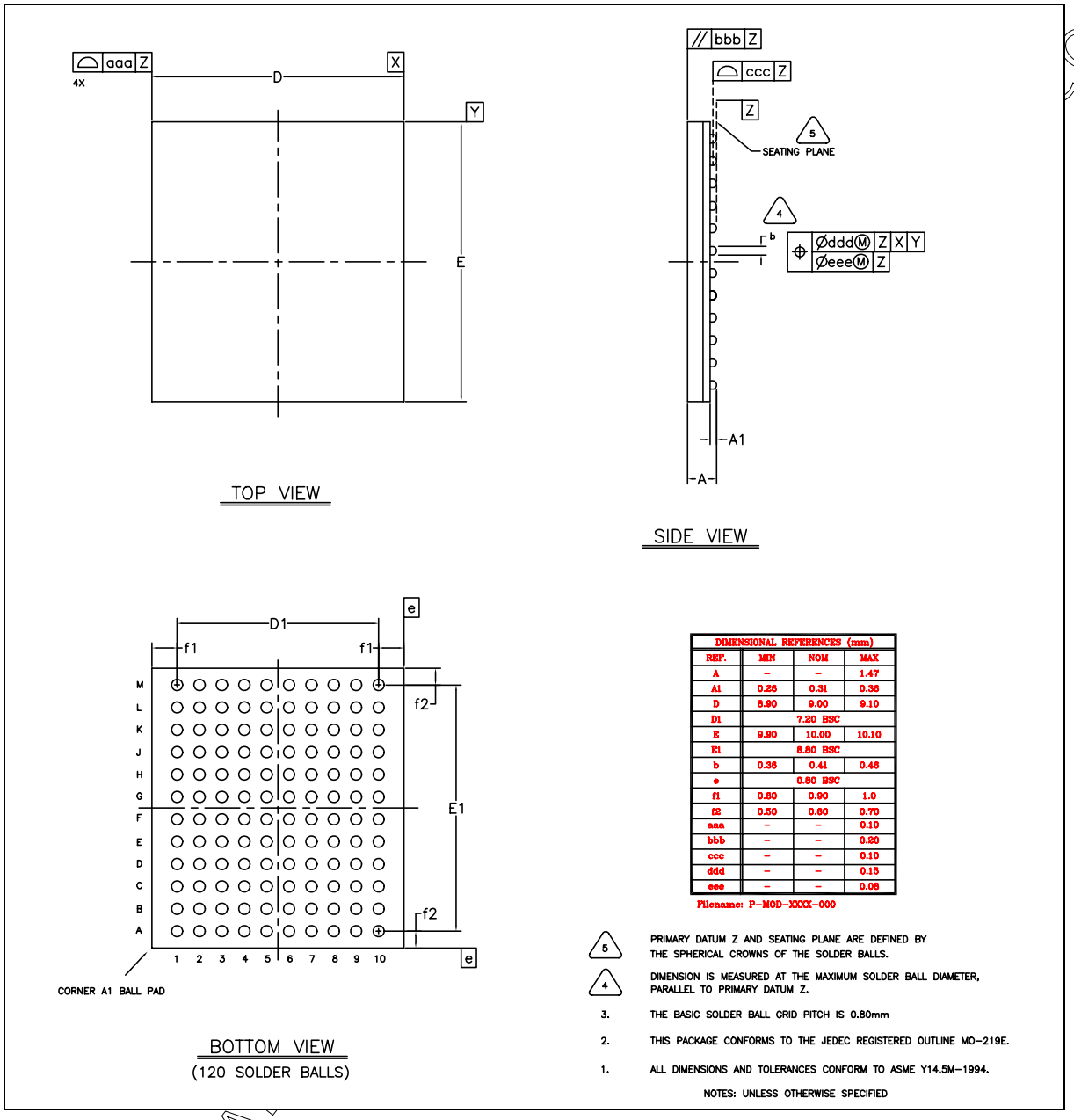


Figure 18: 88-Ball Mechanical Drawing



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.47
A1	0.26	0.31	0.36
D	8.90	9.00	9.10
D1		7.20 BSC	
E	9.90	10.00	10.10
E1		8.80 BSC	
b	0.36	0.41	0.46
e		0.80 BSC	
f1	0.80	0.90	1.0
f2	0.50	0.60	0.70
aaa	–	–	0.10
bbb	–	–	0.20
ccc	–	–	0.10
ddd	–	–	0.15
eee	–	–	0.08

Filename: P-MOD-XXXX-000

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

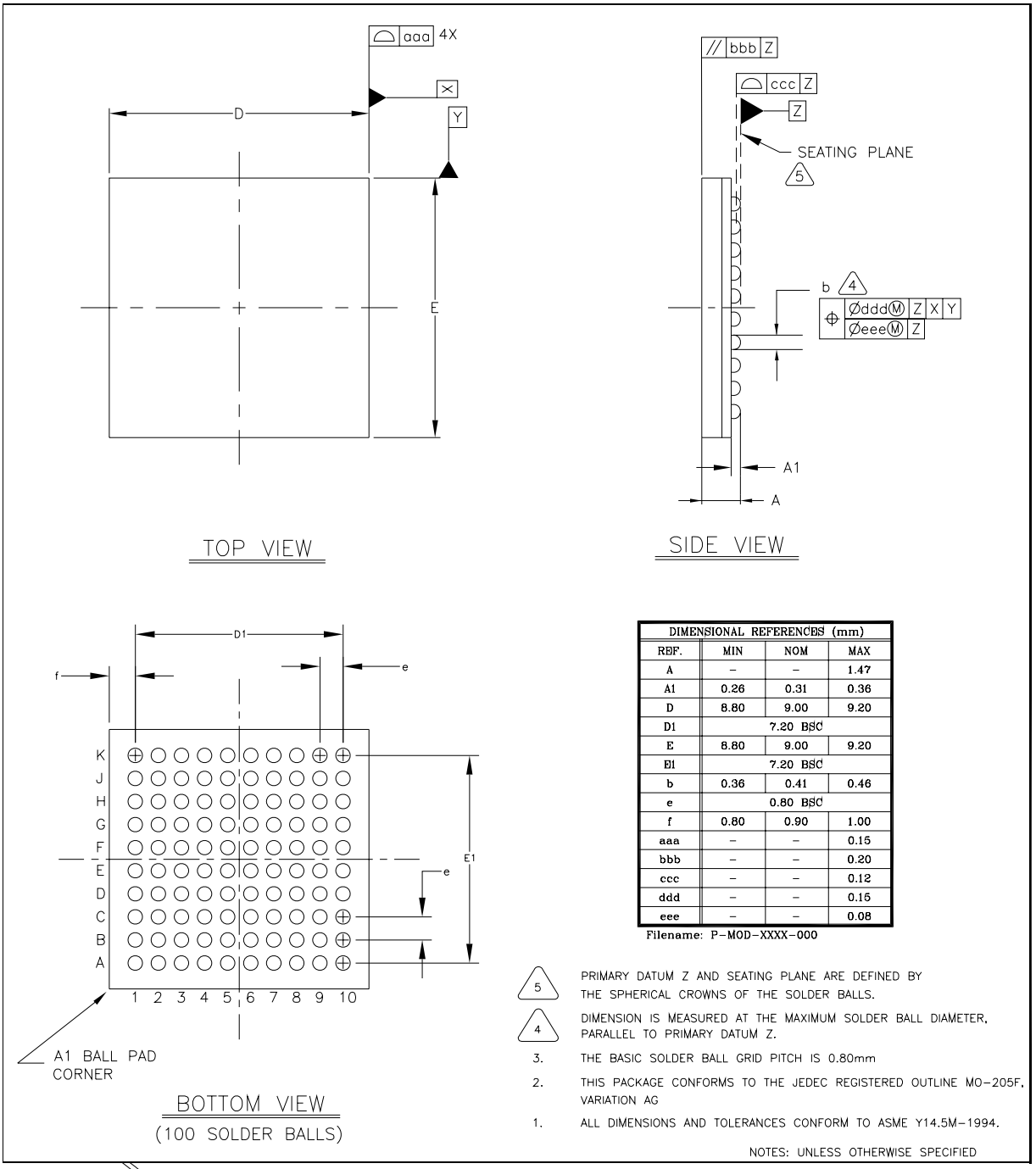
3. THE BASIC SOLDER BALL GRID PITCH IS 0.80mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-219E.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 19: 120-Ball Mechanical Drawing



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.47
A1	0.26	0.31	0.36
D	8.80	9.00	9.20
D1		7.20 BSC	
E	8.80	9.00	9.20
E1		7.20 BSC	
b	0.36	0.41	0.46
e		0.80 BSC	
f	0.80	0.90	1.00
aaa	–	–	0.15
bbb	–	–	0.20
ccc	–	–	0.12
ddd	–	–	0.15
eee	–	–	0.08

Filename: P-MOD-XXXX-000

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 0.80mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-205F, VARIATION AG

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

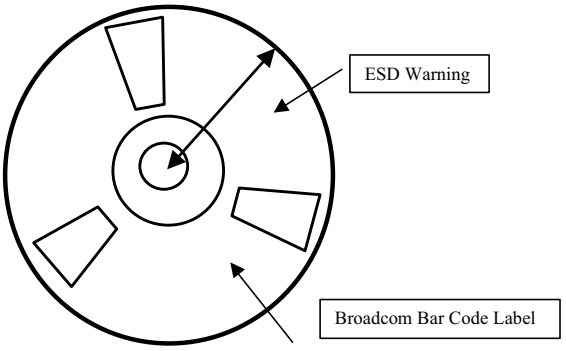
NOTES: UNLESS OTHERWISE SPECIFIED

Figure 20: 100-Ball Mechanical Drawing

TAPE AND REEL SPECIFICATION

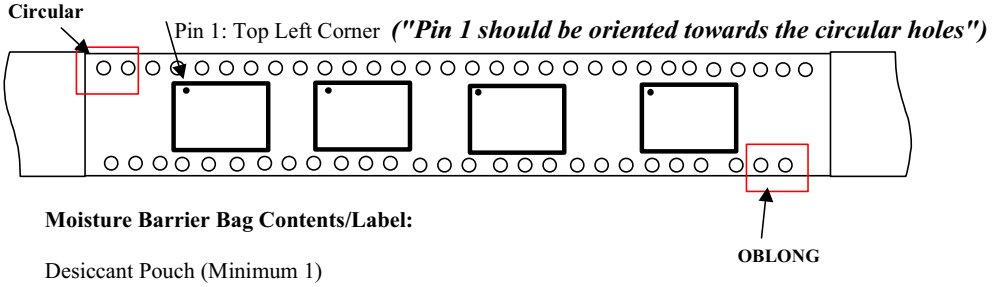
Reel/Labeling/Packing Specification

Reel Specifications:



Device Orientation/Mix Lot Number:

Each Reel may contain up to two individual lot numbers; this is independent of date code.
These individual lots must be labeled on the box, moisture barrier bag and reel.



Moisture Barrier Bag Contents/Label:

Desiccant Pouch (Minimum 1)
Humidity Indicator (Minimum 1)
Reel (Maximum 1)

Figure 21: Reel/Labeling/Packing Specification

Table 15: Reel/Labeling/Packing Specifications

Item	*Value*	*Unit*
Max quantity per reel	2000	–
Reel diameter	13	inches
Hub diameter	4	inches
Tape width	16	mm
Pitch	12	mm

Section 5: Ordering Information

Table 16: Ordering Information

Part Number	*Package*	*Ambient Operating Temperature*
BCM2042A4KFB	Commercial 88-FBGA	0°C to 70°C
BCM2042MA4KFB	Commercial 120-FBGA	0°C to 70°C
BCM2042A4KFBG	RoHS Compliant 88-FBGA	0°C to 70°C
BCM2042MA4KFBG	RoHS Compliant 120-FBGA	0°C to 70°C
BCM2042NA4KFBG	RoHS Compliant 100-FBGA	0°C to 70°C

Broadcom Corporation

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