General Description

The ARF2496K is a low-power, high-integrated single chip RF transceiver using 0.18μm mixed-mode CMOS process optimized for ISM 2.4GHz wireless systems. The ARF2496K contains receiver, transmitter, voltage-controlled oscillator (VCO) and phase-locked loop (PLL). The device is expressly designed for low power consumption. Specific expertise has been applied to save current consumption and thus to extend the battery life, which is of most importance to the portable wireless consumer applications. Power saving mode has also been implemented to further reduce the power consumption. The receiver contains a low-noise amplifier (LNA), a high-frequency mixer, a received signal strength indicator (RSSI), a channel select filter, a limiting amplifier, a demodulator and a data slicer with clock recovery. Current consumption of receive mode is 18mA and transmit mode is 10.5mA at –5dBm output.

Applications

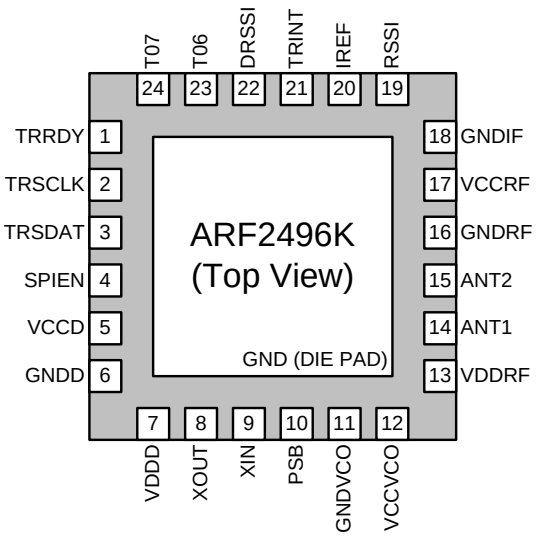
- Wireless Mouse, Presenters, Keyboards and Gamepad
- Wireless VOIP and Headsets
- Remote Controls
- Toys
- Home Automation
- Consumer Electronics

Features

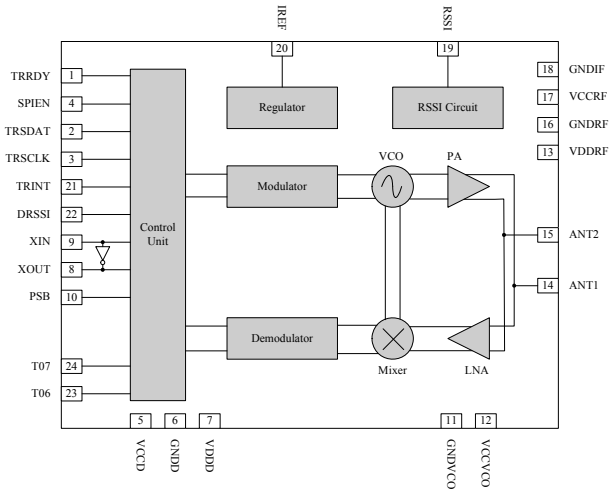
- 2.4GHz GFSK RF transceiver
- Operates in unlicensed worldwide Industrial, Science and Medical (ISM) band (2.400GHz ~ 2.527GHz)
- Sensitively up to –93 dBm
- Output power up to 0 dBm
- Low-noise amplifier, power amplifier, modern and data slicer/recovery on chip
- Low operation voltage from 1.9V to 3.6V
- Low current consumption, 8.2mA@-20dBm at TX mode and 18mA at RX mode
- Programmable 250kbps/1Mbps transfer bit-rate
- Configurable preamble, scramble, source address, destination address and CRC generation
- Programmable data payload length from 1-byte to 32-byte
- 3-wire SPI interface for device configuration
- Complete RSSI function on chip
- Operation temperature range from –40 °C to +85 °C
- Compact 24-pin QFN 4x4 mm package

Table of Contents

Pin Configuration



Block Diagram



Pin Description

Pin No	Pin Name	I/O	Active State	Description
1	TRRDY	I	High	Digital input. Assert to set the ARF2496K to Active Mode.
2	TRSCLK	I/O	N/A	Digital input at Burst Mode and digital output at Direct Mode. Clock signal of the SPI/FIFO interface.
3	TRSDAT	B	N/A	Digital input/output. Data signal of the SPI/FIFO interface.
4	SPIEN	I	High	Digital input. Enable signal of the SPI interface.
5	VCCD	P	N/A	Digital power pin. +3.3V_{DC}.
6	GNDD	P	N/A	Digital ground.
7	VDDD	P	N/A	Digital decoupling power pin.
8	XOUT	O	N/A	Crystal output pin.
9	XIN	I	N/A	Crystal input pin.
10	PSB	I	Low	Digital input. Assert to force ARF2496K to enter Power-Saving Mode or Power-Down Mode, depended on the state of TRRDY.
11	GNDVCO	P	N/A	VCO ground.
12	VCCVCO	P	N/A	VCO power pin. +3.3V_{DC}.
13	VDDRF	P	N/A	RF decoupling power pin.
14	ANT1	B	N/A	RF signal pin. Antenna I/F.
15	ANT2	B	N/A	RF signal pin. Antenna I/F.
16	GNDRF	P	N/A	RF ground.
17	VCCRF	P	N/A	RF power pin. +3.3V_{DC}.
18	GNDIF	P	N/A	Analog IF ground.
19	RSSI	O	N/A	Analog output. Analog RSSI output pin.
20	IREF	I	N/A	Analog input. Reference current input pin.
21	TRINT	O	High	Digital output. Asserted when transmitting or receiving is accomplished.
22	DRSSI	O	N/A	Digital output. Digital RSSI output.
23	T06	N/A	N/A	Reserved for future testing.
24	T07	N/A	N/A	Reserved for future testing.

Electrical Specifications

Absolute Maximum Ratings

Rating	Minimum	Maximum
Storage temperature range	-55 ℃	+125 ℃
VCC	-0.4 V	+3.6 V
Other terminal voltages	VSS-0.4 V	VCC+0.4 V

Recommend Operating Conditions

Operating Condition	Minimum	Maximum
Operating temperature range	-40 ℃	+85 ℃
VCC	1.9 V	3.6 V

DC Electrical Characteristics

Parameter	Test Condition		MIN.	TYP.	MAX.	Unit
V_{IL} (Digital)	VCC = 3.3V		-0.4	-	0.8	V
V_{IH} (Digital)			0.7VCC	-	VCC+0.4	V
V_{OL} (Digital)			-	-	0.4	V
V_{OH} (Digital)			VCC-0.4	-	-	V
Current Consumption	Power-Down Mode		-	400	-	nA
	Power-Saving Mode		-	1	-	μA
	Stand-By Mode	f_{sys}=4MHz	-	12	-	μA
		f_{sys}=16MHz	-	22*		μA
	Transmit Mode	0 dBm	-	13	-	mA
		-5 dBm	-	10.5	-	mA
		-10 dBm	-	9	-	mA
		-20 dBm	-	8.2	-	mA
	Receive Mode	250 kbps	-	18	-	mA
		1 Mbps	-	19	-	mA

*: The current consumption is depended on the CL of the external crystal; please refer to the section – "Global Clock" for detailed information.

AC Electrical Characteristics

Parameter	Description		MIN.	TYP.	MAX.	Unit
f_{sys}	Crystal frequency		4/8/12/16/20*1			MHz
f_{dev}	Frequency deviation		-	±160	-	kHz
RF General Parameter						
Data Rate	Burst Mode		>0	-	1000	kbps
	Direct Mode		250	-	1000	kbps
Channel Spacing			-	1	-	MHz
RF Transmitter Parameter						
Transmit Output Power			-	0	4	dBm
Transmit Output Power Control Range			16	20	-	dBm
Transmit Output Power Control Step			-	5	-	dB
20dB Bandwidth for Modulation Carrier			-	1000	-	kHz
2nd Adjacent TX Power 2MHz			-	-	-20	dBm
3rd Adjacent TX Power 3MHz			-	-	-40	dBm
RF Receiver Parameter						
Sensitivity	0.1% BER @ 250kbps		-	-93	-	dBm
	0.1% BER @ 1Mbps		-	-85	-	dBm
C/I Co-Channel	250kbps		-	9	-	dB
	1Mbps		-	5	-	dB
C/I 1MHz	250kbps		-	-20	-	dB
	1Mbps		-	1	-	dB
C/I 2MHz	250kbps		-	-36	-	dB
	1Mbps		-	-22	-	dB
C/I 3MHz	250kbps		-	-45	-	dB
	1Mbps		-	-35	-	dB
C/I_{Image}	250kbps		-	-30	-	dB
	1Mbps		-	-30	-	dB

*1: 16MHz crystal frequency is required if 1Mbps is employed.

Function Description

Internal State and Operation Mode

Depending on the states of pin PSB, TRRDY and SPIEN, the ARF2496K has the specific internal state and operation mode; User can force the ARF2496K to enter the specific mode for their power management implement. There are five modes of the ARF2496K operation mode; they are Power-Down Mode, Power-Saving Mode, Stand-By Mode, SPI-Access Mode and Active Mode. Figure-1 shows the internal state and operation Mode transferring of the ARF2496K; Table-1 lists the states of PSB, TRRDY and SPIEN for the specific modes.

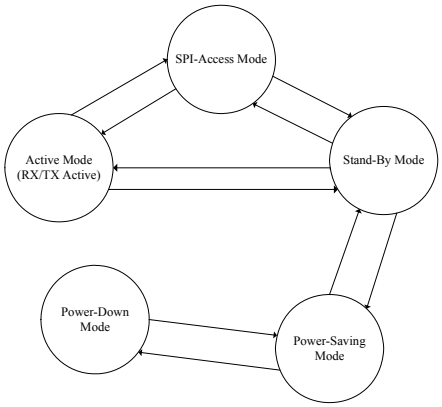


Figure-1 Internal State and Operation Mode

Operation Mode	Pin State		
	PSB	SPIEN	TRRDY
Power-Down Mode	Low	Don't Care	High
Power-Saving Mode	Low	Low	Low
Stand-By Mode	High	Low	Low
SPI-Access Mode	High	High	Low
Active Mode	High	Low	High

Table-1 States of PSB, TRRDY and SPIEN for Specific Operation Mode

Power-Down Mode

Power-Down Mode enables the most low current consumption operation. The typical current consumption of this mode is less than 400nA. The ARF2496K can be forced to this mode to reduce the power consumption, extending the battery life for portable device. The memory content of the ARF2496K, FIFO content and register content for example, will not be maintained in this mode. Typically, the ARF2496K will process the internal reset when it re-active from Power-Down Mode, same operation as that when power-on the ARF2496K. The internal reset duration is 120ms, any operation for ARF2496K should be handled after the specific time; the timing diagram of the internal reset reactive from Power-Down Mode or power-on is shown in Figure-2.

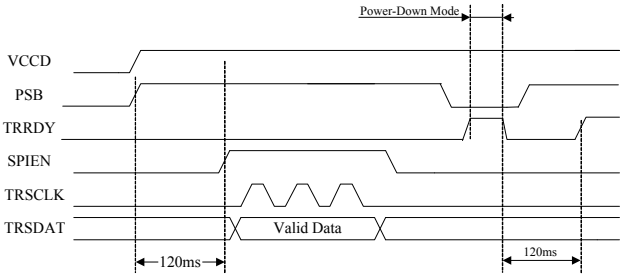


Figure-2 Timing of Power-Down Mode of the ARF2496K

The state transferring of PSB and PSB should follow the order of, assert the state of PSB and then the state of TRRDY to force the ARF2496K to Power-Down Mode; de-assert the state of TRRDY and then the state of PSB to wake up the ARF2496K from Power-Down Mode.

Power-Saving Mode

Power-Saving Mode enables the user to force the ARF2496K to halt the operation of the most internal units and be able to re-active within the short time from this mode. The typical current consumption of this mode is less than 1μA. The memory content of the ARF2496K, FIFO content and register content for example, will be maintained in this mode. The typical re-active time from this mode is 1.5ms; refer to Figure-3 for the detailed timing information.

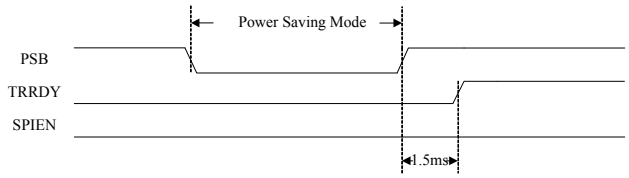


Figure-3 Timing of Power-Saving Mode of the ARF2496K

Stand-By Mode

The ARF2496K will stay in Stand-By Mode if there is no transaction is processing and power saving control is disabled. Particularly unnecessary internal units of ARF2496K for this mode will be shut down for maximum power saving, to minimum the power consumption and extend the battery life for the portable device. The ARF2496K will be forced its operation mode to SPI-Access mode or Active Mode automatically if any SPI or FIFO accesses is processing with no waiting delay. The amount of the power consumption is depended on crystal frequency, 12μA at 4MHz and 22μA at 16MHz for example. The memory content is maintained at Stand-By Mode.

SPI-Access Mode

The ARF2496K will stay in the SPI-Access Mode when the configuration registers are accessed via SPI interface (TRSCLK, TRSDAT and SPIEN pins). Before any data transmitting or receiving, the configuration registers of the ARF2496K should be configured as well. The detailed information is described in the section, Device Registers.

Active Mode

The ARF2496K will be forced to Active Mode if (1) the master controller writes the transmitting data into the FIFO of the ARF2496K for transmitting at TX Mode or (2) the master controller asserts the state of TRRDY to start receiving the RF data in the air at RX Mode.
The typical current consumption of Active Mode is detailed listed in the section, Electrical Specifications, by the specific operation condition.
By setting the state of the bit 7 of register 0x00, the master controller can force the ARF2496K to TX Mode or RX Mode.
Depending on the state of the bit 2 of register 0x02, the master controller can configure the ARF2496K to work in Direct Mode or Burst Mode. Detailed information of Direct Mode and Burst Mode is descried in the section, Data Transfer Modes.

Operation Mode and Pin Behavior

Depended on the operation mode, the pin, TRSDAT of the ARF2496K has the different configuration. Table-2 lists the TRSDAT configuration corresponding to the specific operation modes.

Mode	Input Pins			Configuration of TRSDAT
	PSB	SPIEN	TRRDY	
Power-Down	0	X	1	Input
Power-Saving	0	0	0	Input
Stand-By	1	0	0	Input
SPI-Access	1	1	0	Input/Output
Active (TX)	1	0	1	Input
Active (RX)	1	0	1	Output

Table-2 Configuration of TRSDAT at Different Operation Modes.

Data Transfer Modes

Depended on the states or values of, (1) bit 7, RXBTX, of register 0x00, (2) bit 6, Direct, of register 0x02, (3) bit 0~3, MBPR, of register 0x06, the user can configure the ARF2496K to work in the specific mode for the various applications.
Table-3 lists the modes of the data transmitting and receiving by different settings.

RXBTX	DIRECT	MBPR	Mode
0	0	X*1	RX/Direct Mode
0	1		RX/Burst Mode
1	0		TX/Direct Mode
1	1	0	TX/Burst Mode
1	1	N*2	TX/Multi-Burst Mode

*1: 'X' means don't care.

*2: 'N' means the value of 1~15.

Table-3 Data Transfer Modes

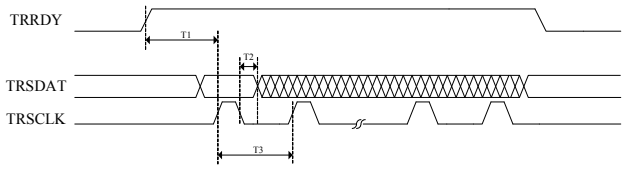
RX/Direct Mode

At RX/Direct Mode, the ARF2496K works as the traditional RF receiver.
The master controller should handle the data receiving by itself. The ARF2496K will not take care of the Sync. Word Handle, Preamble Handle, Address Filtering, De-Scramble and CRC checking; all of these operation should be taken care by the master controller.
To receive the RF data, the master controller should take the steps as following;

(1) Set the RXBTX value to 0.
(2) Set the Direct Value to 0.

(3) Assert the state of TRRDY.
(4) If the state of TRINT is asserted, the master controller should start to read out the received data via pins TRSCLK and TRSDAT with 1Mbps bit-rate.

Figure-4 shows the timing of the data reading from the ARF2496K at RX/Direct Mode.



Item	Description	Min.	Typ.	Max.	Unit
T1	TRRDY to TRCLK time		250		µs
T2	Data bit delay time		15		ns
T3	TRSCLK cycle time (1Mbps)		1		µs
	TRSCLK cycle time (250kbps)		4		

Figure-4 Timing at RX/Direct Mode

RX/Burst Mode

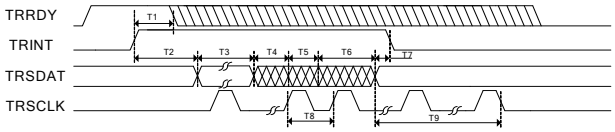
At RX/Burst Mode, the ARF2496K not only operates as a traditional RF receiver but also handles Preamble, Sync. Word, Address Filtering, De-Scramble and CRC Check. To receive data at this mode, the master controller should follow the steps as;

(1) Set RXBTX to 0.
(2) Set Direct to 1.
(3) Set the Device Address in the register 0x0E~0x12 to the specific value; which specify the communication node address of itself.
(4) Set the data payload size, DATLNG, in the register 0x05 to the specific value.
(5) Assert TRRDY to turn on the RF front-end circuit.
(6) Wait for the asserted state of TRINT.
(7) If the state of TRINT is asserted, means that there is RF data received and restored in the FIFO of the ARF2496K; the master controller may read out the data from the FIFO through FIFO interface by using pins TRSCLK and TRSDAT.

Once the state of TRINT is asserted, the master controller may de-assert the state of TRRDY to turn off the RF front-end circuit; to save the current consumption.

Unless the valid data in the FIFO is read out, the ARF2496K can't be able to receive the RF data in the air, even the state of TRRDY is keeping asserted; it means, the master controller should read out the valid data in the FIFO as soon as possible, or the data of next transaction in the air will be lost.

Figure-5 shows the detailed timing information of FIFO data reading for RX/Burst Mode.



Item	Description	Min.	Typ.	Max.	Unit
T1	TRRDY to TRINT time	0			ns
T2	TRINT to first bit time	0			ns
T3	Pre-Dummy cycle		2		Bit
T4	Source Address cycle	0		40	Bit
T5	Reverse cycle*		8		Bit
T6	Data bit cycle	8		256	Bit
T7	Last bit inactive to TRINT time	0		0.5	Bit
T8	TRSCLK cycle time	500			ns
T9	Post-Dummy cycle		3		Bit

*: The cycle is valid only when TX/Multi-Burst Mode is employed in the transmitter.

Figure-5 Timing of RX/Burst Mode

TX/Direct Mode

At TX/Direct Mode, the ARF2496K works as a traditional RF transmitter. The processes of Preamble, Sync. Word, Address Generation, Scramble Generation and CRC Generation should be taken care of by the master controller itself.

For this mode, transmitting bit-rate of 1Mbps/250kbps is both accepted by the ARF2496K. Therefore, the master controller should transfer the data to the ARF2496K with 1Mbps/250kbps bit-rate and the ARF2496K will send it out to the air in 1Mbps/250kbps bit-rate.

To transmit data at this mode, the master controller should have the following steps;

(1) Set RXBTX to 1.
(2) Set Direct to 0.
(3) Assert TRRDY to turn on the RF front-end circuit.
(4) Process the Dummy Cycle; to de-assert TRSDAT and

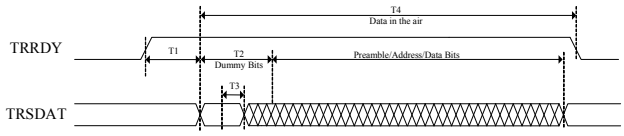
wait for 3-bit time with no operation.

(5) Start to transfer data bits to the ARF2496K with 1Mbps bit-rate.

(6) De-assert the state of TRRDY if the data transfer to the ARF2496K is accomplished.

The maximum TRRDY assertion time at this mode should be not longer than 4ms; for each 4ms transmitting, the master controller should de-assert the state of TRRDY for internal calibration of the ARF2496K; typical internal calibration time is 200μs.

Figure-6 shows the detailed timing information for the data transfer to the ARF2496K.



Item	Description	Min.	Typ.	Max.	Unit
T1	TRRDY to first bit time		250		μs
T2	Dummy cycle		3		bit
T3	Hold time		15		ns
T4	Transmitting duty time			4	ms

Figure-6 Timing of TX/Direct Mode

TX/Burst Mode

At this mode, the ARF2496K will package the following fields to the packet and transmit to the air;

(1) Preamble, automatic generating by the ARF2496K.

(2) Sync. Word, automatic generating by the ARF2496K.

(3) Address Field, automatic attached by the ARF2496K or provided by the master controller, depended on the bit 5 of the configuration register 0x05.

(4) Data Payload; provided by the master controller, through the FIFO interface.

(5) Scramble, automatic generating by the ARF2496K, if enabled.

(6) CRC, automatic generating by the ARF2496K, if enabled.

To transmit data at this mode, the master controller should follow the following steps;

(1) Set RXBTX to 1.

(2) Set Direct to 1.

(3) Set Destination Address in the register 0x09~0x0D to the specific value (must equal to the value of Device Address at receiver side).

(4) Set the data payload size, DATLNG, in the register 0x05 to the specific value (must same as at the receiver side).

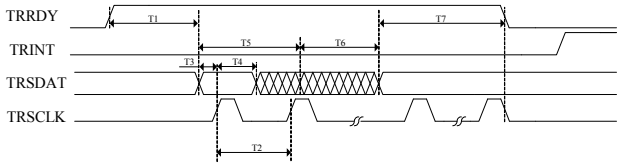
(5) Assert TRRDY.

(6) Transfer the data bit to the ARF2496K following the timing as shown in Figure-7.

(7) De-assert TRRDY.

(8) Optionally wait the assert state of TRINT.

The ARF2496K will start to transmit the packet to the air once the state of TRRDY is de-asserted and when it is accomplished, TRINT is asserted.



Item	Description	Min.	Typ.	Max.	Unit
T1	TRRDY to first bit time	20			μs
T2	TRSCLK cycle time	500			ns
T3	Setup time		15		ns
T4	Hold time		15		ns
T5	Destination Address cycle	0		40	bit
T6	Data cycle	8		256	bit
T7	Post-Dummy cycle		3		bit

Figure-7 Timing of TX/Burst Mode

TX/Multi-Burst Mode

At this mode, the ARF2496K works as at TX/Burst Mode except that the ARF2496K will automatically re-transmit the current packet for specific times which specified in MBPR.

The zero value of MBPR will disable the auto re-transmit function and the value of 1~15 in MBPR will enable the auto re-transmit function; value of 1 in MBPR enable the ARF2496K transmits the current packet two times totally and value of 2 is 3 times and so on.

This function will reduce the packet lost probability in the noisy communication environment.

There is no any information contained inside the repeating packets indicating the current packet is the re-transmitting packet or the new packet; the MCU should check this by itself.

Figure-8 shows the concept timing at this mode.

Figure-8 Timing at TX/Multi-Burst Mode (MBPR = 1)

Timing of TRRDY to TRRDY at RX Mode

If there is a FIFO Read-Access following a FIFO Read-Access, there should be a blocking time to blocks two operation for internal timing order.
Figure-9 shows the detailed timing information.

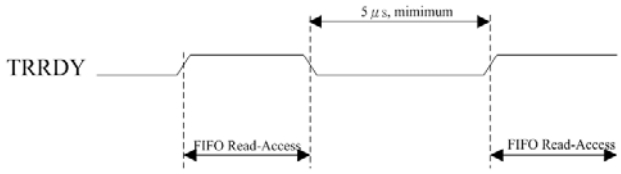


Figure-9 Timing between two FIFO Read-Accesses

Advantage by Using Burst Mode

By using Burst Mode, there are three obvious advantages;

(1) Reduce the current consumption. At Direct Mode, the master controller should assert the state of TRRDY from the beginning of data transmitting to the air and once the state of TRRDY is asserted, the RF front-end circuit is turned on, it consumes larger current consumption to transmit the packet which has the same contents than at Burst Mode, since that at Burst Mode, RF front-end circuit is turned on only when the packet is ready to transmit to the air, not from the assert state of TRRDY.

(2) Minimize the requirement of the master controller performance. At Burst Mode, the bit-rate of data access to/from the ARF2496K is not required to equal to 1Mbps but it requires if at Direct Mode, the user may employ the low-level, low-cost master controller for the application.

(3) Automatic packet handle at Burst Mode lessens the effort of the master controller comparing to Direct Mode.

Packet Format

The typical packet format sent by the transmitter at Burst Mode is shown in Figure-10; it contains Preamble, Address, Burst Counting, Data and CRC.

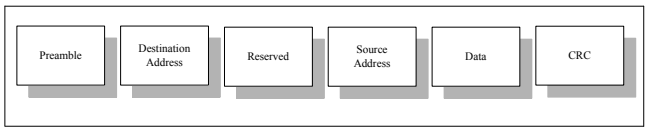


Figure-10 Packet Format at Burst Mode

Preamble

This field is required both at Burst Mode and Direct Mode.
The ARF2496K recognizes the packet coming is in accordance with this field, both for Burst Mode and Direct Mode.
The content of this field is configured by the interlaced binary bit '1' and '0'. Depended on the value of the first bit of Destination Address Field, it takes the different arrangement; if the first bit of Destination Address is binary '1', the last bit of Preamble field should be a binary '0', otherwise, it should be binary '1'.
At Burst Mode, the master controller can configure Preamble length by setting PAL in the register 0x06 and automatically generates at transmitting side and removes at receiving side by the ARF2496K.
At Direct Mode, the master controller should generate and remove this field by itself.

Destination Address

This field identifies the receiver address which specified in the register 0x0E~0x12 at receiving side.
This length of this field can be in the range of 1-byte to 5-byte. The ARF2496K as a receiver will check this field to determinate it should receive this packet in or not; if the content of this field doesn't match to its Device Address, the packet will be dropped.
At Burst Mode, the ARF2496K as a transmitter, the master controller can configure the length of this field by setting ADDRLNG to the specific value in the register 0x08; the master controller may offer the content this field to the ARF2496K by (1) setting the register 0x09~0x0D to the specific value or (2) writing it at Destination Address cycle as shown in Figure-7; by setting DESADDRS in the register 0x05, the ARF2496K will determinate which

source should be referencing.
At Burst Mode, this field is generated at the transmitting side and removed at the receiving side by the ARF2496K automatically. At Direct Mode, the master controller should handle it by itself.

Reserved

This field will be employed at TX/Multi-Burst Mode only. The length of this field is 1-byte.
If the value of MBPR is not zero, this field will be inserted into the transmitting packet. This byte is reserved; any value of this byte shouldn't be ignored.

Source Address

This field carries Device Address value of the transmitter. This field can be employed by setting TSADDRON to 1 in the register 0x05. This field is automatic generated by the ARF2496K, if enabled.

Data

This field contains the content of transmitting data.
The size of this field can be in range of 1-byte to 32-byte; the master controller can configure it by setting DATLNG in the register 0x05.

CRC

This field carries the CRC-16 error detection information. The value of this field is obtained by the content of Data field. At Burst Mode, this field is automatically generating and checking by the ARF2496K, if enabled by setting CRCEN to 1 in the register 0x02.
If any error detected by CRC check, the packet will be dropped if RXCRCERR is 0.
The polynomial is X^16+X^12+X^5+1.

SPI Interface

The ARF2496K can be configured by setting internal registers through SPI interface.

SPI Interface Pins

Table-4 lists the pins of the ARF2496K which employed by the SPI interface.

Pin Name	Pin No.	Description
SPIEN	4	Assert state of this pin will active the SPI interface.
TRSCLK*	2	The clock signal of the SPI interface; the clock signal of the SPI interface should be provided by the master controller. The address bits during SPI access is latched at rising edge. The data bit during SPI writing is latched at rising edge and appeared at falling edge during SPI reading.
TRSDAT*	3	The data signal of the SPI interface.

*: The pin is shared with FIFO interface.

Table-4 Pin List of SPI Interface

SPI Packet Format

Figure-11 shows the packet format of SPI interface.

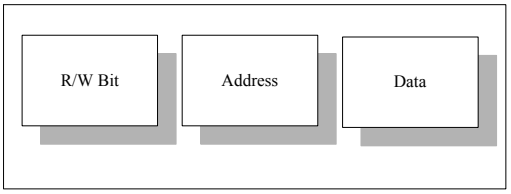
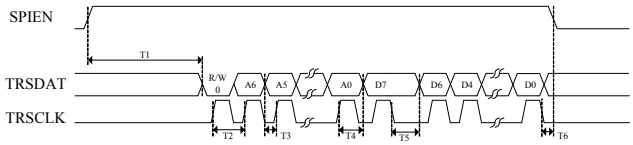


Figure-11 SPI Packet Format

R/W Bit
This bit identifies the current SPI access is for register reading or for register writing; if this bit is binary '0', the current access is for register reading, otherwise, it is for register writing.
Address
The length of this field is 7-bit. This field identifies the address of the target register for the current access.
Data
The length of this field is 8-bit. This field carries the data writing to the target register or reading from the target register.

Timing of SPI Read-Access

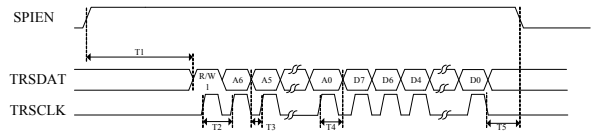


Item	Description	Min.	Typ.	Max.	Unit
T1	SPIEN to first bit time	20			µs
T2	TRSCLK cycle time	200			ns
T3	Setup time	10			ns
T4	Hold time	10			ns
T5	Data bit hold time			20	ns
T6	Last bit to SPIEN time	50			ns

Figure-12 Timing of SPI Read-Access

The pin of the master controller corresponding to TRSDAT should be configured as the input pin during data phase, D7~D0, of the SPI Read-Access.

Timing of SPI Write-Access



Item	Description	Min.	Typ.	Max.	Unit
T1	SPIEN to first bit time	20			µs
T2	TRSCLK cycle time	200			ns
T3	Setup time	10			ns
T4	Hold time	10			ns
T5	Last bit to SPIEN time	50			ns

Figure-13 Timing of SPI Write-Access

Timing of TRRDY to SPIEN

If there is any SPI access following a FIFO Write-Access (at TX Mode), there should a blocking time to block these two operations. Figure-14 shows the detailed timing information.

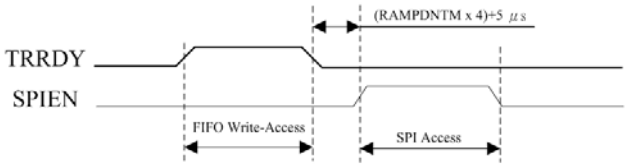


Figure-14 Timing of TRRDY to SPIEN

RSSI Function

The ARF2496K has the most complete RSSI function for the relative power estimation of the allocated channel. Figure-15 shows the equivalent Diagram of the RSSI function.

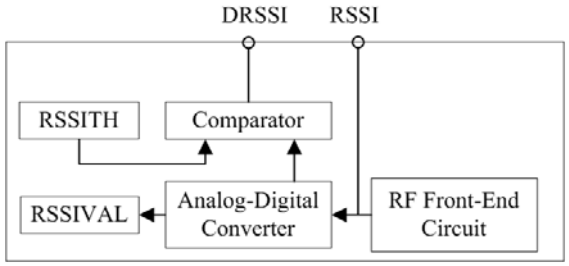


Figure-15 Equivalent Diagram of RSSI Function

Once the master controller sets RSSI_CCA in the register 0x03 to 1, the ARF2496K will start to process the RSSI refresh operation for the current channel.
The refreshed RSSI value is then appeared on the pin, IRSSI, in analog output. The refreshed RSSI value is also forwarded to the ADC to obtain a digital RSSI value.
The digital RSSI value is stored in the RSSIVAL in the register 0x04. Also, the digital RSSI value is compared to RSSITH in the register 0x03, if the digital RSSI value greater than the RSSITH, the pin, DRSSI, will be asserted.
RSSI_CCA in the register 0x03 will be reset to 0 if the RSSI refresh operation is accomplished; the master controller should take the state of DRSSI and the value of RSSIVAL is valid when RSSI_CCA is backing to 0.
The DRSSI output state will be disabled if the state of TRRDY is asserted.
The RRSI function can be only employed at Direct Mode.

Output Power Ramp-Up/Down Function

In order to avoid the transmit spectrum re-grown, the power ramp-up and ramp-down mechanism is adopted in

the ARF2496K. After the PLL is locked for transmission, the output power of the power amplifier is ramp-up stage by stage to the specific power which determined in the RF_POWER register. Once the transmission is accomplished, the output power of the power amplifier is ramp-down smoothly.
The ramp-up function will increase the output power stage by stage within the specific time which is specified in PRAMPUPTM register; similarly the ramp-down function will decrease the output power stage by stage within the specific time which is specified in PRAMPDNTM register. Figure-16 shows the concept of the ramp-up and ramp-down operation. This figure assumes that the output power specified in RF_POWER register is 0dBm and the time of ANATONTM is not zero which is specified in the ANATONTM register.

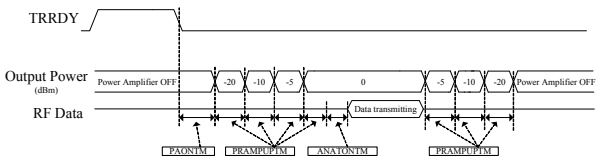


Figure-16 Ramp-Up/Down Function and TRRDY

PLL Pre-Turn-On Time

At TX mode, the PLL will be turned on at the falling edge of TRRDY and the data is transmitted after the frequency PLL is locked. This will take 200μs for the PLL frequency lock.
To turn-on the PLL before the falling edge of TRRDY, the user may set the PLL Pre-Turn-On Time in the register 0x14. Figure-17 shows the timing of the PLL Pre-Turn-On Time function.

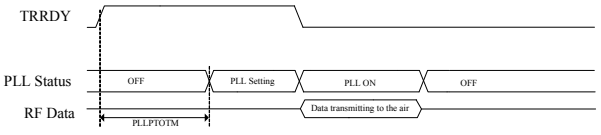


Figure-17 PLL Pre-Turn-On Function

Antenna Interface

The ARF2496K has a differential RF signal antenna interface, ANT1 and ANT2. The user may use a simple current combiner to combine the differential signal to the signal-end signal. The antenna for the ARF2496K should has the impedance of 50Ω.
The sample connection of this interface is shown in the section, Application Circuit.

Global Clock

To supply the global clock for the ARF2496K, the user should follow the connection shown in the section, Application Circuit.
The user may use the low-cost crystal of its frequency is 4, 8, 12, 16 or 20MHz with maximum frequency tolerance +/- 30ppm. Table-5 shows the requirement of the crystal electrical specification.
The total load capacitance seen between the crystal terminals should equal C_L for the crystal to oscillate as the specific frequency.

$$C_L = \frac{1}{\frac{1}{C9} + \frac{1}{C10}} + C_{parasitic}$$

The default setting for the global clock frequency is 16MHz; to use other frequencies as the global clock, the user should specify the value of FXTAL in the register 0x01 corresponding to the crystal frequency.

Frequency tolerance	ESR	C_0	C_L
± 30ppm	100Ω	7.0pF maximum	12pF

Table-5 Requirement of the Crystal Electrical Specification

The typical C_L value for the ARF2496K is 12pF and maximum is up to 20pF. When the crystal with C_L=12pF is using, the typical Stand-By Mode current consumption by 16MHz clock is 22μA and rising to 32μA if C_L=20pF.

Power Supply

The power supply for the ARF2496K should be clear and stable; a noisy power source should be avoided.
If the power source is noisy and unavoidable, using a switch regulator for example, to add a filter between theARF2496K and the power source is necessary.

Device Registers

Register List and Index

Address	Name	R/W	Power-On Value
0x00	T/R and Channel Index	R/W	0x28
0x01	Crystal Frequency and RF Power	R/W	0x03
0x02	Data Function Control	R/W	0x78
0x03	RSSI Function Control	R/W	0x87
0x04	RSSI Value	R-R/W	0x20
0x05	Data Format Control	R/W	0x0F
0x06	Multiple Burst Packet Repeat Control	R/W	0x30
0x07	Power Ramp Control	R/W	0x21
0x08	Address Length	R/W	0x03
0x09	Destination Address [7:0]	R/W	0x00
0x0A	Destination Address [15:8]	R/W	0x00
0x0B	Destination Address [23:16]	R/W	0x00
0x0C	Destination Address [31:24]	R/W	0x00
0x0D	Destination Address [39:32]	R/W	0x00
0x0E	Device Address [7:0]	R/W	0x00
0x0F	Device Address [15:8]	R/W	0x00
0x10	Device Address [23:16]	R/W	0x00
0x11	Device Address [31:24]	R/W	0x00
0x12	Device Address [39:32]	R/W	0x00
0x13	Reserved	R/W	0x00
0x14	PLL Pre-Turn-On Time	R/W	0x00
0x15	PLL Lock Time	R/W	0xB4
0x16	Reserved	R/W	0x00
0x17	Option	R/W	0x22
0x18	RX Turn On Time	R/W	0x04

T/R and Channel Index (0x00)

Bit	Name	R/W	Description
7	RXBTX	R/W	Control the mode of the ARF2496K; Binary 0: RX Mode Binary 1: TX Mode Relative Registers: N/A
6:0	CHNNUM	R/W	Channel Index; to select the operation frequency. The operation frequency will be; $F_{carrier}$ = 2400 + CHNNUM MHz Relative Registers: N/A Effective Modes: TX/Direct, TX/Burst, TX/Multi-Burst, RX/Direct, RX/Burst.

Crystal Frequency and Output Power (0x01)

Bit	Name	R/W	Description
7:5	Reserved	R/W	Reserved. Should be always binary 000.
4:3	RF_POWER	R/W	Output Power setting. Binary 00: -20dBm Binary 01: -10dBm Binary 10: -5dBm Binary 11: 0dBm Relative Registers: RAMPUPTM and RAMPDNTM. Effective Modes: TX/Direct, TX/Burst, TX/Multi-Burst.
2:0	FXTAL	R/W	Select the crystal frequency. Binary 000: 4MHz Binary 001: 8MHz Binary 010: 12MHz Binary 011: 16MHz Binary 100: 20MHz Others: Invalid Relative Registers: N/A Effective Modes: TX/Direct, TX/Burst, TX/Multi-Burst, RX/Direct, RX/Burst.

Data Function Control (0x02)

Bit	Name	R/W	Description
7	Reserved	R/W	Reserved. Should be always binary 0.
6	DIRECT	R/W	(Multi-)Burst Mode and Direct Mode control. Binary 0: Direct Mode Binary 1: (Multi-)Burst Mode Relative Register: N/A
5	DR*	R/W	Transaction bit-rate selection bit. Binary 0: 250kbps Binary 1: 1Mbps Relative Registers: N/A Effective Modes: TX/Direct, TX/Burst, TX/Multi-Burst, RX/Direct, RX/Burst.
4	SCRMEN	R/W	Scramble enable bit. Binary 0: Disable scramble. Binary 1: Enable scramble. Polynomial of Scramble: D^7+D^4+1 Relative Registers: N/A Effective Modes: TX/Burst, TX/Multi-Burst, RX/Burst.
3	CRCEN	R/W	CRC-16 enable bit. Binary 0: Disable CRC. Binary 1: Enable CRC. Relative Registers: RXCRCERR, CRCERR. Effective Modes: TX/Burst, TX/Multi-Burst, RX/Burst.
2:1	Reserved	R/W	Reserved. Should be always binary 00.
0	Reserved	R/W	Reserved. Should be always binary 0.

*: Note that either at Burst or Direct Mode, there is the exception register setting for bit-rate of 250kbps; please refer to the section, Exception Register Setting for 250kbps Communication Bit-rate, for detailed information.

RSSI Function Control (0x03)

Bit	Name	R/W	Description
7:5	Reserved	R/W	Reserved. Should be always binary 100.
4	RSSI_CCA	R/W	RSSI refresh control bit. Binary 0: Not refresh RSSI value. Binary 1: Refresh RSSI value. Relative Registers: RSSITH, RSSI_GM, RSSIVAL. Effective Modes: RX/Direct.
3:0	RSSITH	R/W	Threshold value of DRSSI output. Relative Registers: RSSI_CCA, RSSIVAL. Effective Modes: RX/Direct.

RSSI Value (0x04)

Bit	Name	R/W	Description
7:6	Reserved	R/W	Reserved. Should be always binary 00.
5	AGCEN	R/W	Auto Gain Control enable bit. Binary 0: Disable auto gain control Binary 1: Enable auto gain control Relative Registers: N/A Effective Modes: RX/Burst.
4	RSSI_GM	R/W	Gain mode selection for RSSI function. Binary 0: High gain mode Binary 1: Low gain mode Relative Registers: RSSITH, RSSI_GM, RSSIVAL. Effective Modes: RX/Direct.
3:0	RSSIVAL	R	RSSI value. Transformation of RSSI, RF power input and RSSIVAL is shown in appendix.

Data Format Control (0x05)

Bit	Name	R/W	Description
7	TSADDRON	R/W	Append source address in the transmitting packet. Binary 0: Not appended Binary 1: Appended The content of source address is equal to the device address of the transmitter. Relative Registers: RSADDR. Effective Modes: TX/Burst, TX/Multi-Burst.
6	RSADDR	R/W	Insert the source address before the FIFO data when read out FIFO data. Binary 0: Not insert Binary 1: Insert Relative Registers: TSADDRON. Effective Modes: RX/Burst.
5	DESADDRS	R/W	Destination Address reference source. The ARF2496K will append the destination address into the transmitting which taken from; Binary 0: Registers 0x09~0x0D Binary 1: Provided by the master controller, before the FIFO data writing in. Relative Registers: DESADDR. Effective Modes: TX/Burst, TX/Multi-Burst.
4:0	DATLNG	R/W	Number of data bytes in the packet. Binary 00000: 1Byte Binary 00001: 2 Bytes Binary 00010: 3 Bytes : : Binary 11111: 32 Bytes Relative Register: N/A Effective Modes: TX/Burst, RX/Burst, TX/Multi-Burst.

Multiple Burst Packet Repeat Control (0x06)

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td>OBFPREA</td><td>R/W</td><td>Insert zero symbols before preamble bits.
00: No zero symbols
01: Insert zero symbols
<table>
<tr><th># of zero symbols</th><th>PAL</th><th>DESADDRLNG</th></tr>
<tr><td>16</td><td>00</td><td>001</td></tr>
<tr><td>20</td><td>01</td><td>001</td></tr>
<tr><td>24</td><td>10</td><td>001</td></tr>
<tr><td>28</td><td>11</td><td>001</td></tr>
<tr><td>24</td><td>00</td><td>010</td></tr>
<tr><td>28</td><td>01</td><td>010</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>48</td><td>00</td><td>101</td></tr>
<tr><td>52</td><td>01</td><td>101</td></tr>
<tr><td>56</td><td>10</td><td>101</td></tr>
<tr><td>60</td><td>11</td><td>101</td></tr>
</table>
10: Insert Following patterns
<table>
<tr><th>Pattern</th><th>PAL</th><th>DESADDRLNG</th></tr>
<tr><td>0011001100110011 (16-bit)</td><td>00</td><td>001</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>00110011..00110011 (60-bit)</td><td>11</td><td>101</td></tr>
</table>
11: Insert following patterns
<table>
<tr><th>Pattern</th><th>PAL</th><th>DESADDRLNG</th></tr>
<tr><td>0000111100001111 (16-bit)</td><td>00</td><td>001</td></tr>
<tr><td>:</td><td>:</td><td>:</td></tr>
<tr><td>00001111..00001111 (60-bit)</td><td>11</td><td>101</td></tr>
</table>
Relative Registers: N/A
Effective Modes: TX/Burst, TX/Multi-Burst, RX/Burst.</td></tr>
<tr><td>4:5</td><td>PAL</td><td>R/W</td><td>Preamble Length.
Binary 00: 4 bits
Binary 01: 8 bits
Binary 10: 12 bits
Binary 11: 16 bits
Relative Registers: N/A
Effective Modes: TX/Burst, TX/Multi-Burst, RX/Burst.</td></tr>
<tr><td>3:0</td><td>MBPR</td><td>R/W</td><td>Packet re-transmitting times.
Binary 000: Not re-transmitting
Others: Re-transmitting times
Relative Register: N/A
Effective Modes: TX/Multi-Burst.</td></tr>
</table>

Power Ramp Control (0x07)

Bit	Name	R/W	Description
7:6	Reserved	R/W	Reserved. Should be always binary 00.
5:4	RAMPUPTM	R/W	Ramp-Up Time. Leave it as power-on value is suitable for most applications. Binary 00: 0μs Binary 01: 10μs Binary 10: 20μs Binary 11: 30μs Relative Registers: N/A Effective Modes: TX/Burst, TX/Multi-Burst.
3:2	RAMPDNTM	R/W	Ramp-Down Time. Leave it as power-on value is suitable for most applications. Binary 00: 5μs Binary 01: 10μs Binary 10: 20μs Binary 11: 30μs Relative Registers: N/A Effective Modes: TX/Burst, TX/Multi-Burst.
1:0	PAONTM	R/W	Power Amplifier turn-on delay Time. Leave it as power-on value is suitable for most applications. Binary 00: 0μs Binary 01: 50μs Binary 10: 100μs Binary 11: 150μs Relative Registers: N/A Effective Modes: TX/Burst, TX/Multi-Burst.

Address Length (0x08)

Bit	Name	R/W	Description
7:3	Reserved	R/W	Reserved. Should be always binary 00000.
2:0	ADDRLNG	R/W	Address length of DESADDR and DEVADDR. The length of the address setting to equal or more than 3-byte is strongly recommended. Binary 001: 1 byte Binary 010: 2 byte : : Binary 101: 5 Byte Others: Invalid Relative Register: DEVADDR, DESADDR. Effective Mode: TX/Burst, RX/Burst, TX/Multi-Burst.

Destination Address (0x09~0x0D)

The registers specify the destination address, from the register address 0x09 to 0x0D. The destination address should be set in these registers by byte ordering, byte 0 in the register address 0x09; byte 1 in the register 0x0A and so on. All of these registers are read/write-able and the initial value is zero.
Relative Register: ADDRLNG.
Effective Modes: RX/Burst.

Device Address (0x0E~0x12)

The registers specify the device address, from the register address 0x0E to 0x12. The device address should be set in these registers by byte ordering, byte 0 in the register address 0x0E; byte 1 in the register 0x0F and so on. All of these registers are read/write-able and the initial value is zero.
Setting the Device Address to all 0's or 1's or alternative 1's and 0's value is strongly recommended to be avoided.
Relative Register: ADDRLNG.
Effective Modes: TX/Burst, TX/Multi-Burst.

Reserved (0x13)

Bit	Name	R/W	Description
7:0	Reserved	R/W	Reserved. Should be always binary 00000000.

PLL Pre-Turn-On Time (0x14)

Bit	Name	R/W	Description
7:0	PLLPTOTM	R/W	PLL pre-turn-on time. Binary 00000000: Not pre-turn-on the PLL. Others: PLLPTOTM x 20μs Relative Registers: N/A Effective Modes: TX/Burst, TX/Multi-Burst.

PLL Lock Time (0x15)

Bit	Name	R/W	Description
7:6	PLLCLTM	R/W	PLL lock time; when MBPR is not zero, this lock timer will be inserted into two transactions; to re-lock the PLL frequency. Leave it as power-on value is suitable for most applications. PLL Lock Time = PLLCLTM x 50μs Relative Registers: MBPR Effective Modes: TX/Multi-Burst.
5:4	ANATONTM	R/W	Analog circuit turn-on time. The detail information is shown in the Figure-16. Leave it as power-on value is suitable for most applications. Binary 00: 0μs Binary 01: 10μs Binary 10: 20μs Binary 11: 40μs Relative Registers: N/A Effective Modes: RX/Burst, TX/Burst, TX/Multi-Burst.
3:0	Reserved	R/W	Reserved. Should be always binary 0100.

Reserved (0x16)

Bit	Name	R/W	Description
7:0	Reserved	R/W	Reserved. Should be always binary 00000000.

Reserved (0x17)

Bit	Name	R/W	Description
7:2	Reserved	R/W	Reserved. Should be always binary 001000.
1	TRINTLVL	R/W	Control bit of TRINT active level. Binary 0: Active level is low. Binary 1: active level is high. Relative Registers: N/A Effective Modes: RX/Burst, TX/Burst, TX/Multi-Burst.
0	DRSSILVL	R/W	Control bit of DRSSI active level. Binary 0: Active level is low. Binary 1: active level is high. Relative Registers: N/A Effective Modes: RX/Direct.

RX Turn On Time (0x18)

Bit	Name	R/W	Description
7:6	Reserved	R/W	Reserved. Should be always binary 000.
5:0	RXONTM	R/W	Receiver turn on time counting from the assert state of TRRDY. Leave it as power-on value is suitable for most applications. RX Turn On Time = (RXONTM x 16μs) + 18μs. Relative Registers: N/A Effective Modes: RX/Burst

Exception Register Setting for 250kbps Communication Bit-Rate

In order to obtain the best performance for works under 250kbps communication bit-rate (DR=0 in Register 0x02), the user should configure 4 registers more as described above listing following.

Register Address	Power-On Value	Value for 250kbps bit-rate
0x06	0x30	0xB0
0x39	0xBB	0xB8
0x4F	0x26	0x66
0x77	0x7C	0x5C

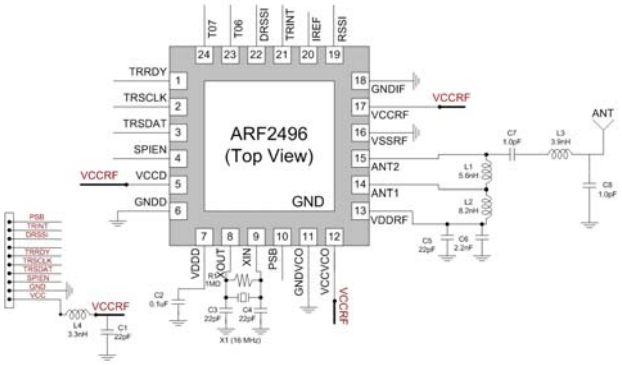
Exception Register Setting for Corner Condition Operation

By using ARF2496K under corner condition, the user should configure 2 registers for optimized operation.

Please refer to the following table.

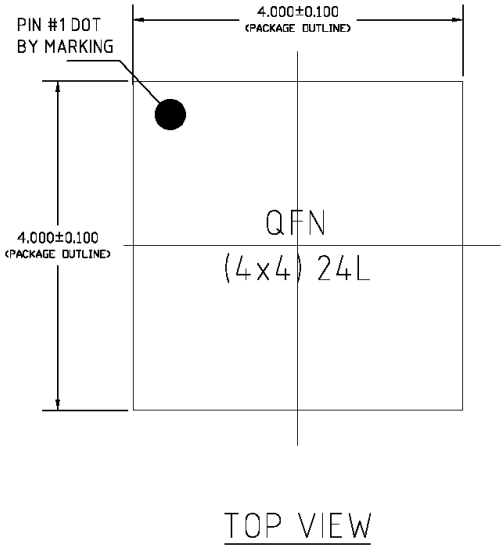
Register Address	Power-On Value	Optimized Value	Bit-rate Applied
0x39	0xBB	0xB9	1 Mbps
0x2C	0x19	0x18	250 kbps

Application Circuit



Component	Description	Value	Tolerance	Units
C1	Ceramic capacitor, 50V, NPO	22	±5%	pF
C2	Ceramic capacitor, 10V, X7R	0.1	±10%	µF
C3	Ceramic capacitor, 50V, NPO	22	±5%	pF
C4	Ceramic capacitor, 50V, X7R	22	±5%	pF
C5	Ceramic capacitor, 50V, NPO	22	±5%	pF
C6	Ceramic capacitor, 50V, NPO	2.2	±10%	nF
C7	Ceramic capacitor, 50V, NPO	1	±0.25pF	pF
C8	Ceramic capacitor, 50V, NPO	1	±0.25pF	pF
L1	Inductor, wore wound	5.6	±0.3nH	nH
L2	Inductor, wore wound	8.2	±0.3nH	nH
L3	Inductor, wore wound	3.9	±0.3nH	nH
L4	Inductor, wore wound	3.3	±0.3nH	nH
R1	Resistor	1	±5%	MΩ
X1	Crystal, C_L=12pF, ESR<100Ω	16	±30ppm	MHz

Package Information

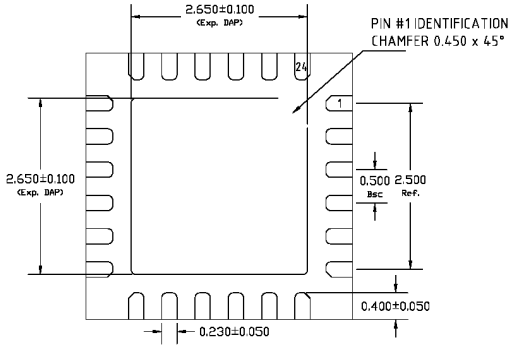


TOP VIEW

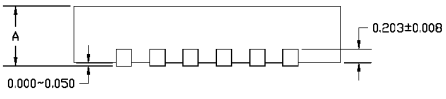
NOTES:

1. ALL DIMENSIONS ARE IN MM UNLESS OTHERWISE SPECIFIED.
2. QFN AND TQFN SHARE THE EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		QFN
A	MAX.	1.000
	NOM.	0.850
	MIN.	0.800



BOTTOM VIEW



SIDE VIEW

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Contact Information

Alfa*Plus* Semiconductor, Inc.

16F, No. 289, Sec. 2, Kuangfu Rd.

Hsinchu, Taiwan 30055

Website: www.alfaplus.com.tw
E-mail: info@alfaplus.com.tw
Tel: +886(3) 516-3270
Fax: +886(3) 516-3267

Revision Information

Ver.	Description	Date
1.0	Initial Draft	4/Dec/06’
1.1	Release Version	8/Dec/06’
1.2	Modify maximum data transmitting time at TX/Direct Mode.	19/Dec/06’
1.3	Modify Figure-7	21/Dec/06’
1.4	(1) Spelling error correction: TEINTLVL→TRINTLVL in P.17. (2) Modify current consumption from maximum value to typical value in P.4.	16/Jan/07’
1.41	(1) fdev=±156kHz →±160kHz (P.4) (2) C7=33nF→1μF (P.18)	9/Feb/07’
1.5	(1) C/I value in Electrical Characteristic (2) Modify Figure-1 (3) Modify Table-2 (4) Modify Figure-5 (5) Modify Figure-6 (6) Modify Device Register initialization value follows the E version of the ARF2496K. (7) Add section, Exception Register Settings for 250kbps Communication Bit-Rate. (8) BOM in Application Circuit.	18/Apr./07’
1.6	(1) Modify “Block Diagram” (2) Burst-Count -> Reserved in section – “Packet Format” (3) CL=20pF->12pF in section – “Global Clock” (4) C9=C10=22pF->20pF in “Application Circuit”	9/July/07’
1.61	(1) Stand-By Mode current consumption 32uA->22uA under CL=12pF condition. (2) Add Stand-By Mode current consumption 12pF condition description in “Global Clock” section. (3) CL=20pF->12pF in BOM.	10/July/07’
1.62	(1) Modify the table in section, ‘Exception Register Setting for 250kbps communication Bit-rate’. (2) Add section, ‘Exception Register Setting for Corner Condition Operation.	19/Feb/08’
1.63	Correct the description and timing parameter in the section ‘RX/Direct Mode’	06/Mar/08’
1.64	(1) Modify description of TX/Direct Mode. (2) Modify standby mode current consumption.(32uA->22uA) (3) Modify Power-saving resume time form 4ms to 1.5ms. (4) Modify ESR	24/June/08’
1.64	(5) C7 required from X5R to X7R.	24/June/08’
1.65	(1) Modify values of pre-dummy and post-dummy cycle of Figure-5. (2) Modify value of post-dummy cycle of Figure-7.	1/July/08’
1.66	(1) Modify the dB value of C/Iimage to -30dB for at 250kbps and 1Mbps.(p.4) (2) Add length recommended note at the description of register ADDRLNG.(p.16) (3) Add value setting recommended note at the description of register Device Address.(p.16)	19/Aug/08’
1.67	Remove TQFN package information. (P19)	4/Sept/08’

Appendix

RSSI Transformation Table

Input PWR (dBm) \ RSSI Value		RSSI (mV)	RSSIVAL
High Gain Mode (RSSI_GM=0)	Low Gain Mode (RSSI_GM=1)		
< -95	< -55	<550	0
-95	-55	550	1
-94	-54	565	
-93	-53	579	
-92	-52	594	
-91	-51	610	2
-90	-50	627	
-89	-49	645	
-88	-48	661	3
-87	-47	680	
-86	-46	697	
-85	-45	713	4
-84	-44	729	
-83	-43	744	
-82	-42	758	5
-81	-41	773	
-80	-40	788	
-79	-39	805	6
-78	-38	821	
-77	-37	839	
-76	-36	858	7
-75	-35	877	
-74	-34	895	
-73	-33	912	8
-72	-32	929	
-71	-31	944	
-70	-30	959	9
-69	-29	974	
-68	-28	989	
-67	-27	1005	10
-66	-26	1021	
-65	-25	1039	
-64	-24	1057	11
-63	-23	1076	
-62	-22	1093	

RSSI Transformation Table (continues)

Input PWR (dBm) \ RSSI Value		RSSI (mV)	RSSIVAL
High Gain Mode (RSSI_GM=0)	Low Gain Mode (RSSI_GM=1)		
-61	-21	1111	12
-60	-20	1127	
-59	-19	1142	
-58	-18	1156	13
-57	-17	1171	
-56	-16	1187	
-55	-15	1202	14
-54	-14	1219	
-53	-13	1234	
-52	-12	1252	15
-51	-11	1269	
-50	-10	1285	
-49	-9	1299	
-48	-8	1311	
-47	-7	1321	
-46	-6	1330	
-45	-5	1338	
-44	-4	1344	
-43	-3	1350	
-42	-2	1355	