1、BTMDC751 Series Radio Architecture

This section discusses the radio architecture for Class 2 designs. The first section covers the RF circuitry within the chip. Subsequent sections provide an overview of the external circuit design and Persistent Store (PS) Key configuration requirements.

BTMDC751 Series Transceiver

1.1.1 Transmitter Architecture

The transmitter uses a conventional IQ modulator, as shows. The baseband Bluetooth signal is generated digitally and modulated in accordance with the Gaussian Frequency Shift Keying (GFSK) modulation scheme employed in Bluetooth. An additional frequency offset of up to ±1MHz can be added to the digital baseband signal. RF Performance Evaluation and Optimisation, discusses the reasons for adding a baseband transmit offset.

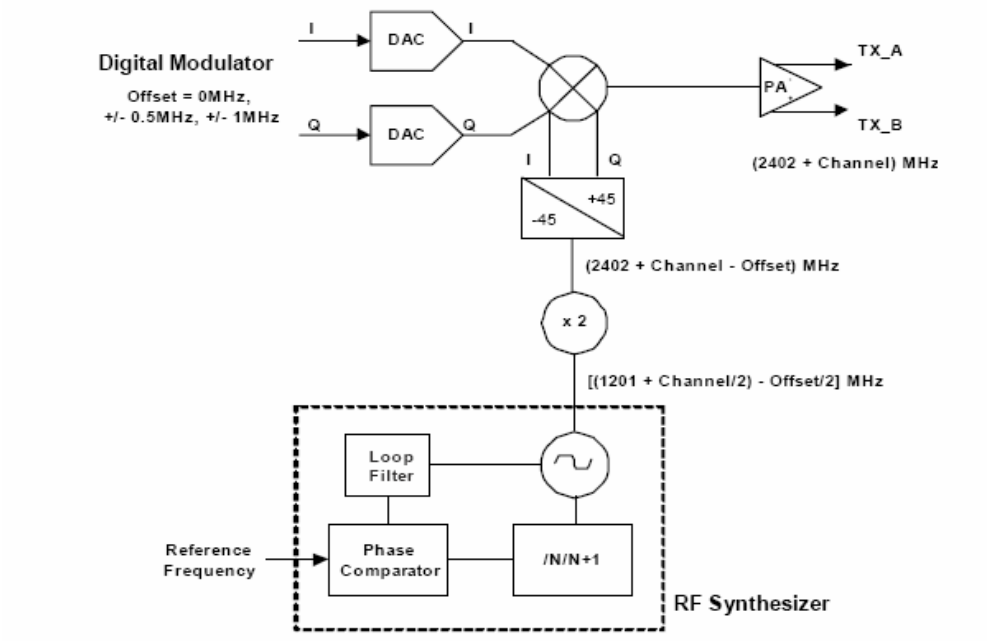

Figure 1.1Figure 1.1: Overview of Transmitter Architecture

1.1.2 Receiver Architecture

shows a receiver of a double conversion design, which uses the same synthesiser as the transmitter. The RF switch enables the use of inputs from either the differential or single-ended receive ports. The differential ports are the same TX_A and TX_B ports utilised by the transmitter. Single-ended inputs use the RF_IN port.

Both differential and single-ended inputs are amplified by a low noise amplifier (LNA) and passed to an IQ mixer where the signal is then down-converted to a first intermediate frequency (IF)

of 1.5MHz. This signal is amplified and filtered before undergoing a second quadrature mix to 2.5MHz. The 2.5MHz signal is further amplified and filtered. The signal is limited, sampled and then digitally demodulated. The 2.5MHz IF block also provides received signal strength indication (RSSI). Figure 1.2