

OM12001 - Automotive Telematics On-board unit Platform

Road Pricing - ECall

Rev. 0.75 — 14th August 2012

Preliminary Specification

Document information

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Revision history

Rev	Date	Description
0.75	9th August 2012	Numerous typos corrected Reference links updated
0.74	6th August 2012	Updated spec for “minus” version, ie. without NFC and security components. Updated label Added IC statement
0.73	1st February 2012	Added RHF indication description to label
0.72	8th December 2011	Revision history added! NFC EMC section updated 2D barcode info added

1. Introduction

OM12001 (ATOP) is the NXP Semiconductors platform for automotive telematics on-board units (OBU's) for applications such as road pricing and eCall, based upon the following technologies:

- GSM for communication
- GPS for localization service
- NFC for short range communication, e.g. configuration and law enforcement
- SmartMX smartcard with Java card JCOP OS for security
- J9 Virtual Machine for application portability and easy creation
- Dedicated processor for Real-Time and connection to system via Ethernet, USB, ADC, CAN, UART, ...
- Targeting 10 years lifetime¹ in automotive conditions

Thanks to on board ATOP security resources, product developers and manufacturers can offer products which guarantee fraud prevention and tamper evidence without extra effort for additional security precautions. These products can be used in end-to-end transaction systems requiring Common Criteria level 4+.

OM12001 (ATOP) can be used by itself as a complete solution for GPS-GSM based road pricing and eCall applications. In this case OM12001 (ATOP) just needs to be complemented with a power supply, speaker, microphone, some knobs, and an optional display. OM12001 (ATOP) provides the processing power and SW application environment resources on board to complement road pricing and eCall with some other added value telematics services.

OM12001 (ATOP) can also be applied as a 'front end' for more elaborate telematics products, by making its resources, i.e. GNSS, mobile communication, Security (ID authentication) available for use by other resources in the OBU.

2 different versions are available

- OM12001/100: Implements all the features described in this document
- OM12001/000: For market where security is not paramount, such as eCall, it does not include NFC short range communication, nor SmartMX security element

2. Product profile

2.1 Features

- Utility processor for interfacing with external world and house-keeping
 - ◆ ARM Cortex M3 micro-controller with Ethernet, CAN, USB Host and device, UART, SPI, I2C Bus, ADCs, DAC, GPIOs, and PWMs
 - ◆ Internal temperature sensor, and heating element²
- Application processor to run customer application code

1. in accordance with NXP's "Knowledge-Based Qualification" ("KBQ", based upon ZVEI's Robustness Validation^[1]), using AEC-Q100-defined qualification tests

2. Heating element present only in OM12001/100

- ◆ Virtual Machine for customer application
- ◆ Communication coprocessor with Quad-band GSM/GPRS terminal
- ◆ Localization coprocessor with GPS receiver
- ◆ Near Field Communication (NFC) controller to connect to external vignette, smart card, mobile phone³
- Security processor for providing a source of trust
 - ◆ SmartMX smartcard running JCOP 2.4.1³
- Mandatory and voluntary certification
 - ◆ R&TTE and FCC passed for safety, EMC and RF
 - ◆ Pre-certification for GCF, including field test
 - ◆ Certification for PTCRB
- Automotive certification
 - ◆ -40 to +85°C operating range
 - ◆ Targeting 10 years lifetime in automotive conditions¹

2.2 Applications

OM12001 (ATOP) can be used for Telematics applications where tamper-resistance, confidentiality, integrity, and authenticity of end-user information are required, e.g.:

- Road pricing
- Pay as you drive insurance
- Stolen vehicles tracking
- Emergency call
- ...

2.3 Quick reference data

OM12001 (ATOP) is available with quad-band support in 2 versions

Table 1. ATOP versions

Name	Description
OM12001/100	Quad-band GPRS/GSM with antenna switch, GPS, NFC, SMX, Cortex M3 microcontroller with Ethernet
OM12001/000	Quad-band GPRS/GSM with antenna switch, GPS, Cortex M3 microcontroller with Ethernet

3. General description

[Figure 1](#) represents OM12001 (ATOP) connections in a typical application, with its connection to batteries, antennas, and SIM. For communication with external world, serial link, GPIOs, and ADCs will connect to screen, keys, and sensors. UART, CAN or USB can be used to connect to on board computer.

3. Only for OM12001/100

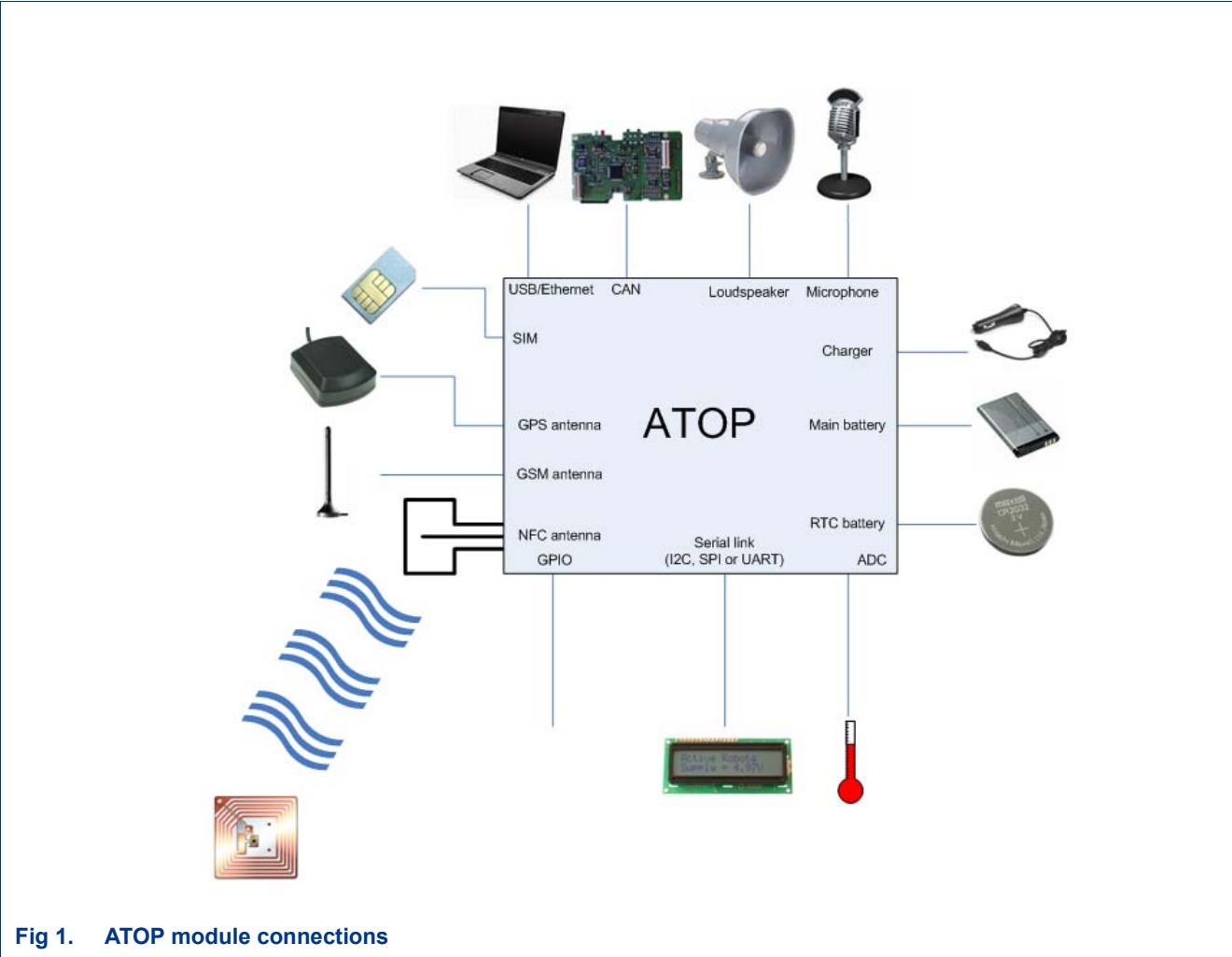


Fig 1. ATOP module connections

[Figure 2](#) represents a more conceptual view of OM12001 (ATOP) from a system point of view.

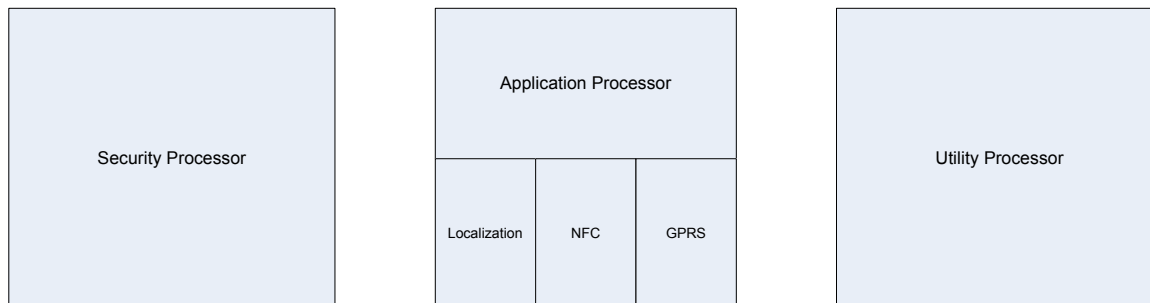


Fig 2. ATOP conceptual view

Three main components can be seen in [Figure 2](#):

- Application processor: This processor will run code specific to the application (roadtolling, insurance, ...) which is portable from one platform to another one in order to avoid recertification:
 - A localization coprocessor provides accurate location information to the application
 - A NFC coprocessor provides connection to an external vignette to increase application security³
 - A Communication coprocessor allows the application to connect to servers and receive update and notifications, receive or generate voice call or SMS
- Security processor which provides a root of trust for signing messages to servers, authenticate the presence of an external vignette, and run secure multiple security applications³
- Utility processor: This processor takes care of all housekeeping tasks such as connecting to external interfaces, displays, but also of power management, waking-up and booting-up the system, i.e. all support tasks which are not part of the high level applications but are required to make the system work.

4. Features

4.1 Utility processor

A LPC1768 micro-controller is available for interfacing to external world and user interface.

- ARM Cortex M3 core running up to 100 MHz
 - ◆ 512 kB on-chip flash memory
 - ◆ 64 kB SRAM memory
 - ◆ Dual AHB system that provides for simultaneous DMA and program execution from on-chip flash with no contention between those functions.
- General Purpose DMA controller (GPDMA) on AHB that can be used with the SSP

serial interfaces, the I2S port, ADCs, DAC as well as for memory transfers

- Serial Interfaces
 - ◆ 3 UARTs
 - ◆ 2 I2Cs
 - ◆ 1 SSP (Synchronous Serial Port) and 1 SPI
 - ◆ I2S output/input
 - ◆ PWM/Capture unit
 - ◆ GPIOs (multiplexed)
- High speed serial interfaces
 - ◆ Ethernet MAC with RMIi interface and dedicated DMA controller
 - ◆ Full Speed USB 2.0 Host/Device controller with integrated PHY
 - ◆ 2 CAN channels
- Analog interfaces
 - ◆ 7 12 bit ADCs (successive approximation)
 - ◆ 1 internal temperature sensor (12 bit ADC)
 - ◆ 1 10 bit DAC
- Debug
 - ◆ ETJAG
 - ◆ Serial Wire Debug

4.2 Application processor

The application processor is actually a Virtual Machine (VM) running on the main CPU of the GSM/GPRS baseband. Using a Virtual Machine offers numerous advantages:

- portability to numerous platforms
- maintainability via secure download and update mechanisms
- large virtualized feature set, such as:
 - ◆ secure network access (https)
 - ◆ cryptography
 - ◆ Near Field Communication (NFC)³

VM has the following features:

- CDC Foundation Profile including following additional API's
 - ◆ Wireless Messaging
 - ◆ Mobile playback
 - ◆ Location
 - ◆ Contactless Communication
 - ◆ Telephony
 - ◆ Power management
- Connection to micro-controller via message passing

4.3 Localization coprocessor

GPS reception is used for localization.

- Best in class acquisition and tracking sensitivity
 - ◆ Internal separate LNA for improved sensitivity

- Advanced proprietary multipath algorithms for robust low dropout tracking in very low signals environment
- SW upgradable
- 1 Pulse per Second (1PPS) output for synchronization with GPS system clock

4.4 GSM/GPRS coprocessor

Connection to mobile networks is provided by a certified communications protocol stack that is field tested worldwide. It runs on a single monolithic IC integrating analog and digital basebands, RF transceiver, power management, and audio codec with best-in-class RF performance and power consumption.

- 32-bit ARM926EJ-S™ control processor, up to 156 MHz
- Communication engine
 - ◆ Support for 2 antennas with internal switch
 - ◆ Quad-band support: GSM 850, PCS 1900, E-GSM 900, and DCS 1800
 - ◆ GPRS multislots class 10, class B
- Audio subsystem
 - ◆ HR / FR / EFR / AMR Vocoders
 - ◆ Noise suppression and echo cancellation
 - ◆ Microphone amplifier with differential input
 - ◆ High-performance 8Ω driver (500mW output power, 1% THD typ)
 - ◆ Digital PCM IO
- SIM card interface
 - ◆ 1.8/2.9V power generation
 - ◆ Compliant with SIM card interface in accordance with GSM11.11
 - ◆ Compliant with ISO7816-3 requirements

4.5 Near Field Communication coprocessor³

To connect to an external device, such as a vignette, mobile phone, or personalization station for a road pricing public scheme, a NFC communication link with the following features is present:

- Reader mode
 - ◆ Allows simultaneous access up to two external cards
 - ◆ Offers baud rate up to 424 kbps
 - ◆ Complete NFC framing and error detection
 - ◆ Supports ISO14443A&B/Mifare
- Virtual Card mode
 - ◆ Direct connection to battery allowing operation with the rest of system is switched off
 - ◆ Access to SmartMX in Mifare emulation mode

4.6 Smartcard & JCOP operating system³

For telematics and other high value applications, it is paramount to protect against data tampering, loading of unauthorized applications, ID stealing, as well as to protect end user privacy. For this, a secured component such as a smartcard is required to be used as a root of trust.

OM12001 (ATOP) relies on a SmartMX component with the following features:

- Common criteria CC EAL5+ certification according to BSI-PP-0002 protection profile
- Latest built-in security features to avoid power (SPA/DPA), timing, and fault attacks
- 80 KB EEPROM
 - ◆ EEPROM with typical 500000 cycles endurance and minimum 20 years retention time
- 6144 B RAM
- 200 KB ROM
 - ◆ 75+ KB available for customer applications
- Secure cryptographic processor
 - ◆ High-performance secured Public Key Infrastructure (PKI)
 - ◆ Secured dual/triple-DES coprocessor
 - ◆ Secured AES coprocessor

For portability and to allow multiple secure application (cardlets) to run in complete isolation, OM12001 (ATOP) offers a Java Card Open Platform operating system (JCOP). V2.4.1 based on independent, third party specifications, i.e. by Sun Microsystems, the Global Platform consortium, the International Organization for Standards (ISO), EMV (Europay, MasterCard, and VISA) and others.

SmartMX family was designed to service high volume, single- and multi-application markets such as eGovernment e.g. Smart Passport, banking/finance, mobile communications, public transportation, pay TV, conditional access, network access, and digital rights management, thus ensuring applications running on OM12001 (ATOP) can rely on the highest level of security available.

4.7 Debug and Security

For application development, but also field return analysis, debug capabilities are a must. However the observability, test and control capabilities given by debug could be used for device tampering.

That is why ATOP debug capabilities are locked until proper authentication. Additionally, security features are present to ensure that only signed SW is executed.

For debug, the following features are present:

- LPC1768 MCU
 - ◆ CPU debug via JTAG or Serial Wire Debug interface
 - ◆ Unique Serial Number
 - ◆ Core Read Protection with multiple levels

For security, the following features will protect against unauthorized debug, code tampering, and insertion:

- Observability
 - ◆ JTAG access locked down until authentication is performed
 - ◆ All sensitive bus are buried down in the PCB
- Code authentication and integrity
 - ◆ Code is signed with RSA to ensure authentication and checked at boot

4.8 Battery and Power management

Thanks to its integration, OM12001 (ATOP) can be connected directly to a mobile phone battery. All voltage conversion and battery charging management will be handled by OM12001 (ATOP).

- Direct connection to mobile phone type battery
 - ◆ Optional connection to coin cells for RTC
- Battery charging management
 - ◆ Full HW and SW support of single cell Li-Ion, Li-Ion polymer battery with voltage, temperature and charge current monitoring
- Support large voltage range
 - ◆ 3.1V to 5.5V for Application processor and coprocessors whenever no connection to GSM network is active (Airplane mode)
 - ◆ 3.4 to 4.8V for Application processor and coprocessors when connection to network is active
 - ◆ 3V to 5.5V for Utility processor
- Integration of all required LDO and DC/DC converters

Thanks to its use of highly integrated components, optimized for power consumption, in a typical application⁴, OM12001 (ATOP) can function for about 30 days on a single 700 mAh battery charge.

Separate power supply pins are provided for microcontroller, RTC, and the rest of the system, so that each part can be separately disabled.

The utility micro-controller can be programmed to wake up OM12001 (ATOP) on external (CAN, GPIO, ...) or RTC events. In this mode, less than 150 μ A of current will be drawn.

1 μ A are drawn by RTC if functionality is required.

For the rest of the system, a 50-100 μ A leakage current can be expected (assuming charger input is not active).

5. Ordering information

Please refer to OM12001 release note for ordering information.

6. Functional description

6.1 LPC1768 Micro-controller

LPC1768 will be responsible for tasks such as:

- booting up the system
- handling RTC and regular wake-up
- interfacing with external sensors, display, buttons via I2C, SPI, UART, ...
- communicating with others car's units via CAN, UART, Ethernet, ...
- controlling operator access for firmware upgrade, data retrieval via USB, UART, ...

4. Car being driven for 1h per day.

Except for a few services provided by NXP to handle communication between the application running on Virtual Machine and virtualized external devices, Utility processor will be completely available to the system integrator.

6.1.1 General features

- ARM Cortex-M3 microcontroller, running up to 100 MHz
- 512 kB on-chip Flash Program Memory with In-System Programming (ISP) and In-Application Programming (IAP) capabilities. Single Flash sector or full-chip erase in 400 ms and 256 bytes programming in 1 ms. Flash program memory is on the ARM local bus for high performance CPU access
 - 10000 erase cycles
 - 10 years retention powered on, 20 years powered off
 - First 8 erase block are 4 KB large, others are 32 KB large
- 32 kB Static RAM with local code/data bus for high-performance CPU access
- Two 16 kB Static RAM blocks with separate access paths for higher throughput, for Ethernet, USB, DMA memory as well as for CPU code and data.
These SRAM blocks may be used for Ethernet, USB, and DMA memory, as well as for general purpose CPU instruction and data storage for general purpose SRAM
- Multilayer AHB matrix interconnect with separate bus for each AHB master
- Advanced Vectored Interrupt Controller, supporting up to 32 vectored interrupts
- Eight channel General Purpose DMA controller (GPDMA) on the AHB multilayer matrix that can be used with the SSP, serial interfaces, the I2S port, as well as for memory-to-memory transfers
- Serial interfaces available externally
 - USB 2.0 Full-speed Device/Host controller with on-chip PHY and associated DMA controller
 - Three UARTs with fractional baud rate generation, one with modem control I/O, one with IrDA support, all with FIFO. These reside on the APB bus
 - One SSP controller with FIFO and multi-protocol capabilities, as well as a SPI port, sharing its interrupt. The SSP controller can be used with the GPDMA controller and reside on the APB bus
 - Two I2C interfaces reside on the APB bus. The second and third I2C interfaces are expansion I2C interfaces with standard port pins rather than special open-drain I2C pins
 - I2S (Inter-IC Sound) interface for digital audio input or output, residing on the APB bus. The I2S interface can be used with the GPDMA
 - Two channels with Acceptance Filter/FullCAN mode residing on the APB bus
- Other APB Peripherals
 - 12 bit A/D converter with input multiplexing among 7 external pins
 - 10 bit D/A converter with DMA support
 - Four general purpose timers with a total of 8 capture inputs and ten compare output pins each. Each timer block has an external count input

- One PWM/Timer block with support for three-phase motor control
- Real-Time Clock (RTC) with separate power pin; clock source can be the RTC oscillator or the APB clock oscillator
- Watchdog Timer. The watchdog timer can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock
- Standard ARM Test/Debug interface for compatibility with existing tools
- Three reduced power modes: Idle, Sleep, and Power-down
- Four external interrupt inputs. In addition every PORT0/2 pin can be configured as an edge sensing interrupt
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt)
- Two independent power domains allow fine tuning of power consumption based on needed features
- Brownout detect with separate thresholds for interrupt and forced reset
- On-chip Power On Reset
- On-chip crystal oscillator with an operating range of 1 MHz to 24 MHz
 - For CAN and USB, a clock generated internally to OM12001 (ATOP) is provided, or an external crystal can be used
- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator
- Versatile pin function selections allow more possibilities for using on-chip peripheral functions

6.1.2 Block diagram

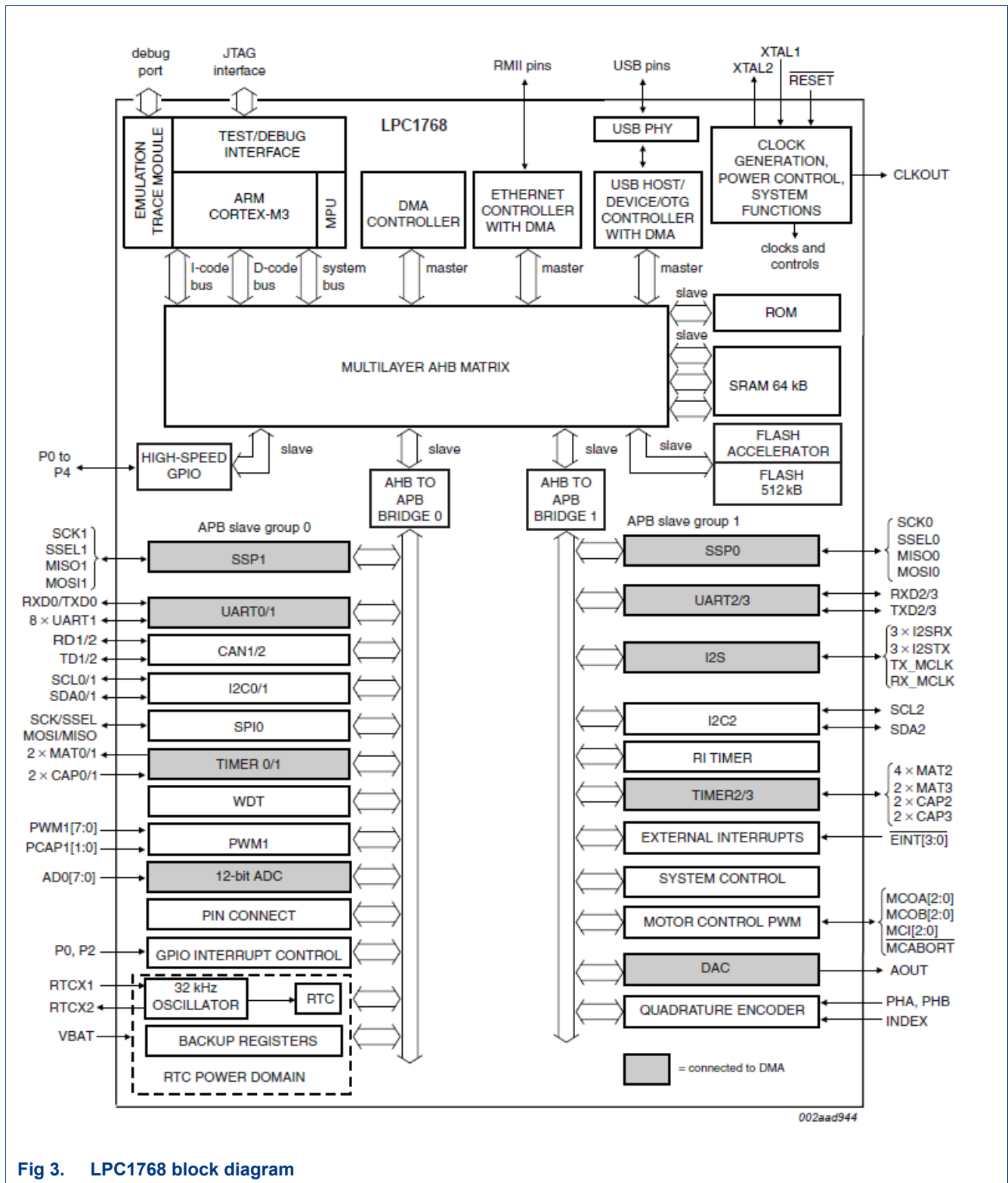


Fig 3. LPC1768 block diagram

6.1.3 Ethernet

Ethernet block supports bus clock rates of up to 100 MHz. The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU.

The Ethernet block and the CPU share the ARM Cortex-M3 D-code and system bus through the AHB-multilayer matrix to access the various on-chip SRAM blocks for Ethernet data, control, and status information.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

6.1.4 USB

LPC1768 features an USB interface with a device and host controller with on-chip PHY.

6.1.4.1 USB device controller

The device controller enables Full Speed (12 Mbit/s) data exchange with a USB Host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the on-chip SRAM.

6.1.4.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of a register interface, a serial interface engine, and a DMA controller. The register interface complies with the OHCI specification.

6.1.5 CAN

6.1.5.1 Description

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring. The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router among a number of CAN buses in industrial or automotive applications.

6.1.5.2 Features

- Two CAN controllers and buses
- Data rates to 1 Mbit/s on each bus
- 32-bit register and RAM access
- Compatible with CAN specification 2.0B, ISO 11898-1

- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers
- Full CAN messages can generate interrupts

6.1.6 Power saving modes

6.1.6.1 Peripheral and clock control

As shown in [Figure 4](#), the CPU clock rate can also be controlled as needed by changing clock sources, re-configuring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, Peripheral Power Control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application.

The LPC1768 include three independent oscillators. These are the main oscillator, the IRC oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Any of the three clock sources can be chosen by software to drive the main PLL and ultimately the CPU.

Following reset, the LPC1768 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency. Main oscillator will be driven by an optional external crystal on customer board. Its presence might be required if an accurate clock is necessary, for instance for USB or HS CAN compliancy.

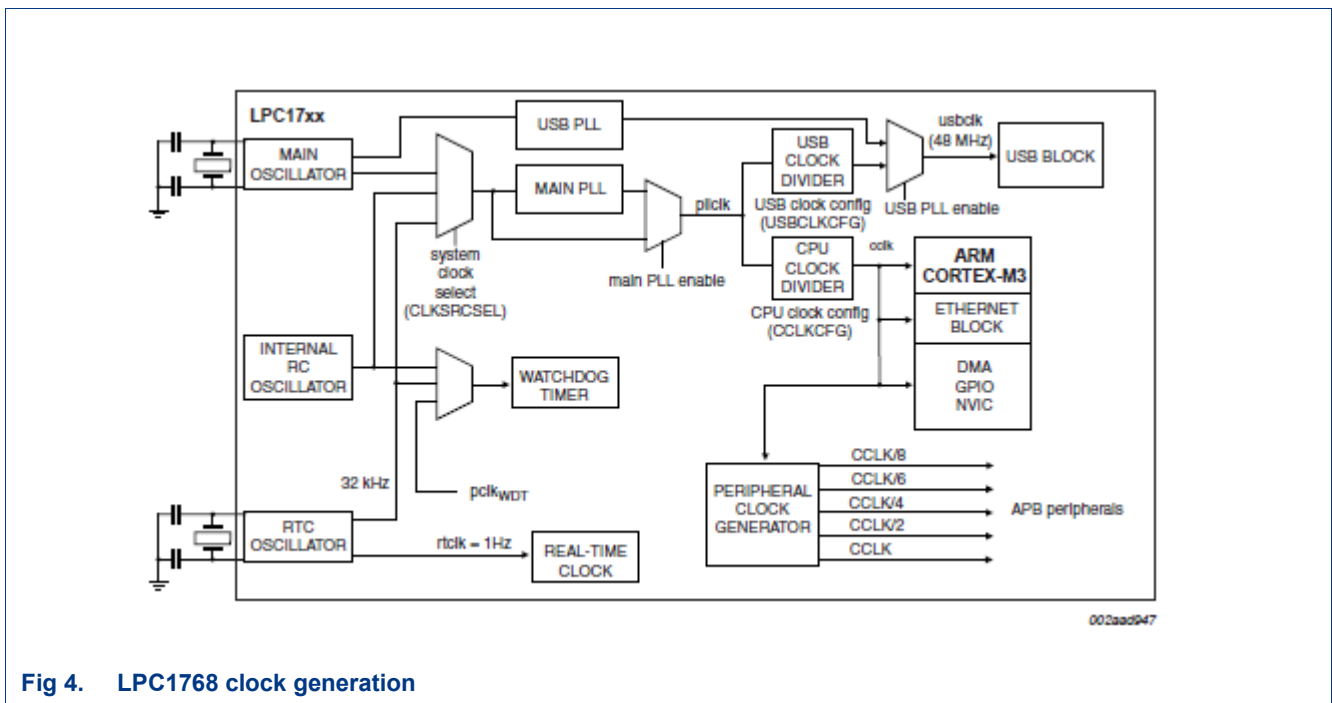


Fig 4. LPC1768 clock generation

6.1.6.2 Power modes

The LPC1768 support a variety of power control features. There are four special modes of processor power reduction:

- Sleep
- Deep-sleep
- Power-down
- Deep power-down

The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, Peripheral Power Control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

Integrated PMU (Power Management Unit) automatically adjust internal regulators to minimize power consumption during Sleep, Deep sleep, Power-down, and Deep power-down modes.

The LPC1768 also implement a separate power domain to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small set of registers for storing data during any of the power-down modes.

Sleep mode: When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

Deep-sleep mode: In Deep-sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep-sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down for a fast wake-up later.

The RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected.

The Deep-sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Deep-sleep mode reduces chip power consumption to a very low value. Power to the flash memory is left on in Deep-sleep mode, allowing a very quick wake-up.

Power-down mode: Power-down mode does everything that Deep-sleep mode does, but also turns off the power to the IRC oscillator and the flash memory. This saves more power but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

Deep power-down mode: The Deep power-down mode can only be entered from the RTC block. In Deep power-down mode, power is shut off to the entire chip with the exception of the RTC module and the RESET pin. The LPC1768 can wake up from Deep power-down mode via the RESET pin or an alarm match event of the RTC.

Wake-up interrupt controller: The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any enabled priority interrupt that can occur while the clocks are stopped in Deep sleep, Power-down, and Deep power-down modes.

The WIC works in connection with the Nested Vectored Interrupt Controller (NVIC). When the CPU enters Deep sleep, Power-down, or Deep power-down mode, the NVIC sends a mask of the current interrupt situation to the WIC. This mask includes all of the interrupts that are both enabled and of sufficient priority to be serviced immediately. With this information, the WIC simply notices when one of the interrupts has occurred and then it wakes up the CPU.

The WIC eliminates the need to periodically wake up the CPU and poll the interrupts resulting in additional power savings.

6.1.7 RTC

The RTC on the LPC1768 is designed to have extremely low power consumption, i.e. less than 1 μ A. The RTC will typically run from the main chip power supply, conserving battery power while the rest of the device is powered up. When operating from a battery, the RTC will continue working down to 2.1 V. Battery power can be provided from a standard 3 V Lithium button cell.

An ultra-low power 32 kHz oscillator will provide a 1 Hz clock to the time counting portion of the RTC, moving most of the power consumption out of the time counting function.

The RTC contains a small set of backup registers (20 bytes) for holding data while the main part of the LPC1768 is powered off.

The RTC includes an alarm function that can wake up the LPC1768 from all reduced power modes with a time resolution of 1 s.

7. Application design-in information

7.1 Battery charging

OM12001 (ATOP) natively handles Lithium Ion battery technology.

There are 3 distinct modes for battery charging, depending on the battery voltage:

- **trickling mode:** In this mode, ATOP will detect whether battery is dead (i.e. voltage drop as soon as a small current is applied). If that is not the case, a small current of 1 mA will be applied until the voltage is higher than 1.5V, and then ATOP will switch to pre-charge mode

- precharge mode: Precharge mode is completely under HW control and will continue until the battery voltage is high enough so that baseband can boot. During precharge, ATOP will provide a 200 mA current. As SW is not yet booted, temperature will not be controlled, i.e. precharge will occur even if battery is outside of advised range for a battery
- fast charge: If battery level is higher than 3.1V (i.e. enough for baseband to boot) and there is voltage on Vcharge for more than 10 ms, then OM12001 (ATOP) will switch to SW charge mode. SW will initiate a fast charge with Constant Current - Constant Voltage (CC-CV) method as described in [Figure 5](#). It will stop when the current drawn on the charger falls below 50 mA or whenever overvoltage/overcurrent is detected or temperature is outside of allowed range (typically 0-50°C). Limiting and dynamic values can be found in [Table 4](#) and [Table 26](#)

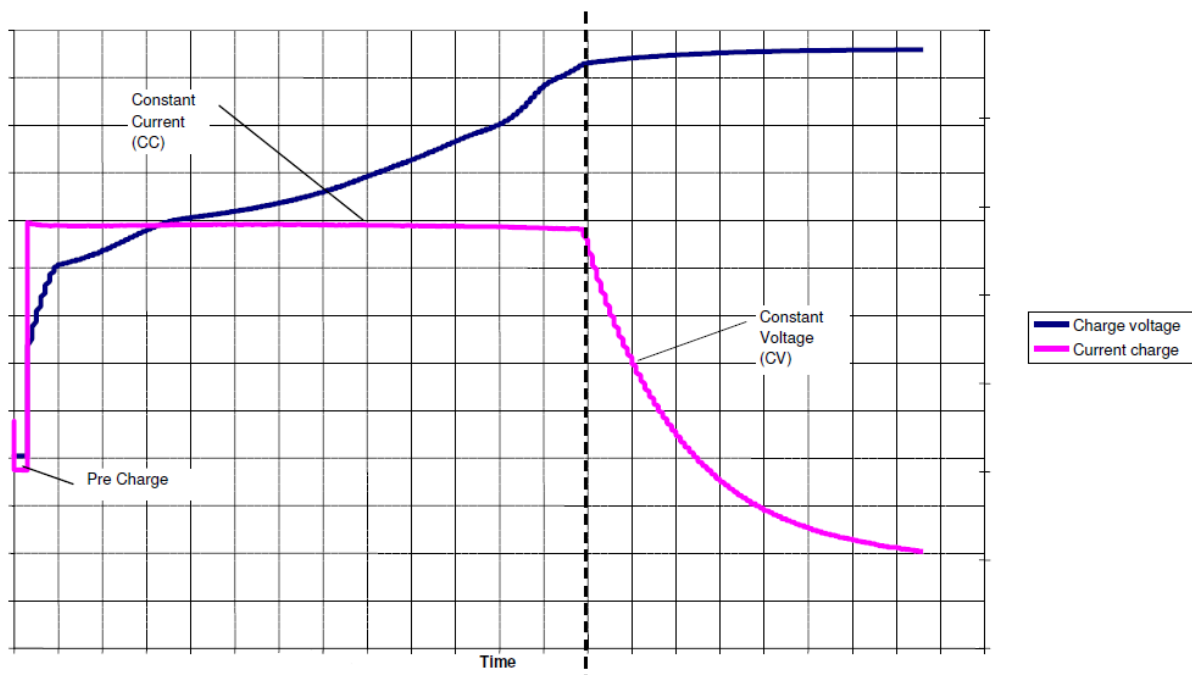


Fig 5. Constant Current - Constant Voltage charging method

[Figure 6](#) presents a typical implementation of the charging circuitry. A 0.1 Ohm resistor is used as a shunt to measure charge current. 2 PMOS transistors are used respectively to enable charging, avoid reverse leakage from battery to charger, and regulate current. They should be properly dimensioned for power dissipation.

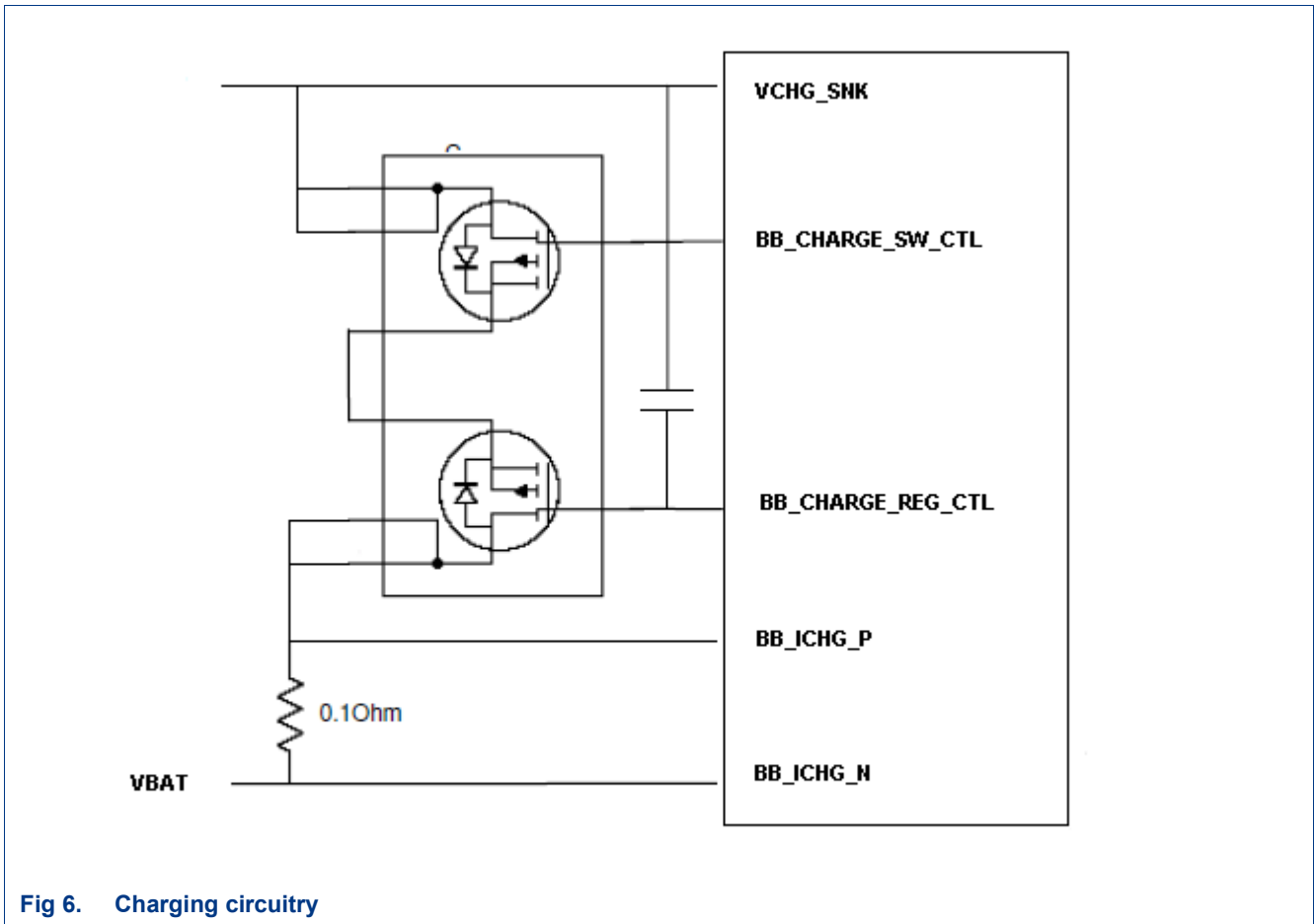


Fig 6. Charging circuitry

Additionally other pins should be connected as follows:

- VBAT_SENSE_P must be connected to the battery
- VBAT_SENSE_N must be connected to ground
- BB_BAT_THERM must be connected to a 10 kOhm pull-down, or to the battery thermistor

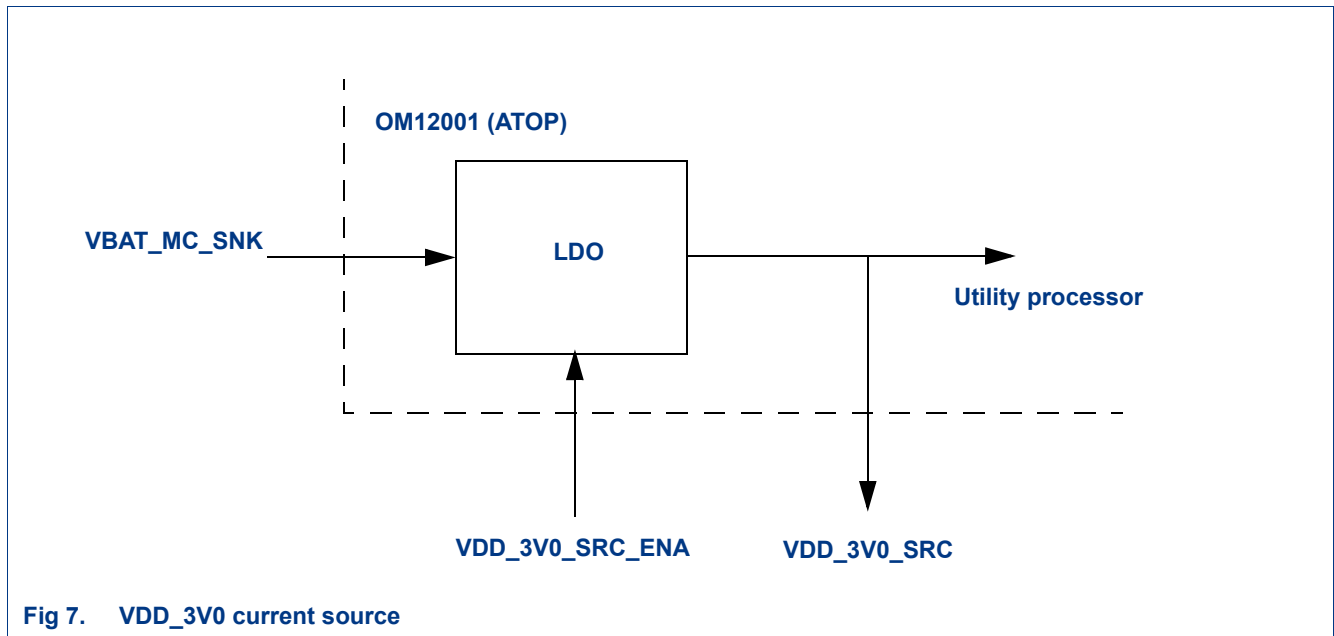
7.2 Application without rechargeable battery

If no rechargeable battery is used in the application, charging control pins must be connected as follows:

- VCHG_SNK must be connected to ground
- BB_CHARGE_[SW|REG]_CTL must be left unconnected
- BB_ICHG_[P|N] must be connected together
- VBAT_SENSE_P must be connected to VBAT_SNK
- VBAT_SENSE_N must be connected to ground
- BB_BAT_THERM must be connected to a 10 kOhm pull-down

7.3 Current source

OM12001 (ATOP) handles internally all its voltage conversion. For Utility Processor, a separate input, VBAT_MC_SNK, is used. Internally, a LDO, controlled by VDD_3V0_SRC_ENA (active high, with internal pull-up), will convert it to the 3V required by the Utility Processor. As described in [Figure 7](#), the output of the LDO is also available externally to power external component, up to a maximum of 100 mA can be drawn. Other limiting values can be found in [Table 13](#).



7.4 RTC

MCU RTC is internally supplied by the output of the LDO described in [Figure 7](#). It can also be supplied by a separate battery such as a coin cell via VBAT_RTC_SNK so that RTC is kept in case of power loss. If this feature is not required it is advised to connect VBAT_RTC_SNK and VDD_3V0_SRC.

8. Application information

8.1 NFC antenna design³

For NFC antenna design, please refer to [Ref. \[6\]](#) for antenna design and [Ref. \[7\]](#) if application requires to boost NFC signal.

[Figure 8](#) describes the internal setup of NFC_ANT pins.

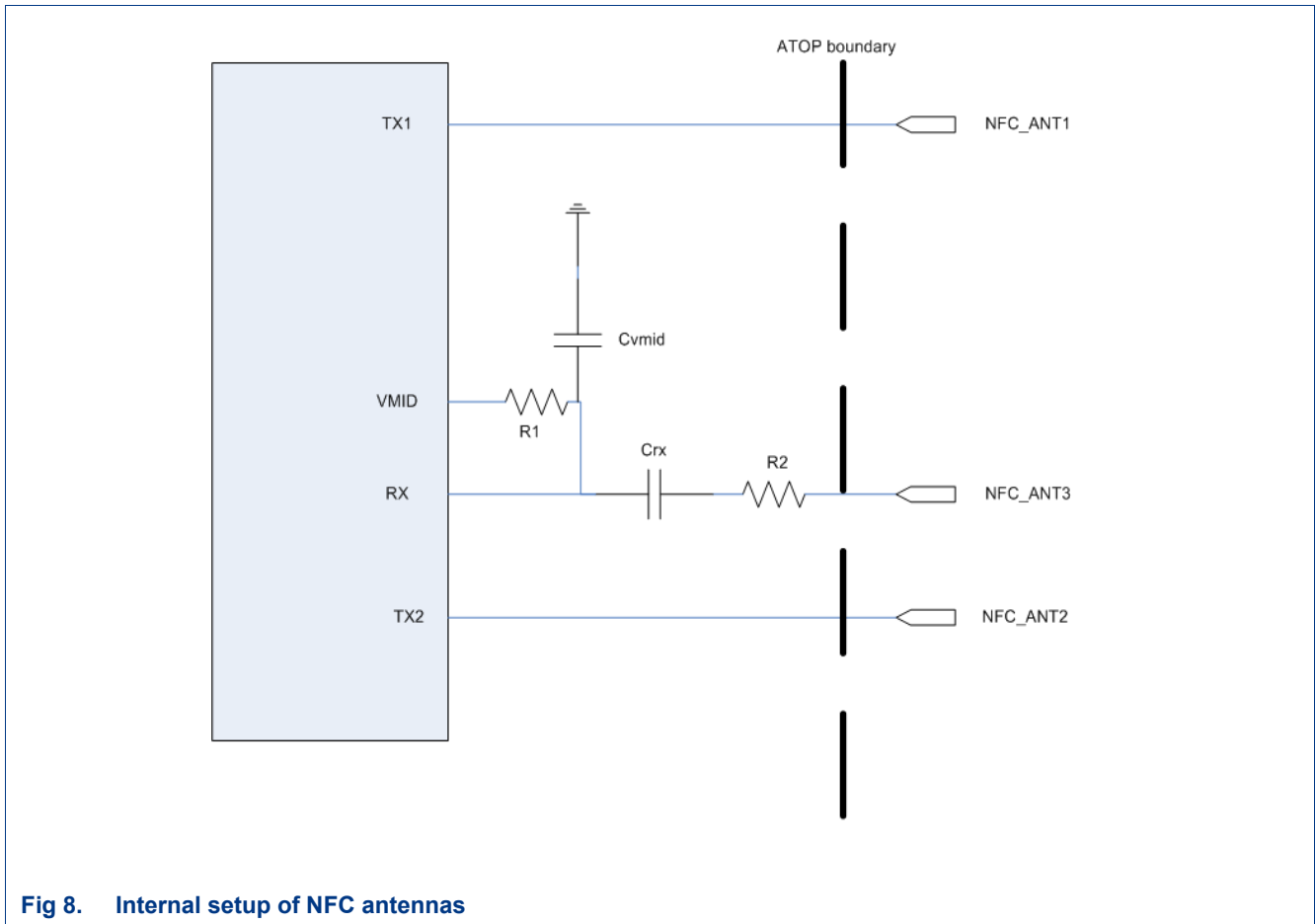


Fig 8. Internal setup of NFC antennas

$$R_1 = 1 \text{ K}\Omega, R_2 = 2.7 \text{ K}\Omega, C_{RX} = 1 \text{ nF}, C_{vmid} = 100 \text{ nF}$$

9. Recommended operating conditions

Table 2. Temperature

Allowed temperature range

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Module storage temperature range	-40		85	°C	Before final reflow, stored in drypack
	Module limited operation temperature range	-40		85	°C	All functions, except for NFC and Secure processor
	Module operating temperature range	-25		85	°C	

[Table 7](#) presents in more details the tests performed to guarantee module lifetime.

10. Limiting values

Table 3. Power supply

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{bat_rf}	Battery voltage for application processor	3.4 ^[1]	4.2	4.8	V	Voltage range allowed in case of connection and transmission to GSM network
$V_{bat_no_rf}$	Battery voltage for application processor	3.1	4.2	5.5	V	Voltage range allowed without connection to GMS network (i.e. airplane mode)
V_{bat_mc}	Battery voltage for utility processor	3.1	4.2	5.5	V	
$V_{bat_rtc_mc}$	Battery voltage for utility processor RTC	2.0	3.3	3.6	V	
$V_{bat_rtc_bb}$	Battery voltage for application processor RTC	2.0	3.0	3.15	V	^[3]
I_{bat}	Battery current			1800 ^[2]	mA	Peak current to be used to dimension decoupling capacitors (on VBAT_SNK)

[1] Note this minimum voltage should take into account the voltage drop due to the high current during transmission, i.e. for a typical battery with a drop of 200 mV, minimum voltage is 3.6V

[2] Occurs only during transmission slot (577 μ s) in case of poor reception

[3] It is not mandatory to connect $V_{bat_rtc_pnx}$ as internal connection is provided, unless it is required to keep application processor RTC active when V_{bat} is disconnected

Table 4. Battery charging

Handled by baseband integrated battery charging unit

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{Charge}	Charge voltage	3.2	4.8	7.5	V	^[1]
I_{bat_empty}	Empty battery current		1		mA	for $V_{BAT_SNK} < 1.5V$
$I_{PreCharge}$	Pre-charge current	160	200	240	mA	pre-charge current, i.e. for $V_{BAT_SNK} < 3.35V$
$I_{FastCharge}$	Fast charge current	200		1400	mA	For $V_{BAT_SNK} > 3.35V$, Settable with 100mA steps, with additional step at 450 mA
$V_{FastCharge}$	Fast Charge Voltage	3.45	4.2	5.5	V	Settable with 50 mV step between 3.45 to 4.9V and 2 additional points at 5.25 and 5.55V
V_{SW_CTL}	Maximum voltage allowed on BB_CHARGE_SW_CTL	-	-	V_{BAT_SNK}	V	
V_{SW_REG}	Maximum voltage allowed on BB_CHARGE_SW_REG	-	-	V_{CHG_SNK}	V	

[1] Charge voltage should obviously be higher than Vbat. Voltage drop into external transistors and resistors should be taken into account

Table 5. Limiting values for micro-controller pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IAmc}	Analog input voltage	on ADC related pins		-0.5	5.1	V
V_{Imc}	Input voltage	5V tolerant I/O pins ^{[1][2][3]}		-0.5	5.5	V
		other I/O pins ^[2]		-0.5	3.6	V
V_{imc_xtal1}	Input voltage for XTAL1	Internal oscillator input	0	-	1.8	V
V_{omc_xtal2}	Output voltage	Internal oscillator output	0	-	1.8	V

[1] 5V tolerant pins, i.e. all I/O with MC prefix, except for oscillator IOs

[2] V_{bat_mc} must be present

[3] 3-state outputs go into 3-state mode when V_{bat_mc} is grounded

Table 6. Limiting values for GSM baseband interfaces

SIM interface, analog audio and PCM interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{Ibb}	Input voltage		-0.4		3.2	V
I_{Ibb}	Input current				20	mA
I_{Obb}	Output current				20	mA

Table 7. Limiting values for GSM antennas

Due to their ESD protection implementation GSM antennas are DC grounded

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{IDC}	Input resistance	DC voltage			1.96	Ω
I_{maxDC}	Maximum current	DC current			140	mA
	Load mismatch	for all phase angles, before permanent degradation or damage			20:1	VSWR
	Spurious (low bands)	for all phase angles, no parasitic oscillations > -30 dbm			12:1	VSWR
	Spurious (high bands)	for all phase angles, no parasitic oscillations > -30 dbm			8:1	VSWR

Table 8. Limiting values for GPS passive antenna input

Due to its ESD protection implementation GPS antenna is DC grounded

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{IDC}	Input resistance	DC voltage			0.14	Ω
I_{maxDC}	Maximum current	DC current			540	mA

Table 9. Limiting values for GPS active antenna input and antenna bias

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{maxDC}	Maximum voltage	DC voltage	-25		25	V
I_{maxDC}	Maximum current	DC current			70	mA

11. Characteristics

12. Static characteristics

12.1 Pins

Table 10. Characteristics for micro-controller pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{Omc}	Output voltage		0		3.0	V
V_{IHmc}	High level input voltage		2.0			V
V_{ILmc}	Low level input voltage				0.8	V
I_{ILmc}	Low level input current	$V_I=0$ V; no pull-up			3	μ A
I_{IHmc}	High level input current	$V_I=3.0$ V; no pull-down			3	μ A
V_{OHmc}	High level output voltage	$I_{OHmc}=-4$ mA	2.6			V
V_{OLmc}	Low level output voltage	$I_{OLmc}=-4$ mA			0.4	V
I_{OLmc}	Low level output current	$V_{OL}=0.4$ V	4			mA
I_{OHmc}	High level output current	$V_{OH}=2.6$ V	-4			mA
I_{OLSmc}	Low level short circuit output current	$V_I=3.0$ V [1]			-45	mA
I_{OHSmc}	High level short circuit output current	$V_I=0$ V [1]			50	mA
I_{OZmc}	Off state output current	$V_O=3.0$ or 0 V; no pull-up/down			3	μ A
I_{pdmc}	Pull-down current	$V_I=5$ V	10	50	150	μ A
I_{pumc}	Pull-up current	$V_I=0$ V; $3.0 < V_I < 5$ V	-15	-50	-85	μ A
			0	0	0	μ A
$I_{latchmc}$	I/O latchup current	$-1.5 < V_I < 4.5$ V; $T_j < 125^\circ$ C			100	mA

[1] Only allowed for a short time period

Table 11. Characteristic for baseband digital interface
namely SIM interface, PCM, UART, JTAG

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IHbb}	High level input voltage		2.4			V
V_{ILbb}	Low level input voltage				0.4	V
I_{IHbb}	High level input current		-10		+10	μ A
I_{ILbb}	Low level input current		-10		+10	μ A
V_{OHbb}	High level output voltage		2.7			V
V_{OLbb}	Low level output voltage				0.1	V
R_{pubb}	Pull-up resistance			100		k Ω
R_{pdbb}	Pull-down resistance			100		k Ω
C_{iLbb}	Input capacitance				0.1	pF

Table 12. Characteristic for GPS digital interface
namely JTAG and GPS_UART2_RXD

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IHbb}	High level input voltage		1.7			V
V _{ILbb}	Low level input voltage				0.7	V
I _{IHbb}	High level input current		-10		+10	μA
I _{ILbb}	Low level input current		-10		+10	μA
V _{OHbb}	High level output voltage		1.7			V
V _{OLbb}	Low level output voltage				0.7	V
R _{pubb}	Pull-up resistance			60		kΩ
R _{pdbb}	Pull-down resistance			75		kΩ
I _O	Output current		6			mA

12.2 Current sources

Table 13. V_{dd_3v0_src} current source
Can be used to supply external components

Symbol	Parameter	Min	Typ	Max	Unit	Note
V _{dd_3v0}	Output voltage	2.9	3.0	3.1	V	For T _j =-40 to 125°C
I _{vdd3v0_max}	maximum current			100	mA	
ΔV _{dd_3v0}	Load regulation		0.0008	0.004	%/mA	
ΔV _{dd_3v0}	Line regulation	-0.1		0.1	%/V	For V _{bat} variation
t _{on_dd_3v0}	Turn on time		240		μS	Measured from the time VDD_3V0_SRC_ENA exceeds 1.4V

Table 14. V_{sim_src} current source
To be only used to supply SIM cards^[1]

Symbol	Parameter	Min	Typ	Max	Unit	Note
V _{sim_src}	Output voltage	2.75	2.90	3.00	V	Appropriate SIM card voltage is automatically detected and selected by the software
		1.65	1.80	1.95	V	
I _{sim_src}	Output current			80	mA	Full power mode
				3	mA	Sleep mode
ΔV _O /V _O	Relative output voltage			50	mV/V	For V _{bat} variation
t _{on_dd_3v0}	Settling time		10		μS	from power-down

[1] Voltage is dynamically controlled to reduce power consumption when SIM card is not accessed

12.3 Voltage references

Table 15. V_{io_ref} voltage reference
To be used as a reference to connect to BB_* test pins (JTAG)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V _{io_ref}	Output voltage	2.70	2.80	2.95	V	
ΔV _O /V _O	Relative output voltage			50	mV/V	For V _{bat} variation

Table 16. V_{perm_ref} voltage reference

To be used as a reference to connect to BB_* functional pins

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{perm_ref}	Output voltage	2.82 ^[1]	3.0 ^[2]	3.18 ^[3]	V	Follows VBAT_SNK if <3V

[1] For VBAT_SNK = 3.1V

[2] For VBAT_SNK = 3.6V

[3] For VBAT_SNK = 5.5V

Table 17. V_{adc_ref} voltage reference

used as power supply reference for internal ADCs

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{adc_ref}	Output voltage	2.9	3.0	3.1	V	For $T_j = -40$ to 125°C
$\Delta V/V$	Line regulation	-0.1		0.1	%/V	For V_{bat} variation

12.4 Clocks

Table 18. 1PPS

This pulse is synchronized with GPS system clock

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Pulse width		125		μs	
	Jitter	-50	3	50	ns	Stationary and receiving 4 or more satellites

Table 19. BB_EXT_CLK

This clock is coupled to GSM network

Symbol	Parameter	Min	Typ	Max	Unit	Note
$f_{bb_ext_clk}$	frequency		26/N		MHz	for N= 1, 2, ..., 8
			156/M		MHz	for M=9, 10, ..., 16
$\Delta f/f_0$	frequency drift		0.7	1	ppm	

Table 20. Micro-controller clock

External crystal required for high speed CAN, for all other purposes, internal RC oscillator is sufficient

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{mc_xtal}	Crystal frequency	1	-	24	MHz	In case of externally oscillator, connected to MC_XTAL_(1 2)
$V_{(rms)mc_xtal}$	Oscillation amplitude	0.2	-		V (RMS)	
t_{hmc_xtal}	Clock High time	$t_{cycle} \times 0.4$	-		ns	
t_{lmc_xtal}	Clock Low time	$t_{cycle} \times 0.4$	-		ns	
t_{rmc_xtal}	Clock rise time			5	ns	
t_{fmc_xtal}	Clock fall time			5	ns	
f_{mc_ircl}	Oscillator frequency	3.96	4	4.04	MHz	Frequency of internal RC oscillator

13. Dynamic characteristics

13.1 Power consumption

All measured current consumption have been measured at 25°C with a power supply at 3.7V

Table 21. Utility processor power consumption

Includes LDO

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Cortex M3 at 12 MHz	7	7 ^[1]		mA	at 25°C, code while(1){}
	Cortex M3 at 100 MHz		42 ^[1]		mA	
	Powerdown mode		150		µA	^[2]
	RTC active		1		µA	backup registers saved ^[3]

[1] No peripherals enabled

[2] Wake-up can be initiated by event on RTC, CAN, USB and most GPIOs

[3] If a separate power source such as coin cell battery is connected to VBAT_RTC_SNK and no power is supplied via VBAT_MC_SNK

Table 22. Application processor consumption characteristics

Baseband ARM and memories power consumption additionally to GSM/GPRS function

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Application processor	0 ^[1]	20	60	mA	

[1] Leakage currents are included in [Table 23](#)

Table 23. Communication coprocessor consumption characteristics

Covers baseband RF frontend as well as memories (PSRAM and flash)

Symbol	Parameter	Min	Typ	Max	Unit	Note
	complete GSM function network attachment		115 ^[1]		µAh	Energy consumption equivalent to 300s of idle mode
	complete GSM function active in idle mode	1.085 ^[2]	1.31 ^[3]	2.05 ^[4]	mA	Average consumption, assuming typical setting for mobile network. Peak consumption for GSM/GPRS at maximum power can reach up to 1600 mA during transfer slots (577 µs)
	complete GSM function during voice call	79 ^[5]	114 ^[6]	220 ^[7]	mA	
	complete GPRS function during data transfer (Class 10: 2T+3RX)	140 ^[5]	205 ^[6]	400 ^[7]	mA	
	complete GSM function in sleep mode		600		µA	GSM function active
	complete GSM function leakage current		50		µA	

[1] Network dependent, assumes a typical 7s radio measurement plus 0.5s network inscription

[2] BS_PA_MFRMS = 9, i.e. paging from network will be checked every 2100 ms

[3] BS_PA_MFRMS = 5, i.e. paging from network will be checked every 1175 ms. This is typically the setting used by most mobile operators

- [4] BS_PA_MFRMS = 2, i.e. paging from network will be checked every 470 ms
 [5] PCL = 19, i.e. 4.9db amplification for GSM900
 [6] PCL = 7, i.e. 29.2db amplification for GSM900
 [7] PCL = 5, i.e. 33.1 db amplification for GSM900

Table 24. Security processor power consumption

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Function switched off			0	μA	included in NFC coprocessor
	Function active		6		mA	

Table 25. NFC coprocessor power consumption

Covers NFC and SMX

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Function switched off		2		μA	
	Power down		35		μA	RF field detection on
	Function active		30		mA	
	function active with RF transmission ongoing		90	130	mA	

13.2 Battery charging

Table 26. Battery charging

Measured at 3.7V, 25°C

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Battery overvoltage detection	60	90	130	mV	Battery voltage in excess of VFAST above which fast charge is automatically disabled
	Battery overcurrent detection	190	210	230	mA	Battery current in excess of programmed current above which fast charge is automatically disabled
	Fast charge stop		50		mA	
$\Delta V_{Oreg}/V_{Oreg}$	Relative regulator output voltage variation	-1		+1	%	
$\Delta I_{Oreg}/I_{Oreg}$	Relative regulator output current variation	-12		+12	%	
I_{qvchg}	Quiescent current drawn from VCHG_SNK		3		mA	
I_{qbb_ighgp}	Quiescent current drawn from BB_ICHG_P			40	μA	during charge
I_{qbb_ighgn}	Quiescent current drawn from BB_ICHG_P			60	μA	during charge
I_{qvat_snk}	Quiescent current drawn from VBAT_SENSE_[P N]			200	μA	during charge

14. Thermal characteristics

14.1 Internal heater²

As described in [Table 2](#), OM12001 (ATOP) can operate between -40 and +85°C, except for the NFC and Security processor which are limited to a -25 to +85°C temperature range.

To ensure that operating range can be rapidly reached, an internal heater is available to heat-up the device.

The internal heater is controlled by internal micro-controller pin P2.5 (active high).

Internal temperature should be monitored when heater is used. It must not be enabled for more than a few seconds if current temperature is greater than 25°C as otherwise there is a risk of destruction for the heater.

Table 27. Internal heater characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Current drawn	500	600	700	mA	
	Power dissipated	1600	2500	3400	mW	Dependant on V_{bat}

14.2 Internal temperature sensor

OM12001 (ATOP) includes an internal temperature sensor. This sensor is used by GSM baseband to tune its VCXO to achieve network lock-on but is also accessible to the internal micro-controller which can use it to.

Internal micro-controller (LPC1768) has also access to this sensor to adapt its behavior to conditions, i.e enabling internal heater in case of low temperature,

[Figure 9](#) presents accuracy of the internal temperature measurement depending on ambient temperature.

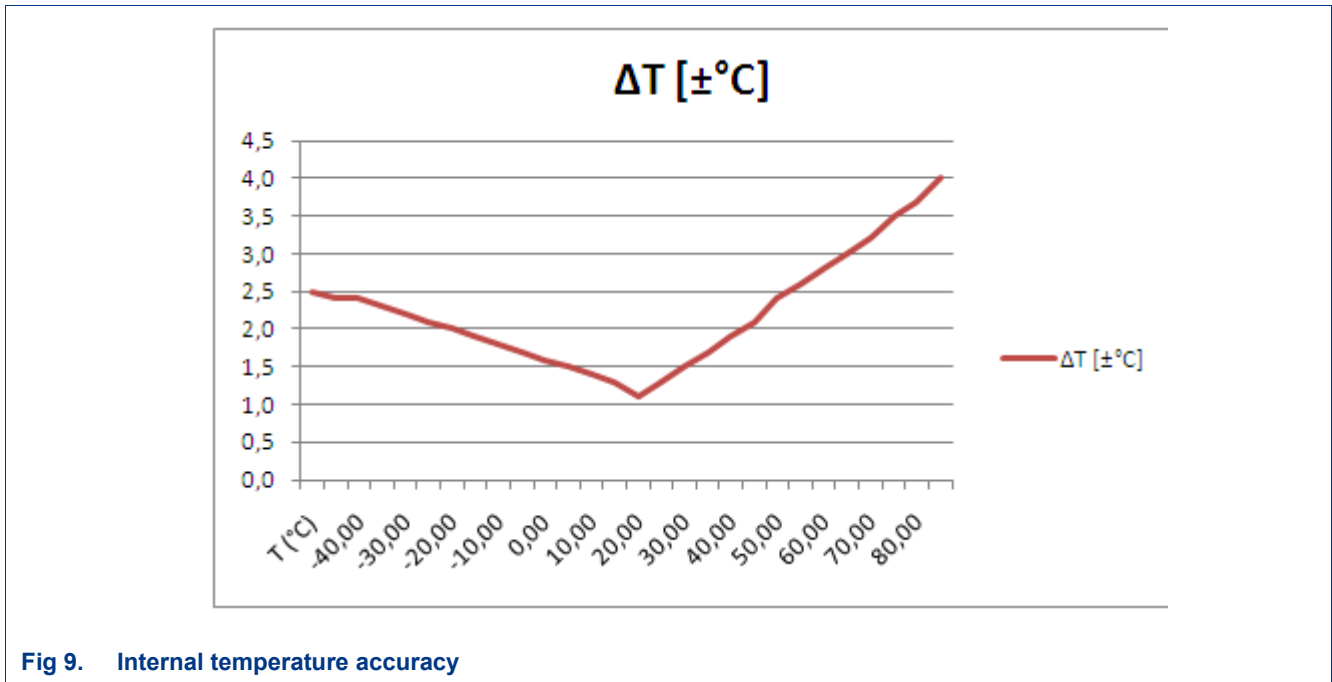


Fig 9. Internal temperature accuracy

14.3 Battery temperature sensor

To improve lifetime, it is recommended to avoid charging batteries, outside of the temperature range specified by their manufacturers, typically 0 to 50°C.

For Lithium-Ion battery, the charger circuit inside OM12001 (ATOP) will use by default the internal temperature sensor. However, in some cases, depending on implementation, it can be expected the temperature of the battery will be significantly different from module temperature. It is then recommended to use a battery with internal sensor. OM12001 (ATOP) supports the use of an external thermistor dedicated to battery.

Note that even if a separate thermistor is not used, this input is used to detect battery presence.

Table 28. Battery temperature sensor

Symbol	Parameter	Min	Typ	Max	Unit
R _{thermin}	Internal pull-up		10		kΩ
R _{tol}	input resistor tolerance accuracy	-1		1	%

15. Handling information

16. Soldering

OM12001 (ATOP) is a laminate based module with a metal cover and a Land Grid Array (LGA) at the bottom side of the product. The OM12001 (ATOP) can be assembled using a standard Surface Mount Technology (SMT) reflow process in a convection oven.

[Figure 10](#) and [Table 29](#) indicate the maximum and minimum limits of the solder profile. The applied profile has to fit within these limits.

It is recommended to use a standard no-clean SAC solder paste for a lead free assembly process.

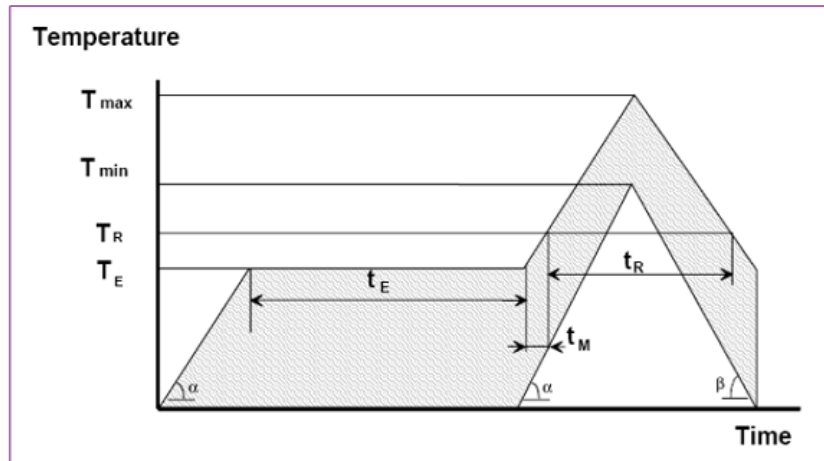


Fig 10. Reflow profile

Table 29. Reflow profile parameters

Symbol	Parameter	Min	Unit
α	Temperature gradient (ramp-up)	< 3	°C/s
β	Temperature gradient (cool-down)	< 5	°C/s
T_E	Preheat (soak) temperature	150 to 200	°C
t_E	Preheat time	60 to 180	s
t_M	Time to melting	6 to 35	s
T_R	Reflow temperature	> 217	°C
t_R	Reflow time	60 to 150	s
T_{Min}	Minimum peak temperature	235	°C
T_{Max}	Maximum peak temperature	260	°C
	Maximum time above 250°C	10	s
	Maximum time 25°C to peak temperature	8	mn

17. Mounting

17.1 PCB layout

The PCB footprint design is a copy of the metal LGA pattern at the bottom side of the ATOP package.

17.2 Stencil design

The dimensions of the solder stencil apertures can be found in [Figure 11](#). In general there are 2 aperture sizes applied for the stencil:

- 0.7 mm diameter for the inner pads⁵

- 0.8 mm for the outer pads

The recommendation for the stencil thickness is 150 µm.

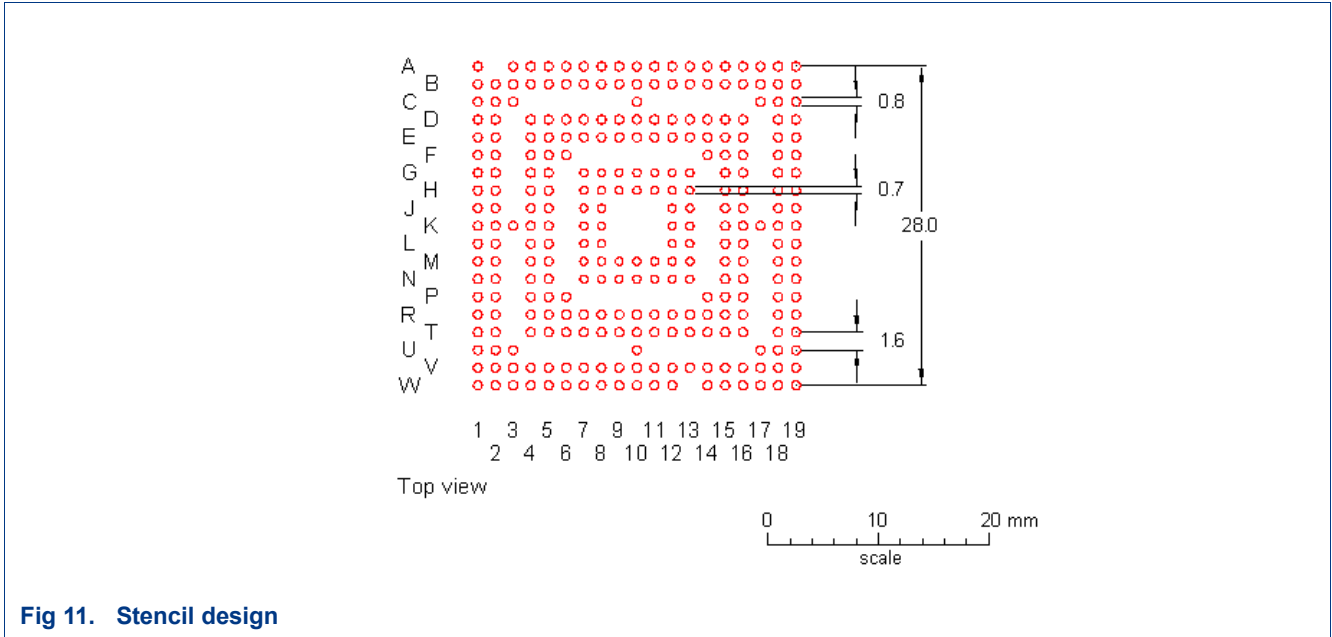


Fig 11. Stencil design

18. Marking

[Figure 12](#) shows label present on the module.



Fig 12. OM12001/100 labelling

Labelling can be decoded as follows:

- First line: Product name, ie OM12001/100 or OM12001/000
- Second line: Serial number
- Third line: Production info, including production site, RHF-2006 indicator⁶, date code
- Fourth line: BOM number
- Fifth line: FCC ID, ie XXMOM12001100 or XXMOM12001000 and Notified body for CE certification
- Sixth line: IC ID, ie 8764A-OM12001100 or 8764A-OM12001000
- Seventh line: IMEI

DataMatrix 2D barcode includes the following information:

- Serial number
- EMS Internal product code
- Date code
- Product name, ie OM12001/100 or OM12001/000
- IMEI Type Allocation Code (TAC) iteration number⁷

6. E standing for Exempted, ie. incorporates product containing exempted Lead that do contain Halogens/Antimony. For example products with eutectic solder die-attach (HSOP/SIL-P) packages and glass-diodes containing Lead

7. 1 stands for a TAC value of 35374505 for OM12001. IMEI can be computed by concatenating TAC, the 6 last digits of serial number and Check Digit, (CD) computed with Luhn formula

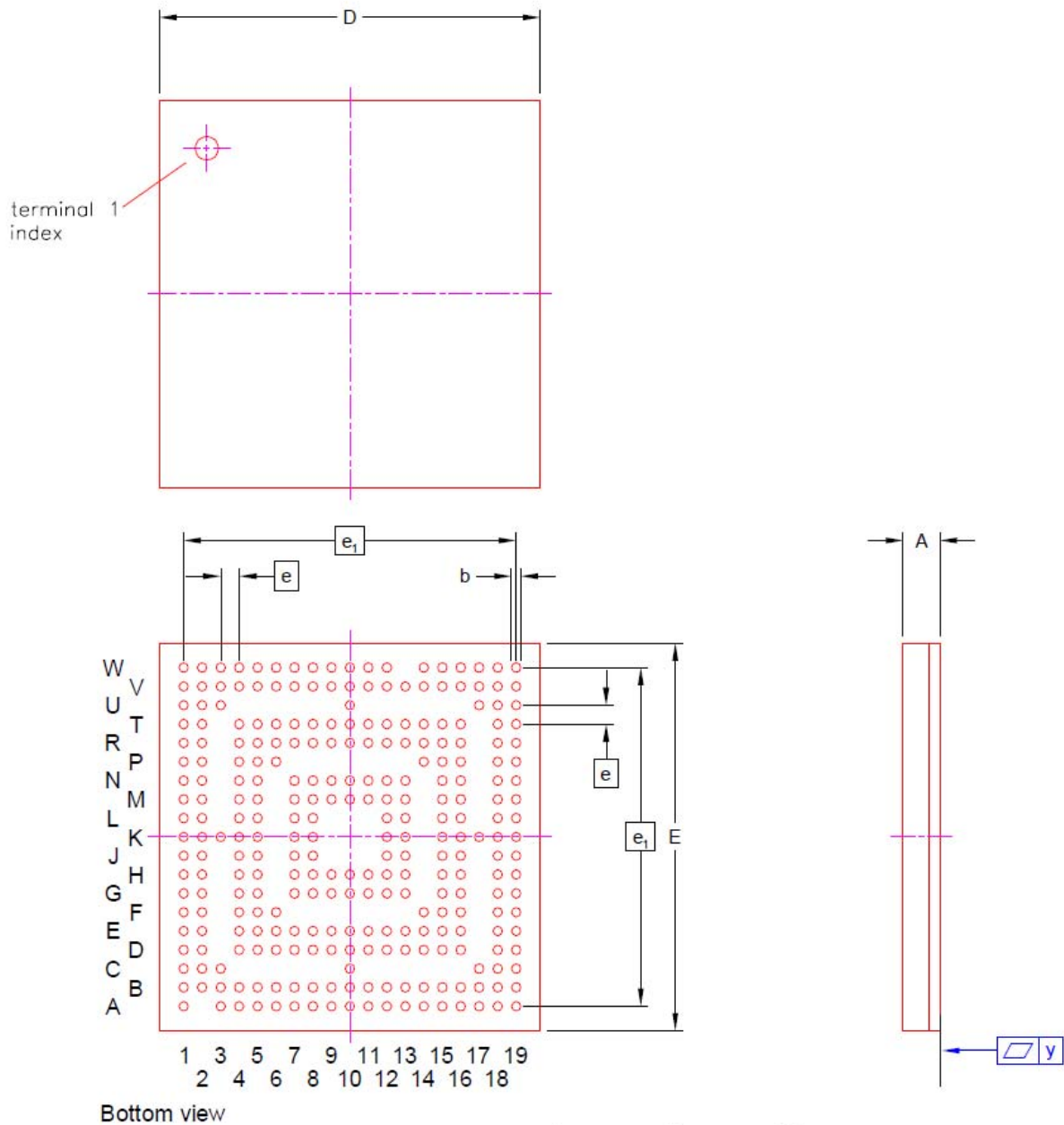
19. Packing information

OM12001 (ATOP) modules are packed in trays. Before packing and shipping, trays have been dry baked for 16 hours at 125°C, according to IPC/JEDEC J-Std-033B.1.

OM12001 (ATOP) has been tested according to IPC/JEDEC J-STD 020D and is classified as Moisture Sensitivity Level 3 (MSL3).

20. Package outline

ATOP presents itself as a 33x33x3.35 mm module. Ball size is 0.8 mm with a 1.6mm pitch.



Dimensions

Unit	A	b	D	E	e	e ₁	y
max	3.58	0.85	33.1	33.1			
mm nom	3.38	0.80	33.0	33.0	1.6	28.8	0.1
min	3.18	0.75	32.9	32.9			

Note

1. Protrusions of 0.25 mm maximum in the 4 corners of the package carrier are not included.

Fig 13. OM12001 (ATOP) package outline and dimensions

21. Support information

For support, please contact support.telematics@nxp.com

22. Test information

For production and end of line testing the following tools will be provided:

- SW tools to interface to module:
 - parameters setting (e.g. battery settings, ...)
 - file download
 - flash update

23. Safety instructions

OM12001 (ATOP) is a class A digital device marketed for use in a commercial, industrial or business environment.

It has been tested to be conform to FCC as well as to R&TTE Articles 3.1(a) and (b), safety and EMC respectively, and relevant Article 3.2 requirements using NXP reference board. The manufacturer of the final product integrating OM12001 (ATOP) must assess its equipment against the Essential requirements of the R&TTE and FCC Directives

OM12001 (ATOP) is compliant with the following standards:

- Mandatory european standards
 - R&TTE Article 3.1a: Electrical safety (EN60950)
 - R&TTE Article 3.1a: SAR (EN62209-1): MPE calculation as distance > 20 cm
 - R&TTE Article 3.1b: EMC (EN301489-1 and -7 for GSM, EN301489-3 V1.4.1, EN300440-2 for NFC and GPS)
 - R&TTE Article 3.2: Radiated RF (EN301511 for GSM, EN302291-1-2 V1.1.1 for NFC and GPS)
 - Notified Body opinion according to Annex IV: Evaluation of compliance with essential requirements
- Mandatory US and Canadian standards
 - FCC EMC: part 15B
 - FCC RF: part 24 for PCS1900, part 22 for GSM850, part 15.225 for GPS and NFC
 - FCC certificate from Telecom Certification body
- Voluntary certification
 - Global Certification Forum (GCF), including field tests
 - PCS-1900 Type Certification Review Board (PTCRB)

Reports are available upon requests

SAR according to EN 62209-1 has not been checked and replaced by MPE calculation, hence the antenna(s) used in the final application must be installed to provide a separation distance of at least 20 centimeters from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. Additionally, for FCC compliance, the system antenna(s) gain must not exceed 2.24 dBi for mobile and fixed or mobile operating configurations.

Manufacturer of the final product using OM12001 (ATOP) will have to provide instructions for antenna installation and transmitter operating conditions to satisfy to RF exposure compliance.

Manufacturer of the final product using OM12001 (ATOP) should take care that OM12001 (ATOP) is always within the operating limits (such as temperature, power supply, ...) described in the present document, in particular it must be supplied by a limited power source according to EN 60950-1.

Physically, the clearance and creepage distances required by the end product must be withheld when the module is installed. The cooling of the end product shall not negatively be influenced by the installation of the module.

Manufacturers of devices incorporating this module are advised to clarify any regulatory questions and to have their complete product tested and approved for R&TTE, FCC compliance and all relevant regulations.

23.1 FCC Labeling

If the FCC and IC IDs are not visible when the module is installed inside the host device, then the outside of the device into which the module is installed must also

display a label referring to the enclosed module. This exterior label can use wording such as the following: or "Contains FCC ID: XXMOM12001000 or XXMOM12001100." And "Contains IC : 8764A-OM12001000 or 8764A-OM12001100." Any similar wording that expresses the same meaning may be used.

Intentionally left blank.

24. Appendix

25. Abbreviations

Table 30. Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AHB	AMBA High Performance Bus
ATOP	Automotive Telematic On-board unit Platform
CLK	Clock
CPU	Central Processing Unit
DAC	Digital to Analog Converter
DCS	Digital Cellular System
DES	Data Encryption Standard
DMA	Direct Memory Access
DPA	Differential Power Analysis
DSP	Digital Signal Processor
EEPROM	Electrically Erasable Programmable Read Only Memory
GP	General Purpose
GPIO	General Purpose Input Output
IF	Intermediate Frequency
IRQ	Interrupt ReQuest
JCOP	Java Card Open Platform
LDO	Low DropOut
LNA	Low Noise Amplifier
MCU	Micro-Controller Unit
MIDP	Mobile Information Device Profile
NFC	Near Field Communication
NiMH	Nickel Metal Hybrid
OBU	On Board Unit
OS	Operating System
OTP	One Time Programmable
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PKI	Public Key Infrastructure
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RF	Radio Frequency
ROM	Read Only Memory

Table 30. Abbreviations ...continued

Acronym	Description
RSA	A public-key encryption technology developed by RSA Data Security, Inc. The acronym stands for Rivest, Shamir, and Adelman, the inventors of the technique
RTC	Real Time Clock
RTOS	Real Time Operating System
SAW	Surface Acoustic Wave
SIM	Subscriber Identification Module
SNR	Signal to Noise Ratio
SPA	Simple Power Analysis
SPI	Serial Peripheral Interface
TCXO	Temperature Controlled Crystal Oscillator
UART	Universal Asynchronous Receiver Transmitter

26. Glossary

<term> — <definition>

27. References

- [1] **ZVEI - Zentralverband Elektrotechnik- und Elektronikindustrie e.V. —**
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- [2] **LPC1768 datasheet —**
http://www.nxp.com/documents/data_sheet/LPC1769_68_67_66_65_64_63.pdf
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http://www.nxp.com/documents/user_manual/UM10360.pdf
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