Baseband Hardware

- 16MHz main clock input
- Firmware execution from either internal ROM or external flash
- Built-in internal ROM or 4M flash for program memory
- Built-in 32 KB RAM for data storage and baseband data transfer buffering
- New features for Bluetooth 2.1
  - Encryption Pause and Resume
  - Erroneous Data Reporting
  - Extended Inquiry Response
  - Link Supervision Timeout Changed Event
  - Non-Flushable Packet Boundary Flag
  - Secure Simple Pairing
  - Sniff Subtracting
- Support both Pico-net and Scatter-net applications
- Hard-wired logic for modulation, demodulation, access code correlation, whitening, forward error correction (FEC), header error check (HEC), shorten hamming code, CRC generation/checking, frame check sequence (FCS), encryption bit stream generation, and transmit pulse shaping
- Adaptive Frequency Hopping (AFH) avoids occupied RF channels
- Fast Connection supported

RF Hardware

- Fully Bluetooth 2.1 + EDR system in 2.4 GHz ISM band.
- Combined TX/RX RF terminal simplifies external matching and reduces external antenna switches.
- Build-in channel filter.
- To avoid temperature variation, temperature sensor with temperature calibration is utilized into bias current and gain control.

- Fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.
- Crystal oscillation with build-in digital trimming for temperature/process variations.

Audio processor

- 16-bit/32-bit run time configurable audio processor
- Single cycle data computing up to 60 MIPS
- Support 64 kb/s A-Law or μ-Law PCM format, or CVSD (Continuous Variable Slope Delta Modulation) for SCO channel operation.
- SBC and optional MP3 supported

Stereo Audio Codec

- 16 bit stereo codec
- Dual mono microphone and stereo line in for ADC
- 94dB SNR stereo DAC playback
- Integrate headphone amplifier for 16Ω speakers
- Capacitor-less headphone driver stage for single-ended speakers

Peripherals

- Built-in Lithium-ion battery charger
- Integrate 3V, 1.8V LDO and Switching mode regulator
- Built-in 10-bit Aux-ADC for battery monitor and voltage sense.

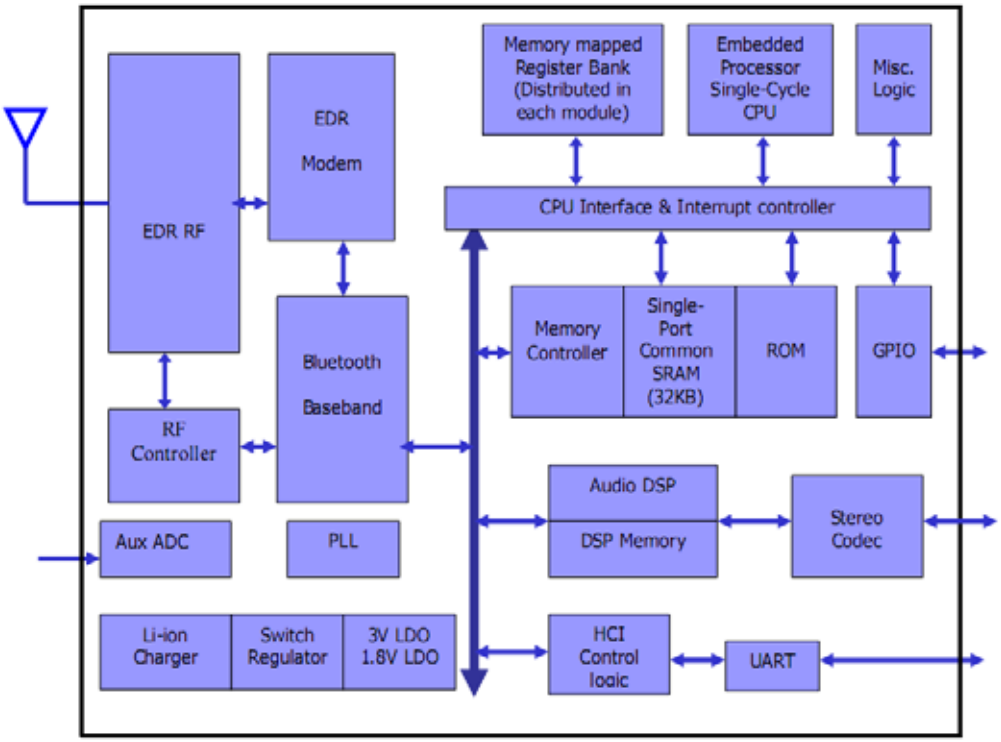
Flexible HCI interface

- High speed HCI-UART (Universal Asynchronous Receiver Transmitter) interface

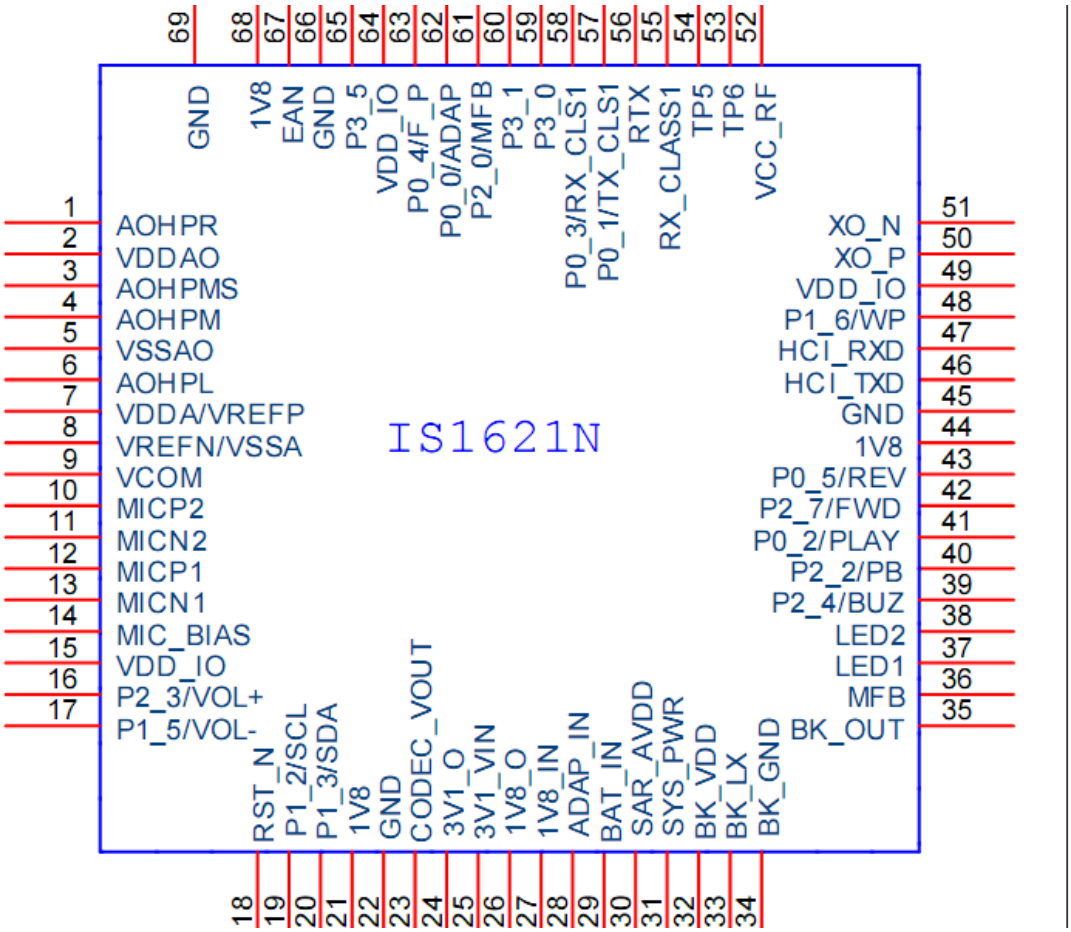
Package

- 68QFN standard package

3. Functional Diagram



4. Pin Assignment



5 Pin Descriptions

Pin No.	I/O	Pin Name	Pin Descriptions
1	AO	AOHPR	R-channed single ended analog headphone output
2	P	VDDAO	Positive power supply dedicated to CODEC output amplifiers.
3	AI	AOHPMS	Headphone common mode sense input
4	AO	AOHPM	Headphone common mode output
5	P	VSSAO	Negative power supply dedicated to CODEC output amplifiers
6	AO	AOHPL	L-channel single ended analog headphone output
7	P	VDDA/VREFP	Positive power supply/reference voltage for CODEC
8	P	VREFN/VSSA	Negative reference/power supply for CODEC Must be connected to the PCB analog ground(AGND)
9	AO	VCOM	Internal biasing voltage for CODEC
10	AI	MICP2	Mic 2 mono differential analog positive input
11	AI	MICN2	Mic 2 mono differential analog negative input
12	AI	MICP1	Mic 1 mono differential analog positive input
13	AI	MICN1	Mic 1 mono differential analog negative input
14	P	MIC_BIAS	Electric microphone biasing voltage
15	P	VDD_IO	I/O power supply input
16	I/O	P2_3/VOL+	GPIO, default pull-high input Be triggered by a LOW level signal Volume up key as the default setting
17	I/O	P1_5/VOL-	GPIO, default pull-high input Be triggered by a LOW level signal Volume down key as the default setting

18	AI	RST_N	System Reset Pin
19	I/O	P1_2/SCL	GPIO, default pull-high input EEPROM clock Clock signal for OLED driving IC BIST Testing
20	I/O	P1_3/SDA	GPIO, default pull-high input EEPROM data Data signal for OLED driving IC BIST Testing
21	P	1V8	Core 1.8V power input
22	P	GND	Digital ground.
23	P	CODEC_VOUT	3.1V LDO output for CODEC power
24	P	3V1_O	3.1V LDO output
25	P	3V1_VIN	3.1V LDO input
26	P	1V8_O	1V8 LDO Output
27	P	1V8_IN	1V8 LDO Input

Pin No.	I/O	Pin Name	Pin Descriptions
28	P	ADAP_IN	External power adaptor input
29	P	BAT_IN	Battery input
30	P	SAR_AVDD	SAR 1.8V input
31	P	SYS_PWR	System Power Output
32	P	BK_VDD	Buck VDD Power Input
33	P	BK_LX	Buck feedback input
34	P	BK_GND	Buck ground
35	P	BK_OUT	Buck output
36	P	MFB	Multi-Function Push Button key, push high
37	AI	LED1	LED Driver 1
38	AI	LED2	LED Driver 2
39	I/O	P2_4/BUZ	GPIO, default pull-high input HIGH or toggle to drive Buzzer/Charging Status/I2C CSB IC BIST testing/ASIC functional testing System Configuration, H: Boot Mode
40	I/O	P2_2	GPIO, default pull-low input. Reserve LED driver/ MFB function Be triggered by a HIGH level signal.
41	I/O	P0_2/Play	GPIO, default pull-high input Be triggered by a LOW level signal Play/Pause key as the default setting
42	I/O	P2_7/FWD	GPIO, default pull-high input Be triggered by a LOW level signal FWD key as the default setting

43	I/O	P0_5/REV	GPIO, default pull-high input Be triggered by a LOW level signal REV key as the default setting ASIC functional testing
44	P	1V8	Core 1.8V power input
45	P	GND	Digital ground
46	O	HCI_TXD	HCI TX data
47	I	HCI_RXD	HCI RX data
48	I/O	P1_6	GPIO P1_6, default pull-high input EEPROM WP. RTS for OLED.
49	P	VDD_IO	I/O power supply input
50	I	XO_P	16MHz Crystal input positive
51	I	XO_N	16MHz Crystal input negative
52	RP	VCC_RF	RF power input for both VCO and IO power
53	I/O	TP6	RF test point

Pin No.	I/O	Pin Name	Pin Descriptions
54	I/O	TP5	RF test point
55	I	RX_CLASS1	Class1/Class2 RX path without TR combiner Combine with P0_1/P0_3 to control the external TR Switch & LNA.
56	I/O	RTX	Class 2 RTX path (TR combiner active); Class1/Class2 TX path
57	I/O	P0_1/TX_CLS1	GPIO, default pull-high input Class1/Class2 Control signal of external TR switch HIGH is TX duration
58	I/O	P0_3/RX_CLS1	GPIO, default pull-high input Class1/Class2 Control signal of external TR switch HIGH is RX duration
59	I/O	P3_0	GPIO, default pull-high input UART_CTS is implemented for OLED control ASIC functional testing
60	I/O	P3_1	GPIO, default pull-high input Be triggered by a HIGH level signal External MCU wake-up signal ASIC functional testing
61	I/O	P2_0	GPIO, default pull-high input I2C SCLK ASIC functional testing System Configuration, H: Application L: Baseband

62	I/O	P0_0/ADAP	GPIO, default pull-low input. Adapter Plug-In Indicator/Reserve LED driver/I2C MCLK IC BIST testing
63	I/O	P0_4/F_P	GPIO, default pull-high input Be triggered by a LOW level signal Fast paring key/External Regulator Enable/I2C SDATA
64	P	VDD_IO	I/O power supply input
65	I/O	P3_5	GPIO 3_5, default pull-high input.
66	P	GND	Digital ground.
67	I	EAN	Embedded ROM/External Flash enable H: Embedded; L: External Flash
68	P	1V8	Core 1.8V power input
69	P	GND	Exposed pad as ground

NOTE: Default GPIO Setting

A. P0_1/P0_3 is configured in EEPROM for Class1/Class2 applications.

B. Class1/Class2 Control Signal of external TR switch:

P0_1 High: TX, P0_3 High: RX

C. Music Control:

Play/Pause: P0_2, FWD: P2_7, REV: P0_5,Volume up:P2_3,Volume down:P1_5

D. EEPROM/OLED Control:

P1_6:EEPROM WP/UART_RTS for OLED Control

P1_2:EEPROM Clock/Clock Signal for OLED driving

P1_3:EEPROM Data/Data Signal for OLED driving

P3_0:UART_CTS for OLED control

P3_1:External MCU wake-up signal

E. I2C:

SCLK:P2_0, SDATA: P0_4, CSB:P2_4,MCLK:P0_0

F. External Power Manager Control Signal:

P0_0: Adapter Plug-In Indicator

P2_2: MFB function

P0_4: External Regulator Enable

P2_4: Charging Status

G. Other Function:

Fast Paring Key:P0_4

Buzzer: P2_4

System Configuration: P2_0, P2_4