Technical Description

The Equipment Under Test (EUT) i s a Wireless Slim Keyboard. It can pai r with a corresponding dongle. The 2.4GHz module in the EUT is operating in the frequency range from 2408MHz to 2474MHz (67 channels wi th 1MHz channel spacing). The EUT is powered by 3.0VDC (2 x 1.5VDC "AAA" size batteries).

2.4GHz Bluetooth Module:
Modulation Type: FSK
Antenna Type: Integral, Internal (PCB Trace)
Frequency Range: 2408MHz - 2474MHz, 1MHz channel spacing, 67 channels

Nominal field strength is 96.0dBµV/m @ 3m
Production Tolerance of field strength is +/- 3dB
Antenna gain is 1.1dBi

The functions of main ICs are mentioned below.

1. 2.4GHz module MA13361

1) MA13361 acts as the 2.4GHz radio core of 2.4Ghz module
2) 12MHz crystal (X1) provides clock for MA13361
3) U2 (24C02) is serial EEPROM for parameter backup of MA13361

MA13361

RF 2.4G SOC for Keyboard Device

Specification V1.0

MosArt

SEMICONDUTOR CORP.

Content

1. General Description 2
2. Features 2
3. Block Diagram 3
4.Pin Assignments & IC Top Code 4
5. Pin Out & Description 5
6. DC/AC & 2.4Ghz RF Character 7
7. Package Type 9
8. Key Matrix 10
9. Application circuit 11
9.1 Dual cell Battery (Package) 11
9.2 Dual-cell Battery (dice) :support Volume,Caps LED 12
9.3 A singlel-cell Battery (Package) 13
9.4 A singlel-cell Battery (dice) :support Volume,Caps LED 14
10. Pad Diagram 15

1. General Description

The MA13361 is a RF 2.4G SOC that can transceiver data's from the Keyboard device and sends these data's via RF at 2.4 GHZ.

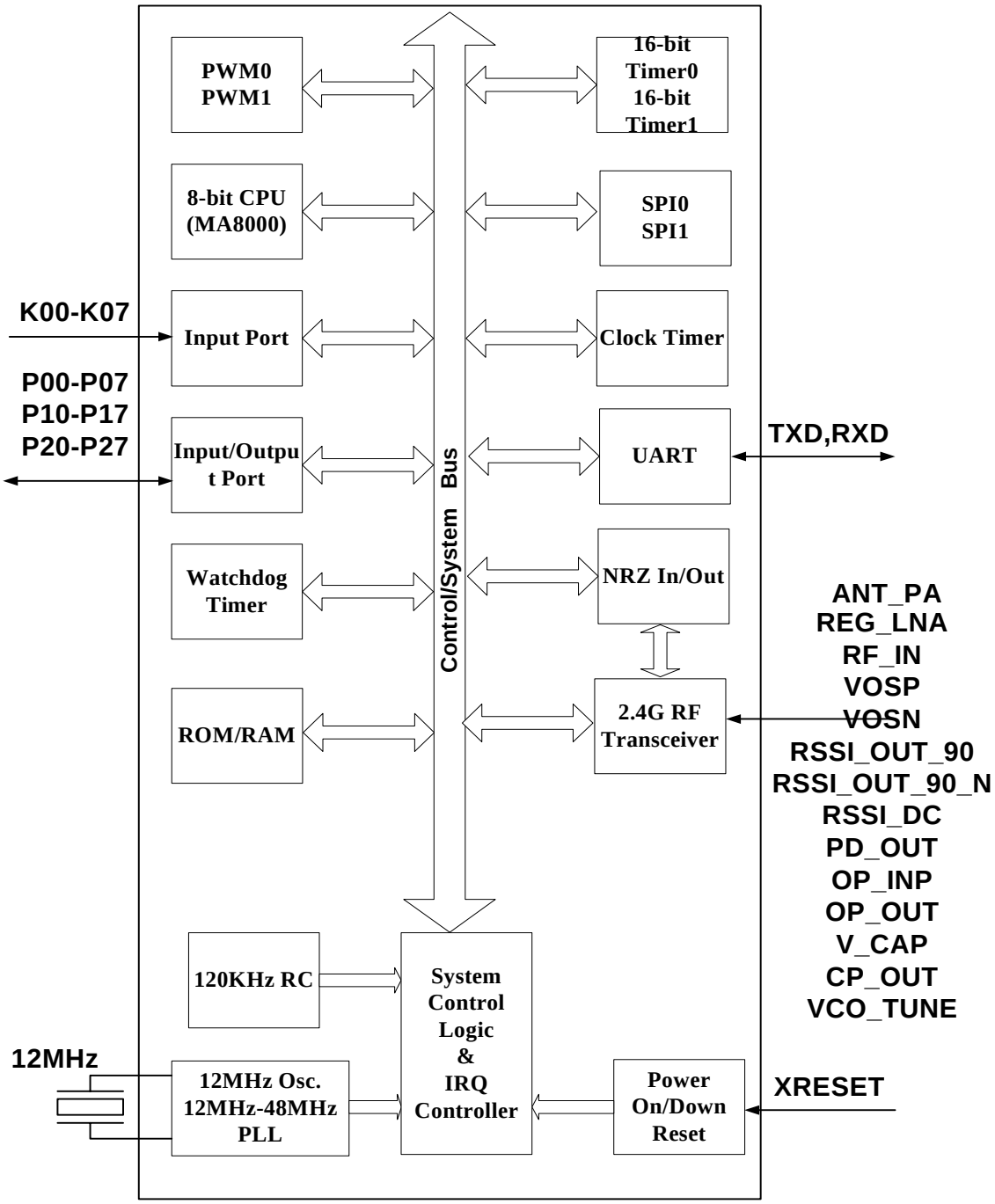
The MA13361 is equipped with a complete set of FSK transceiver that also provides 64 RF channels. This will reduce the extra external component for 2.4G Keyboard.

The MA13361 operates a wireless keyboard device transmitter. MA13361 can transmit command and echo status or data format, which communicate to MA64101 for RF2.4G application

2. Features

- 2.4G SOC chip built-in 2.4G RF transceiver
- FSK modulation type
- Hopping Type : FHSS
- 375k bps air-protocol,2 ways
- 67 RF channels.
- Key matrix : 8 x 18 keys
- Battery low detection.
- Built-in 8k bytes OTP-ROM.
- Built-in 512 bytes SRAM.
- Support EEPROM to reserve ID and channel number
- Support Volume scroll and Z axis scroll

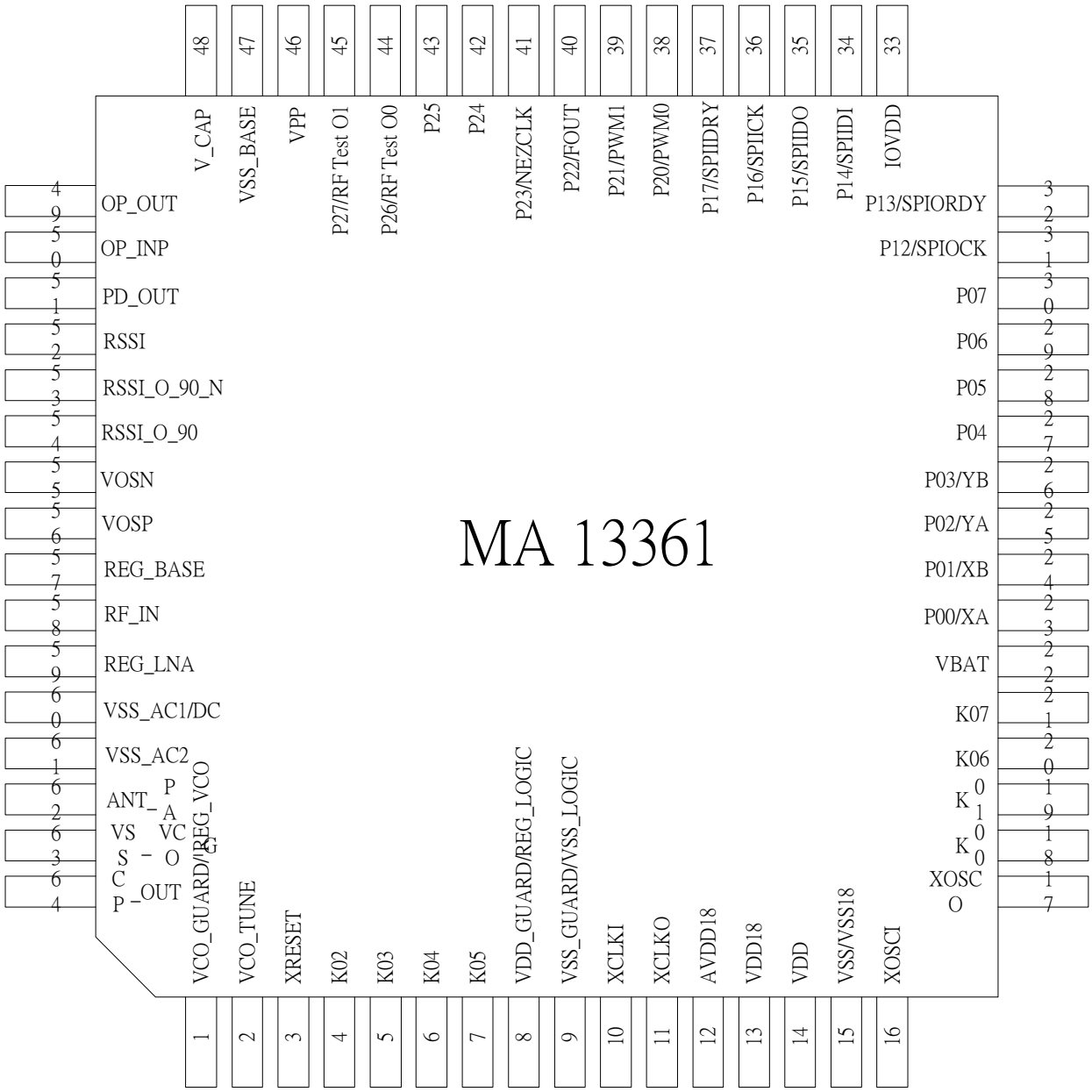
3. Block Diagram



4.Pin Assignments & IC Top Code

64-pin LQFP Package

Top code: MA13361



5. Pin Out & Description

PIN #	Pin Name	Input/Output	Pin Description
1	VCO_GUARD/ REG_VCO	Analog	RF power ring for VCO circuit (1.8V)
2	VCO_TUNE	Analog	RF VCO frequency tuning voltage
3	XRESET	Input	System reset input
4	K02	Input	I/O pin with software selectable
5	K03	Input	I/O pin with software selectable
6	K04	Input	I/O pin with software selectable
7	K05	Input	I/O pin with software selectable
8	VDD_GUARD/REG_LOGIC	Analog	RF power regulator for logic circuit (1.8V)
9	VSS_GUARD/VSS_LOGIC	Analog	RF ground ring for logic circuit
10	XCLKI	Input	External Crystal 12MHz Input
11	XCLKO	Output	External Crystal 12MHz Output
12	AVDD18	Analog	12MHz Crystal power input (1.8V)
13	VDD18	Power	Power pin (1.8V) (Regulator output)
14	VDD	Power	Power pin (3.3V) (For RF circuit)
15	VSS/ VSS18	Power	Ground pin (3.3V)
16	XOSCI	Input	External Crystal 32KHz Input
17	XOSCO	Output	External Crystal 32KHz Output
18	K00	Input	I/O pin with software selectable
19	K01	Input	I/O pin with software selectable
20	K06	Input	I/O pin with software selectable
21	K07	Input	I/O pin with software selectable
22	VBAT	Analog	Battery voltage input
23	P00/XA	I/O0	I/O pin with software selectable
24	P01/XB	I/O0	I/O pin with software selectable
25	P02/YA	I/O0	I/O pin with software selectable
26	P03/YB	I/O0	I/O pin with software selectable
27	P04	I/O0	I/O pin with software selectable
28	P05	I/O0	I/O pin with software selectable
29	P06	I/O0	I/O pin with software selectable
30	P07	I/O0	I/O pin with software selectable
31	P12/SPI0CK	I/O0	I/O pin with software selectable
32	P13/SPI0RDY	I/O0	I/O pin with software selectable
33	IOVDD0	Power	I/O0 Power pin
34	P14/SPI1DI	I/O1	I/O pin with software selectable
35	P15/SPI1DO	I/O1	I/O pin with software selectable
36	P16/SPI1CK	I/O1	I/O pin with software selectable
37	P17/SPI1RDY	I/O1	I/O pin with software selectable
38	P20/PWM0	I/O1	I/O pin with software selectable
39	P21/PWM1	I/O1	I/O pin with software selectable
40	P22/FOUT	I/O1	I/O pin with software selectable
41	P23/NRZCLK	I/O1	I/O pin with software selectable

42	P24	I/O1	I/O pin with software selectable
43	P25	I/O1	I/O pin with software selectable
44	P26/RFTESTO0	I/O1	I/O pin with software selectable
45	P27/RFTESTO1	I/O1	I/O pin with software selectable
46	VPP	Power	OTP Write Power pin (6.5V)
47	VSS_BASE	Analog	RF regulator ground for base-band circuit
48	V_CAP	Analog	Sample and Hold capacitor
49	OP_OUT	Analog	Data filter OP output
50	OP_INP	Analog	Data filter OP positive input
51	PD_OUT	Analog	Phase detect output
52	RSSI_DC	Analog	RSSI DC output
53	RSSI_O_90_N	Analog	RSSI limiting Amplify, negative output 90°
54	RSSI_O_90	Analog	RSSI limiting Amplify, positive output 90°
55	VOSN	Analog	RSSI offset negative cancel pin
56	VOSP	Analog	RSSI offset positive cancel pin
57	REG_BASE	Analog	RF regulator for base-band circuit (1.8V)
58	RF_IN	Analog	RF input pin
59	REG_LNA	Analog	RF power regulator for LNA circuit (1.8V)
60	VSS_ANT_DC	Analog	Antenna DC ground pin
61	VSS_ANT_AC	Analog	Antenna AC ground pin
62	ANT_PA	Analog	Antenna connected pin
63	VSS_VCO_G	Analog	RF ground ring for VCO circuit
64	CP_OUT	Analog	RF charge pump output

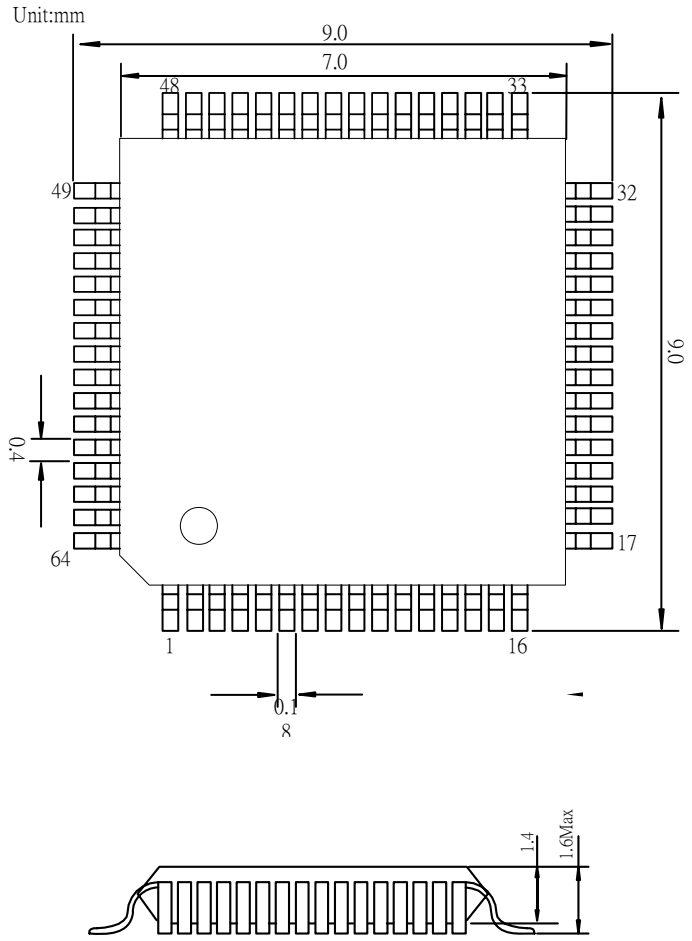
6. DC/AC & 2.4Ghz RF Character

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power supply						
Vdd	Supply voltage		2.4	3.0	3.6	V
Iss	Operation current (3.0V)	Osc = 120kHz RC (RAM mode)		45		uA
Iss	Operation current (3.0V)	Osc = 120kHz RC (ROM mode)		80		uA
Iss	Operation current (3.0V)	Osc = 12MHz (ROM mode)		5.5		mA
Input (VDD=3.3V, IOVDD0=3.3V, IOVDD1=3.3V)						
V_{IH}	high level input voltage		1.8			Vdd
V_{IL}	low level input voltage				0.8	Vdd
I_{IH}	high level input voltage	vdd=3.3v, vin=3.3v	0		0.5	uA
I_{IL}	low level input voltage	vdd=3.3v, vin=0v	-0.5		0	uA
Input (IOVDD0=1.8V or IOVDD1=1.8V)						
V_{IH}	high level input voltage		1.2			Vdd
V_{IL}	low level input voltage				0.8	Vdd
I_{IH}	high level input voltage	vdd=3.3v, vin=1.8v	0		0.5	uA
I_{IL}	low level input voltage	vdd=3.3v, vin=0v	-0.5		0	uA
Output (VDD=3.3V, IOVDD0=3.3V, IOVDD1=3.3V)						
I_{OL}	low level output current	vdd=3.3v, vout=0.6v		10		mA
I_{OH}	high level output current	vdd=3.3v, vout=2.7v		10		mA
Output (IOVDD0=1.8V, IOVDD1=1.8V)						
I_{OL}	low level output current	vdd=3.3v, vout=0.36v		3		mA
I_{OH}	high level output current	vdd=3.3v, vout=1.44v		3		mA
2.4GHz RF (VDD=2.4V-3.6V)						
f_{BAND}	Operation frequency range		2400		2483	MHz
f_{DATA}	Operation data rate			300	500	kbps
2.4GHz RF Receiver (VDD=2.4V-3.6V)						
f_{BW}	Channel filter bandwidth			1		MHz
f_{STOP1}	Adjacent channel rejection			15		dB
f_{STOP2}	Alternate channel rejection			30		dB
P_{-1dB}	-1dB compression			-27		dBm
S_{MIN}	Receiver sensitivity	@300kpbs, F_{dev}=250KHz		-85		dBm
2.4GHz RF Transmit (VDD=2.4V-3.6V)						
P_{OUT_MAX}	Maximum output power			2		dBm
P_{OUT_MIN}	Minimum output power	vdd=3.3v, vd18=1.8v		-8		dBm
2.4GHz RF Current						
I_{SYN}	Synthesizer current	vdd=3.3v, vd18=1.8v		8		mA
I_{TX}	RF TX current (0dBm output power)	vdd=3.3v, vd18=1.8v		32		mA
I_{RD}	RF RX current	vdd=3.3v, vd18=1.8v		24		mA
2.4GHz Frequency Synthesizer (VDD=2.4V-3.6V)						
T_{LOCK}	PLL lock time	@300kpbs		150		uS
Pn_{OUT_BAND}	Out of band phase noise	@1MHz offset		-100		dBC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Crystal Oscillator						
$f_{Crystal}$	Crystal range		4	12	32	MHz
f_{TRO}	Crystal tolerance			±10		ppm
T_{START}	Start-up time	@12MHz		300		uS
RC Oscillator						
f_{RC}	RC range		20	24	32	KHz
Temperature						
Ambient Operating Temperature (power applied)			-20		80	^{0}C
Storage Temperature			-65		150	^{0}C

7. Package Type

64pin/LQFP(7 x 7 x 1.4)



8. Key Matrix

	R0	R1	R2	R3	R4	R5	R6	R7
C0	Pause	Power	H4	Sleep	Ctrl-R	Wake up	Ctrl-L	F5
C1	Q	Tab	A	Esc	Z	N-CHG K131	‘~	1!
C2	W	Caps	S	K45	X	CHG K132	F1	2@
C3	E	F3	D	F4	C	ROMA K133	F2	3#
C4	R	T	F	G	V	B	5%	4$
C5	U	Y	J	H	M	N	6^	7&
C6	I	]}	K	F6	,<	K56	=+	8*
C7	O	F7	L	H1	.>	APP	F8	9(
C8	P	[{	;:	‘”	K42	/?	-_	0)
C9	Scroll	H2	**FN**	Alt-L	**ID Key**	Alt-R	H3	Print
C10	K14	Backspace	|	F11	Enter	F12	F9	F10
C11	7 Pad	4 Pad	1 Pad	Space	Num	↓	Del	Power
C12	8 Pad	5 Pad	2 Pad	0 Pad	/ Pad	→	Ins	Sleep
C13	9 Pad	6 Pad	3 Pad	. Pad	* Pad	- Pad	Page Up	Page Down
C14	+ Pad	K107	Enter Pad	↑	Play/Pause	←	Home	End
C15	Wake up	Shift-L	Shift-R	Volume-	Volume+	Next Track	Prev Track	Media
C16	Mail	Win-L	WWW Forward	WWW Stop	WWW Back	WWW Refresh	Mute	WWW Search
C17	KR-L	WWW Favorite	Win-R	My Computer	Stop	Calculator	Web/Home	KR-R

USB HID usage code：H1=0x01 0x01 0x03(Usage page = 0x0C Report ID = 0x01)

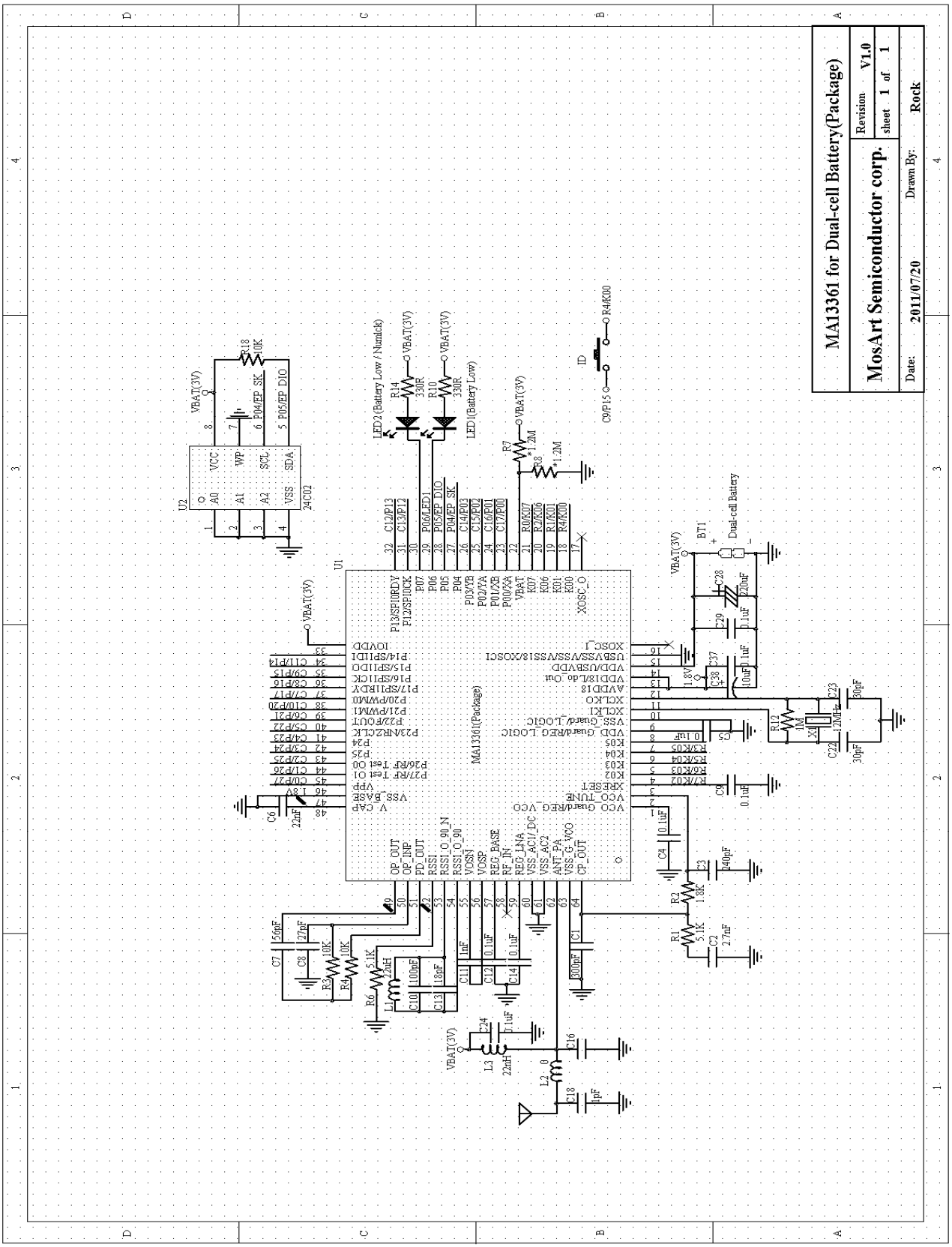
H2=0x01 0x02 0x03(Usage page = 0x0C Report ID = 0x01)

H3=0x01 0x03 0x03(Usage page = 0x0C Report ID = 0x01)

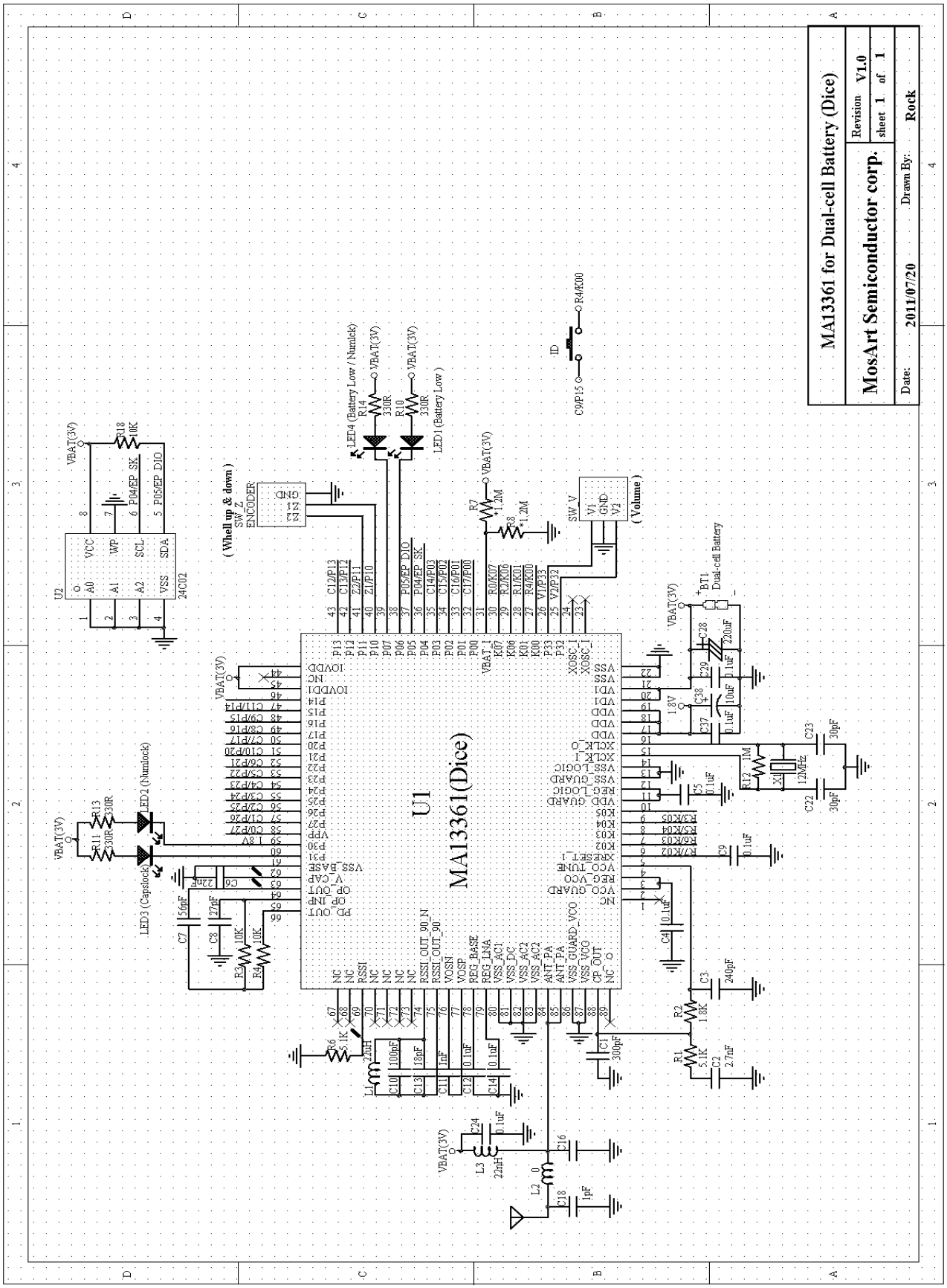
H4=0x01 0x04 0x03(Usage page = 0x0C Report ID = 0x01)

9. Application circuit

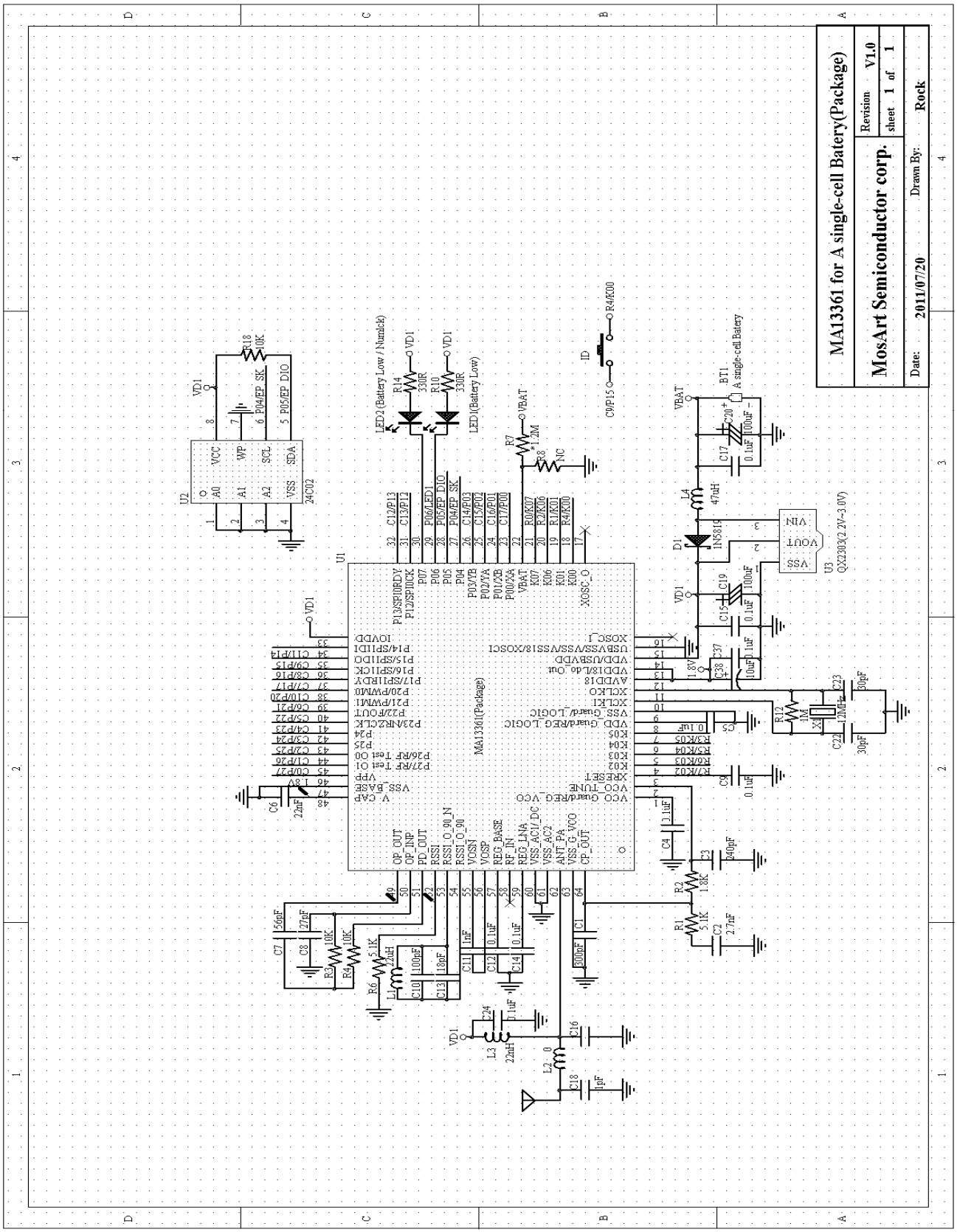
9.1 Dual cell Battery (Package)



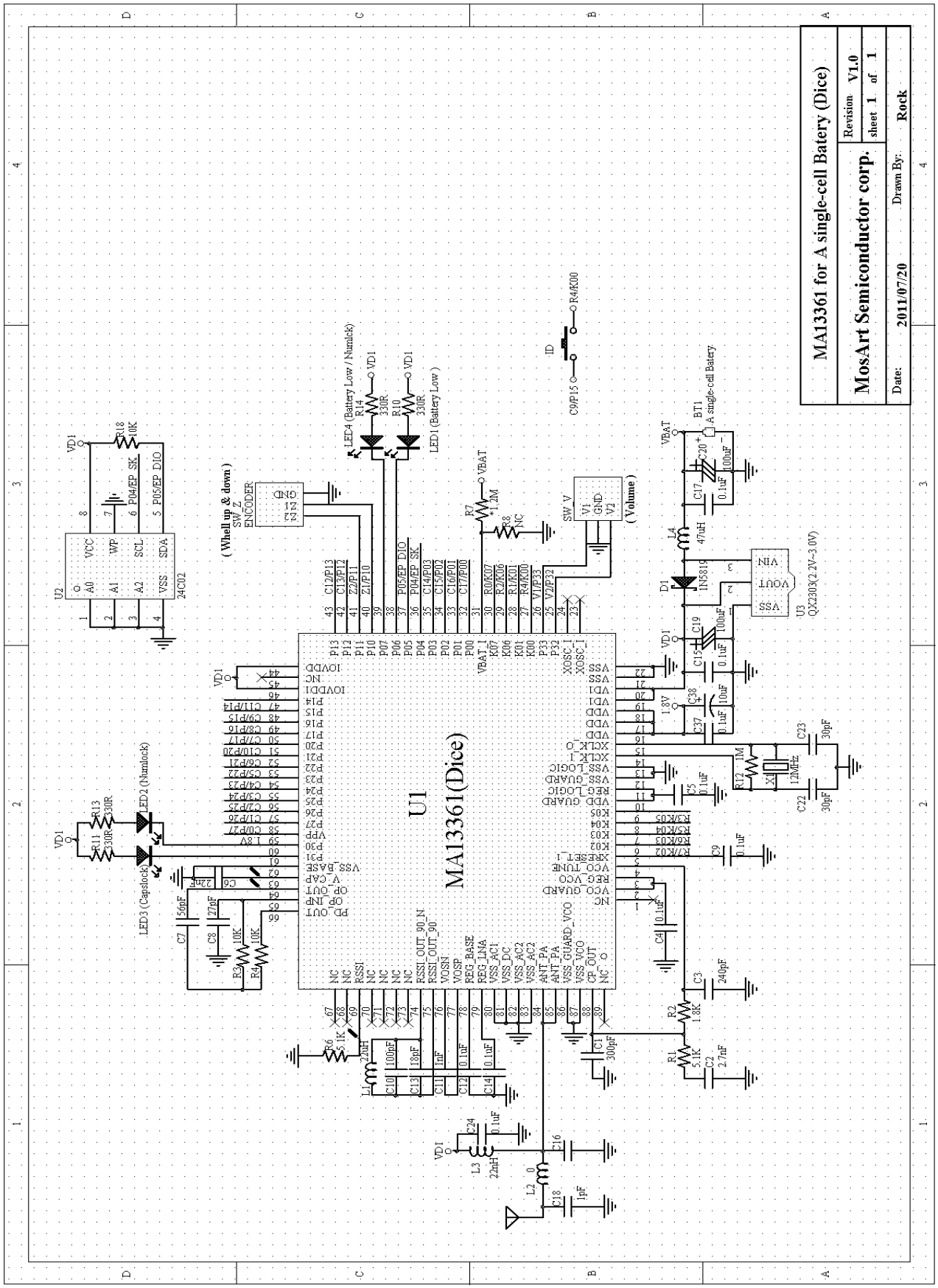
9.2 Dual-cell Battery (dice) :support Volume,Caps LED



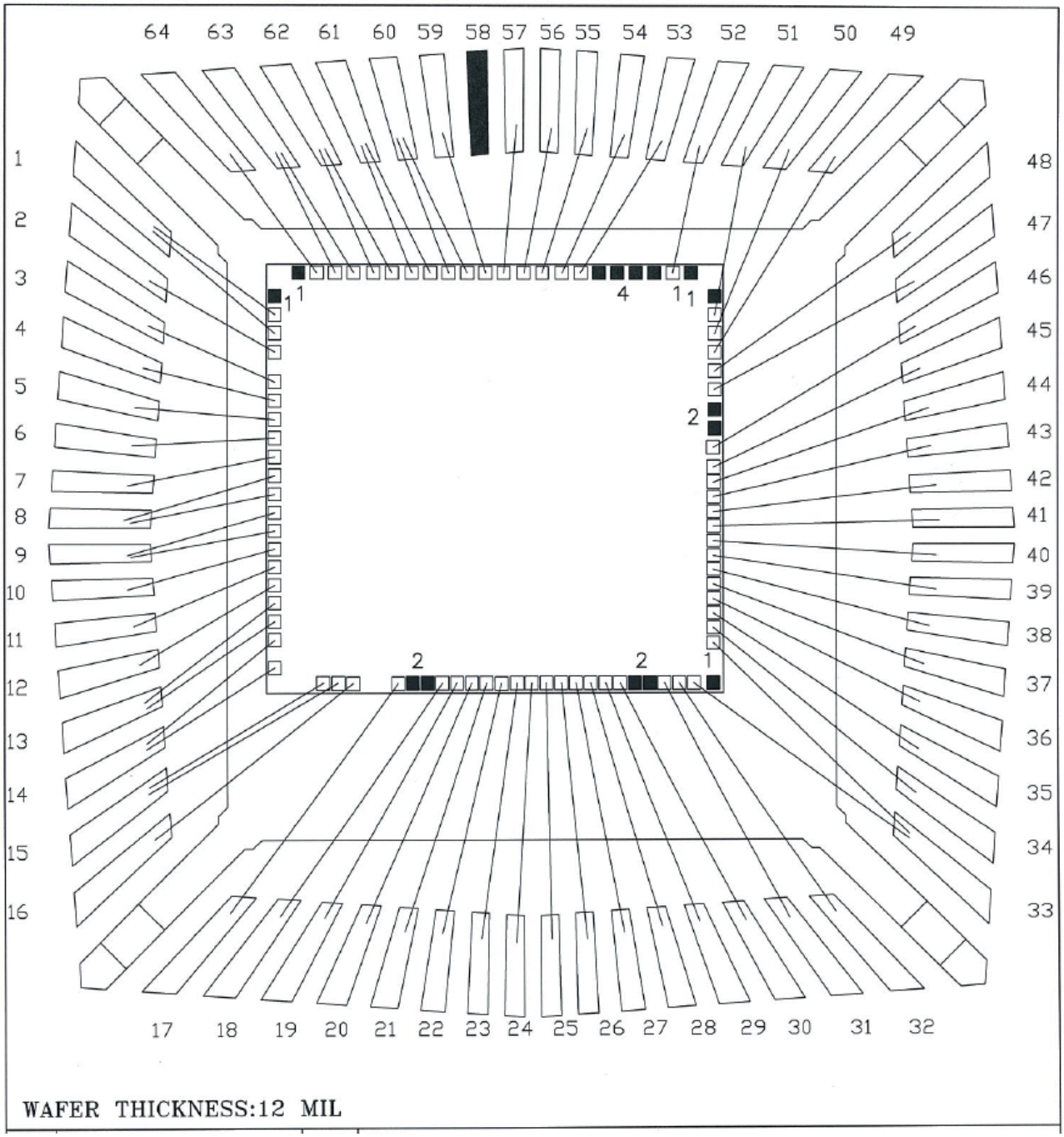
9.3 A singlel-cell Battery (Package)



9.4 A singlel-cell Battery (dice) :support Volume,Caps LED



10. Pad Diagram



Pad#	Pad Name	X 座標(um)	Y 座標(um)	Pin#	Pin Name
0	Lead-Frame PAD			NC	
1	DUMMY_PAD	173.730	46.000	NC	
2	VCO_GUARD	273.730	46.000	1	
3	REG_VCO	373.730	46.000	1	
4	VCO_TUNE	473.730	46.000	2	
5	XRESET_I	633.440	46.000	3	
6	K0_IO[2]	733.440	46.000	4	
7	K0_IO[3]	833.440	46.000	5	
8	K0_IO[4]	933.440	46.000	6	
9	K0_IO[5]	1033.440	46.000	7	
10	VDD_GUARD	1133.440	46.000	8	
11	REG_LOGIC	1233.440	46.000	8	
12	VSS_GUARD	1333.440	46.000	9	
13	VSS_LOGIC	1433.440	46.000	9	
14	XCLK_I	1533.440	46.000	10	
15	XCLK_O	1633.440	46.000	11	
16	VDD	1733.440	46.000	12	
17	VDD	1833.440	46.000	13	
18	VDD	1933.440	46.000	13	
19	VD1	2033.440	46.000	14	
20	VD1	2183.920	46.000	14	
21	VSS	2265.470	310.360	15	
22	VSS	2265.470	390.360	15	
23	XOSC_I	2267.660	471.595	16	
24	XOSC_O	2267.660	716.165	17	
25	P3_IO[2]	2265.500	795.475	NC	
26	P3_IO[3]	2265.500	875.475	NC	
27	K0_IO[0]	2265.500	955.475	18	
28	K0_IO[1]	2265.500	1035.475	19	
29	K0_IO[6]	2265.500	1115.475	20	
30	K0_IO[7]	2265.500	1195.475	21	
31	VBAT_I	2267.660	1276.165	22	
32	P0_IO[0]	2265.500	1360.475	23	
33	P0_IO[1]	2265.500	1440.475	24	
34	P0_IO[2]	2265.500	1520.475	25	
35	P0_IO[3]	2265.500	1600.475	26	
36	P0_IO[4]	2265.500	1680.475	27	
37	P0_IO[5]	2265.500	1760.475	28	

38	P0_IO[6]	2265.500	1840.475	29	
39	P0_IO[7]	2265.500	1920.475	30	
40	P1_IO[0]	2265.500	2000.475	NC	
41	P1_IO[1]	2265.500	2080.475	NC	
42	P1_IO[2]	2265.500	2160.475	31	
43	P1_IO[3]	2265.500	2240.475	32	
44	IOVDD0	2265.470	2319.930	33	
45	DUMMY_PAD	2265.470	2425.470	NC	
46	IOVDD1	2048.930	2425.470	33	
47	P1_IO[4]	1968.385	2425.500	34	
48	P1_IO[5]	1888.385	2425.500	35	
49	P1_IO[6]	1808.385	2425.500	36	
50	P1_IO[7]	1728.385	2425.500	37	
51	P2_IO[0]	1648.385	2425.500	38	
52	P2_IO[1]	1568.385	2425.500	39	
53	P2_IO[2]	1488.385	2425.500	40	
54	P2_IO[3]	1408.385	2425.500	41	
55	P2_IO[4]	1328.385	2425.500	42	
56	P2_IO[5]	1248.385	2425.500	43	
57	P2_IO[6]	1168.385	2425.500	44	
58	P2_IO[7]	1088.385	2425.500	45	
59	VPP	982.000	2425.470	46	
60	P3_IO[0]	880.000	2434.000	NC	
61	P3_IO[1]	780.000	2434.000	NC	
62	VSS_BASE	673.730	2434.000	47	
63	V_CAP	573.730	2434.000	48	
64	OP_OUT	473.730	2434.000	49	
65	OP_INP	373.730	2434.000	50	
66	PD_OUT	273.730	2434.000	51	
67	DUMMY_PAD	173.730	2434.000	NC	
68	DUMMY_PAD	46.000	2306.270	NC	
69	RSSI	46.000	2206.270	52	
70	FIL_LIM_N_PAD	46.000	2106.270	NC	
71	FIL_LIM_PAD	46.000	2006.270	NC	
72	IF_FIL_N_PAD	46.000	1906.270	NC	
73	IF_FIL_PAD	46.000	1806.270	NC	
74	RSSI_OUT_90_N	46.000	1706.270	53	
75	RSSI_OUT_90	46.000	1606.270	54	
76	VOSN	46.000	1498.135	55	

77	VOSP	46.000	1398.135	56	
78	REG_BASE	46.000	1290.000	57	
79	REG_LNA	46.000	1190.000	59	
80	VSS_AC1	46.000	1090.000	60	
81	VSS_DC	46.000	990.000	60	
82	VSS_AC2	46.000	890.000	61	
83	VSS_AC2	46.000	790.000	61	
84	ANT_PA	46.000	681.865	62	
85	ANT_PA	46.000	581.865	62	
86	VSS_GUARD_VCO	46.000	473.730	63	
87	VSS_VCO	46.000	373.730	63	
88	CP_OUT	46.000	273.730	64	
89	DUMMY_PAD	46.000	173.730		