# Circuits Description

### 1. Frequency Source

It is a twice-frequency-conversion superheterodyne receiver with the first intermediate frequency being 21.4 MHz, and the second intermediate frequency 450 KHz. The first reference frequency is provided by a phase-locked loop, and so is the transmitting frequency. The schematic circuit diagram is shown as Figure 1.

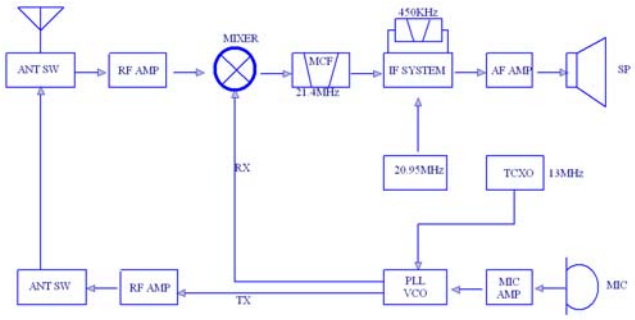



Figure 1 Schematic Circuit Diagram

### 2. Receiving System

It adopts the twice-frequency-conversion superheterodyne method to demodulate the signal.

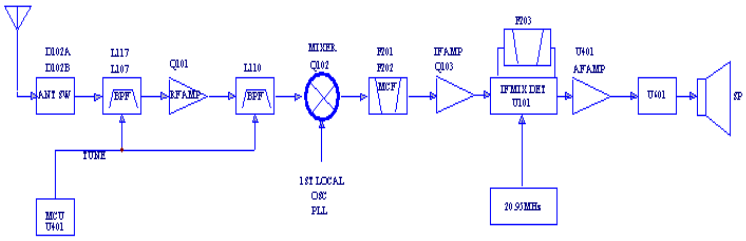



Figure 2 Circuit of Receiving System

### 2.1 Low-noise RF Amplifier

The signal, receiving from the antenna, going through the antenna switch and LC band-pass filter, will be amplified by the RF amplifier (Q101). After that, it will be filtered by another band-pass filter and sent to the first frequency mixer (Q102).

### 2.2 First Frequency Mixer

When the signal from the RF amplifier comes to the first frequency mixer (Q102), it will be mixed with the local oscillator signal from the PLL frequency synthesizer, generating the first IF signal (21.4MHz). The output IF signal will then be filtered by two monolithic crystal filter (F201, F202) to further eliminate the adjacent channel interference.

### 2.3 IF Amplifier

After amplified by Q103, the first IF signal arrives at the IF processing chip U101 where it will be mixed with another local oscillator signal. The second mixing brings the second IF signal which will go through a 450kHz ceramic filter (T101) to filter out unwanted spurious signals. The filtered IF signal will then be amplified and discriminated in U101.

### 2.4 Audio Amplifier

The demodulated signal from U101 will be subsequently amplified by U401, and filtered by the following low-pass and high-pass filters. After that, the signal will be amplified by the audio power amplifier (U601) that is controlled by the volume control circuit, and sent to drive the loudspeaker.

### 2.5 Noise Suppression Circuit

Part of the AF signal from the U101 enters the U101 again, and the noise component is amplified and rectified by a filter and an amplifier to produce a DC voltage corresponding to the noise level. The DC signal from the U101 goes to the analog port of the microprocessor (U401).In U401, the input voltage is compared with the threshold to decide whether or not to output sound through speaker. If the input voltage is higher than the threshold, a high level will be sent by U401, via Q603, to let U601 open. (See Figure 3)

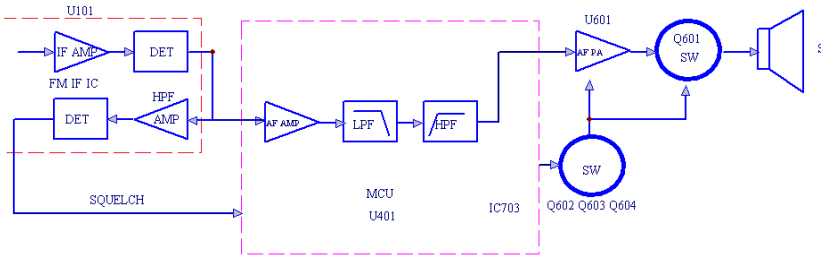



Figure 3 Circuits of Audio Amplifier and Noise Suppression

### 2.6 Receive signaling

The AF signal from the U101 etnter the U401. U401 determines whether the CTCSS or CDCSS matches the preset value, and control the speaker output sounds according to the squelch results.

## 3. PLL Frequency Synthesizer

Phase-locked loop (PLL) frequency synthesizer provides the first local oscillator signal for the receiving system, and the carrier signal for the transmitting system.

### 3.1 Circuit of Phase-locked Loop

The step frequency of PLL is 5KHz or 6.25KHz. The output signal of voltage-controlled oscillator (VCO) will go through Q303 acting as a buffer and amplifier, and then divided by a programmable dual-channel frequency counter in U301. The signal will then be compared in a phase comparator in U301 with the reference signal (5KHz or 6.25KHz) divided from a 13MHz reference signal. The comparator output will be filtered by a low-pass filter, and sent to VCO where it will be used to control the oscillation frequency. (See Figure 4)

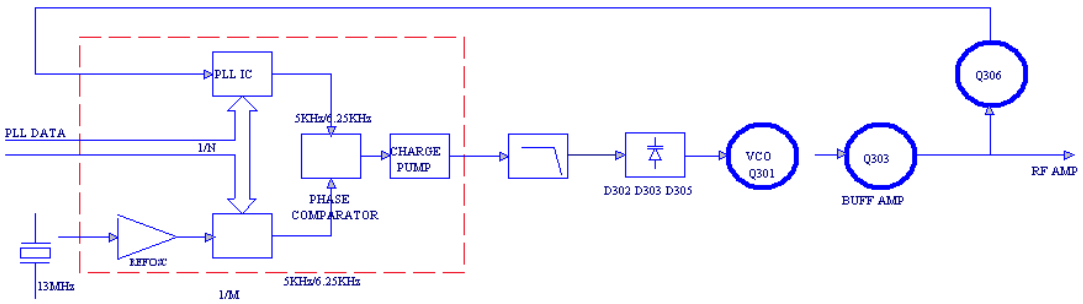



Figure 4 Circuit of Phase-locked Loop

### 3.2 VCO

First of all, an initial signal will be produced by the VCO (Q301), and sent to the phase comparator to generate a control voltage signal. The control voltage signal will be used to determine the capacitance of the varactor (D302 D303 D305) to ensure the oscillation frequency is synchronized with the preferring frequency value. The output of Q301 will be sent to Q303 for amplification and buffering.

## 4. Transmitting System

### 4.1 CTCSS / CDCSS Encoder

A necessary signal for CTCSS/CDCSS encoding is generated by U401 and FM-modulated to the PLL reference signal. Since the reference OSC does not modulate the loop characteristic frequency or higher, modulation is performed at the VCO side by adjusting the balance. (See Fig. 5)

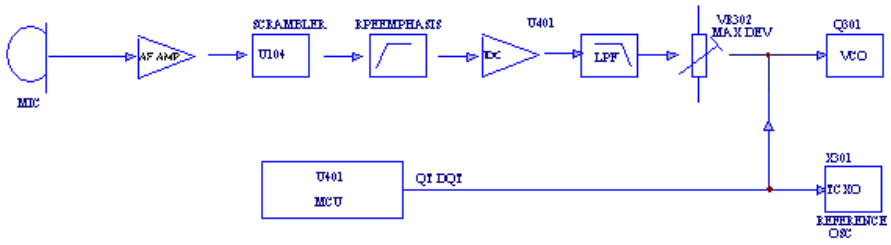



**Figure 5 Audio Processing、CDCSS、CTCSS**

### 4.2 RF Amplifier

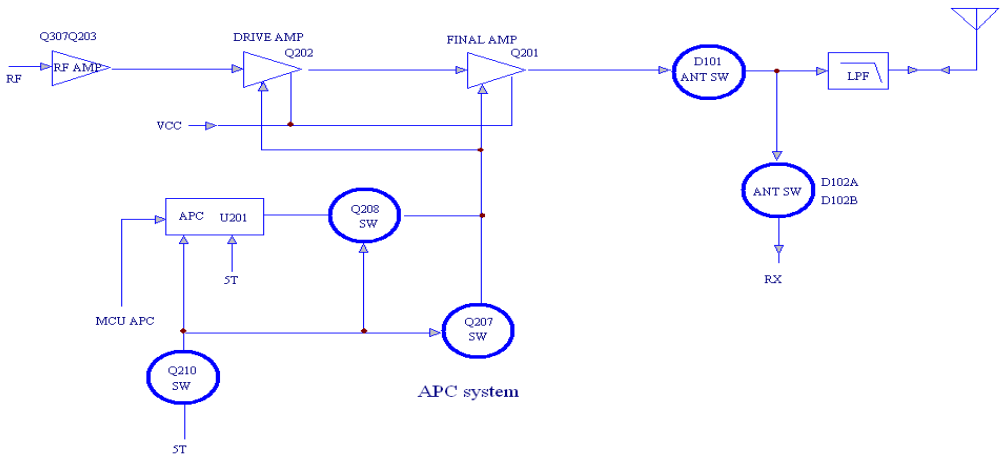
The signal from Q304 will firstly be amplified in Q307 and Q203, and then further amplified by two power amplifiers Q202 and Q201 to reach the preferring RF power of 4.0W.

### 4.3 Antenna Switch and LPF

There are a low-pass filter group and an antenna switch in front of the antenna. The antenna switch is a transmitting/receiving switch made up of D101, D102A and D102B. The switch will be open when transmitting and closed when receiving.

### 4.4 Automatic Power Control Circuit

The automatic power control (APC) circuit is used to maintain the stability of the current in Q201. Current changes in Q201 will cause voltage changes in R204, R205 and R206. The voltage of the signal from U201(1/2) will be compared in U201(2/2) with the reference voltage from U401. The VG of the RF power amplifier and other amplifiers will be adjusted according to the comparison result. Moreover, it is obvious that the power increase or decrease is achieved by changing the reference voltage. It is shown in Figure 6.



**5. Power Supply**

A battery is served as the power supply for the circuits, providing 5V voltage to the PLL circuit (VCO-V) and the receiving and transmitting system (RX, TX).

**6. Control System**

The control system known as U401 is operated in 32.768 kHz.

7. RF Specification

Frequency range: 136-174MHz

Rated power: 4W