WIRELESS

Error! No text of specified style in document.FW75 and C200

CDMA 1xRTT

Wireless Modules

System Integration Manual

locate, communicate, accelerate

Abstract

This document describes the features and the integration of u-blox LISA-C200 and FW75 CDMA2000 1xRTT wireless modules.

These modules are complete and cost efficient CDMA solutions offering 153 kb/s data speed dual-band 800/1900 MHz data transmission technology in compact form factors.

Document Information	
Title	**Error! No text of specified style in document.** FW75 and C200
Subtitle	CDMA 1xRTT Wireless Modules
Document type	System Integration Manual
Document number	CDMA-2X-11004-P1
Document status	Objective Specification

Document status information	
Objective Specification	This document contains target values. Revised and supplementary data will be published later.
Advance Information	This document contains data based on early testing. Revised and supplementary data will be published later.
Preliminary	This document contains data from product verification. Revised and supplementary data may be published later.
Released	This document contains the final product specification.

This document applies to the following products:

Name	Type number	Firmware version	PCN / IN
LISA-C200	LISA-C200-00S		n.a.
LISA-C200	LISA-C200-20S		n.a.
FW75-C200	FW-C200-00S		n.a.
FW75-C200	FW-C200-20S		n.a.

Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

AT Commands Manual: This document provides the description of the supported AT commands by the **Error! No text of specified style in document.** module to verify all implemented functionalities.

System Integration Manual: This Manual provides hardware design instructions and information on how to set up production and final product tests.

Application Note: document provides general design instructions and information that applies to all u-blox Wireless modules. See Section Related documents for a list of Application Notes related to your Wireless Module.

How to use this Manual

The **Error! No text of specified style in document.** System Integration Manual provides the necessary information to successfully design in and configure these u-blox wireless modules.

This manual has a modular structure. It is not necessary to read it from the beginning to the end.

The following symbols are used to highlight important information within the manual:

☞ An index finger points out key information pertaining to module integration and performance.

A warning symbol indicates actions that could negatively impact or damage the module.

Questions

If you have any questions about u-blox Wireless Integration, please:

- Read this manual carefully.
- Contact our information service on the homepage http://www.u-blox.com
- Read the questions and answers on our FAQ database on the homepage http://www.u-blox.com

Technical Support

Worldwide Web

Our website (www.u-blox.com) is a rich pool of information. Product information, technical documents and helpful FAQ can be accessed 24h a day.

By E-mail

Contact the nearest of the Technical Support offices by email. Use our service pool email addresses rather than any personal email address of our staff. This makes sure that your request is processed as soon as possible. You will find the contact details at the end of the document.

Helpful Information when Contacting Technical Support

When contacting Technical Support please have the following information ready:

- Module type (e.g. LISA-C200) and firmware version
- Module configuration
- Clear description of your question or the problem

- A short description of the application
- Your complete contact details

Contents

1 System description

1.1 Overview

u-blox C200 wireless modules integrate a complete CDMA 1xRTT 153 kb/s packet data modem into a single module solution. These modems are certified to operate on US CDMA carriers. In addition they can operate on carriers requiring SIM data card interface.

Comment [RC1]: We should review the description. Today its called “CSIM”

2 3G CDMA 2000 1xRTT Characteristics

2	3G CDMA 2000 1xRTT Characteristics
3	CDMA Terrestrial Radio Access Frequency Division Duplex (FDD) operating mode

2	3G CDMA 2000 1xRTT Characteristics
4	Dual-band support: • Band Class 0 – US Cellular • Band Class 1 – US PCS

2	3G CDMA 2000 1xRTT Characteristics
5	CDMA Packet Switched data up to 153 kb/s DL/UL

Table 1: 3G CDMA 2000 1xRTT characteristics

These modems are US CDMA certified to support 1xRTT data speeds on US CDMA carriers Sprint and Verizon.

It is strictly a data modem for embedded solutions. Data communication is through 2 data interfaces; 5 wires UART and Full Speed USB. The interfaces are intended to support a vast quantity of AT commands that will enable easy adoption to existing host application processors.

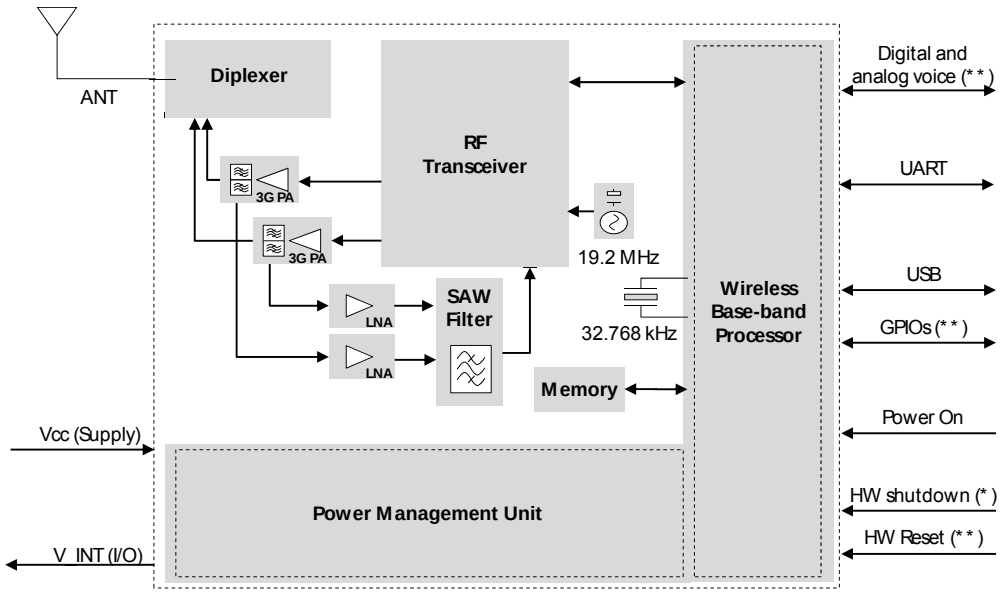
Power on is initiated by HW logic and Power down by HW logic and SW control.

LISA-C200 antenna interface is provided through a 50 ohm pad while FW75-C200 uses the popular "U.FL" RF connector.

Other key components are the extensive SW AT commands meeting the needs of :

- Carrier AT commands
- Industry standard AT command both 3GPP and 3GPP2
- u-blox AT Commands

5.1 Architecture



(*): FW75

(**): LISA-C200

Figure 1: Block diagram

5.1.1 Functional blocks

Error! No text of specified style in document. modules consist of the following internal functional blocks: RF front-end, RF transceiver, Baseband section and Power Management Unit.

RF Front-End

The Antenna connector is directly connected to the Diplexer which separates the 800 and 1900 MHZ bands. Each 800 & 1900 MHz RF chain are connected to their respective transceiver paths via duplexers as shown in prior block diagram.

Each duplexer provides the filtering and Rx/Tx path separation before connecting to the LNA and RF PA devices.

A separate shield compartment houses the 800 MHZ and 1900 MHZ RF power amplifiers. This compartment provides high Tx signal isolation, preventing de-sensing of the Rx frontend circuitry.

RF Transceiver

The transceiver includes the following key components:

- Dual-band 800 & 1900 MHz CDMA transceiver, excluding the RF Power Amplifiers, duplexers and diplexer.
- 19.2 MHz Crystal Oscillator

While operating, the RF transceiver performs direct up-conversion and down-conversion of the baseband I/Q signals, with the RF voltage controlled gain amplifier being used to set the uplink TX

power. In the downlink path, the internal LNA enhances the RX sensitivity. An internal automatic gain control amplifier optimizes the signal levels before delivering to the analog I/Q to baseband for further digital processing.

In all the modes, Tx & Rx RF synthesizers are an on-chip voltage controlled oscillator are used to generate the local oscillator signal.

The frequency reference to RF synthesizers are provided by an free running 19.2 MHz XO. The Rx path locks and tracks to the base station carrier. An learning algorithm is implemented to capture the temperature characteristic of the xtal, comparing the XO and carrier frequencies, while measuring the thermistor in close proximity to the crystal oscillator. A lookup table is saved over temperature and time. The known frequency difference of the free running crystal oscillator is corrected in the baseband processor enabling quick acquisition.

Baseband section and power management unit

Another shielding section includes all the digital circuitry and the power supplies, basically the following functional blocks:

- Wireless baseband processor, a mixed signal ASIC which integrates:
  - Microprocessor for controller functions, CDMA upper layer software
  - ARM9 coprocessor and HW accelerator for CDMA Layer 1 control software and routines
  - Dedicated HW for peripherals control, as UART, USB, etc
- Memory system in a Multi-Chip Package (MCP) integrating two devices:
  - NOR flash non-volatile memory
  - DDR SRAM volatile memory
- Power Management Unit (PMU), used to derive all the system supply voltages from the module supply VCC

5.2 Pin description

Table 2 provides a summary of the module pin names and descriptions.

☞ For the exact specification including pin numbering and additional information see the *LISA-C200 Data Sheet* [1] or the *FW75-C200 Data Sheet* [2].

Name	Module	Power domain	I/O	Description	Remarks
VCC	All	VCC	-	Battery Input	Module supply input
V_INT	FW75	-	O	Digital I/O Interfaces supply output	V_INT = 2.85V (typical) generated by the module when it is switched-on and the RESET_N (external reset input pin) is not forced to the low level.
	LISA-C200	-	O	Digital I/O Interfaces supply output	V_INT = 1.8V (typical) generated by the module when it is switched-on and the RESET_N (external reset input pin) is not forced to the low level.
PWR_ON	All	POS	I	Power-on input	PWR_ON pin has Internal pull-up resistor.
GPIO1..10	LISA-C200	GDI	I/O	GPIO	GPIO6..10 Reserved.
RESET_N	LISA-C200	ERS	I	External reset input	RESET_N pin has Internal pull-up resistor.
HW_SHUTDOWN	FW75	ERS	I	External Shutdown input	HW_SHUTDOWN pin has Internal pull-up resistor.
ANT	All	ANT	-	I/O	RF antenna

Name	Module	Power domain	I/O	Description	Remarks
STATUS	FW75-C200	GDI	O	LED Indicator	Indicated by buffered External LED : Off – Not Powered On – Powered, associated, and authenticated but not transmitting or receiving. Slow Blink but not associated or authenticated; searching. Intermittent Blink - Activity proportional to transmitting/receiving speed. For voice applications, turning off and on the intermittent blink based on the ring pulse cycle can indicate a ring event.
RI	All	GDI	O	UART ring indicator	Circuit 125 (RI) in ITU-T V.24. Value at internal reset: T/PU. Use to wake up host processor. The output signal is active low.
CTS	All	GDI	O	UART clear to send	Circuit 106 (CTS) in ITU-T V.24. Internal active pull-up to 1.8v . Internal passive pull-up to 2.85v
RTS	All	GDI	I	UART ready to send	Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to 1.8v . Internal passive pull-up to 2.85v
RXD	All	GDI	O	UART received data	Circuit 104 (RxD) in ITU-T V.24. Internal active pull-up to 1.8v . Internal passive pull-up to 2.85v
TXD	All	GDI	I	UART transmitted data	Circuit 103 (TxD) in ITU-T V.24. Internal active pull-up to 1.8v . Internal passive pull-up to 2.85v
VUSB_DET	All	USB	I	USB detect input	Input for VBUS (5 V typical) USB supply sense.
USB_D-	All	USB	I/O	USB Data Line D-	90 Ω nominal differential impedance Pull-up or pull-down resistors and external series resistors as required by the *USB 2.0 high-speed specification* [9] are part of the USB pad driver and need not be provided externally.
USB_D+	All	USB	I/O	USB Data Line D+	90 Ω nominal differential impedance Pull-up or pull-down resistors and external series resistors as required by the *USB 2.0 high-speed specification* [9] are part of the USB pad driver and need not be provided externally.
MIC_N	LISA-C200	AUDIO	I	Differential analog audio input (negative)	Differential analog microphone input Internal DC blocking 0.1uF capacitor.
MIC_P	LISA-C200	AUDIO	I	Differential analog audio input (positive)	Differential analog microphone input Internal DC blocking 0.1uF capacitor.
SPK_P	LISA-C200	AUDIO	O	Differential analog audio output (positive)	Differential analog audio output shared for all path modes: earpiece, headset and loudspeaker mode.
SPK_N	LISA-C200	AUDIO	O	Differential analog audio output (negative)	Differential analog audio output shared for all path modes: earpiece, headset and loudspeaker mode.
PCM_SYNC	LISA-C200	GDI	O	Digital Sync	Digital Audio Sync pulse.
PCM_DO	LISA-C200	GDI	O	Data Output	Digital Audio Output.
PCM_CLK	LISA-C200	GDI	O	Clock Output	Digital Audio Clock Output.
PCM_DI	LISA-C200	GDI	I	Data Input	Digital Audio Input.
SCL	LISA-C200	DDC	O	I^2C bus clock line	Fixed open drain. No internal pull-up. Value at internal reset: T.

Name	Module	Power domain	I/O	Description	Remarks
SDA	LISA-C200	DDC	I/O	I²C bus data line	Fixed open drain. No internal pull-up. Value at internal reset: T.
SIM_CLK	All	SIM	O	SIM/UIM clock	Value at internal reset: L.
SIM_IO	All	SIM	I/O	SIM/UIM data	Internal 4.7 kΩ pull-up resistor to VSIM. Value at internal reset: L/PD.
SIM_RST	All	SIM	O	SIM/UIM reset	Value at internal reset: L.
VSIM	ALL	-	O	SIM/UIM supply output	1.80 V typical or 2.90 V typical generated by the module according to the SIM card type.
SIM_GND	FW75-C200	SIM/UIM	O	UIM GROUND	
RSVD	All	RSVD	-	RESERVED pin	Unless otherwise specified, leave unconnected.
GND	All	GND	-	Ground	All GND pads must be connected to ground.

Table 2: Pin description summary

5.3 Power management

5.3.1 Power supply circuit overview

Error! No text of specified style in document. modules feature a power management concept optimized for the most efficient use of supplied power. This is achieved by hardware design utilizing a power efficient circuit topology (Figure 2), and by power management software controlling the module's power saving mode.

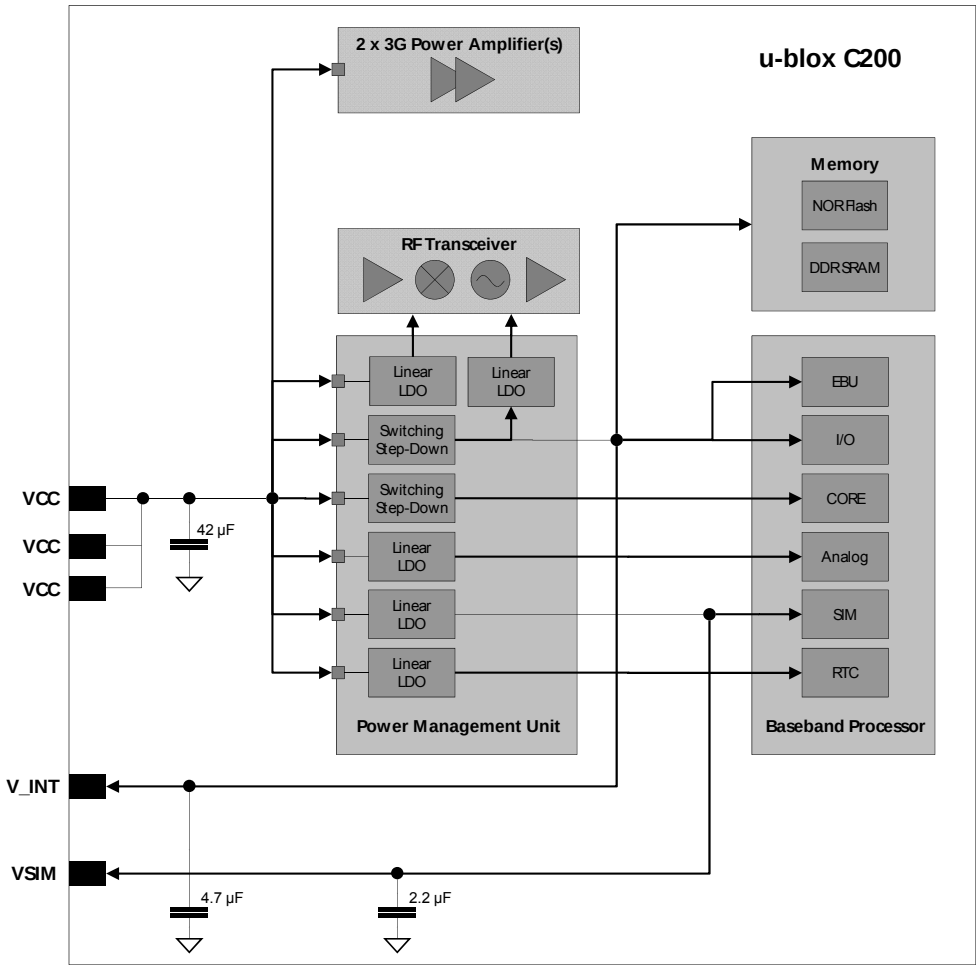


Figure 2: Power management simplified block diagram

Pins with supply function are reported in Table 3.

Error! No text of specified style in document. modules must be supplied via the **VCC** pins. There is only one main power supply input, available on the three[1] or five[2] **VCC** pins that must be all connected to the external power supply

The **VCC** pins are directly connected to the RF power amplifiers and to the integrated Power Management Unit (PMU) within the module: all supply voltages needed by the module are generated from the **VCC** supply by integrated voltage regulators.

When a 1.8 V or a 3 V SIM card type is connected, **Error! No text of specified style in document.** modules automatically supply the SIM card via the **VSIM** pin. Activation and deactivation of the SIM interface with automatic voltage switch from 1.8 to 3 V is implemented, in accordance to the ISO-IEC 7816-3 specifications.

The 2.8 voltage domain used internally also available on the **V_INT** pin, to allow more economical and efficient integration of the **Error! No text of specified style in document.** modules in the final application.

The integrated Power Management Unit also provides the control state machine for system start up and system shut down control.

5.3.2 Module supply (VCC)

Error! No text of specified style in document. modules must be supplied through the **VCC** pins by a DC power supply. Voltages must be stable: during operation, the current drawn from **VCC** can vary by some orders of magnitude.

Name	Description	Remarks
VCC	Module power supply input	**VCC** pins are internally connected, but all the available pads or pins must be connected to the external supply in order to minimize the power loss due to series resistance. Clean and stable supply is required: low ripple and low voltage drop must be guaranteed. Voltage provided must always be above the minimum limit of the operating range.
GND	Ground	**GND** pins are internally connected but a good (low impedance) external ground can improve RF performance: all available pads or pins must be connected to ground.

Table 3: Module supply pins

☞ Higher ESD protection level can be required if **VCC** is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin.

☞ The voltage provided to the **VCC** pins must be within the normal operating range limits as specified in the *LISA-C200 Data Sheet* [1] or *FW75-C200 Data Sheet* [2]. Complete functionality of the module is only guaranteed within the specified minimum and maximum **VCC** voltage operating range.

☞ Ensure that the input voltage at the **VCC** pins never drops below the minimum limit of the operating range when the module is switched on.

Operation above the operating range maximum limit is not recommended and extended exposure beyond it may affect device reliability.

[1] LISA-C200.
[2] FW75-C200.

Stress beyond the VCC absolute maximum ratings can cause permanent damage to the module: if necessary, voltage spikes beyond VCC absolute maximum ratings must be restricted to values within the specified limits by using appropriate protection.

☞ When designing the power supply for the application, pay specific attention to power losses and transients. The DC power supply must be able to provide a voltage profile to the **VCC** pins with the following characteristics:

- Voltage drop during transmission must be lower than 250 mV

☞ Any degradation in power supply performance (due to losses, noise or transients) will directly affect the RF performance of the module since the single external DC power source indirectly supplies all the digital and analog interfaces, and also directly supplies the RF power amplifier (PA).

5.3.2.1 VCC application circuits

Error! No text of specified style in document. modules must be supplied through the **VCC** pins by one (and only one) proper DC power supply that must be one of the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Li-Ion battery
- Primary (disposable) battery

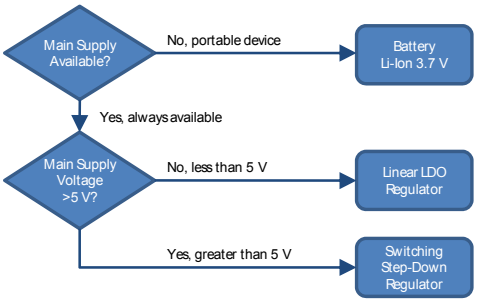


Figure 3: VCC supply concept selection

The switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the **Error! No text of specified style in document.** modules operating supply voltage. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less than 5 V). In this case the typical 90% efficiency of the switching regulator will diminish the benefit of voltage step-down and no true advantage will be gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they will dissipate a considerable amount of energy in thermal power.

If **Error! No text of specified style in document.** modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Lithium-Ion battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided.

The use of primary (not rechargeable) battery is uncommon, since the most cells available are seldom capable of delivering the peak current due to high internal resistance.

Keep in mind that the use of batteries requires the implementation of a suitable charger circuit (not included in **Error! No text of specified style in document.** modules). The charger circuit should be designed in order to prevent over-voltage on **VCC** beyond the upper limit of the absolute maximum rating.

The following sections highlight some design aspects for each of the supplies listed above.

Switching regulator

The characteristics of the switching regulator connected to **VCC** pins should meet the following requirements:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering greater than 1.2 Amps for safe design margin
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile
- **High switching frequency:** for best performance and for smaller applications select a switching frequency ≥ 600 kHz (since L-C output filter is typically smaller for high switching frequency). The use of a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be carefully evaluated since this can produce noise in the **VCC** voltage profile. An additional L-C low-pass filter between the switching regulator output to **VCC** supply pins can mitigate the ripple on **VCC**, but adds extra voltage drop due to resistive losses on series inductors
- **PWM mode operation**: select preferably regulators with Pulse Width Modulation (PWM) mode. While in active mode Pulse Frequency Modulation (PFM) mode and PFM/PWM mode transitions must be avoided to reduce the noise on the **VCC** voltage profile. Switching regulators able to switch between low ripple PWM mode and high efficiency burst or PFM mode can be used, provided the mode transition from idle mode (current consumption approximately 2 mA) to active mode (current consumption approximately 100 mA): it is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold (e.g. 60 mA)
- **Output voltage slope**: **(not necessary for CDMA solution, ok to delete-RJC)** the use of the soft start function provided by some voltage regulator must be carefully evaluated, since the voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 1 ms to allow a proper switch-on of the module

Figure 4 and the components listed in Table 4 show an example of a high reliability power supply circuit, where the module **VCC** is supplied by a step-down switching regulator capable of delivering 2.5 A current pulses with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz. The use of a switching regulator is suggested when the difference from the available supply rail to the **VCC** value is high: switching regulators provide good efficiency transforming a 12 V supply to the typical 3.8 V value of the **VCC** supply.

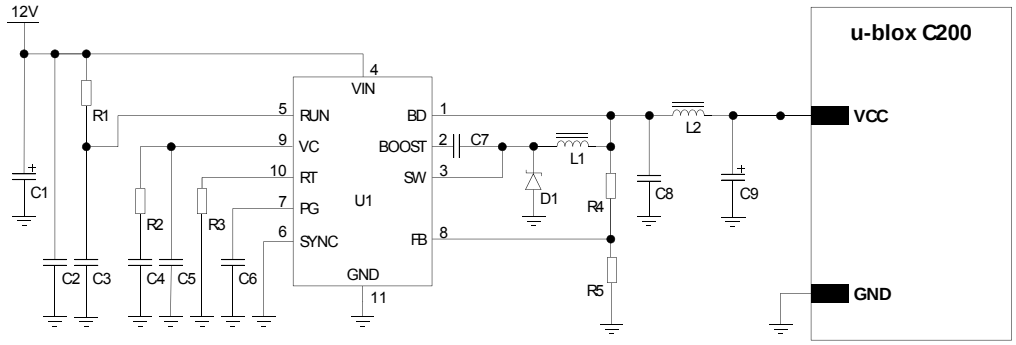


Figure 4: Suggested schematic design for the VCC voltage supply application circuit using a step-down regulator

6	Reference	7	Description	8	Part Number – Manufacturer

6	Reference	7	Description	8	Part Number – Manufacturer
9	C1	10	47 µF Capacitor Aluminum 0810 50 V	MAL215371479E3 – Vishay	
C2		10 µF Capacitor Ceramic X7R 5750 15% 50 V		C5750X7R1H106MB – TDK	
C3		10 nF Capacitor Ceramic X7R 0402 10% 16 V		GRM155R71C103KA01 – Murata	
C4		680 pF Capacitor Ceramic X7R 0402 10% 16 V		GRM155R71H681KA01 – Murata	
C5		22 pF Capacitor Ceramic COG 0402 5% 25 V		GRM1555C1H220JZ01 – Murata	
C6		10 nF Capacitor Ceramic X7R 0402 10% 16 V		GRM155R71C103KA01 – Murata	
C7		470 nF Capacitor Ceramic X7R 0603 10% 25 V		GRM188R71E474KA12 – Murata	
C8		22 µF Capacitor Ceramic X5R 1210 10% 25 V		GRM32ER61E226KE15 – Murata	
C37		330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ		T520D337M006ATE045 - KEMET	
D1		Schottky Diode 40 V 3 A		MBRA340T3G - ON Semiconductor	
L1		10 µH Inductor 744066100 30% 3.6 A		744066100 - Wurth Electronics	
L2		1 µH Inductor 7445601 20% 8.6 A		7445601 - Wurth Electronics	
R1		470 kΩ Resistor 0402 5% 0.1 W		2322-705-87474-L - Yageo	
R2		15 kΩ Resistor 0402 5% 0.1 W		2322-705-87153-L - Yageo	
R3		22 kΩ Resistor 0402 5% 0.1 W		2322-705-87223-L - Yageo	
R4		390 kΩ Resistor 0402 1% 0.063 W		RC0402FR-07390KL - Yageo	
R5		100 kΩ Resistor 0402 5% 0.1 W		2322-705-70104-L - Yageo	
U1		Step Down Regulator MSOP10 3.5 A 2.4 MHz		LT3972IMSE#PBF - Linear Technology	

Table 4: Suggested components for the VCC voltage supply application circuit using a step-down regulator

Low Drop-Out (LDO) linear regulator

The characteristics of the LDO linear regulator connected to the **VCC** pins should meet the following requirements:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a proper voltage value to the **VCC** pins and of delivering 1.2 A
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range (i.e. check the voltage drop from the max input voltage to the min output voltage to evaluate the power dissipation of the regulator)
- **Output voltage slope**: **(not necessary for CDMA solution, ok to delete-RJC)** the use of the soft start function provided by some voltage regulators must be carefully evaluated, since the voltage at the **VCC** pins must ramp from 2.5 V to 3.2 V within 1 ms to allow a proper switch-on of the module

Figure 5 and the components listed in Table 5 show an example of a power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering 1.2 Amps, with proper power handling capability. The use of a linear regulator is suggested when the difference from the available supply rail and the VCC value is low: linear regulators provide high efficiency when transforming a 5 V supply to the 3.6 V typical value of the VCC supply.

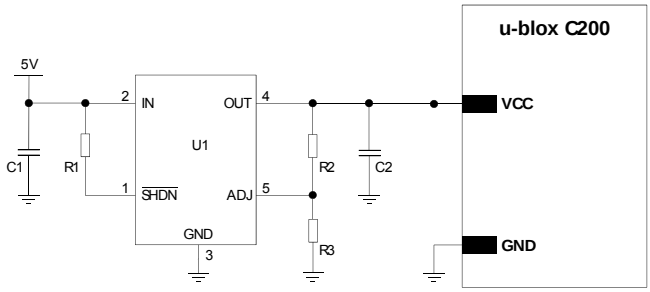


Figure 5: Suggested schematic design for the VCC voltage supply application circuit using an LDO linear regulator

11	Reference	12	Description	13	Part Number - Manufacturer

11	Reference	12	Description	13	Part Number - Manufacturer
14	C1	15	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	16	GRM188R60J106ME47 - Murata

11	Reference	12	Description	13	Part Number - Manufacturer
17	C2	18	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	19	GRM188R60J106ME47 - Murata

11	Reference	12	Description	13	Part Number - Manufacturer
20	R1	21	47 kΩ Resistor 0402 5% 0.1 W	22	RC0402JR-0747KL - Yageo Phycomp

11	Reference	12	Description	13	Part Number - Manufacturer
23	R2	24	4.7 kΩ Resistor 0402 5% 0.1 W	25	RC0402JR-074K7L - Yageo Phycomp

11	Reference	12	Description	13	Part Number - Manufacturer
26	R3	27	2.2 kΩ Resistor 0402 5% 0.1 W	28	RC0402JR-072K2L - Yageo Phycomp

11	Reference	12	Description	13	Part Number - Manufacturer
29	U1	30	LDO Linear Regulator ADJ 3.0 A	31	LT1764AEQ#PBF - Linear Technology

Table 5: Suggested components for VCC voltage supply application circuit using an LDO linear regulator

Rechargeable Li-Ion battery

Rechargeable Li-Ion batteries connected to the **VCC** pins should meet the following requirements:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its output circuit must be capable of delivering 1.2 A to the **VCC** pins and must be capable of delivering a DC current greater than the module maximum average current consumption to **VCC** pins. The maximum pulse discharge current and the maximum DC discharge current are not always reported in battery data sheets, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop greater than 250 mV during peak currents (Max Tx Power).

Primary (disposable) battery

The characteristics of a primary (non-rechargeable) battery connected to **VCC** pins should meet the following requirements:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its output circuit must be capable of delivering 1.2 A to the **VCC** pins and must be capable of delivering a DC current greater than the module maximum average current consumption at the **VCC** pins. The maximum pulse and the maximum DC discharge current is not always reported in battery data sheets, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop greater than 250 mV during peak currents (Max Tx Power).

Additional recommendations for the VCC supply application circuits

To reduce voltage drops, use a low impedance power source. The resistance of the power supply lines (connected to the **VCC** and **GND** pins of the module) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible in order to minimize power losses.

Three[3] or five[4] pins are allocated for **VCC** supply. Another seven pins are designated for **GND** connection. Even if all the **VCC** pins and all the **GND** pins are internally connected within the module, it is recommended to properly connect all of them to supply the module in order to minimize series resistance losses.

The placement cermic capacitors on the **VCC** line on the main board close to the connector will benefit operation.

To reduce voltage ripple and noise, place the following near the **VCC** pins:

- 100 nF capacitor (e.g Murata GRM155R61A104K) to filter digital logic noise from clocks and data sources
- 22 µF capacitor (e.g. Murata GRM31CR60J226K) to supply local DC energy.

[3] LISA-C200.
[4] FW75.

Figure 6 shows the complete configuration but the mounting of each single component depends on the application design.

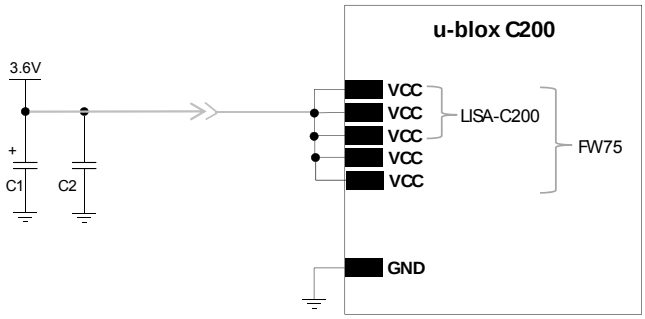


Figure 6: Suggested schematic design to reduce voltage ripple and noise and to avoid undershoot/ overshoot on voltage drops

32	Reference	33	Description	34	Part Number - Manufacturer

32	Reference	33	Description	34	Part Number - Manufacturer
35	C1	36	22 µF Capacitor Ceramic 6.3 V 45	37	GRM31CR60J226K - Murata

32	Reference	33	Description	34	Part Number - Manufacturer
38	C2	39	100 nF Capacitor Ceramic X7R 0402 10% 16 V	40	GRM155R61A104KA01 - Murata

Table 6: Suggested components to reduce voltage ripple and noise and to avoid undershoot/ overshoot on voltage drops

40.1.1 Current consumption profiles

During operation, the current drawn by the **Error! No text of specified style in document.** modules through the **VCC** pins can vary by several orders of magnitude. This ranges from continuous high current drawn in CDMA connected mode, to the low current consumption during in idle mode.

40.1.1.1 3G connected mode

During a CDMA connection, the module can transmit and receive continuously due to the Frequency Division Duplex (FDD) mode of operation with the Code Division Multiple Access (CDMA). The current consumption depends again on output RF power, which is always regulated by network commands. These power control commands are logically divided into a slot of 1.25 ms, thus the rate of power change can reach a maximum rate of 800 Hz. Since transmission and reception are continuously enabled due to FDD CDMA implemented in the 3G that differs from the TDMA implemented in the 2G case. In the worst scenario, corresponding to a continuous transmission and reception at maximum output power (approximately 250 mW or 24 dBm), the current drawn by the module at the VCC pins is in the order of continuous 600-700 mA. Even at lowest output RF power (approximately 0.01 µW or -50 dBm), the current is in the order of less than 100 mA due to module baseband processing and transceiver activity.

Comment [s2]: I guess it is CDMA, correct?

An example of current consumption profile of the data module in CDMA continuous transmission mode is shown in Figure 7.

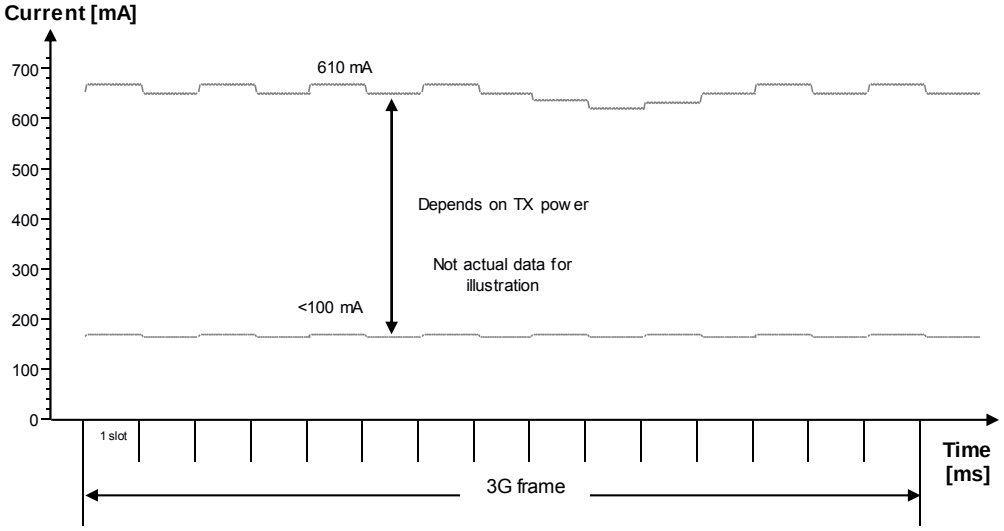


Figure 7: VCC current consumption profile versus time during a CDMA connection, with VCC=3.8 V

Comment [s3]: Is this graphic applicable to CDMA too?

When a packet data connection is established, the actual current profile depends on the amount of transmitted packets; there might be some periods of inactivity between allocated slots where current consumption drops about 100 mA. Alternatively, at higher data rates the transmitted power is likely to increase due to the higher quality signal required by the network to cope with enhanced data speed.

40.2 System functions

40.2.1 Module power on

The module power on sequence is initiated in one of these ways:

- Rising edge on the **VCC** pin to a valid voltage for module supply **AND** if the **PWR_ON** pin is permanently low when VCC is applied
- Falling edge on the **PWR_ON** pin (pin must be held low for >300 msec)

Name	Description	Remarks
PWR_ON	Power on input	**PWR_ON** pin has internal pull up resistor. Recommended to use open collector or drain configuration to pull down.

Table 7: Power on pin

☞ The **PWR_ON** pin ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin.

40.2.1.1 Rising edge on VCC

- \When a supply is connected to **VCC** pins, the module supply supervision circuit controls the subsequent activation of the power up state machines: the module is switched on when the voltage rises up to the **VCC** operating range minimum limit (3.4 V) starting from a voltage value lower than 2.25 V (See *LISA-C200 Data Sheet* [1] or the *FW75-C200 Data Sheet* [2]). Provided that the **PWR_ON** pin is is permanently low when VCC is applied.

40.2.1.2 Falling edge on PWR_ON

The module power on sequence starts when a falling edge is forced on the **PWR_ON** input pin. After applying a falling edge, it is suggested to hold a low level on the **PWR_ON** signal for at least 300 ms to properly switch on the module.

The electrical characteristics of the **PWR_ON** input pin are different from the other digital I/O interfaces: the high and the low logic levels have different operating ranges and the pin is **not-tolerant** to voltages up to the battery voltage. The detailed electrical characteristics are described in the *LISA-C200 Data Sheet* [1] or the *FW75-C200 Data Sheet* [2].

Once the module has been turned on, **PWR_ON** pin has no effect. On the other hand it makes no sense to keep this pin low once the module has been turned on: if the pin is kept low it will draw unnecessary current.

Following are some typical examples of application circuits to turn the module on using the **PWR_ON** input pin.

The simplest way to turn on the module is to use a push button that shorts the **PWR_ON** pin to ground.

If the **PWR_ON** input is connected to an external device (e.g. application processor), it is suggested to use an open drain output on the external device.

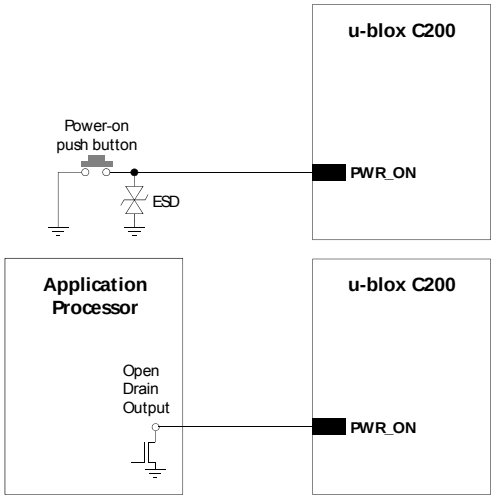


Figure 8: PWR_ON application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
ESD	CT0402S14AHSG - EPCOS	Varistor array for ESD protection

Table 8: Example of pull-up resistor and ESD protection for the PWR_ON application circuits

40.2.1.3 Additional considerations

The module is switched on when the voltage rises up to the **VCC** operating range: the first time that the module is used, it is switched on in this way. Then, the proper way to switch off the module is by means of the AT+CPWROFF command. When the module is in power-off mode, i.e. the AT+CPWROFF command has been sent and a voltage value within the operating range limits is still provided to the **VCC** pin, the digital input-output pads of the baseband chipset (i.e. all the digital pins of the module) are locked in tri-state (i.e. floating). The power down tri-state function isolates the module pins from its environment, when no proper operation of the outputs can be guaranteed.

The module can be switched on from power-off mode by forcing a proper start-up event (i.e. a falling edge on the **PWR_ON** pin). After the detection of a start-up event, all the digital pins of the module are held in tri-state until all the internal LDO voltage regulators are turned on in a defined power-on sequence. Then, as described in **Datasheet** the baseband core is still held in reset state for a time interval: the internal reset signal (which is not available on a module pin) is still low and any signal from the module digital interfaces is held in reset state. The reset state of all the digital pins is reported in the pin description table of the *LISA-C200 Data Sheet* [1] or the *FW75-C200 Data Sheet* [2]. When the internal signal is released, the configuration of the module interfaces starts: during this phase any digital pin is set in a proper sequence from the reset state to the default operational configuration. Finally, the module is fully ready to operate when all interfaces are configured.

☞ The Internal Reset signal is not available on a module pin.

40.2.2 Module power off

The correct way to switch off **Error! No text of specified style in document.** modules is by means of +CPWROFF AT command (more details in *u-blox C200 AT Commands Manual* [3]): in this way the current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed.

An under-voltage shutdown will be done if the **VCC** supply is removed, but in this case the current parameter settings are not saved in the module's non-volatile memory and a proper network detach cannot be performed.

40.2.3 Module reset

The module reset can be performed:

Forcing a low level on the **RESET_N** input pin, causing an "external" or "hardware" reset (LISA-C200 only)

AT+CFUN command (more details in *u-blox C200 AT Commands Manual* [3]): in this case an "internal" or "software" reset is performed, causing an asynchronous reset of the baseband processor

40.3 RF connection

The **ANT** connector has 50 Ω nominal characteristic impedance and must be connected to the antenna through a 50 Ω transmission line to allow transmission and reception of radio frequency (RF) signals in the Cell and PCS operating bands.

Name	Description	Remarks
ANT	RF connector	Zo = 50 Ω nominal characteristic impedance.
FW75		U.FL connector
LISA-C200		Surface Mount pad

Table 9: Antenna connector

☞ The **ANT** port ESD immunity rating is 500 V (according to IEC 61000-4-2). Higher protection level could be required if the line is externally accessible on the application board.

Choose an antenna with optimal radiating characteristics for the best electrical performance and overall module functionality. Focus on minimizing the insertion loss between radiating antenna and the module RF connector. Overall system performance depends on antenna reception and transmission. See section 74.2 for further details regarding antenna guidelines.

40.4Serial communication

Error! No text of specified style in document. modules provide the following serial communication interfaces where AT command interface and Packet-Switched Data communication are concurrently available:

- One asynchronous serial interface (UART) that provides RS-232 functionality conforming to *ITU-T V.24 Recommendation* [4], with limited data rate. One full-speed USB 2.0 compliant interface, with maximum data rate of 12 Mb/s.

Error! No text of specified style in document. modules are designed to operate as a CDMA wireless modem, which represents the data circuit-terminating equipment (DCE) as described by the *ITU-T V.24 Recommendation* [4]. A customer application processor connected to the module through one of the interfaces represents the data terminal equipment (DTE).

All the interfaces listed above are controlled and operated with:

- Sprint required AT Commands
- Verizon required AT Commands
- AT commands according to *3GPP TS 27.010* [7]
- AT commands according to *3GPP TS 27.005* [6]
- AT commands according to *3GPP TS 27.010*
- u-blox AT commands

☞ For the complete list of supported AT commands and their syntax refer to the *u-blox C200 AT Commands Manual* [3].

The USB interface, using all the lines provided (**VUSB_DET**, **USB_D+** and **USB_D-**), can be used for firmware upgrade:

☞ To directly enable PC (or similar) connection to the module for firmware upgrade, provide direct access on the application board to the **VUSB_DET**, **USB_D+** and **USB_D-** lines of the module . Also provide access to the **PWR_ON** & **HW_SHUTDOWN** pins, or enable the DC supply connected to the **VCC** pin to start the module firmware upgrade The following sub-chapters describe serial interface configuration and provide a detailed description of each interface for the application circuits.

40.4.1 Serial interfaces configuration

UART and USB serial interfaces are available as AT command interface and for Packet-Switched Data communication. The serial interfaces are configured as described in Table 10 (for information about further settings, please refer to the *u-blox C200 AT Commands Manual* [3]).

Note : The UART is 5 wire implementation therefore DTR, DSR, Data Carrier Detect and Data Terminal Ready functions are not available.

Interface	AT Settings	Comments
UART interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: • Channel 0: control channel • Channel 1: AT commands • Channel 2:/data connection •
	AT+IPR=115200	Baud rate: 115200 b/s
	AT+ICF=0,0	Frame format: 8 bits, no parity, 1 stop bit
	AT&K3	HW flow control enabled
USB interface	Enabled	•

Table 10: Default serial interfaces configuration

40.4.2 Asynchronous serial interface (UART)

The UART interface is a 5-wire unbalanced asynchronous serial interface that provides AT commands interface, PSD data communication, firmware upgrade.

UART interface provides RS-232 functionality conforming to the ITU-T V.24 Recommendation (more details available in *ITU Recommendation* [4]), with CMOS compatible signal levels: 0 V for low data bit or ON state, and 2.8 V for high data bit or OFF state. One external voltage translators (e.g. Maxim MAX13234E) could be used to provide RS-232 (5 lines) compatible signal levels. This chip translates the voltage levels from 1.8 V (module side) to the RS-232 standard. For detailed electrical characteristics refer to *LISA-C200 Data Sheet* [1] or the *FW75-C200 Data Sheet* [2].

Note : FW75-C200 logic levels are 2.8v interface. LISA-C200 logic levels are 1.8v interface.

The **Error! No text of specified style in document.** modules are designed to operate as a CDMA wireless modem, which represents the data circuit-terminating equipment (DCE) as described by the *ITU-T V.24 Recommendation* [4]. A customer application processor connected to the module through the UART interface represents the data terminal equipment (DTE).

☞ The signal names of the **Error! No text of specified style in document.** modules UART interface conform to the *ITU-T V.24 Recommendation* [4].

UART interfaces include the following lines:

Name	Description	Remarks
RI	Ring Indicator	Module output
RTS	Ready to send	Module hardware flow control input Circuit 105 (Request to send) in ITU-T V.24 FW75 - Internal active pull-up to **V_INT** (2.8 V) interface. LISA-C200- Internal active pull-up to **V_INT** (1.8 V) interface.

Name	Description	Remarks
CTS	Clear to send	Module hardware flow control output Circuit 106 (Ready for sending) in ITU-T V.24 FW75-C200 - Internal active pull-up to **V_INT** (2.8 V) interface. LISA-C200- Internal active pull-up to **V_INT** (1.8 V) interface.
TxD	Transmitted data	Module data input Circuit 103 (Transmitted data) in ITU-T V.24 Internal active pull-up to **V_INT** (2.8 V) enabled. FW75-C200- Internal active pull-up to **V_INT** (2.8 V) interface. LISA-C200- Internal active pull-up to **V_INT** (1.8 V) interface.
RxD	Received data	Module data output Circuit 104 (Received data) in ITU-T V.24 FW75-C200- Internal active pull-up to **V_INT** (2.8 V) interface. LISA-C200- Internal active pull-up to **V_INT** (1.8 V) interface.
GND	Ground	

Table 11: UART interface signals

The UART interface pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the lines connected to these pins.

UART application circuits

Providing the TxD, RxD, RTS and CTS lines only (not using the complete V.24 link)

Modem **DSR**, **DCD**, **RI** and **DTR** lines is not available in the application, the application circuit described in Figure 9 must be implemented:

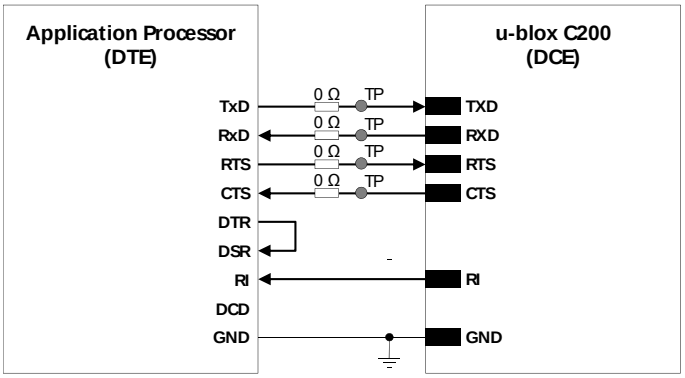


Figure 9: UART interface application circuit with partial V.24 link (5-wire) in the DTE/DCE serial communication

TxD, **RxD**, **RTS** and **CTS** lines are provided as described in Figure 9 the procedure to enable power saving depends on the HW flow-control status. If HW flow-control is enabled (AT&K3, that is the default setting) power saving will be activated by AT+UPSV=1. Through this configuration, when the module is in idle-mode, data transmitted by the DTE will be buffered by the DTE and will be correctly received by the module when active-mode is entered.

If the HW flow-control is disabled (AT&K0), the power saving can be enabled by AT+UPSV=2. The module is in idle-mode until a high-to-low (i.e. OFF-to-ON) transition on the **RTS** input line will switch the module from idle-mode to active-mode in 20 ms. The module will be forced in active-mode if the **RTS** input line is held in the ON state.

Additional considerations

☞ If the module USB interface is connected to the application processor, it is highly recommended to provide direct access to **RxD**, **TxD**, **CTS** and **RTS** lines of the module for execution of firmware upgrade over UART and for debug purpose: testpoints can be added on the lines to accommodate the access and a 0 Ω series resistor must be mounted on each line to detach the module pin from any other connected device. Otherwise, if the USB interface is not connected to the application processor, it is highly recommended to provide direct access to **VUSB_DET**, **USB_D+**, **USB_D-** lines for execution of firmware upgrade over USB and for debug purpose. In both cases, provide as well access to **RESET_N** pin, or to the **PWR_ON** pin, or enable the DC supply connected to the **VCC** pin to start the module firmware upgrade.

☞ If the UART interface is not used, all the UART interface pins can be left unconnected, but it is highly recommended to provide direct access to the **RxD**, **TxD**, **CTS** and **RTS** lines for execution of firmware upgrade and for debug purpose.

40.4.3 USB interface

Error! No text of specified style in document. modules provide a full-speed USB interface at 12 Mb/s compliant with the *Universal Serial Bus Revision 2.0 specification* [9]. It acts as a USB device and can be connected to any USB host such as a PC or other Application Processor.

The USB-device shall look for all upper-SW-layers like any other serial device. This means that **Error! No text of specified style in document.** modules emulate all serial control logical lines.

☞ If the logical DTR line isn't enabled by the USB host, the module doesn't answer to AT commands by the USB interface.

Name	Description	Remarks
VUSB_DET	USB detect input	Apply 5 V typical to enable USB
USB_D+	USB Data Line D+	90 Ω nominal differential impedance. Pull-up or pull-down resistors and external series resistors as required by the *USB 2.0 high-speed specification* [9] are part of the USB pad driver and need not be provided externally.
USB_D-	USB Data Line D-	90 Ω nominal differential impedance. Pull-up or pull-down resistors and external series resistors as required by the *USB 2.0 high-speed specification* [9] are part of the USB pad driver and need not be provided externally.

Table 12: USB pins

☞ The USB interface pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting a very low capacitance (i.e. less or equal to 1 pF) ESD protection (e.g. Tyco Electronics PESD0402-140 ESD protection device) on the lines connected to these pins.

Error! No text of specified style in document. module identifies itself by its VID (Vendor ID) and PID (Product ID) combination, included in the USB device descriptor. VID and PID of **Error! No text of specified style in document.** modules are the following:

VID = 0x1546 PID = 0x1121

40.4.3.1 USB application circuit

Since the module acts as a USB device, the USB supply (5.0 V typ.) must be provided to **VUSB_DET** by the connected USB host. The USB interface is enabled only when a valid voltage as USB supply is detected by the **VUSB_DET** input. Neither the USB interface, nor the whole module is supplied by the **VUSB_DET** input: the **VUSB_DET** senses the USB supply voltage and absorbs few microamperes.

The **USB_D+** and **USB_D-** lines carry the USB serial data and signaling. The lines are used in single ended mode for relatively low speed signaling handshake, as well as in differential mode for fast signaling and data transfer.

USB pull-up or pull-down resistors on pins **USB_D+** and **USB_D-** as required by the *Universal Serial Bus Revision 2.0 specification* [9] are part of the USB pad driver and do not need to be externally provided.

External series resistors on pins **USB_D+** and **USB_D-** as required by the *Universal Serial Bus Revision 2.0 specification* [9] are also integrated: characteristic impedance of **USB_D+** and **USB_D-** lines is specified by the USB standard. The most important parameter is the differential characteristic impedance applicable for odd-mode electromagnetic field, which should be as close as possible

to 90 Ω differential: signal integrity may be degraded if the PCB layout is not optimal, especially when the USB signaling lines are very long.

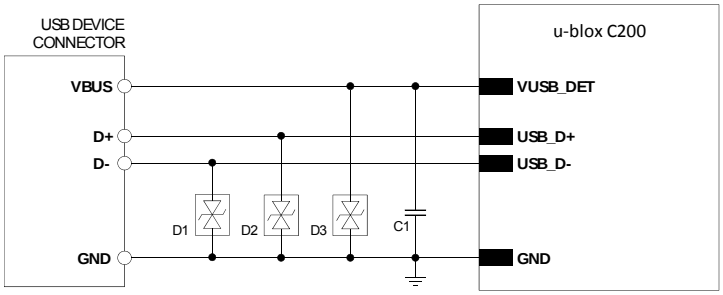


Figure 10: USB Interface application circuit

41	Reference	42	Description	43	Part Number - Manufacturer

41	Reference	42	Description	43	Part Number - Manufacturer
44	D1, D2, D3	45	Very Low Capacitance ESD Protection	46	PESD0402-140 - Tyco Electronics

41	Reference	42	Description	43	Part Number - Manufacturer
47	C2	48	100 nF Capacitor Ceramic X7R 0402 10% 16 V	49	GRM155R61A104KA01 - Murata

Table 13: Component for USB application circuit

☞ If the USB interface is not connected to the application processor, it is highly recommended to provide direct access to the **VUSB_DET**, **USB_D+**, **USB_D-** lines for execution of firmware upgrade over USB and for debug purpose: testpoints can be added on the lines to accommodate the access. Otherwise, if the USB interface is connected to the application processor, it is highly recommended to provide direct access to the **RxD**, **TxD**, **CTS** and **RTS** lines for execution of firmware upgrade over UART and for debug purpose. In both cases, provide as well access to **RESET_N** pin, or to the **PWR_ON** pin, or enable the DC supply connected to the **VCC** pin to start the module firmware upgrade

☞ If the USB interface is not used, the **USB_D+**, **USB_D-** and **VUSB_DET** pins can be left unconnected, but it is highly recommended to provide direct access to the lines for execution of firmware upgrade and for debug purpose.

49.1.1 MUX Protocol (3GPP 27.010)

Comment [rjc4]: Again SW lead needs to state compliance to feature list.. Stefano may be able to provide comments

Error! No text of specified style in document. modules have a software layer with MUX functionality, *3GPP TS 27.010 Multiplexer Protocol* [7], available on the UART physical link. The USB interface doesn't support the multiplexer protocol.

This is a data link protocol (layer 2 of OSI model) which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows a number of simultaneous sessions over theUART: the user can concurrently use AT command interface on one MUX channel and Packet-Switched Data communication on another MUX channel.. Each session consists of a stream of bytes transferring various kinds of data such as SMS, PSD, AT commands in general. This permits, for example, SMS to be transferred to the DTE when a data connection is in progress.

The following virtual channels are defined:

- Channel 0: control channel
- Channel 1;AT commands
- Channel 2: data connection

49.2 Reserved pins (RSVD)

Error! No text of specified style in document. modules have pins reserved for future use. All the **RSVD** pins/pads must be left unconnected on the application board.

49.3 Schematic for LISA-C200 and FW75-C200 modules integration

Comment [tgri5]: Do we need a separate schematic for LISA?

Figure 11 shows the integration an LISA-C200 / FW75-C200 modules into an application board, using all the module interfaces.

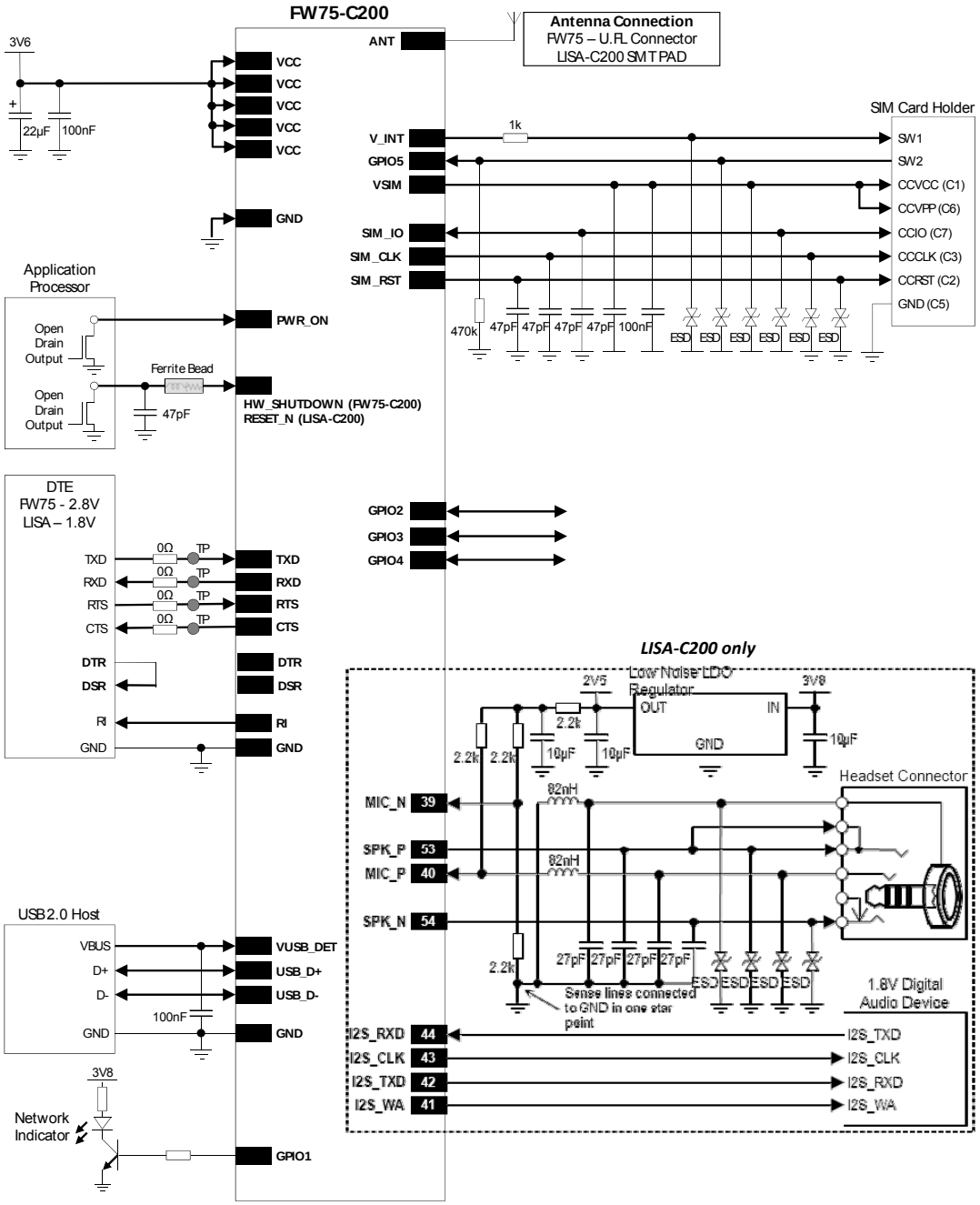


Figure 11: Example of schematic diagram to integrate FW75-C200/LISA-C200 module in an application board, using all the interfaces

☞ UART FW75-C200 and LISA-C200 pins use different voltage levels (1.8V LISA-C200, 2.8V FW75-C200)

49.4 Approvals

Error! No text of specified style in document. modules have been or will be approved under the following schemes:

- CDG1 CDMA Development Group 1 Radio Conformance Testing
- CDG2 CDMA Development Group 2 Inter-operability
- Sprint Carrier Certification
- Verizon Carrier Certification
- FCC Federal Communications Commission
- IC Industry Canada

49.4.1.1 Statement to be included in users guide - United States only

Radiofrequency radiation exposure Information: this equipment complies with FCC radiation exposure limits prescribed for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and your body.

49.4.1.2 Statement to be included in users guide – Canada only

The antenna used for the transmitter must be installed to provide a separation distance of at least 7.87 inches (20 cm) from all persons.

L'antenne de l'émetteur doit être installé à une distance d'au moins 7,87 pouces (20 cm) de toutes les personnes.

49.4.1.3 Modifications

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

Manufacturers of mobile or fixed devices incorporating the Error! No text of specified style in document. **modules are authorized to use the FCC Grants and Industry Canada Certificates of the** Error! No text of specified style in document. **modules for their own final products according to the conditions referenced in the certificates.**

The FCC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating for FW75: "Contains FCC Id XU9-FW75"

And for LISA C200 "Contains FCC Id XU9-LISAC200"

The IC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating for FW75: "Contains IC 8694A-FW75"

And for LISA C200 "Contains IC 8694A-LISAC200"

Canada, Industry Canada (IC) Notices

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
Canada, avis d'Industrie Canada (IC)

Les changements ou modifications n'ont pas était expressément approuvés par la partie responsable de la conformité, ils pourraient annulée l'autorité de l'utilisateur pour exploiter l'équipement.

50 Design-In

50.1 Design-in checklist

50.1.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at **VCC** pin above the minimum operating range limit.
- ☑ DC supply must be capable of supporting 1.2 A, providing a voltage at **VCC** pin above the minimum operating range limit and with a maximum 250 mV voltage drop from the nominal value.
- ☑ **VCC** supply should be clean, with very low ripple/noise: suggested passive filtering parts can be inserted.
- ☑ Connect only one DC supply to **VCC**: different DC supply systems are mutually exclusive.
- ☑ Don't apply loads which might exceed the limit for maximum available current from **V_INT** supply.
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested low capacitance ESD protection and passive filtering parts on each SIM signal.
- ☑ Check UART signals direction, since the signal names follow the *ITU-T V.24 Recommendation* [4].
- ☑ Provide appropriate access to USB interface and/or to UART **RxD**, **TxD** lines and access to **PWR_ON** and/or **HW_SHUTDOWN** lines on the application board in order to flash/upgrade the module firmware.
- ☑ Provide appropriate access to USB interface and/or to UART **RxD**, **TxD**, **CTS**, **RTS** lines for debugging.
- ☑ Add a proper pull-up resistor to a proper supply on each DDC (I^2C) interface line, if the interface is used.
- ☑ Capacitance and series resistance must be limited on each line of the DDC interface.
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ Insert the suggested passive filtering parts on each used analog audio line.
- ☑ Provide proper precautions for ESD immunity as required on the application board.
- ☑ All unused pins can be left floating on the application board Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to **ANT** coax connector or Printed Circuit Board 50 transmission line impedance for LISA-C200
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment.
- ☑ Ensure no coupling occurs with other noisy or sensitive signals (primarily SIM signals).
- ☑ **VCC** line should be wide and short.
- ☑ Ensure proper grounding.

☑ Consider “No-routing” areas for the Data Module footprint.
☑ Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.
☑ Design **USB_D+ / USB_D-** connection as 90 Ω differential pair.

50.1.2 Antenna checklist

☑ Antenna should have 50 Ω impedance, V.S.W.R less than 3:1, recommended 2:1 on operating bands in deployment geographical area.

☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).

50.2 Connectors (FW75)

The following design information is to aid the design for proper selection of mating connectors and antennas.

50.2.1 FW75-C200 modem connector

Manufacturer	Series Name	Part No.	Specification	Description	Remarks
Molex	SlimStack	52991-0808	PS-54-167-002	Receptacle 80 pins, 0.50mm pitch, 4mm stacking height	Website : www.molex.com • Drawing: 529910708_sd.pdf (mechanical, land pattern and reel specifications) • Data sheet : 05339160208_PCB_RECEPTABLES.pdf

Table 14: FW75-C200 modem connector

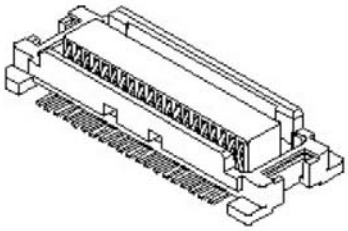


Figure 12: FW75-C200 modem connector

50.2.2 FW75-C200 Board to Board host connector

51	Manufacturer	52	Series Name	53	Part No.	54	Specification	55	Description	56	Remarks

51	Manufacturer	52	Series Name	53	Part No.	54	Specification	55	Description	56	Remarks
57	Molex	58	SlimStack	59	53916-0808	60	PS-54-167-002	61	Header 80 pins, 0.50mm pitch, 4mm stacking height	62	Website : www.molex.com • Drawing: 539160208_sd.pdf (mechanical, land pattern and reel specifications) • Data sheet : 05339160208_PCB_HEADERS.pdf

Table 15: FW75-C200 host mate connector

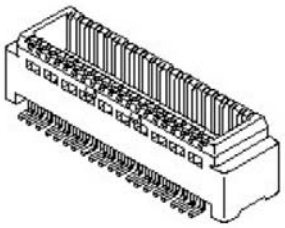


Figure 13: FW75-C200 host mate connector

62.1.1 FW75-C200 RF antenna connector

63	Manufacturer	64	Series No.	65	Part No.	66	Specification	67	Description	68	Remarks

63	Manufacturer	64	Series No.	65	Part No.	66	Specification	67	Description	68	Remarks
69	Molex	70	73412	71	73412-0110	72	PS-73598-02	73	Microcoaxial RF, 50 Ω, PCB Vertical Jack Receptacle, SMT, 1.25mm (.049"") Mounted Height	74	Website : www.molex.com • Drawing: 734120110_sd.pdf (mechanical, land pattern and reel specifications) • Data sheet: 0734120110_RF_COAX_CONNECTORS .pdf

Table 16: FW75-C200 antenna connector

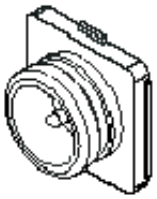


Figure 14: FW75-C200 antenna connector

74.1 Design Guidelines

The following design guidelines must be met for optimal integration of LISA-C200 module on the final application board.

74.1.1 Layout guidelines per pin function

This section groups u-blox C200 module pins by signal function and provides a ranking of importance in layout design. See Table 17 for a list of pins ranked by their importance in layout design. See *LISA-C200 Data Sheet* [1] or the *FW75 Data Sheet* [2] for the complete pin lists.

Rank	Function	Pin(s)	Layout	Remarks
1st	**RF Connector**	**ANT**		Design for 50 Ω characteristic impedance.
74.1.1.1.1.1.2 2nd	74.1.1.1.1.1.3 **Main DC Supply**	74.1.1.1.1.1.4 **VCC**		**VCC** line should be wide and short. Route away from sensitive analog signals.
74.1.1.1.1.1.4.2 3rd	74.1.1.1.1.1.4.3 **USB Signals**	74.1.1.1.1.1.4.4 **USB_D+** **USB_D-**		Route USB_D+ and USB_D- as differential lines: design for 90 Ω differential impedance.
4th	**Ground**	**GND**	**Careful Layout**	Provide proper grounding.
5th	**Sensitive Pin :**		**Careful Layout**	Avoid coupling with noisy signals.
	Power On HW_SHUTDOWN	**PWR_ON** **HW_SHUTDOWN**		
6th	**Digital pins and supplies:**		Common Practice	Follow common practice rules for digital pin routing.
	SIM Card Interface	VSIM, SIM_CLK, SIM_IO, SIM_RST		
	UART	TXD, RXD, CTS, RTS, RI		
	External Reset	HW_SHUTDOWN		
	General Purpose I/O	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5		
	USB detection	VUSB_DET		
	Supply for Interfaces	V_INT		

Table 17: Pin list in order of decreasing importance for layout design

74.2 Antenna guidelines

Antenna characteristics are essential for good functionality of the module. Antenna radiating performance has direct impact on the reliability of connections over the Air Interface. A bad termination of **ANT** can result in poor performance of the module.

The following parameters should be checked:

Item	Recommendations
Impedance	50 Ω nominal characteristic impedance
Frequency Range	Depends on the **Error! No text of specified style in document.** module HW version and on the Mobile Network used. LISA-C200: - Cell Band B0: 824..894 MHz - PCS Band B1 B2: 1850..1990 MHz
Input Power	>2 W peak
V.S.W.R	<2:1 recommended, <3:1 acceptable
Return Loss	S_{11}<-10 dB recommended, S_{11}<-6 dB acceptable
Gain	<3 dBi

Table 18: General recommendation for CDMA antenna

To preserve the original u-blox FCC ID, antenna gain shall remain below Cell Band 2 dBi, PCS Band 3 dBi

CDMA antennas are typically available as:

- Linear monopole: typical for fixed applications. The antenna extends mostly as a linear element with a dimension comparable to lambda/4 of the lowest frequency of the operating band. Magnetic base may be available. Cable or direct RF connectors are common options. The integration normally requires the fulfillment of some minimum guidelines suggested by antenna manufacturer
- Patch-like antenna: better suited for integration in compact designs (e.g. mobile phone). These are mostly custom designs where the exact definition of the PCB and product mechanical design is fundamental for tuning of antenna characteristics

For integration observe these recommendations:

- Ensure 50 Ω antenna termination by minimizing the V.S.W.R. or return loss, as this will optimize the electrical performance of the module. See section 74.2.1
- Select antenna with best radiating performance. See section 74.2.2
- If a cable is used to connect the antenna radiating element to application board, select a short cable with minimum insertion loss. The higher the additional insertion loss due to low quality or long cable, the lower the connectivity
- Follow the recommendations of the antenna manufacturer for correct installation and deployment
- Do not include antenna within closed metal case
- Do not place antenna in close vicinity to end user since the emitted radiation in human tissue is limited by S.A.R. regulatory requirements
- Do not use directivity antenna since the electromagnetic field radiation intensity is limited in some countries
- Take care of interaction between co-located RF systems since the RF transmitted power may interact or disturb the performance of companion systems

- Place antenna far from sensitive analog systems or employ countermeasures to reduce electromagnetic compatibility issues that may arise

74.2.1 Antenna termination

The **Error! No text of specified style in document.** modules are designed to work on a 50 Ω load. However, real antennas have no perfect 50 Ω load on all the supported frequency bands. Therefore, to reduce as much as possible performance degradation due to antenna mismatch, the following requirements should be met:

Measure the antenna termination with a network analyzer: connect the antenna through a coaxial cable to the measurement device, the $|S_{11}|$ indicates which portion of the power is delivered to antenna and which portion is reflected by the antenna back to the module output.

A good antenna should have an $|S_{11}|$ below -10 dB over the entire frequency band. Due to miniaturization, mechanical constraints and other design issues, this value will not be achieved. An $|S_{11}|$ value of about -6 dB - (in the worst case) - is acceptable.

Figure 15 shows an example of this measurement:

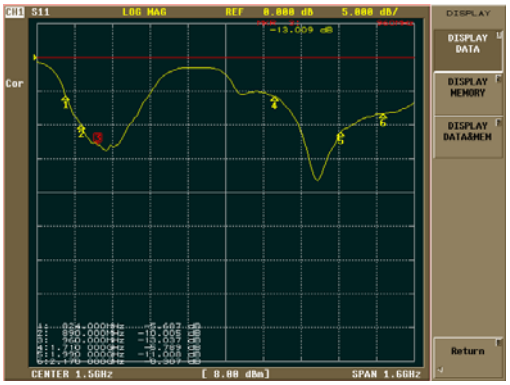


Figure 15: $|S_{11}|$ sample measurement of a penta-band antenna that covers in a small form factor the 4 bands (850 MHz, 900 MHz, 1800 MHz and 1900 MHz)

Figure 16 shows comparable measurements performed on a wideband antenna. The termination is better, but the size of the antenna is considerably larger.

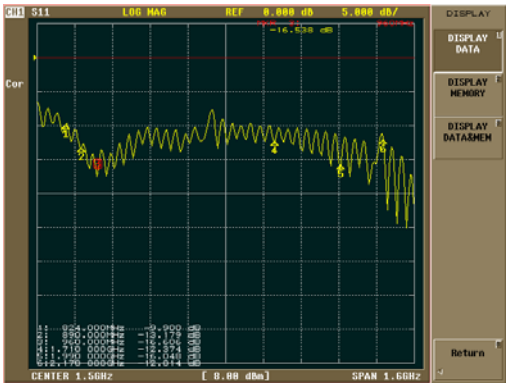


Figure 16: $|S_{11}|$ sample measurement of a wideband antenna

74.2.2 Antenna radiation

An indication of the antenna's radiated power can be approximated by measuring the $|S_{21}|$ from a target antenna to the measurement antenna, using a network analyzer with a wideband antenna. Measurements should be done at a fixed distance and orientation, and results compared to measurements performed on a known good antenna. Figure 17 through Figure 18 show measurement results. A wideband log periodic-like antenna was used, and the comparison was done with a half lambda dipole tuned at 900 MHz frequency. The measurements show both the $|S_{11}|$ and $|S_{21}|$ for the penta-band internal antenna and for the wideband antenna.

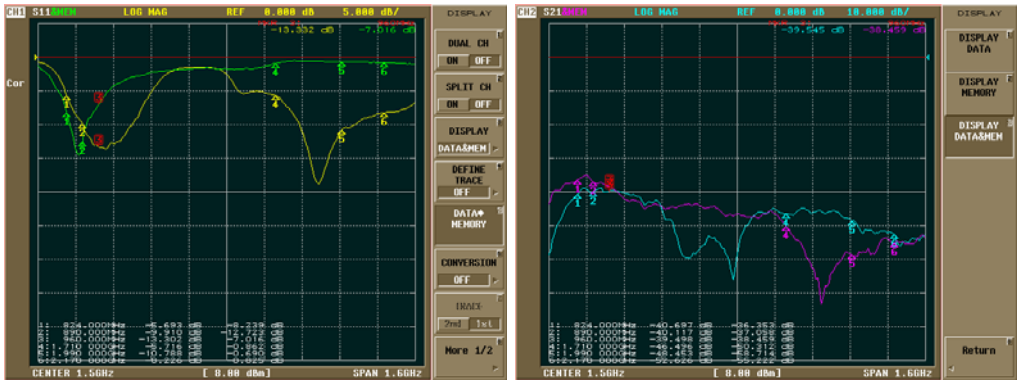


Figure 17: $|S_{11}|$ and $|S_{21}|$ comparison between a 900 MHz tuned half wavelength dipole (green/purple) and a penta-band internal antenna (yellow/cyan)

The half lambda dipole tuned at 900 MHz is known and has good radiation performance (both for gain and directivity). Then, by comparing the $|S_{21}|$ measurement with antenna under investigation for the frequency where the half dipole is tuned (e.g. marker 3 in Figure 17) it is possible to make a judgment on the antenna under test: if the performance is similar then the target antenna is good.

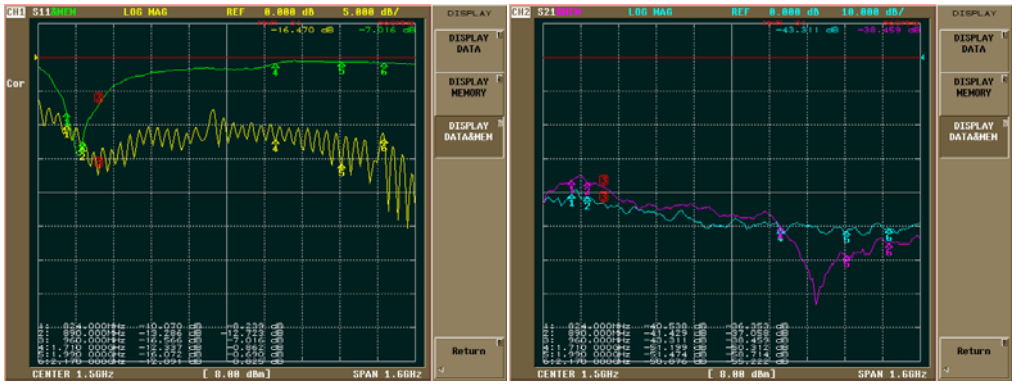


Figure 18: $|S_{11}|$ and $|S_{21}|$ comparison between a 900 MHz tuned half wavelength dipole (green/purple) and a wideband commercial antenna (yellow/cyan)

Instead if $|S_{21}|$ values for the tuned dipole are much better than the antenna under evaluation (like for marker 1/2 area of Figure 18, where dipole is 5 dB better), then it can be argued that the radiation of the target antenna (the wideband dipole in this case) is considerably less.

The same procedure should be repeated on other bands with half wavelength dipole re-tuned to the band under investigation.

☞ For good antenna radiation performance, antenna dimensions should be comparable to a quarter of the wavelength. Different antenna types can be used for the module, many of them (e.g. patch antennas, monopole) are based on a resonating element that works in combination with a ground plane. The ground plane, ideally infinite, can be reduced down to a minimum size that must be similar to one quarter of the wavelength of the minimum frequency that has to be radiated (transmitted/received). Numerical sample: frequency = 1 GHz → wavelength = 30 cm → minimum ground plane (or antenna size) = 7.5 cm. Below this size, the antenna efficiency is reduced.

74.3 ESD immunity test precautions

The immunity of the device (i.e. the application board where **Error! No text of specified style in document.** module is mounted) Electrostatic Discharge must be certified in compliance to the testing requirements standard [12], and the requirements for radio and digital cellular radio telecommunications system equipment standards [13] and [14].

The ESD test is performed at the enclosure port referred to as the physical boundary through which the EM field radiates. If the device implements an integral antenna, the enclosure port is seen as all insulating and conductive surfaces housing the device. If the device implements a removable antenna, the antenna port can be separated from the enclosure port. The antenna port comprises the antenna element and its interconnecting cable surfaces.

The applicability of the ESD test depends on the device classification, as well the test on other ports or on interconnecting cables to auxiliary equipments depends to the device accessible interfaces and manufacturer requirements.

Contact discharges are performed at conductive surfaces whereas air discharges are performed on insulating surfaces. Indirect contact discharges are performed on the measurement setup horizontal and vertical coupling planes.

Implement the following precautions to satisfy ESD immunity test requirements performed at the device enclosure in compliance to the category level and shown in the following table.

Application	Category	Immunity Level
All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration	Contact Discharge	4 kV
	Air Discharge	8 kV

Table 19: Electromagnetic Compatibility (EMC) ESD immunity requirement, standards "EN 61000-4-2, EN 301 489-1 V1.8.1, EN 301 489-7 V1.3.1"

Although EMC certification (including ESD immunity testing) must be performed in the final application of the radio equipment EUT, results are provided for LISA modules performing the test with a representative configuration to show that requirements can be met.

Since an external antenna is used, the antenna port can be separated from the enclosure port. The reference application is not enclosed in a box so the enclosure port is not indentified with physical surfaces. Therefore, some test cases cannot be applied. Only the antenna port is identified as accessible for direct ESD exposure.

The reference application implements all precautions described in the sections below. ESD immunity test results and applicability are reported in Table 20 according to test requirements [12], [13] and [14].

Category	Application	Immunity Level
Contact Discharge to coupling planes (indirect contact discharge)	Enclosure	+2 kV / -2 kV
		+4 kV / -4 kV
Contact Discharges to conducted surfaces (direct contact discharge)	Enclosure port	Not Applicable[5]
Contact Discharges to conducted surfaces (direct contact discharge)	Antenna port (only antenna with completely insulating surface can be used)	Not Applicable[6]
Air Discharge at insulating surfaces	Enclosure port	Not Applicable[7]
Air Discharge at insulating surfaces	Antenna port (only antenna with completely insulating surface can be used)	+2 kV / -2 kV
		+4 kV / -4 kV
		+8 kV / -8 kV

Table 20: Enclosure ESD immunity level result, standards "EN 61000-4-2, EN 301 489-1 V1.8.1, EN 301 489-7 V1.3.1" for LISA application reference design.

74.3.1 General precautions

The following module interfaces can have a critical influence in ESD immunity testing, depending on the application board handling. The following precautions are suggested:

HW_SHUTDOWN pin (FW75-C200 only)

Sensitive interface is the reset line (**HW_SHUTDOWN** pin):

- A 47 pF bypass capacitor (e.g. Murata GRM1555C1H470JA01) have to be mounted on the line termination connected to the **HW_SHUTDOWN** pin to avoid a module reset caused by an electrostatic discharge applied to the application board enclosure
- A series ferrite bead (e.g. Murata BLM15HD182SN1) must be added on the line connected to the **HW_SHUTDOWN** pin to avoid a module reset caused by an electrostatic discharge applied to the application board enclosure
- It is recommended to keep the connection line to **HW_SHUTDOWN** as short as possible

Reset_N pin (LISA-C200 only)

Sensitive interface is the reset line (**Reset_N** pin):

- A 47 pF bypass capacitor (e.g. Murata GRM1555C1H470JA01) have to be mounted on the line termination connected to the **Reset_N** pin to avoid a module reset caused by an electrostatic discharge applied to the application board enclosure

[5] LISA mounted on application design:
Not Applicability -> EUT with insulating enclosure surface, EUT without enclosure surface
Applicability -> EUT with conductive enclosure surface
[6] LISA mounted on application design:
Not Applicability -> Antenna with insulating surface
Applicability -> Antenna with conductive surface
[7] LISA mounted on application design:
Applicability -> EUT with insulating enclosure surface
Not Applicability -> EUT with conductive enclosure surface, EUT without enclosure surface

- A series ferrite bead (e.g. Murata BLM15HD182SN1) must be added on the line connected to the **Reset_N** pin to avoid a module reset caused by an electrostatic discharge applied to the application board enclosure
- It is recommended to keep the connection line to **Reset_N** as short as possible

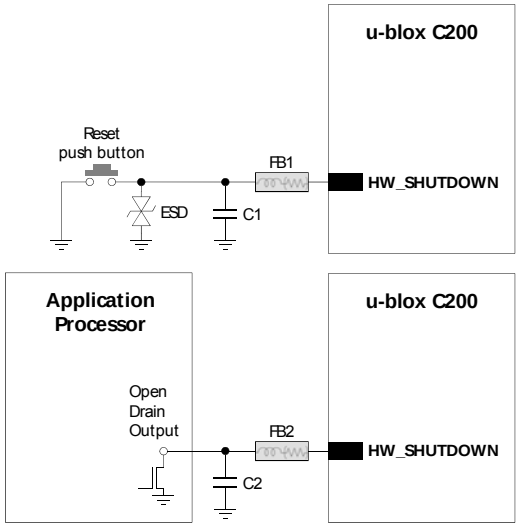


Figure 19: HW_SHUTDOWN application circuits for ESD immunity test

75	Reference	76	Description	77	Remarks

75	Reference	76	Description	77	Remarks
78	ESD	79	Varistor for ESD protection.	80	CT0402S14AHSG - EPCOS

75	Reference	76	Description	77	Remarks
81	C1, C2	82	47 pF Capacitor Ceramic C0G 0402 5% 50 V	83	GRM1555C1H470JA01 - Murata

75	Reference	76	Description	77	Remarks
84	FB1, FB2	85	Chip Ferrite Bead for Noise/EMI Suppression	86	BLM15HD182SN1 - Murata

75	Reference	76	Description	77	Remarks
87	Rint	88	10 kΩ Resistor 0402 5% 0.1 W	89	Internal pull-up resistor

Table 21: Example of components as ESD immunity test precautions for the HW_SHUTDOWN line

SIM interface

Sensitive interface is the SIM interface (**VSIM** pin, **SIM_RST** pin, **SIM_IO** pin, **SIM_CLK** pin):

- A 47 pF bypass capacitor (e.g. Murata GRM1555C1H470J) have to be mounted on the lines connected to **VSIM**, **SIM_RST**, **SIM_IO** and **SIM_CLK** to assure SIM interface functionality when an electrostatic discharge is applied to the application board enclosure
- It is suggested to use as short as possible connection lines at SIM pins

89.1.1 Antenna interface precautions

The antenna interface **ANT** can have a critical influence on the ESD immunity test depending on the application board handling. Antenna precaution suggestions are provided:

- If the device implements an embedded antenna and the device insulating enclosure avoids air discharge up to +8 kV / -8 kV to the antenna interface, no further precautions to ESD immunity test should be needed
- If the device implements an external antenna and the antenna and its connecting cable are provided with a completely insulating enclosure to avoid air discharge up to +8 kV / -8 kV to the whole antenna and cable surfaces, no further precautions to ESD immunity test should be needed
- If the device implements an external antenna and the antenna or its connecting cable are not provided with completely insulating enclosure to avoid air discharge up to +8 kV / -8 kV to the whole antenna and cable surfaces, the following precautions to ESD immunity test should be implemented on the application board

A higher protection level is required at the **ANT** port if the line is externally accessible on the application board. ESD immunity test requires protection up to +4 kV / -4 kV for direct Contact Discharge and up to +8 kV / -8 kV for Air Discharge applied to the antenna port.

89.1.2 Module interfaces precautions

Comment [rjc6]: I need to check these contact numbers

All the module pins that are externally accessible should be included in the ESD immunity test since they are considered to be a port as defined in [13]. Depending on applicability, and in order to satisfy ESD immunity test requirements and ESD category level, pins connected to the port should be protected up to +4 kV / -4 kV for direct Contact Discharge, and up to +8 kV / -8 kV for Air Discharge applied to the enclosure surface.

The maximum ESD sensitivity rating of all the pins of the module, except the **ANT** pin, is 1 kV (Human Body Model according to JESD22-A114F). A higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array or CT0402S14AHSG).

For the USB interface a very low capacitance (i.e. less or equal to 1 pF) ESD protection (e.g. Tyco Electronics PESD0402-140 ESD protection device) can be mounted on the lines connected to **USB_D+** and **USB_D-** pins.

For the SIM interface a low capacitance (i.e. less than 10 pF) ESD protection (e.g. Infineon ESD8V0L2B-03L or AVX USB0002) must be placed near the SIM card holder on each line (**VSIM**, **SIM_IO**, **SIM_CLK**, **SIM_RST**).

90 Features description

90.1 Firmware (upgrade) Over The Air (FOTA

Error! No text of specified style in document. modules will support this feature. Sprint Carrier requirement.

Not required for Verizon Carrier.

90.2 TCP/IP

Via the AT commands it's possible to access the TCP/IP functionalities. For more details about AT commands see the *u-blox C200 AT Commands Manual* [3].

90.2.1 Multiple PDP contexts and sockets

Two PDP context types are defined:

- "external" PDP context: IP packets are built by the DTE, the MT's IP instance runs the IP relay function only
- "internal" PDP context: the PDP context (relying on the MT's TCP/IP stack) is configured, established and handled via the data connection management packet switched data commands described in *u-blox C200 AT Commands Manual* [3]

Multiple PDP contexts are supported. The DTE can access these PDP contexts either alternatively through the physical serial port, or simultaneously through the virtual serial ports of the multiplexer (multiplexing mode MUX), with the following constraints:

- Using the MT's embedded TCP/IP stack, only 1 internal PDP context is supported. This IP instance supports up to 7 sockets
- Using only external PDP contexts, it is possible to have at most 3 IP instances (with 3 different IP addresses) simultaneously. If in addition the internal PDP context is used, at most 2 external PDP contexts can be activated

Secondary PDP contexts (PDP contexts sharing the IP address of a primary PDP context) are also supported. Traffic Flow Filters for such secondary contexts shall be specified according to *3GPP TS 23.060* [8].

At most 2 secondary PDP contexts can be activated, since the maximum number of PDP contexts, both normal and secondary, is always 3.

90.3 HTTP

Error! No text of specified style in document. modules will support this feature in the upcoming FW version.

Appendix

A Glossary

ADC	Analog to Digital Converter
AP	Application Processor
AT	AT Command Interpreter Software Subsystem, or attention
CBCH	Cell Broadcast Channel
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DDC	Display Data Channel
DSP	Digital Signal Processing
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTM	Dual Transfer Mode
DTR	Data Terminal Ready
EBU	External Bus Interface Unit
CDMA	CODE Division Multiple Access
FDD	Frequency Division Duplex
FEM	Front End Module
FOAT	Firmware Over AT commands
FTP	File Transfer Protocol
FTPS	FTP Secure
GND	Ground
GPIO	General Purpose Input Output
GPS	Global Positioning System
HF	Hands-free
HTTP	HyperText Transfer Protocol
HTTPS	Hypertext Transfer Protocol over Secure Socket Layer
HW	Hardware
I/Q	In phase and Quadrature
I²C	Inter-Integrated Circuit
I²S	Inter IC Sound
IP	Internet Protocol
IPC	Inter Processor Communication
LNA	Low Noise Amplifier
MCS	Modulation Coding Scheme

NOM	Network Operating Mode
PA	Power Amplifier
PBCCH	Packet Broadcast Control Channel
PCM	Pulse Code Modulation
PCS	Personal Communications Service
PFM	Pulse Frequency Modulation
PMU	Power Management Unit
RF	Radio Frequency
RI	Ring Indicator
RTC	Real Time Clock
RTS	Request To Send
RXD	RX Data
SAW	Surface Acoustic Wave
SIM	Subscriber Identification Module
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SRAM	Static RAM
TCP	Transmission Control Protocol
TDMA	Time Division Multiple Access
TXD	TX Data
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
USB	Universal Serial Bus

Related documents

[1] LISA-C200 Data Sheet, Docu No CDMA-2X-11001

[2] FW75 Data Sheet, Docu No CDMA-1X-11006

[3] u-blox C200 AT Commands Manual, Docu No CDMA-2X-11002

[4] ITU-T Recommendation V.24, 02-2000. List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE). http://www.itu.int/rec/T-REC-V.24-200002-I/en

[5] 3GPP TS 27.007 - AT command set for User Equipment (UE) (Release 1999)

[6] 3GPP TS 27.005 - Use of Data Terminal Equipment - Data Circuit terminating; Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS) (Release 1999)

[7] 3GPP TS 27.010 - Terminal Equipment to User Equipment (TE-UE) multiplexer protocol (Release 1999)

[8] 3GPP TS 23.060 - General Packet Radio Service (GPRS); Service description; Stage 2 (Release 1999)

[9] Universal Serial Bus Revision 2.0 specification, http://www.usb.org/developers/docs/

[10] I2C-Bus Specification Version 2.1 Philips Semiconductors (January 2000), http://www.nxp.com/acrobat_download/literature/9398/39340011_21.pdf

[11] GPS Implementation Application Note, Docu No GSM.G1-CS-09007

[12] CENELEC EN 61000-4-2 (2001): "Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test".

[13] ETSI EN 301 489-1 V1.8.1: “Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements”

[14] ETSI EN 301 489-7 V1.3.1 “Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 7: Specific conditions for mobile and portable radio and ancillary equipment of digital cellular radio telecommunications systems (GSM and DCS)“

Some of the above documents can be downloaded from u-blox web-site (http://www.u-blox.com).

Revision history

91 Revision	92 Date	93 Name	94 Status / Comments

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95	-	96	11/24/11	97	rcam	98	Initial Release

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