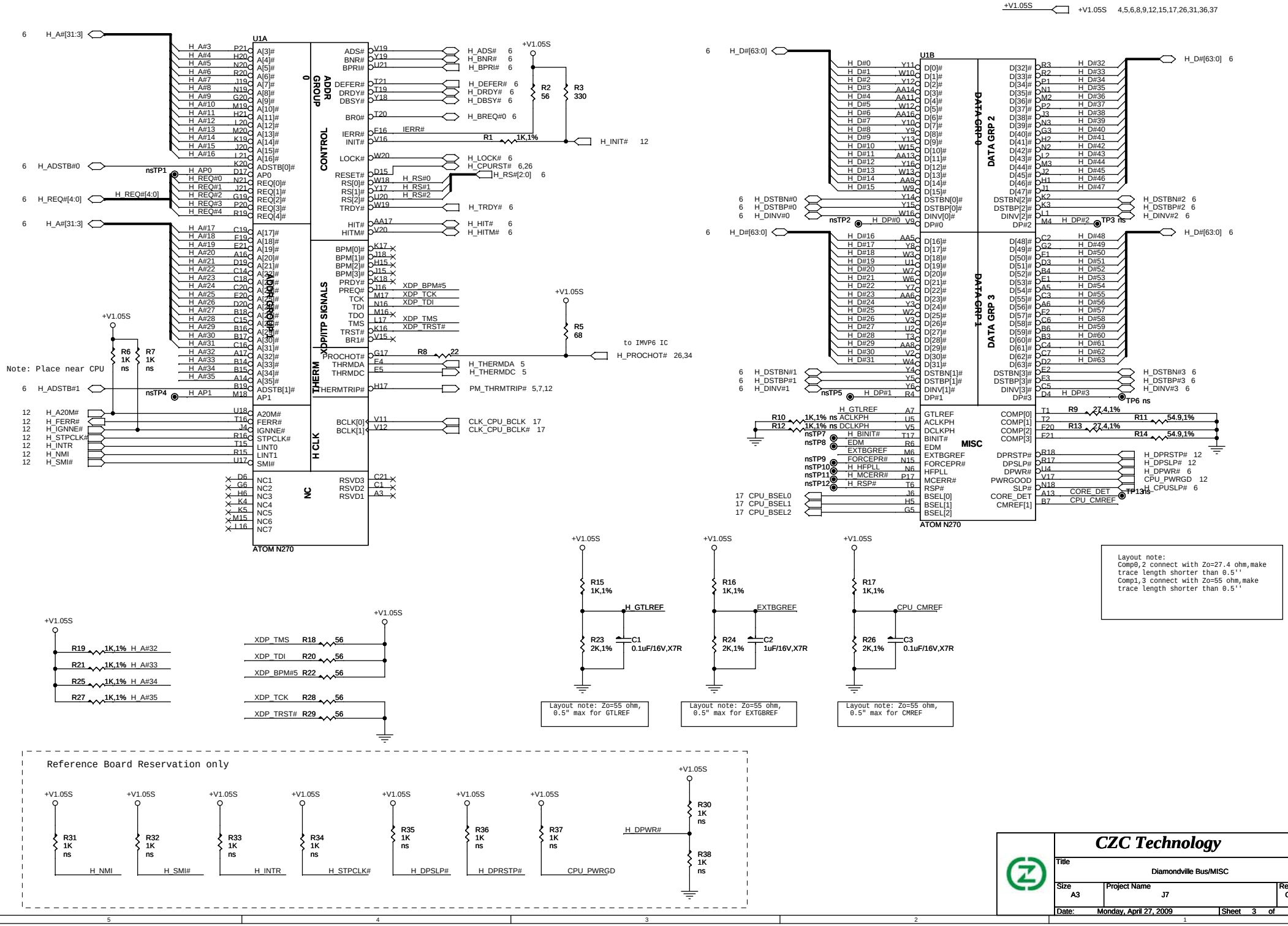
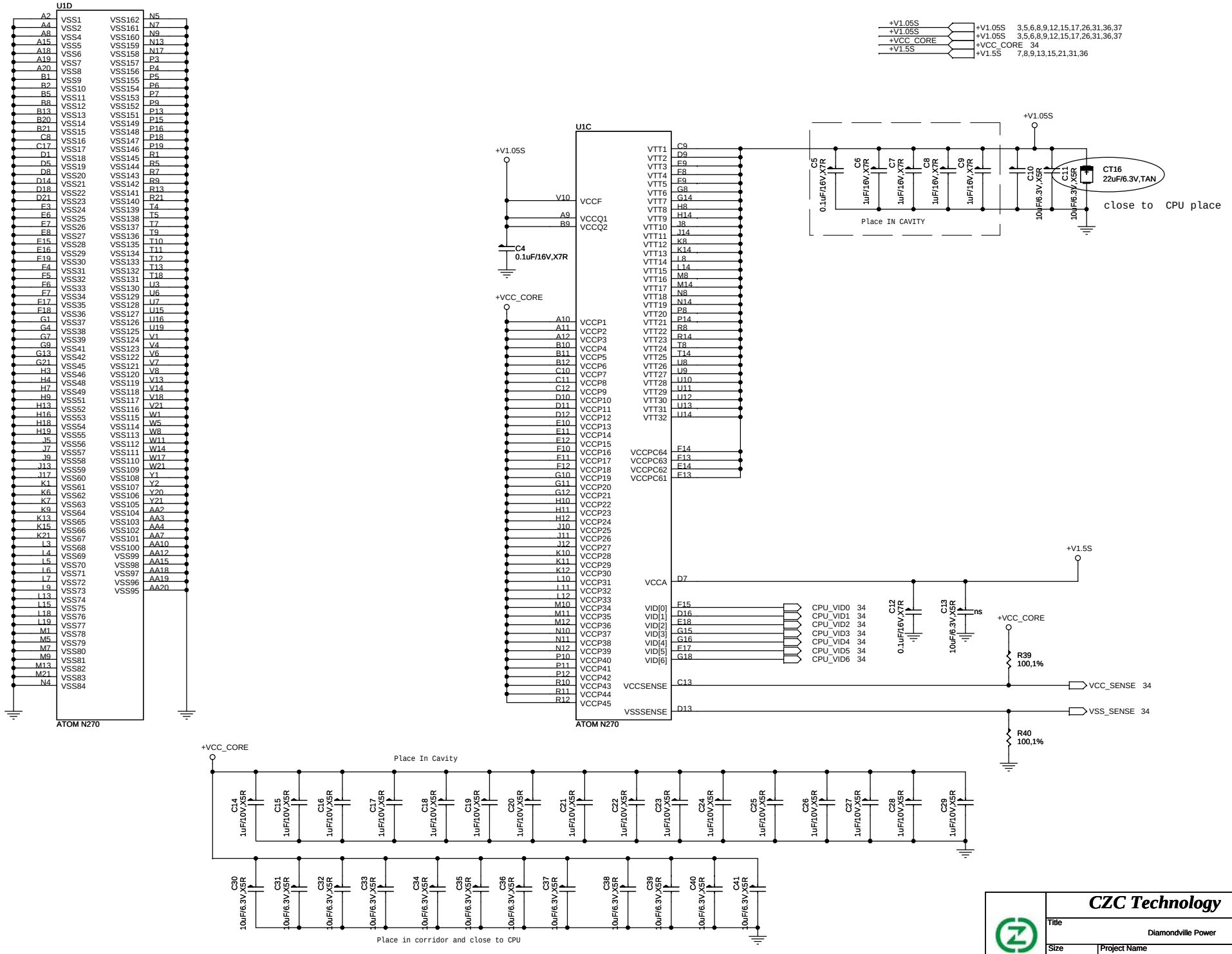
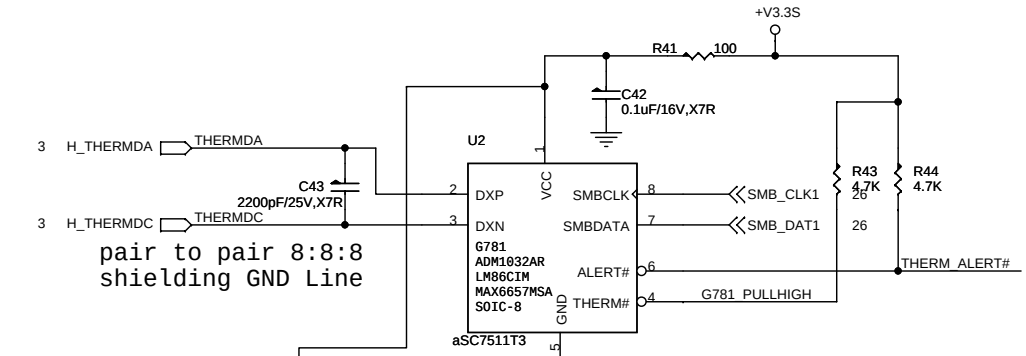

+V1.05S +V1.05S 4,5,6,8,9,12,15,17,26,31,36,37
U1A
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
NC
ATOM N270
H_A#[31:3]
H_ADSTB#0
H_REQ#[4:0]
nsTP1
nsTP4
H_ADS# 6
H_BNR# 6
H_BPRI# 6
H_DEFER# 6
H_DRDY# 6
H_DBSY# 6
H_BREQ#0 6
IERR#
H_INIT# 12
H_LOCK# 6
H_CPURST# 6,26
H_RS#[2:0] 6
H_TRDY# 6
H_HIT# 6
H_HITM# 6
XDP_BPM#5
XDP_TCK
XDP_TDI
XDP_TMS
XDP_TRST#
to IMVP6 IC
H_PROCHOT# 26,34
H_THERMDA 5
H_THERMDC 5
PM_THRMTRIP# 5,7,12
CLK_CPU_BCLK 17
CLK_CPU_BCLK# 17
Note: Place near CPU
R1 1K,1%
R2 56
R3 330
R5 68
R8 22
R6 1K ns
R7 1K ns
U1B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
H_D#[63:0]
H_DSTBN#0
H_DSTBP#0
H_DINV#0
H_DSTBN#1
H_DSTBP#1
H_DINV#1
H_DSTBN#2 6
H_DSTBP#2 6
H_DINV#2 6
H_DSTBN#3 6
H_DSTBP#3 6
H_DINV#3 6
nsTP2
nsTP5
TP3 ns
TP6 ns
R9 27.4,1%
R11 54.9,1%
R13 27.4,1%
R14 54.9,1%
R10 1K,1% ns ACLKPH
R12 1K,1% ns DCLKPH
nsTP7 H_BINIT#
nsTP8 EDM
nsTP9 FORCEPR#
nsTP10 H_HFPLL
nsTP11 H_MCERR#
nsTP12 H_RSP#
H_DPRSTP# 12
H_DPSLP# 12
H_DPWR# 6
CPU_PWRGD 12
H_CPUSLP# 6
TP13 ns
CORE_DET
CPU_CMREF
17 CPU_BSEL0
17 CPU_BSEL1
17 CPU_BSEL2
R15 1K,1% H_GTLREF R23 2K,1% C1 0.1uF/16V,X7R
R16 1K,1% EXTBGREF R24 2K,1% C2 1uF/16V,X7R
R17 1K,1% CPU_CMREF R26 2K,1% C3 0.1uF/16V,X7R
Layout note: Zo=55 ohm, 0.5" max for GTLREF
Layout note: Zo=55 ohm, 0.5" max for EXTGBREF
Layout note: Zo=55 ohm, 0.5" max for CMREF
Layout note:
Comp0,2 connect with Zo=27.4 ohm,make trace length shorter than 0.5''
Comp1,3 connect with Zo=55 ohm,make trace length shorter than 0.5''
R19 1K,1% H_A#32
R21 1K,1% H_A#33
R25 1K,1% H_A#34
R27 1K,1% H_A#35
XDP_TMS R18 56
XDP_TDI R20 56
XDP_BPM#5 R22 56
XDP_TCK R28 56
XDP_TRST# R29 56
Reference Board Reservation only
R31 1K ns H_NMI
R32 1K ns H_SMI#
R33 1K ns H_INTR
R34 1K ns H_STPCLK#
R35 1K ns H_DPSLP#
R36 1K ns H_DPRSTP#
R37 1K ns CPU_PWRGD
H_DPWR#
R30 1K ns
R38 1K ns
CZC Technology
Title
Diamondville Bus/MISC
Size A3
Project Name J7
Rev C
Date: Monday, April 27, 2009
Sheet 3 of 43

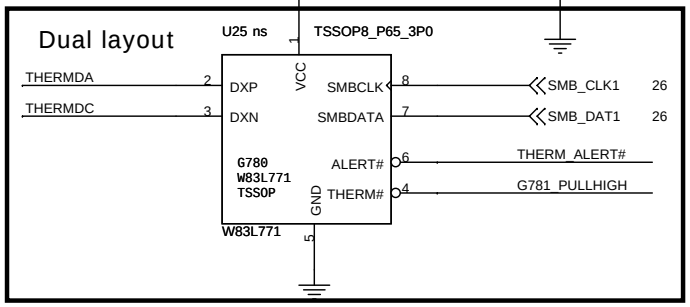


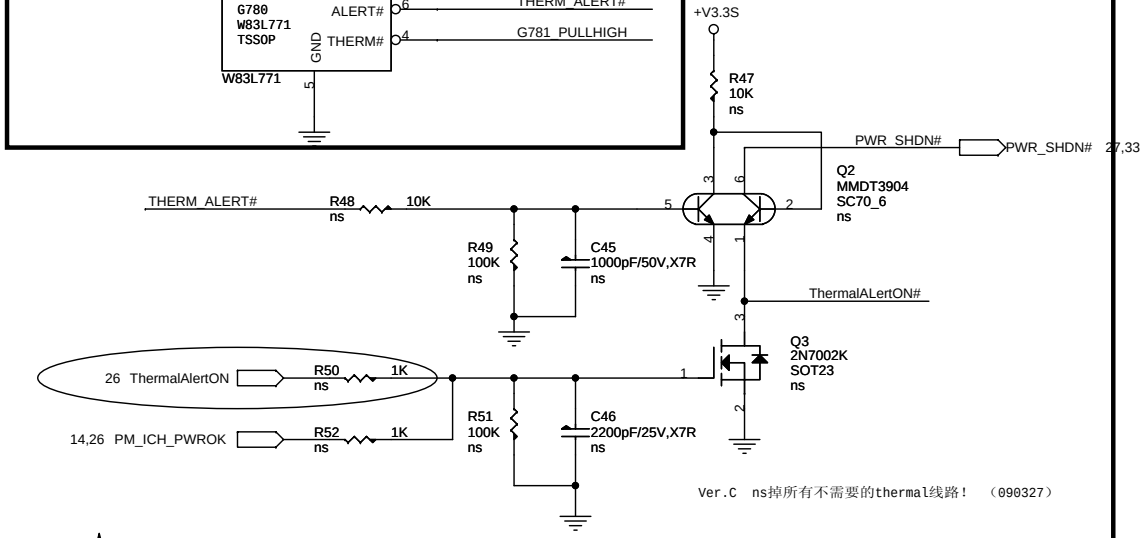
Title	Diamondville Power
Size	A3
Project Name	J7
Rev	C
Date:	Monday, April 27, 2009
Sheet	4 of 43

CZC Technology

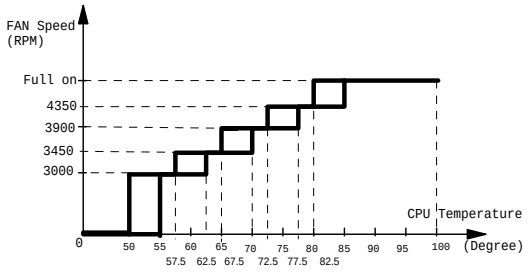
CPU Thermal



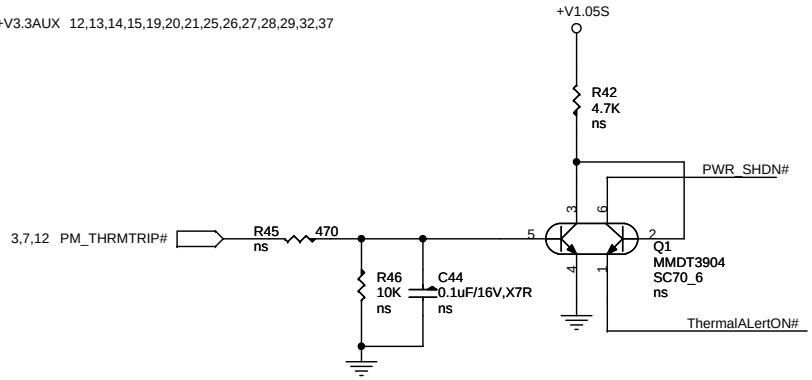




Ver.C ns掉所有不需要的thermal线路！ （090327）

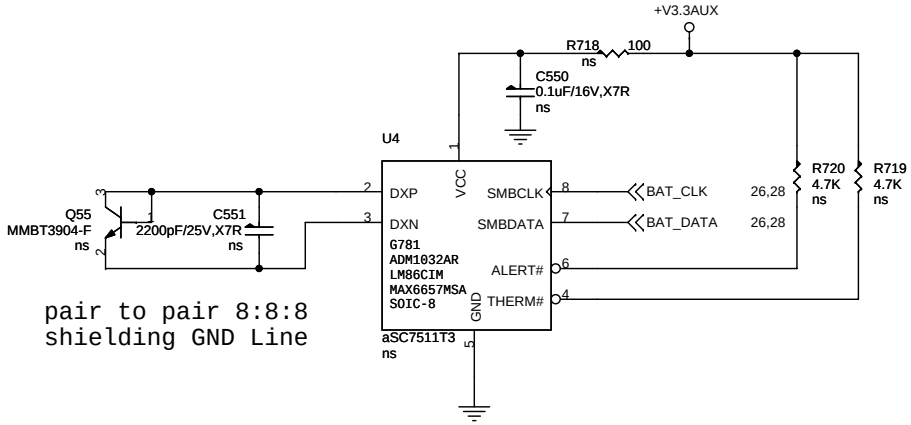


+V3.3S +V3.3S 7,8,9,11,12,13,14,15,17,18,19,20,21,22,23,24,25,26,32,33,34,36,37
+V1.05S +V1.05S 3,4,6,8,9,12,15,17,26,31,36,37
+V3.3AUX +V3.3AUX 12,13,14,15,19,20,21,25,26,27,28,29,32,37

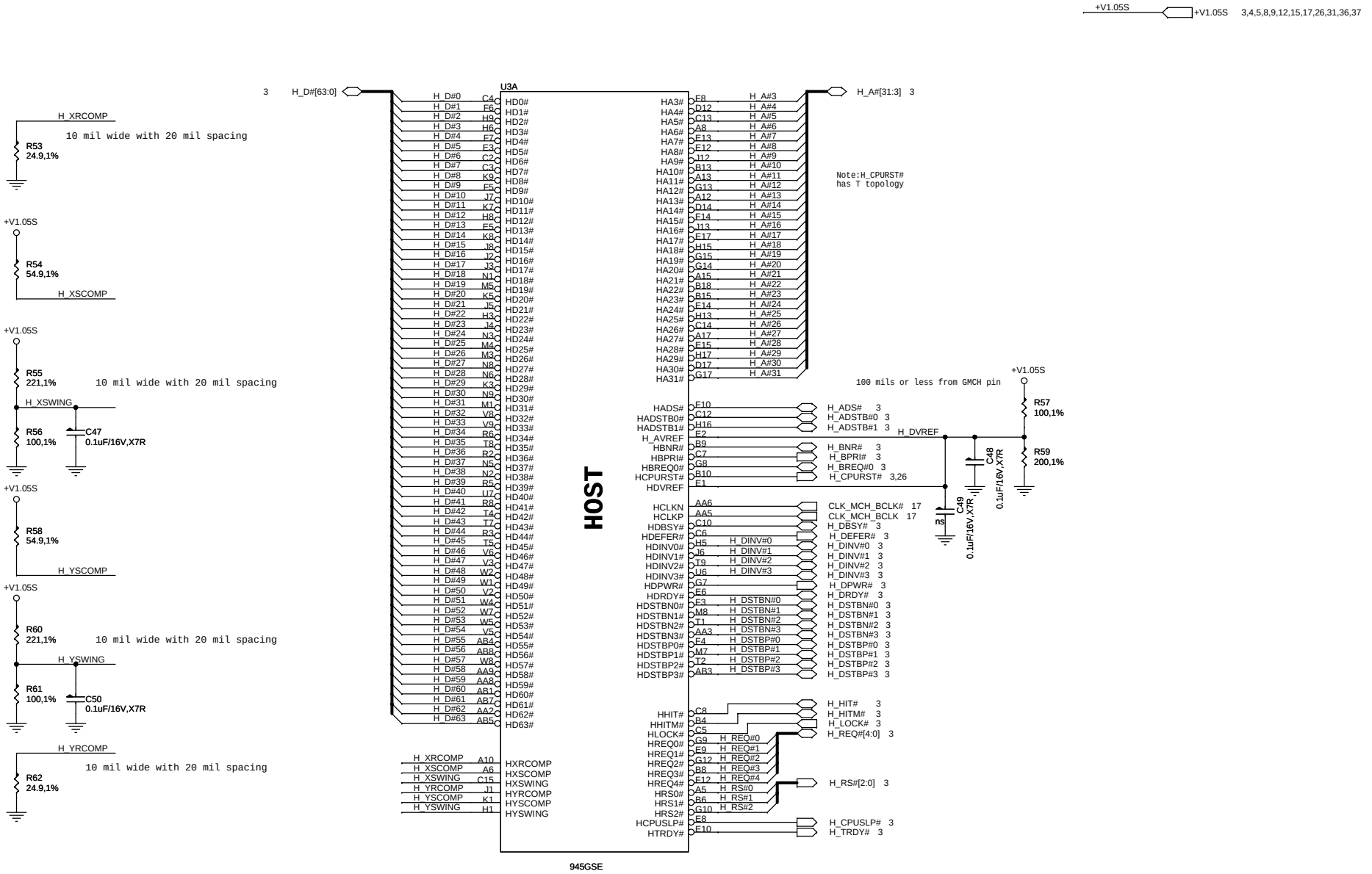


System Thermal

Note: Need be placed near the area of the highest temp

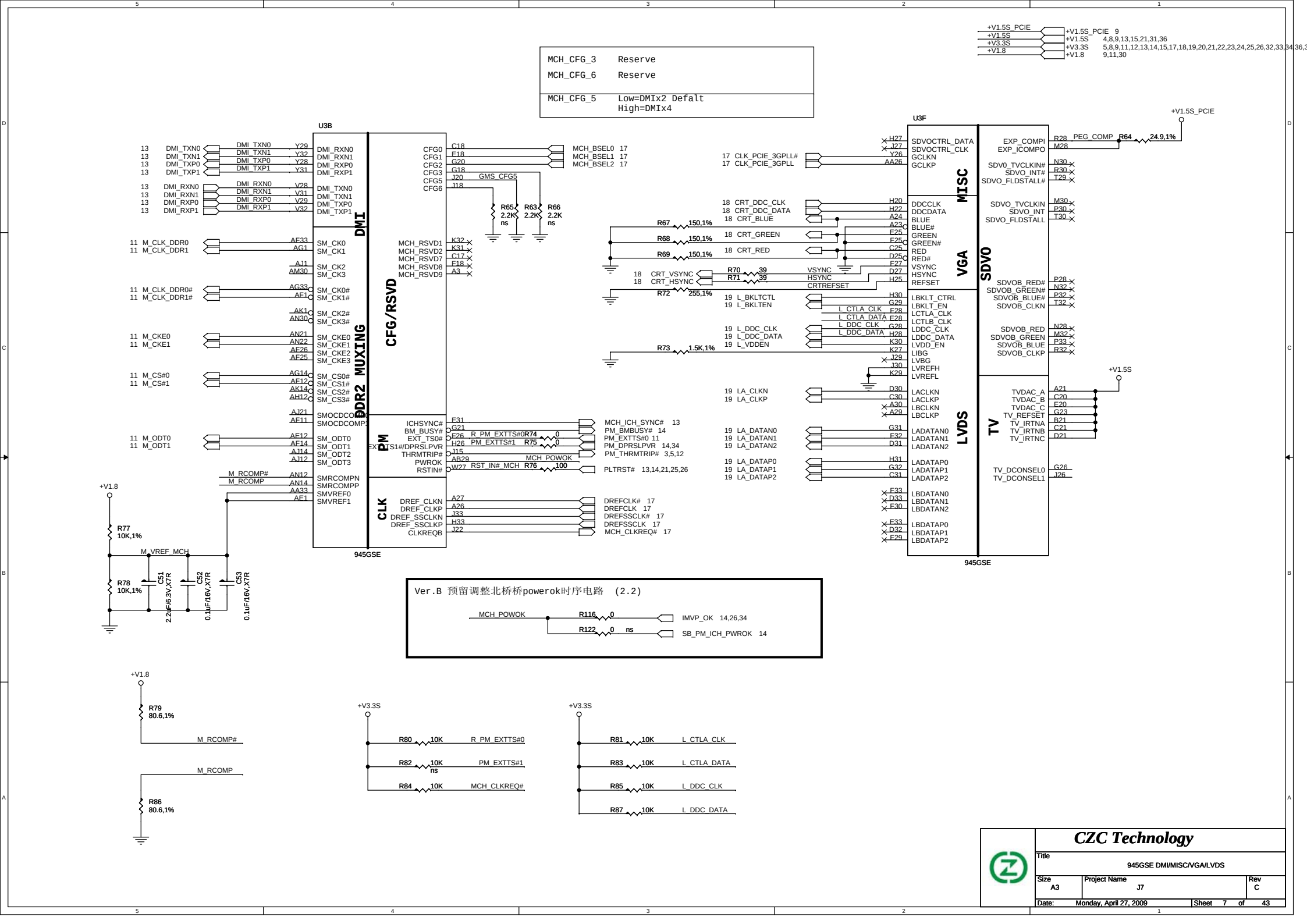


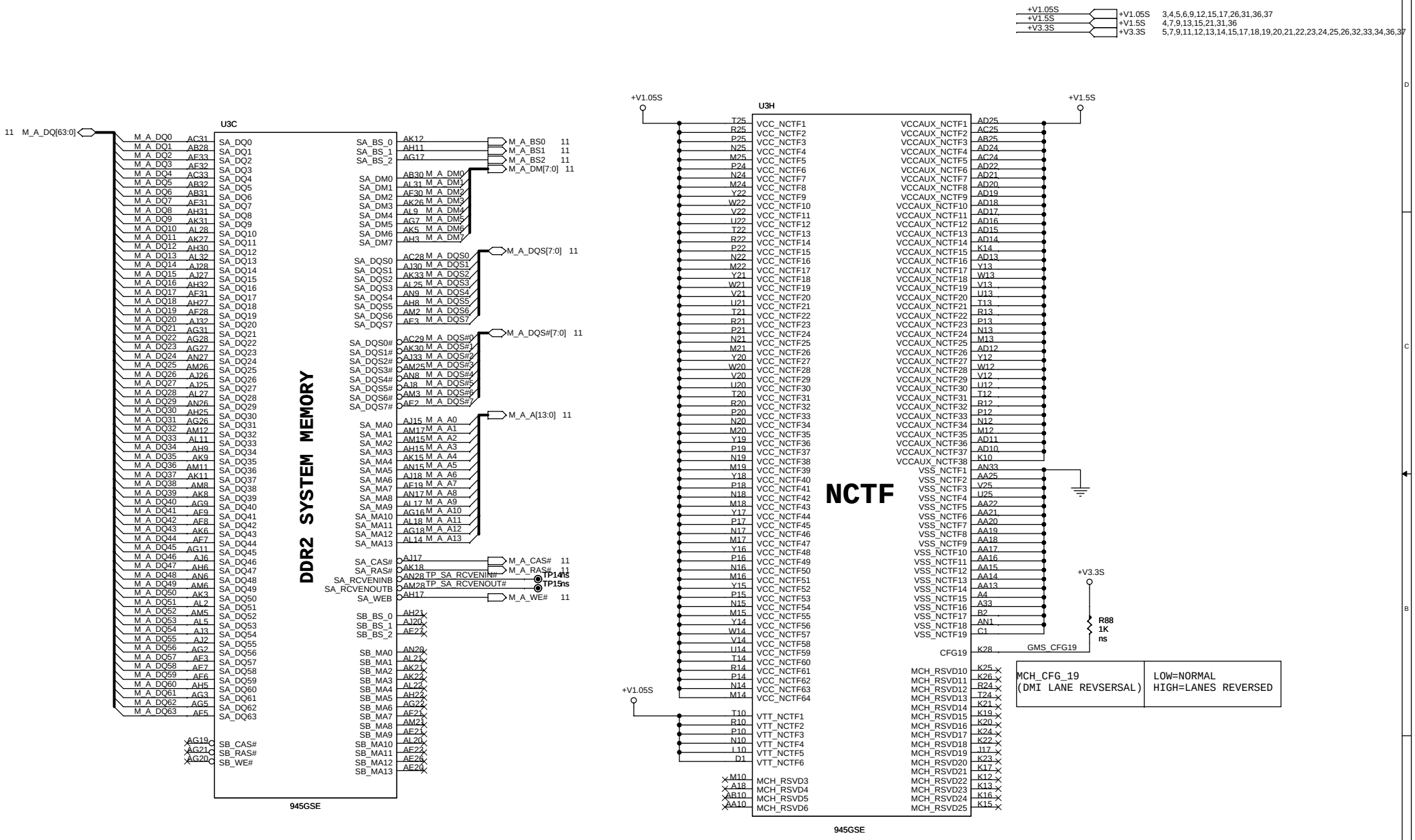
CZC Technology		
Title: CPU THERMAL SENSOR		
Size: Custom	Project Name: J7	Rev: C
Date: Monday, April 27, 2009	Sheet 5 of 43	



Title	945GSE FSB	
Size: A3	Project Name: J7	Rev: C
Date: Monday, April 27, 2009	Sheet 6 of 43	

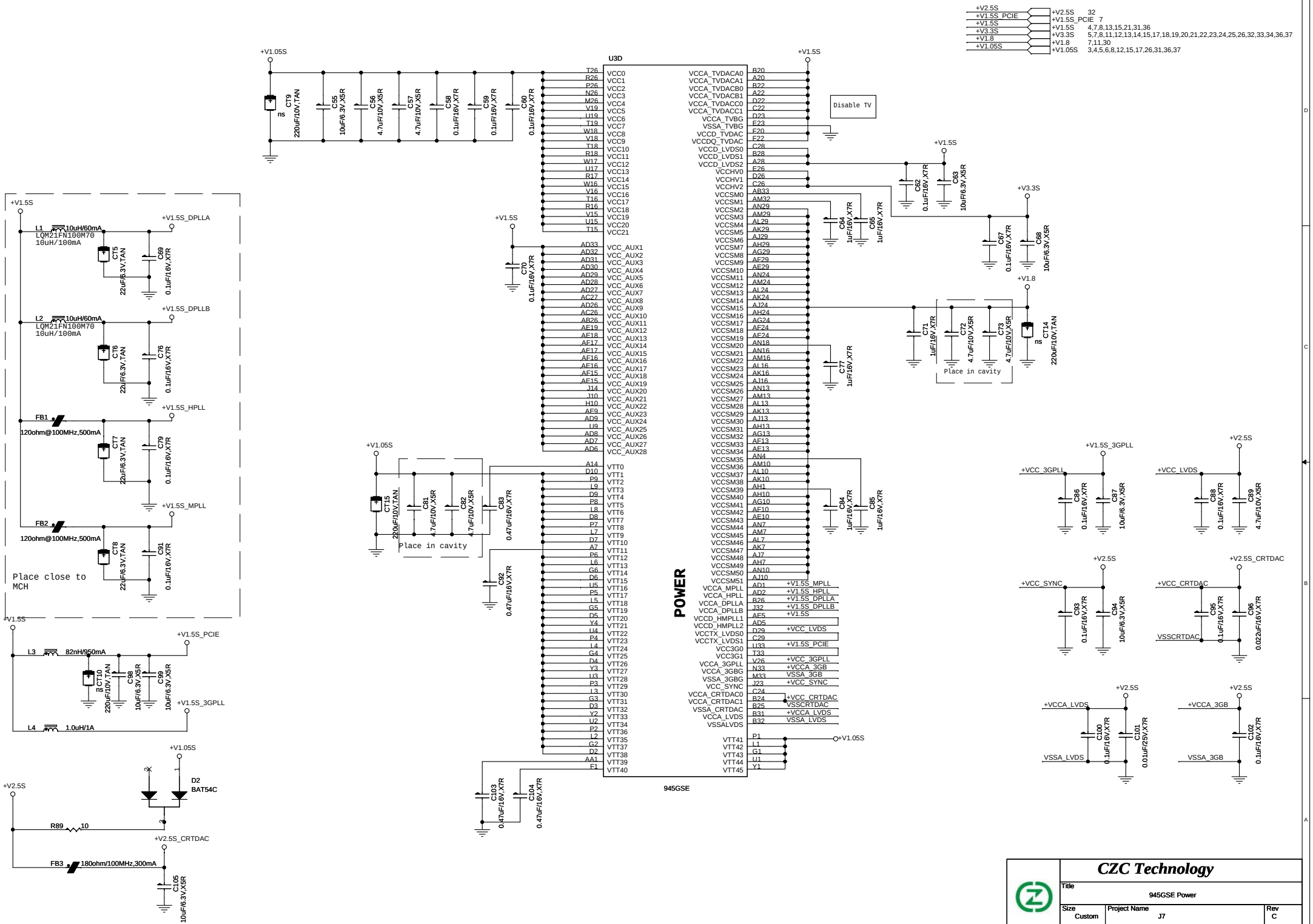
CZC Technology

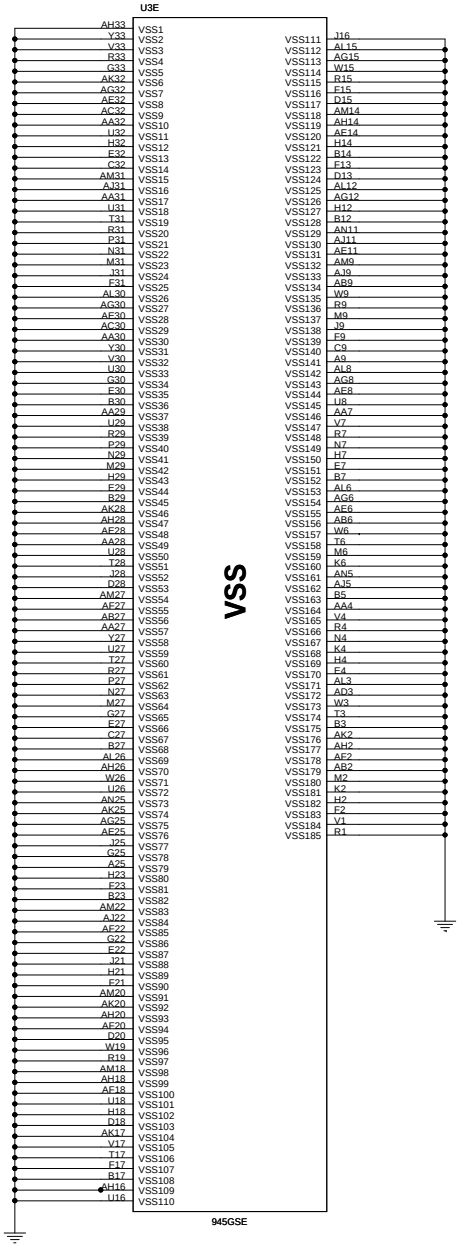

MCH_CFG_3 Reserve
MCH_CFG_6 Reserve
MCH_CFG_5 Low=DMIx2 Defalt
High=DMIx4
+V1.5S_PCIE
+V1.5S
+V3.3S
+V1.8
U3B
DMI
DDR2 MUXING
CFG/RSVD
PM
CLK
945GSE
U3F
MISC
VGA
LVDS
SDVO
TV
M_VREF_MCH
M_RCOMP#
M_RCOMP
R_PM_EXTTS#0
PM_EXTTS#1
MCH_CLKREQ#
L_CTLA_CLK
L_CTLA_DATA
L_DDC_CLK
L_DDC_DATA
Ver.B 预留调整北桥桥powerok时序电路 (2.2)
MCH_POWOK
IMVP_OK 14,26,34
SB_PM_ICH_PWROK 14
CZC Technology
Title
945GSE DMI/MISC/VGA/LVDS
Size A3
Project Name J7
Rev C
Date: Monday, April 27, 2009
Sheet 7 of 43

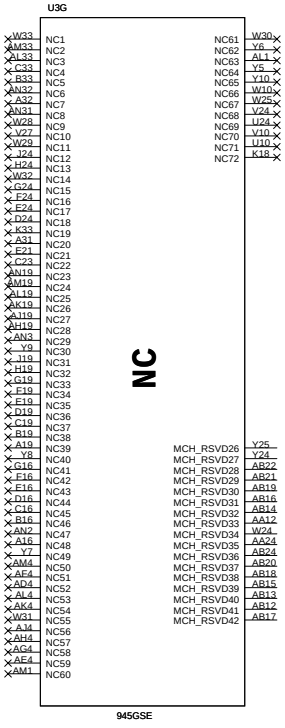


Title	945GSE DDRII
Size	A3
Project Name	J7
Rev	C
Date:	Monday, April 27, 2009
Sheet	8 of 43

CZC Technology


+V2.5S +V2.5S 32
+V1.5S_PCIE +V1.5S_PCIE 7
+V1.5S +V1.5S 4,7,8,13,15,21,31,36
+V3.3S +V3.3S 5,7,8,11,12,13,14,15,17,18,19,20,21,22,23,24,25,26,32,33,34,36,37
+V1.8 +V1.8 7,11,30
+V1.05S +V1.05S 3,4,5,6,8,12,15,17,26,31,36,37
U3D
945GSE
POWER
Disable TV
Place in cavity
Place close to MCH
+V1.5S_DPLLA
+V1.5S_DPLLB
+V1.5S_HPLL
+V1.5S_MPLL
+V1.5S_3GPLL
+V1.5S_PCIE
+V2.5S_CRTDAC
L1 10uH/60mA LQM21FN100M70 10uH/100mA
L2 10uH/60mA LQM21FN100M70 10uH/100mA
FB1 120ohm@100MHz,500mA
FB2 120ohm@100MHz,500mA
L3 82nH/950mA
L4 1.0uH/1A
R89 10
FB3 180ohm/100MHz,300mA
D2 BAT54C
+V1.5S_3GPLL
+V2.5S
+VCC_3GPLL
+VCC_LVDS
+VCC_SYNC
+VCC_CRTDAC
VSSCRTDAC
+VCCA_LVDS
VSSA_LVDS
+VCCA_3GB
VSSA_3GB
CZC Technology
Title 945GSE Power
Size Custom
Project Name J7
Rev C
Date: Monday, April 27, 2009
Sheet 9 of 43





CZC Technology		
Title: 945GSE GND		
Size: Custom	Project Name: J7	Rev: C
Date: Monday, April 27, 2009	Sheet 10 of 43	

Foxconn: AS0A426-N2RN-7F
LCDCON (620200010002)

DIM1
DDR2_RVS_5.2
DDR2S200H52_REV

DDRII

SO-DIMM 0

Address: 1010 000x=A0H

CLOCK 0,1
CKE 0,1

+V1.8 7,9,30
+V0.9S 30
+V3.3S 5,7,8,9,12,13,14,15,17,18,19,20,21,22,23,24,25,26,32,33,34,36,37

Layout note:电容靠近DDR slot VDD PIN

RN1 RN2 RN3 RN4 RN5 RN6 — 56 x4
R90 56 M_A_A8
R91 56 M_A_CAS#

R92 10K DIMM_SA0
R93 10K DIMM_SA1
R94 10K,1%
R95 10K,1%
R729 0 ns MBIAS_VREF

Close to DDRII pin

Title	DDR2 SODIMM
Size	Custom
Project Name	J7
Rev	C
Date:	Monday, April 27, 2009
Sheet	11 of 43

CZC Technology

+V1.05S
+V3.3S
+V3.3A_RTC
+V3.3AUX

+V1.05S 3,4,5,6,8,9,15,17,26,31,36,37
+V3.3S 5,7,8,9,11,13,14,15,17,18,19,20,21,22,23,24,25,26,32,33,34,36,37
+V3.3A_RTC 15
+V3.3AUX 5,13,14,15,19,20,21,25,26,27,28,29,32,37

U5A

RTC_X1 AB1 RTCX1
RTC_X2 AB2 RTCX2
RTC_RST# AA3 RTCRST#
SM_INTRUDER# Y5 INTRUDER#
ICH_INTVRMEN W4 INTVRMEN
RTC

W1 EE_CS
Y1 EE_SHCLK
Y2 EE_DOUT
W3 EE_DIN

V3 LAN_CLK
U3 LAN_RSTSYNC
U5 LAN_RXD0
V4 LAN_RXD1
T5 LAN_RXD2
U7 LAN_TXD0
V6 LAN_TXD1
V7 LAN_TXD2
LAN CPU

C410 10pF/50V,NPO ns

22 HDA_BITCLK R101 39 ACZ_BITCLK_R U1 ACZ_BIT_CLK
22 HDA_SYNC R102 39 ACZ_SYNC_R R6 ACZ_SYNC
22 HDA_RST# R103 39 ACZ_RST#_R R5 ACZ_RST#
22 HDA_SDATAIN0 T2 ACZ_SDIN0
T3 ACZ_SDIN1
T1 ACZ_SDIN2
22 HDA_SDATAOUT R105 39 ACZ_SDATAOUT_R T4 ACZ_SDOUT
AC-97/AZALIA

20 SATA_LED# SATA_LED#_R AE18 SATALED#
20 SATA_RXN0 AE3 SATA0RXN
20 SATA_RXP0 AE3 SATA0RXP
20 SATA_TXN0 C142 3900pF/50V,X7R SATA_TXN0_C AG2 SATA0TXN
20 SATA_TXP0 C143 3900pF/50V,X7R SATA_TXP0_C AH2 SATA0TXP
AE7 SATA2RXN
AE7 SATA2RXP
AG6 SATA2TXN
AH6 SATA2TXP
17 CLK_PCIE_SATA# AE1 SATA_CLKN
17 CLK_PCIE_SATA AE1 SATA_CLKP

Short pins AH10 and AG10 at the package. Place R within 500mils of ICH7 ball

R108 24.9,1% SATA_RBIAS_PN AH10 SATARBIASN
AG10 SATARBIASP
SATA

AE15 DIOR#
AH15 DIOW#
AE16 DDACK#
IDEREQ AH16 IDEIRQ
IORDY AG16 IORDY
AE15 DDREQ
IDE

NH82801GBM

LAD0 AA6 LPC_AD0 LPC_AD0 21,26
LAD1 AB5 LPC_AD1 LPC_AD1 21,26
LAD2 AC4 LPC_AD2 LPC_AD2 21,26
LAD3 Y6 LPC_AD3 LPC_AD3 21,26
LDRQ0# AC3 LDRQ0#
LDRQ1#/GPIO23 AA5 LDRQ1#
LFRAME# AB3 LPC_FRAME# 21,26
A20GATE AE22 CPU_A20GATE- CPU_A20GATE- 26
A20M# AH28 H_A20M# 3
CPUSLP# AG27
TP1/DPRSTP# AE24 H_DPRSTP#_R R98 0 H_DPRSTP# 3
TP2/DPSLP# AH25 H_DPSLP#_R R99 0 H_DPSLP# 3
FERR# AG26 H_FERR# H_FERR# 3
GPIO49/CPUPWRGD AG24 CPU_PWRGD 3
IGNNE# AG22 H_IGNNE# 3
INIT3_3V# AG21 FWH_INIT#
INIT# AE22 H_INIT# 3
INTR AE25 H_INTR 3
RCIN# AG23 H_RCIN# H_RCIN# 26
NMI AH24
SMI# AE23 H_SMI#_R R104 0 H_SMI# 3
STPCLK# AH22 H_STPCLK# 3
THERMTRIP# AE26 H_THRMTRIP_R R106 24.9,1% PM_THRMTRIP# 3,5,7

R106 need to place within 2" of ICH7
R104 must be placed within 2" of R129 W/O stub

DD0 AB15
DD1 AE14
DD2 AG13
DD3 AF13
DD4 AD14
DD5 AC13
DD6 AD13
DD7 AC12
DD8 AE13
DD9 AE12
DD10 AB13
DD11 AC14
DD12 AE14
DD13 AH13
DD14 AH14
DD15 AC15
DA0 AH17
DA1 AE17
DA2 AF17
DCS1# AE16
DCS3# AD16

+V3.3A_RTC
1uF/16V,X7R C140
RTC_RST# R96 20K
1uF/16V,X7R C141
R97 1M
SM_INTRUDER#
D3 BAT54C SOT23
R100 1K
RTCCN1 CONN2_R HWS2_1P25
+V3.3AUX

CMOS Settings CLRCMOS:
Clear CMOS Shunt
Keep CMOS Open

RTC_RST#
CLRCMOS JOPEN RESISTOR_1 ns

Ver.C 晶振修改为小封装！ （090327）
RTC_X1 C144 10pF/50V,NPO
R107 10M
Y1 32.768kHz,20ppm,12.5pF X4S67x15
RTC_X2 C145 10pF/50V,NPO

+V3.3A_RTC
R111 332K,1%
ICH_INTVRMEN
DEL R116

ICH7 intel VccSus1.05 enable strap

	INTVRMEN		
Enable(default)	1	STUFF	UNSTUFF
Disable	0	UNSTUFF	STUFF

+V1.05S
R110 56 H_DPRSTP# ns
R112 56 H_DPSLP# ns
R114 56 H_FERR#
R117 56 PM_THRMTRIP#

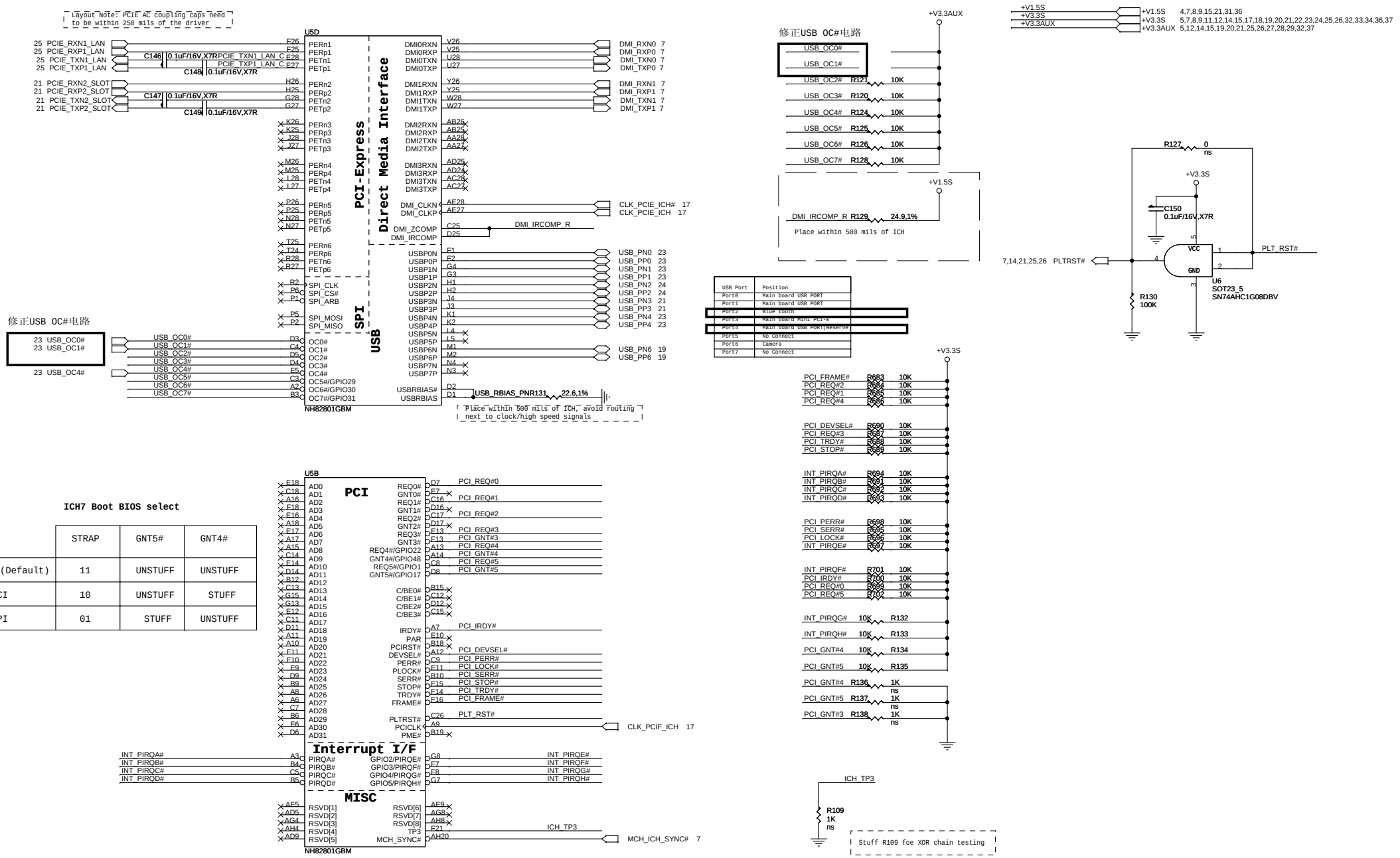
H_DPRSTP# should be routed as "Daisy chain" CMOS topology, routed from ICH to IMVP to CPU in this order exactly

+V3.3S
R113 10K H_RCIN#
R115 10K CPU_A20GATE-
R118 1K ACZ_SDATAOUT_R ns
R119 1K FWH_INIT# ns
R416 10K LDRQ0#
R417 10K LDRQ1#
R562 4.7K IORDY
R430 10K IDEREQ

R118 strap functionality based on ICH_TP3 strap:
XOR chain entrance(ICH_TP3 pulled low)
PCIE port config bit 1(ICH_TP3 not pulled low)

CZC Technology

Title: ICH7M IDE/SATA/LPC/RTC/AUDIO
Size: Custom | Project Name: J7 | Rev: C
Date: Monday, April 27, 2009 | Sheet 12 of 43

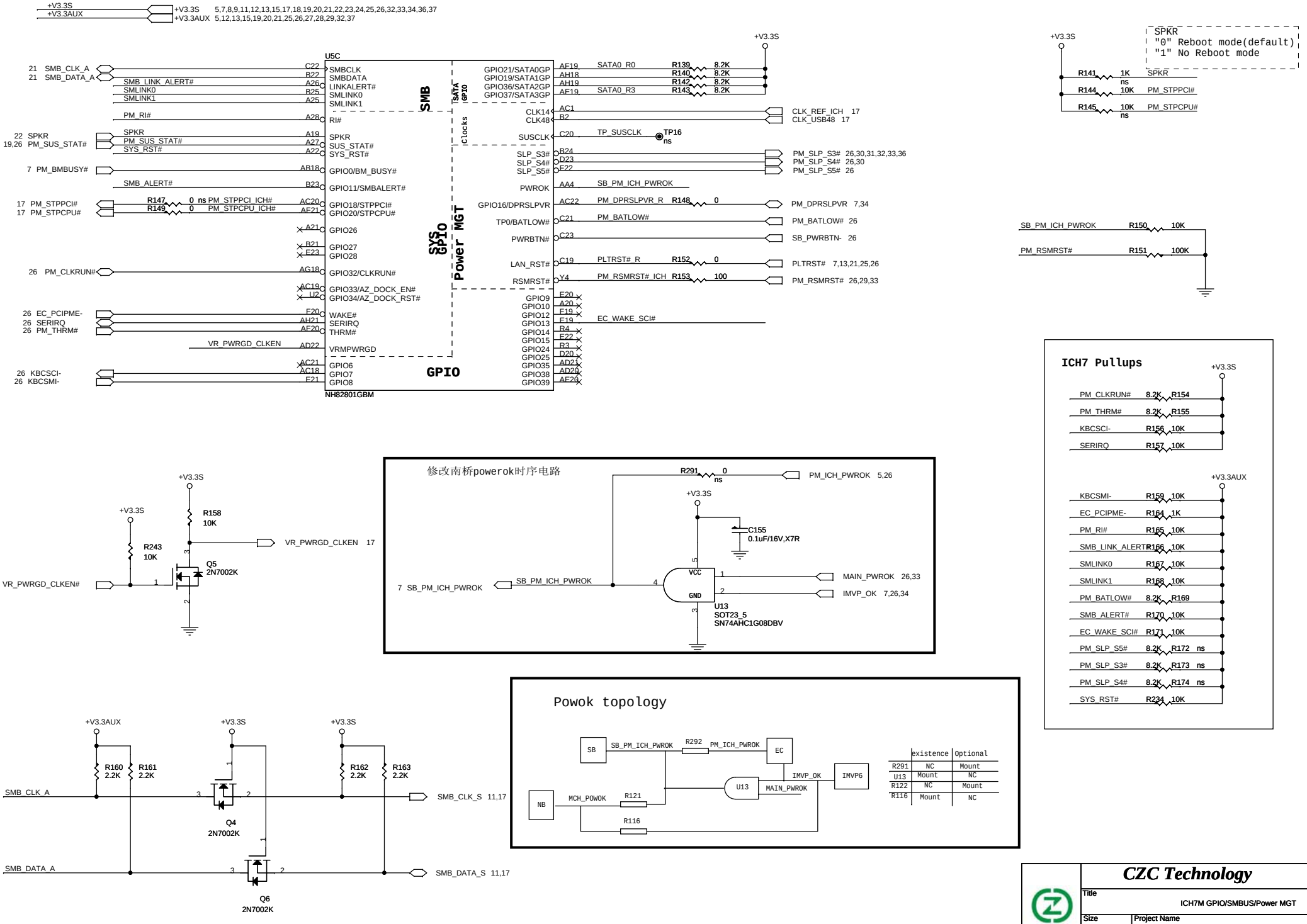


	STRAP	GNT5#	GNT4#
LPC(Default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

USB Port	Position
Port0	Main board USB PORT
Port1	Main board USB PORT
Port2	Blue tooth
Port3	Main board Mini PCI-E
Port4	Main board USB PORT(Reserve)
Port5	No Connect
Port6	Camera
Port7	No Connect

Title	ICH7M PCI-E/PCI/DMI/USB
Size	Custom
Project Name	J7
Rev	C
Date:	Monday, April 27, 2009
Sheet	13 of 43

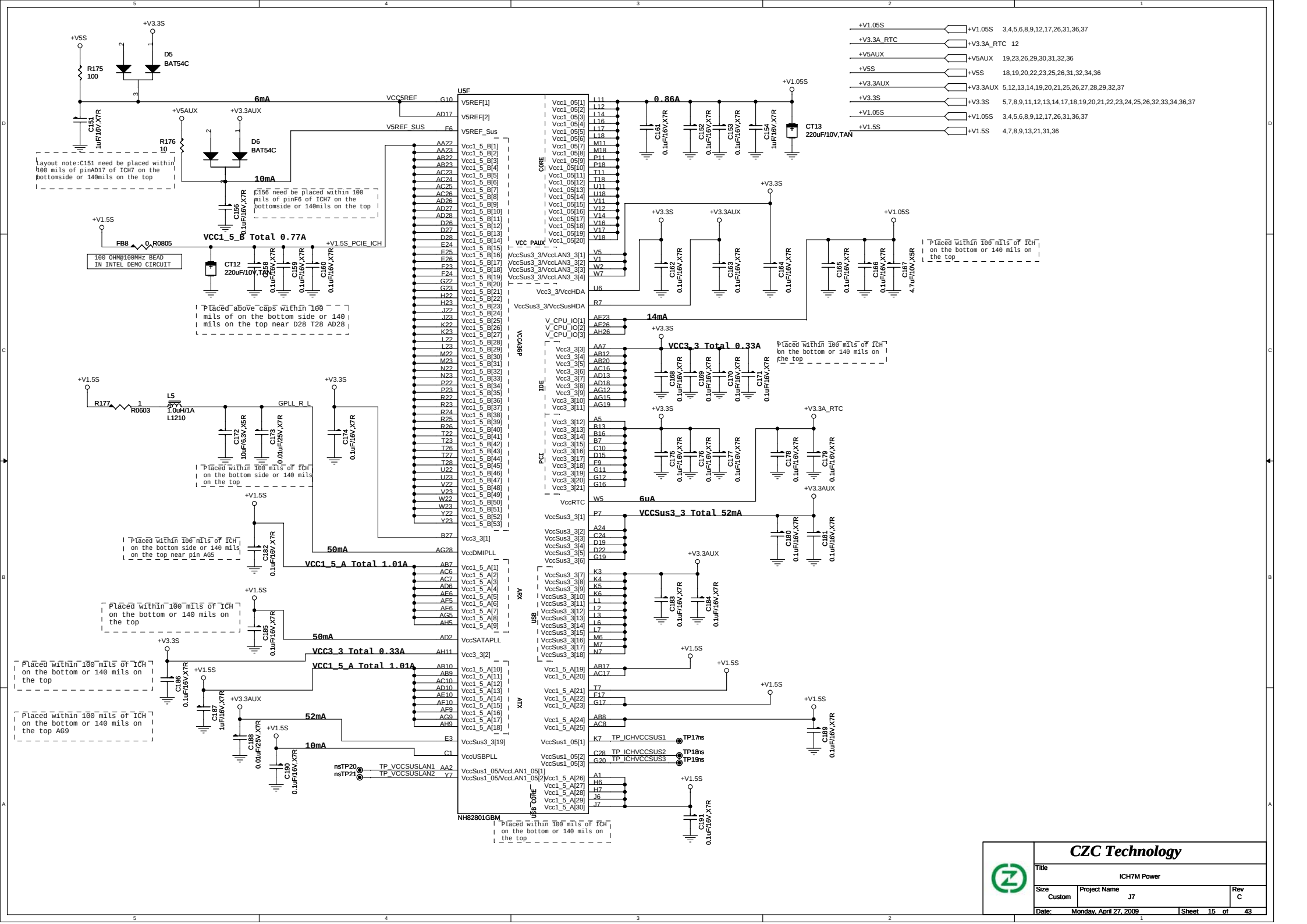
CZC Technology



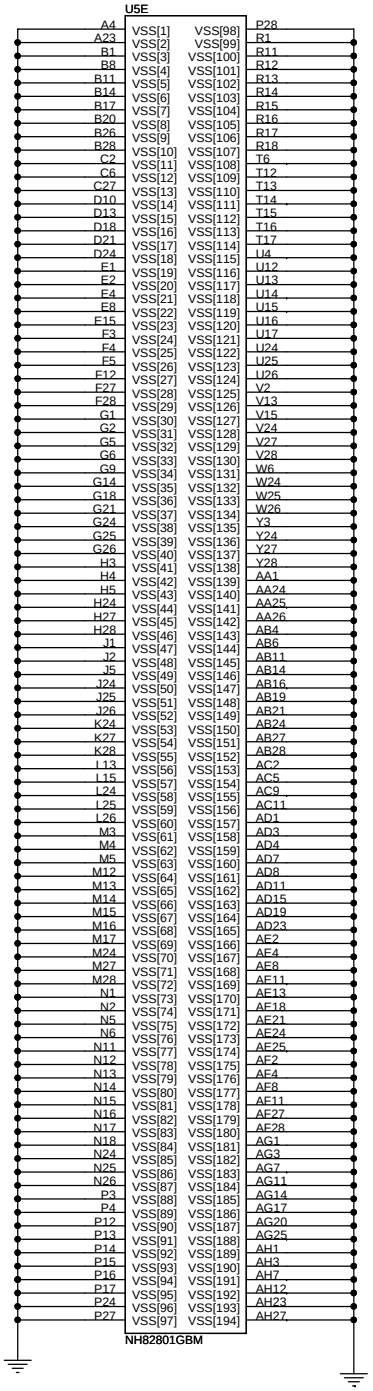
	existence	Optional
R291	NC	Mount
U13	Mount	NC
R122	NC	Mount
R116	Mount	NC

CZC Technology

Title	ICH7M GPIO/SMBUS/Power MGT	
Size A3	Project Name J7	Rev C
Date: Monday, April 27, 2009	Sheet 14 of 43	

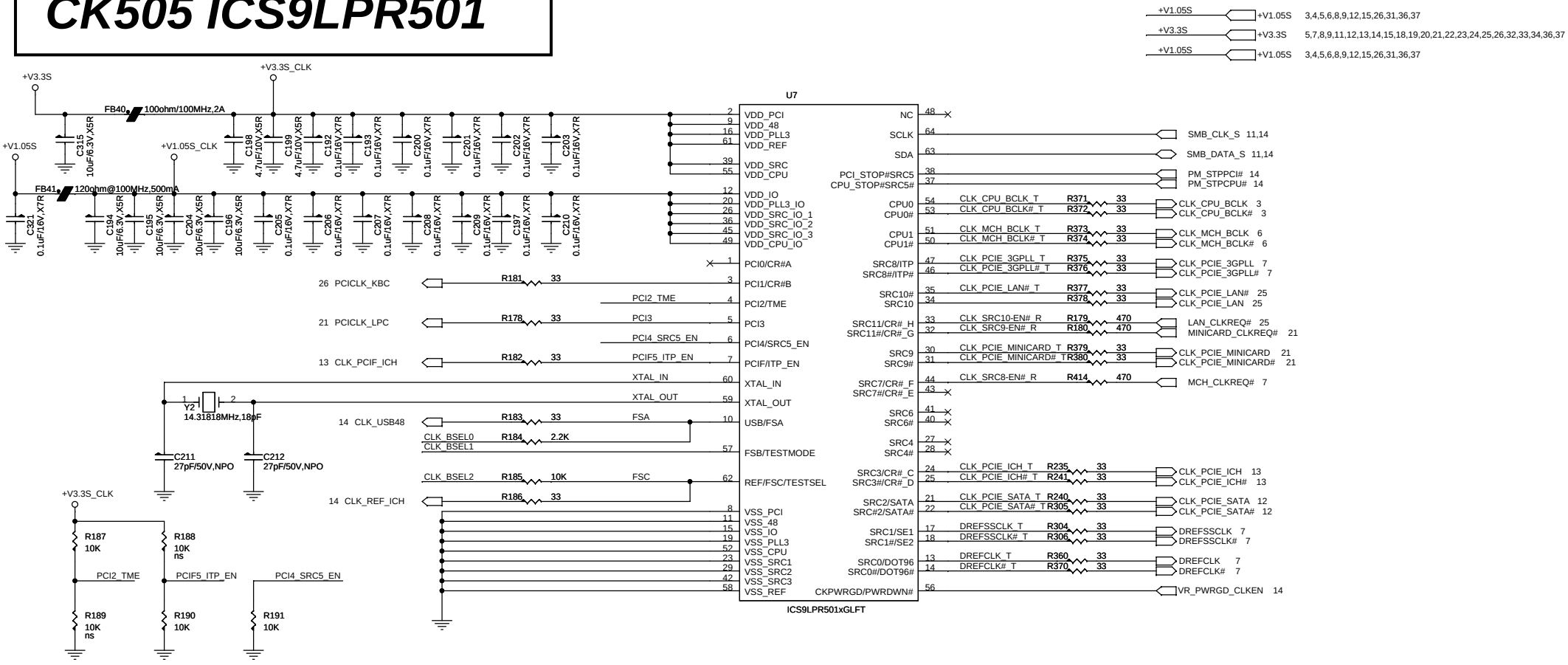


CZC Technology			
Title: ICH7M Power			
Size: Custom	Project Name: J7		Rev: C
Date: Monday, April 27, 2009		Sheet 15 of 43	

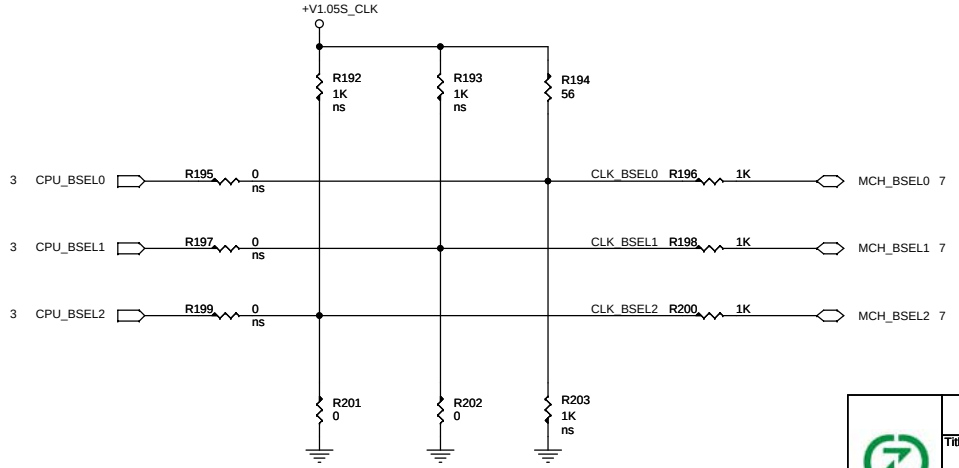


CZC Technology		
Title: ICH7M GND		
Size: A3	Project Name: J7	Rev: C
Date: Monday, April 27, 2009	Sheet 16 of 43	

CK505 ICS9LPR501

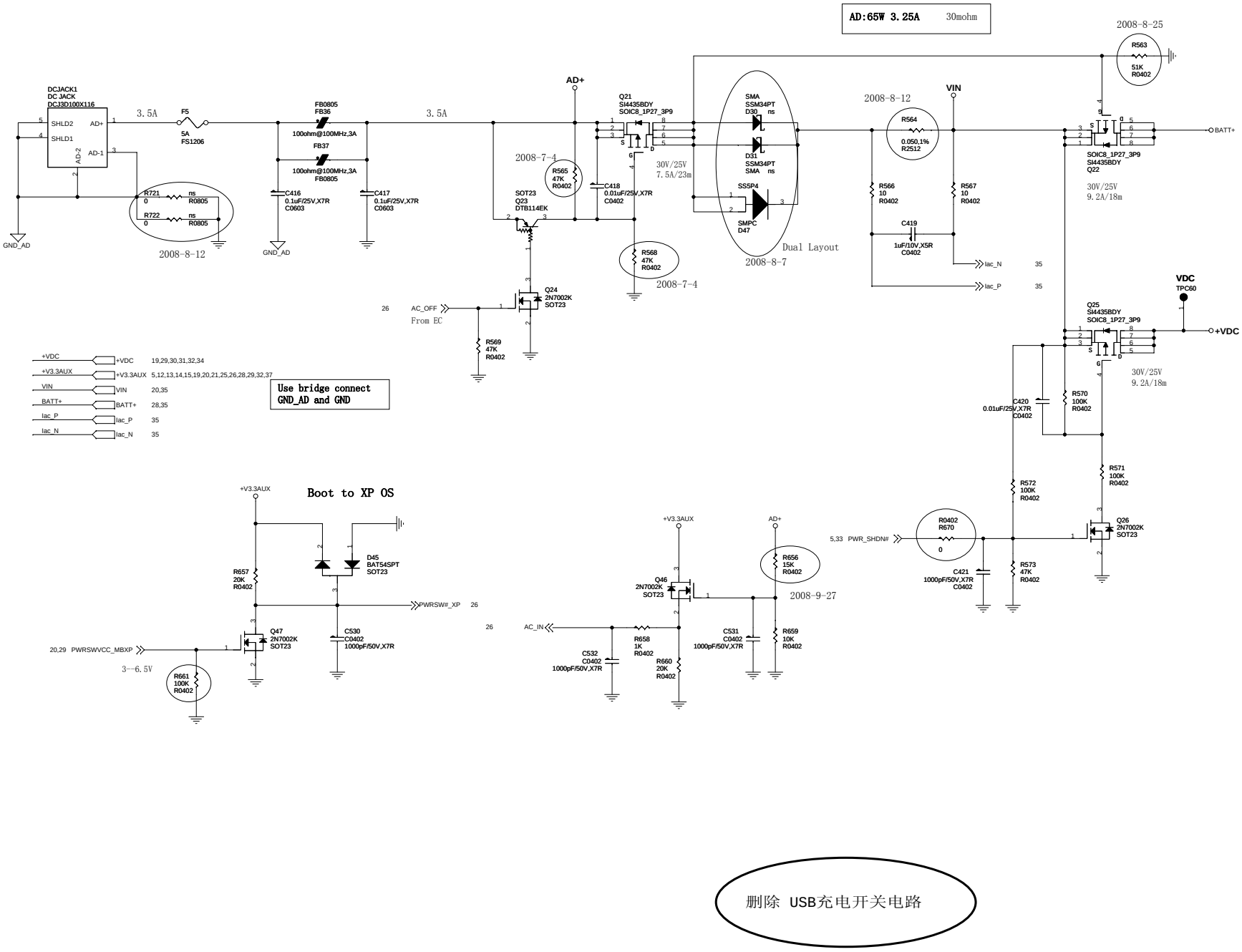


FSC BSEL2	FSA BSEL1	FSA BSEL0	Host Clock frequency MHz
1	0	1	100
0	0	1	133
0	1	1	166
0	1	0	200
0	0	0	266
1	0	0	333
1	1	0	400
1	1	1	Reserved



CZC Technology

Title: CK505		
Size: A3	Project Name: J7	Rev: C
Date: Monday, April 27, 2009	Sheet 17 of 43	


AD:65W 3.25A 30mohm
2008-8-25
DCJACK1
DC JACK
DCJ3D100X116
SHLD2
SHLD1
AD+
AD-2
AD-1
3.5A
F5
5A
FS1206
FB0805
FB36
100ohm@100MHz,3A
FB37
100ohm@100MHz,3A
FB0805
C416
0.1uF/25V,X7R
C0603
C417
0.1uF/25V,X7R
C0603
R721
0
ns
R0805
R722
0
ns
R0805
GND_AD
2008-8-12
AD+
Q21
Si4435BDY
SOIC8_1P27_3P9
SMA
SSM34PT
D30 ns
D31
SSM34PT
SMA ns
SS5P4
SMPC
D47
30V/25V
7.5A/23m
Dual Layout
2008-8-7
R565
47K
R0402
2008-7-4
SOT23
Q23
DTB114EK
C418
0.01uF/25V,X7R
C0402
R568
47K
R0402
2008-7-4
Q24
2N7002K
SOT23
26
AC_OFF
From EC
R569
47K
R0402
2008-8-12
VIN
R564
0.050,1%
R2512
R566
10
R0402
R567
10
R0402
C419
1uF/10V,X5R
C0402
Iac_N
35
Iac_P
35
R563
51K
R0402
SOIC8_1P27_3P9
Si4435BDY
Q22
BATT+
30V/25V
9.2A/18m
VDC
TPC60
Q25
Si4435BDY
SOIC8_1P27_3P9
+VDC
30V/25V
9.2A/18m
C420
0.01uF/25V,X7R
C0402
R570
100K
R0402
R571
100K
R0402
R572
100K
R0402
R0402
R670
0
5,33 PWR_SHDN#
Q26
2N7002K
SOT23
C421
1000pF/50V,X7R
C0402
R573
47K
R0402
+VDC +VDC 19,29,30,31,32,34
+V3.3AUX +V3.3AUX 5,12,13,14,15,19,20,21,25,26,28,29,32,37
VIN VIN 20,35
BATT+ BATT+ 28,35
Iac_P Iac_P 35
Iac_N Iac_N 35
Use bridge connect
GND_AD and GND
Boot to XP OS
+V3.3AUX
D45
BAT54SPT
SOT23
R657
20K
R0402
PWRSW#_XP
26
Q47
2N7002K
SOT23
C530
C0402
1000pF/50V,X7R
20,29 PWRSWVCC_MBXP
3--6.5V
R661
100K
R0402
+V3.3AUX
AD+
Q46
2N7002K
SOT23
R656
15K
R0402
2008-9-27
AC_IN
26
R658
1K
R0402
R660
20K
R0402
C532
C0402
1000pF/50V,X7R
C531
C0402
1000pF/50V,X7R
R659
10K
R0402
删除 USB充电开关电路
CZC 创智成
Anfeng
Title
Adapter In
Size
C
Document Number
J7
Rev
C
Date:
Monday, April 27, 2009
Sheet
27
of
43
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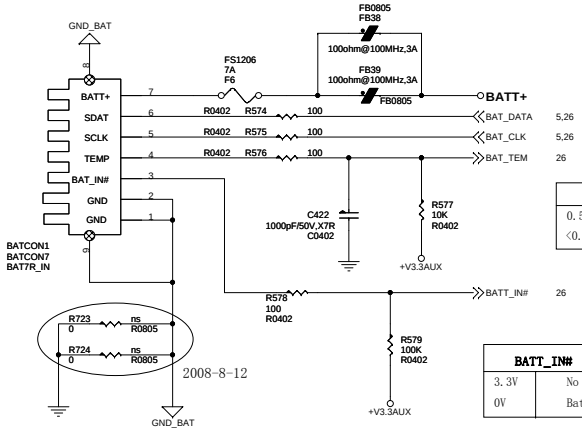
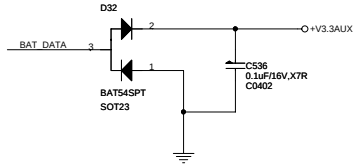
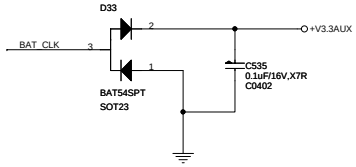


BAT_TEM	
0.5-3.0V	Battery OK
<0.5V or >3.0V	Battery Fail

BATT_IN#	
3.3V	No Battery
0V	Battery In





修改Batcon1的footprint为BAT7R_IN

BATT+ BATT+ 27,35

+V3.3AUX +V3.3AUX 5,12,13,14,15,19,20,21,25,26,27,29,32,37

RTC MF52 D 103 F 3950		
Temperature	Voltage	RT
-15	3.0	74.18K
70	0.5	1.740K

Use bridge connect
GND_AD and GND

Del CPU Power Debug Circuit

2008-9-28

CPU Core Debug

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vout
0	0	1	1	0	0	0	1.2000V
0	1	1	0	0	0	0	0.9000V

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Title: Battery In

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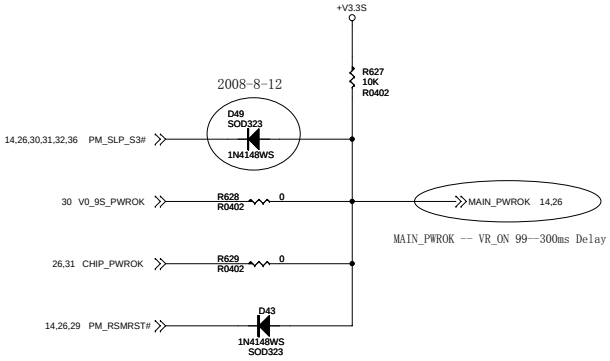

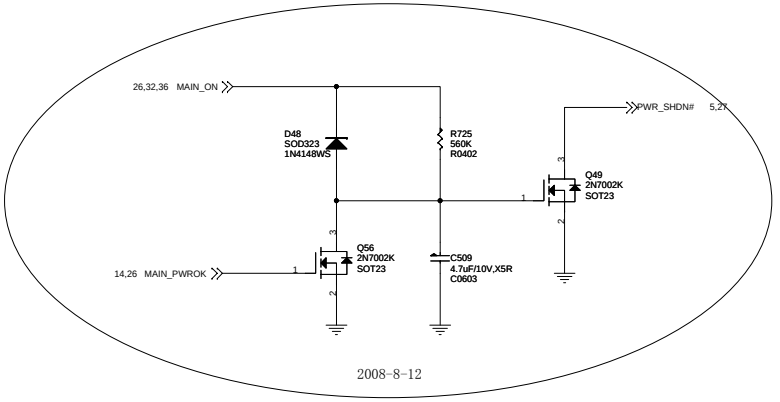

+V3.3S +V3.3S 5,7,8,9,11,12,13,14,15,17,18,19,20,21,22,23,24,25,26,32,34,36,37

CZC 创智成	Anfeng	
Title: Power Good Logic		
Size: C	Document Number: J7	Rev: C
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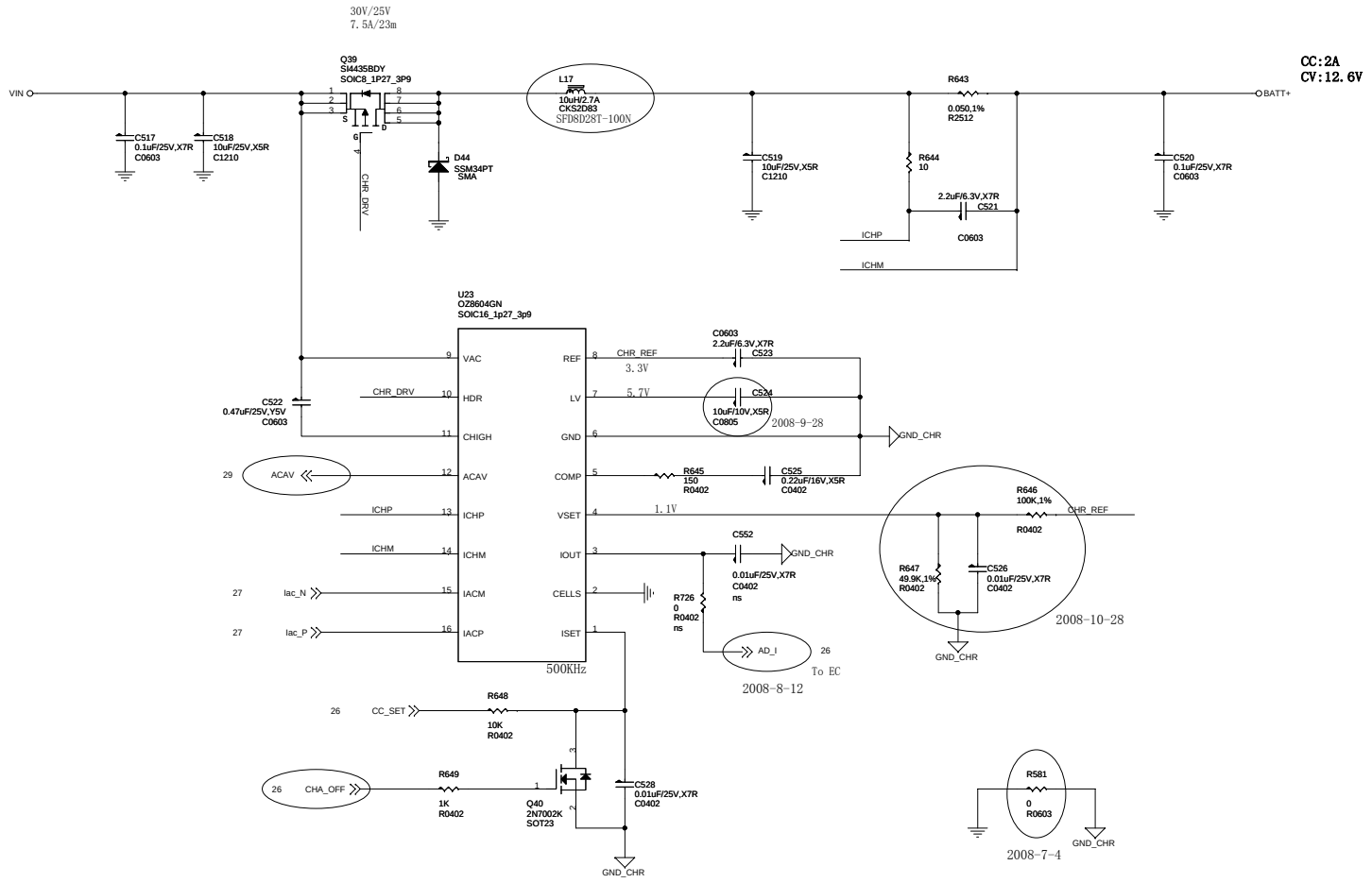

CC_SET	Charge Current
3.0V	2.0A
1.5V	1.0A
0.45V	300mA
<0.15V	=CHA_OFF

BATT+ — BATT+ 27,28

VIN — VIN 20,27

CZC 创智成 Anfeng

Title: Charger

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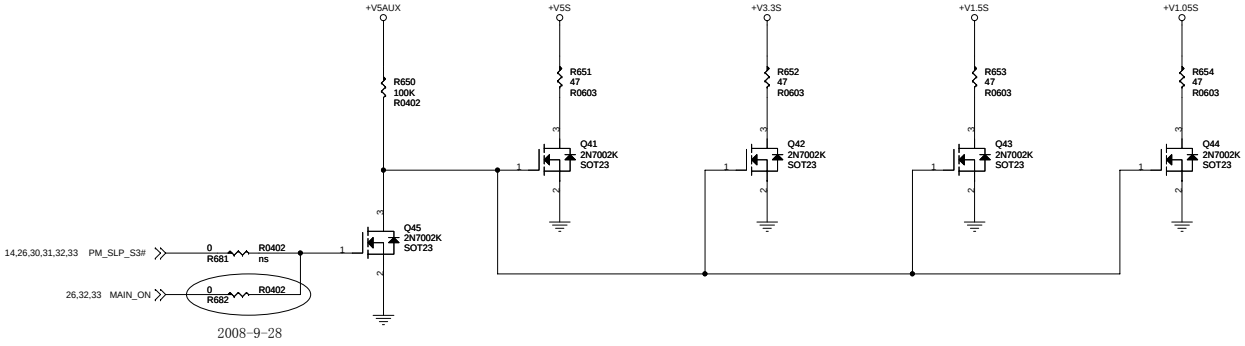
+V3.3S
+V5S
+V3.3S 5,7,8,9,11,12,13,14,15,17,18,19,20,21,22,23,24,25,26,32,33,34,37
+V5S 15,18,19,20,22,23,25,26,31,32,34

+V5AUX
+V1.05S
+V1.5S
+V5AUX 15,19,23,26,29,30,31,32
+V1.05S 3,4,5,6,8,9,12,15,17,26,31,37
+V1.5S 4,7,8,9,13,15,21,31



2008-9-28

CZC 创智成 Anfeng

Title
Discharge Circuit

Size	Document Number	Rev
C	J7	C

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H_CPU2
BOSSC237PT276D118
mh24x40x50

H_CPU3
BOSSC237PT276D118
MH38X60

+V1.05S
C61
0.1uF/16V,X7R

FD1 FD2 FD3 FD4 FD5 FD6 FD7 FD8
FMARKC ns

H_S1 H_S2 H_S3 H_S4
BOSSC237PT276D118
MH30X55X70 / mh24x40x50

E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17
EMI ns

H_S6 H_S7 H_S8 H_S5 H_S11
BOSSC237PT276D118
MH30X55X70 / mh24x40x50

USB_GND2

E18 E19 E20 E21 E22 E23 E24 E25 E26
EMI ns

GND_CRT USB_GND2 GND_AUD

H_S9 H_S10
BOSSC237PT276D118
MH30X55X70 / mh24x40x50

+V3.3AUX
C539
0.1uF/16V,X7R

+V3.3AUX
C534 C414 C412 C409 C506
0.1uF/16V,X7R

+V3.3S
C533 C504 C408
0.1uF/16V,X7R

For EMI

For EMI

+V1.05S +V1.05S 3,4,5,6,8,9,12,15,17,26,31,36

+V3.3AUX +V3.3AUX 5,12,13,14,15,19,20,21,25,26,27,28,29,32

+V3.3S +V3.3S 5,7,8,9,11,12,13,14,15,17,18,19,20,21,22,23,24,25,26,32,33,34,36

+VDC +VDC 19,27,29,30,31,32,34

CZC Technology		
Title: SCREW HOLE		
Size: Custom	Project Name: J7	Rev: C
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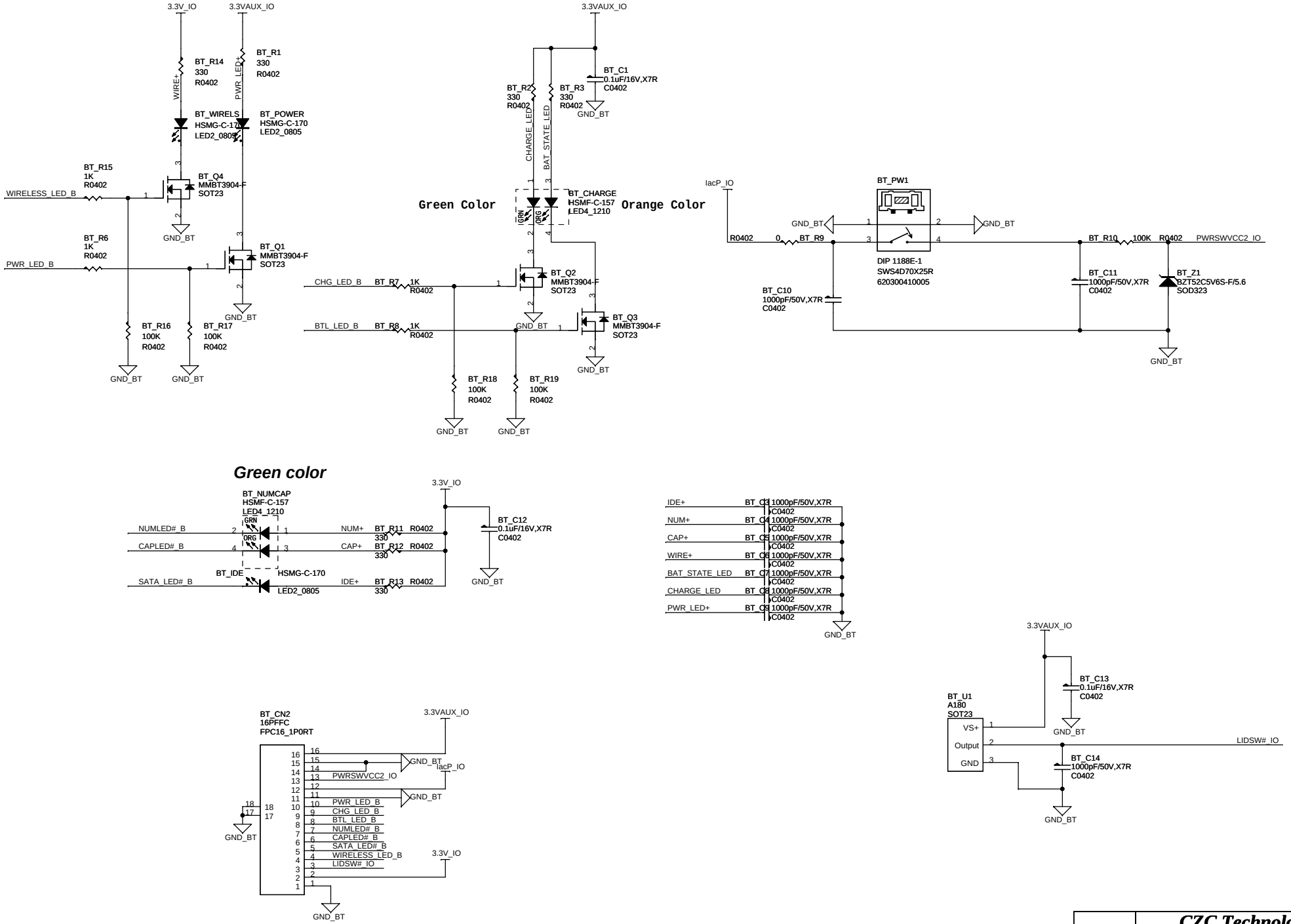

CZC Technology		Jack Ouyang
Title	Button BOARD	
Size A3	Project Name J7	Rev C
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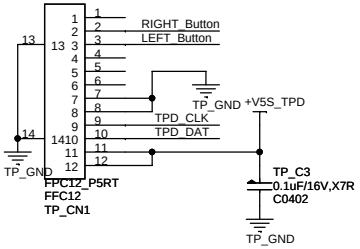
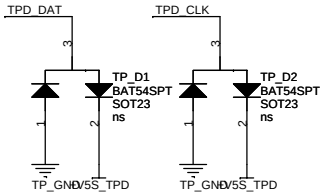
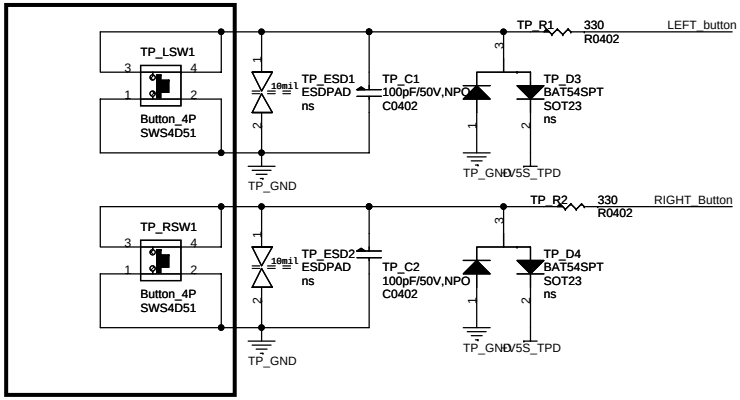
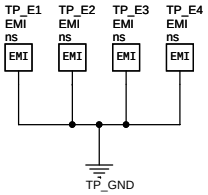
Synaptics : TM-00450-001

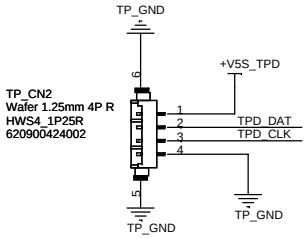




Ver.C 修改按键封装！ （090327）







CZC Technology		Jack Ouyang
Title: HDD_BAT IOBOARD		
Size: A3	Project Name: J7	Rev: C
Date: Monday, April 27, 2009	Sheet 39 of 43	