QN8000

Single-Chip Low-Power FM Transmitter for Portable Devices

General Description

The QN8000 is a high performance single-chip stereo FM transmitter designed for low-power portable audio & multimedia devices, cell phones, GPS personal navigation devices, and automotive accessories.

The QN8000 integrates complete transmitter function, from stereo audio input to RF antenna port, for worldwide FM band personal area broadcast. It includes variable input gain programming, selectable pre-emphasis, precision low-spur MPX stereo encoding & pilot tone generation, low-noise PLL-based modulation, and an on-chip power amplifier with variable output level and RF band-pass filtering to ensure optimum transmit spectrum purity.

Integrated crystal oscillator and on-chip digital calibration circuits eliminate external tuning components and enable tuning-free manufacturing. Support for 7.6 MHz reference clock and crystals ensure high audio performance. Integrated saturation detection and programmable audio interface eliminate distortion, optimize audio fidelity, and support wide range of input audio levels. Low power idle mode extends battery life. Integrated LDO enables direct connect to battery and provides high PSRR for superior noise suppression, in particular TDMA noise from GSM/GPRS phones.

The QN8000 can be operated continuously from 76MHz to 108MHz, supporting North America, Europe, Asia, and Japan FM broadcast bands.

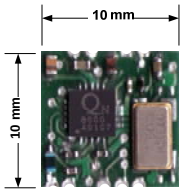
2 and 3-wire serial interfaces provide simple access to all programmable functions. A parallel (static GPIO) control interface is also available for simplified operation without an MCU.

Designed for FCC Part 15.239 & other standards compliant unlicensed FM band operations, the QN8000 is fabricated in high reliability CMOS and features very low current consumption which extends battery life.

Features

- **Worldwide FM band support (76~108MHz)**
  - *Fully Integrated PLL synthesizer*
  - *No external VCO required*
  - *Continuous 100kHz channel selection*
  - *Fast power-up & channel switching*
- **High audio fidelity**
  - *65dB Stereo SNR, less than 0.2% THD*
  - *Fully integrated programmable 50 & 75μs pre-emphasis (no external capacitor required)*
- **Small footprint** (*4x4 mm x 0.85 mm QFN20)*
  - *Low external component count (8 passives)*
  - *Standalone 7.6MHz crystal support, no tuning capacitors required*
- **Very low power consumption**
  - *14mA Typical (Transmit Mode)*
  - *1.2mA (Idle Mode), 1μA (Sleep)*
- **Integrated power amplifier**
  - *On-chip BPF for best spectral performance*
  - *Precision output power control*
- **Programmable audio interface**
  - *On-chip adjustable input buffer amplifiers*
  - *Integrated Input Saturation Detection*
- **Flexible control interface**
  - *2 and 3-wire serial, and parallel (static GPIO)*
- **Robust operation**
  - *-25^{0}C to +85^{0}C operation*
  - *ESD protection on all Input and Output pads*
- **ROHS compliant, Pb-free**
- **Moisture Sensitivity Level (MSL)-1**

Typical Applications



Reference Module (footprint less than 10 x 10 mm)

- Portable Audio & Media Players
- GPS Portable Navigation Devices
- PDAs, Cell Phones
- Automotive and Accessories

CONTENTS

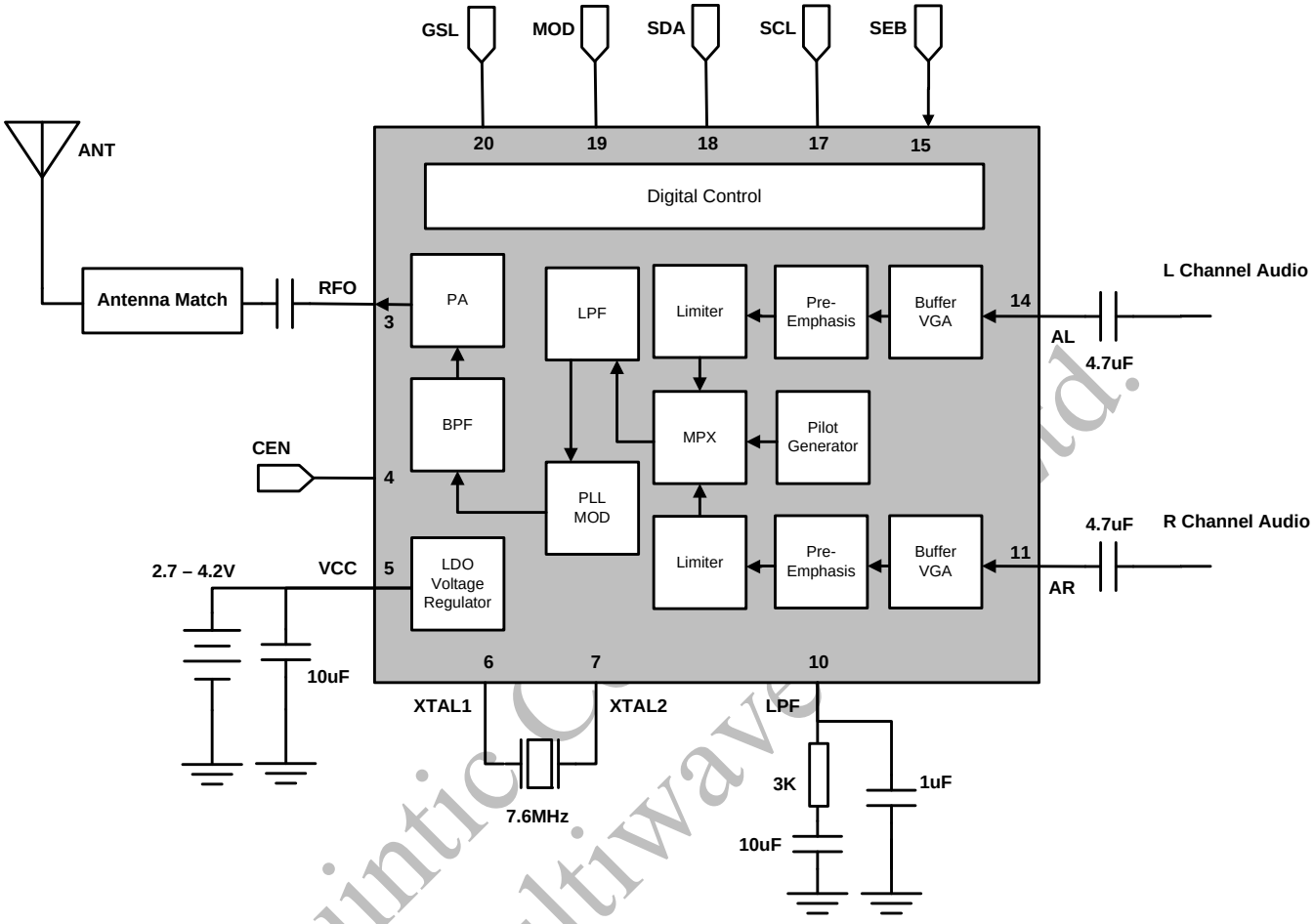
NOTE: This specification applies to production versions of the chip, beginning with A2.

Users are responsible for compliance with local regulatory requirements for low power unlicensed FM broadcast operation. Quintic is not responsible for any violations resulting from user's intentional or unintentional breach of regulatory requirements in personal or commercial use.

REVISION HISTORY

REVISION	CHANGE DESCRIPTION	DATE	APPROVAL
1.0	Production Document	24/8/2007	TN

1. FUNCTIONAL BLOCK DIAGRAM



2. PIN ASSIGNMENT

(Top View)

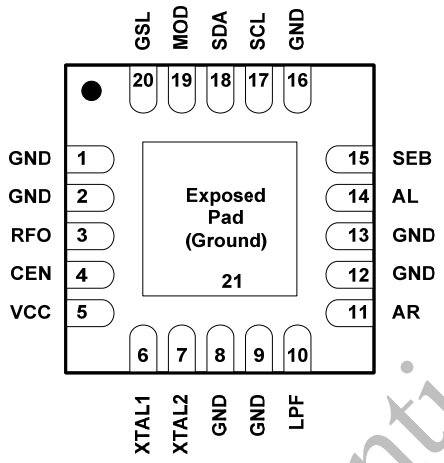


Table 1 Pin Descriptions

PINS	NAME	DESCRIPTION
1	GND	Ground
2	GND	Ground
3	RFO	Transmitter RF output. Connect to matched antenna (refer to Application Notes)
4	CEN	Chip enable pin; >2.0V powers up the chip, < 0.2V powers down the chip.
5	VCC	Voltage Supply. Can connect directly to Li-Ion or other battery (2.7V to 4.2V)
6	XTAL1	On-chip crystal driver port 1. If using a 7.6MHz clock source, connect this pin to ground.
7	XTAL2	On-chip crystal driver port 2. If using a 7.6MHz clock source, connect this pin to the clock source.
8	GND	Ground
9	GND	Ground
10	LPF	Loop filter pin for on-chip PLL.
11	AR	Audio right channel input.
12	GND	Audio Ground
13	GND	Audio Ground
14	AL	Audio left channel input.
15	SEB	Bus enable pin if 3-wire serial used; will be address select pin if 2-wire serial used, SEB low use default address, SEB high use register controlled address.
16	GND	Ground
17	SCL	Clock for 2-wire or 3-wire serial bus.
18	SDA	Bi-directional data line for 2-wire or 3-wire serial bus.
19	MOD	Bus mode, 'high' = 3 wire serial operation. 'low' = 2 wire serial operation.
20	GSL	Parallel (static-GPIO) interface selection pin, 'high' = parallel interface.
21	PAD	Exposed pad, must be soldered to the ground on the PCB.

3. ELECTRICAL SPECIFICATIONS

Table 2 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
Vcc	Supply voltage	VCC to GND	-0.3	5	V
Va	Analog signals	XTAL1, XTAL2, LPF, AR, AL to GND	-0.3	Vcc+0.3	V
V_{IO}	Logic signals	CEN, SEB, SCL, SDA, MOD, GSL to GND	-0.3	Vcc + 0.3	V
T_A	Operation temperature		-40	+105	°C
T_s	Storage temperature		-55	+150	°C
ESD	Human body model	EIA/JESD22-A114-B MIL-STD-883E M3015	2000		V
	Machine Model	EIA/JESD22-A115-A MIL-STD-883E M3015	200		V
	Charged Device Model	EIA/JESD22-101 MIL-STD-883E M3015	800		V
MSL	Moisture Sensitivity Level	IPC/JEDEC J-STD-20		1	

Table 3 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Vcc	Supply voltage	VCC to GND	2.7	3.0	4.2	V
T_A	Operating temperature		-25		+85	°C
V_{ain}	L/R channel input signal level	Single ended peak to peak voltage	150	1000	2800	mV

Table 4 DC Characteristics

(Vcc = 2.7 ~ 3.6 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.0V and T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_C	Supply current	TX mode		14		mA
		Idle mode [1]		4		mA
		Standby mode [2]		1.2		mA
		Power down [3]		1	10	μA
V_{IH} [4]	High level input voltage		2.0			V
V_{IL} [4]	Low level input voltage				0.8	V
V_{OH} [5]	High level output voltage		0.9*Vcc			V
V_{OL} [5]	Low level output voltage				0.1*Vcc	V

Notes:

1. Audio input buffer, PLL, crystal oscillator, bias circuit and interface is power on, the rest of the circuit is power down.
2. STNBY = 1, only crystal oscillator, bias circuit and interface is power on, the rest of the circuit is off
3. CEN = low, leakage current, max is high temperature
4. At pin CEN, SEB, SCL, MOD and GSL
5. At pin SDA

Table 5 AC Characteristics

(Vcc = 2.7 ~ 3.6 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.0V and T_A = 25°C)

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
R_i	Input audio impedance	At pin AL and AR	5		40	KΩ
C_i	Input audio capacitance[2]	At pin AL and AR		2	5	pF
Gv	Input audio VGA gain	RIN[1:0] = 01	-6		15	dB
ΔGv	Audio VGA gain step	For any gain setting	2	3	4	dB
τ_{emph}	Pre-emphasis time constant[2]	PETC = 1	71.3	75	78.7	μs
		PETC = 0	47.5	50	52.5	
SNR_{audio}	Audio SNR [4]	MONO, Δf = 22.5KHz	65	69		dB
		STEREO, Δf = 67.5KHz, Δf_{pilot} = 6.75KHz	65	69		
THD_{audio}	Audio THD [4]	STEREO, Δf = 67.5KHz, Δf_{pilot} = 6.75KHz		0.1	0.2	%
S_{LR}	L/R separation [3,4]		40			dB
B_{LR}	L/R Channel imbalance [3,4]	L and R channel gain imbalance at 1KHz offset from DC			1	dB
M_{pilot}	Pilot modulation [1,3]	Relative to peak modulation	8	9	10	%
Sup_{sub}	38KHz sub-carrier [3,4] suppression		40			dB
P_{out}	RF output voltage swing[5]	RF Channel frequency = 88MHz	97		117	dBμV
ΔG_p	Power gain step	Over process, temperature	4	5	6	dB
ΔG_{perrf}	Power gain flatness	Over 76MHz ~ 108 MHz	-2		2	dB
P_{mask}	RF output spectrum mask[6]	120KHz to 240KHz offset		-35	-30	dBc
		240KHz to 600KHz offset		-40	-35	
		>600KHz offset			-45	
F_{rf}	RF channel frequency		76		108	MHz
F_{ch}	Channel frequency step			100		KHz
F_{err}	Channel center frequency accuracy		-2		2	KHz
F_{perr}	Pilot tone frequency accuracy[2]		-2		2	Hz

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
F_{pk}	Modulation peak frequency deviation	STEREO		75		KHz
		MONO		22.5		
F_{xtal}	Crystal frequency			7.6		MHz
F_{xtal_err}	Crystal frequency accuracy	Over temperature, and aging	-20		20	ppm

Notes:
1. 500mV rms 1KHz tone at AL pin, no input signal at AR pin
2. Guaranteed by design
3. Stereo (MONO = 0)
4. 450mV rms 1KHz tone at AL pin, no input signal at AR pin
5. Into matched antenna (see Application Note for details)
6. Within operating band 76MHz to 108MHz

Table 6 Timing Characteristics

(Vcc = 2.7 ~ 3.6 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.0V and T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
τ_{pup}	Chip power up time	From rising edge of CEN to PLL settle and transmitter ready for transmission			0.6	Sec
τ_{astby}	Auto standby time [2]	TMOUT [1:0] = 00		1		Min
		TMOUT [1:0] = 01		3		
		TMOUT [1:0] = 10		5		
		TMOUT [1:0] = 11		Never		
τ_{chsw}	Channel switching time[1]	From any channel to any channel			0.1	Sec
τ_{wkup}	Wake up time from standby to transmit				0.2	Sec

Notes:
1. Guaranteed by design
2. Chip automatic goes from idle to standby mode; TMOUT = 11 equivalent to auto standby disabled

Table 7 2-Wire Interface Timing Characteristics

(Vcc = 2.7 ~ 3.6 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.0V and T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	2 wire clock frequency				400	KHz
t_{LOW}	Clock low time		1.3			µs
t_{HI}	Clock high time		0.6			µs
t_{ST}	SCL input to SDA falling edge start [1,3]		0.6			µs
t_{STHD}	SDA falling edge to SCL falling edge start[3]		0.6			µs
t_{rc}	SCL rising edge[3]	Level from 30% to 70%			300	ns
t_{fc}	SCL falling edge[3]	Level from 70% to 30%			300	ns
t_{dtHD}	SCL falling edge to next SDA rising edge[3]		100			ns
t_{dtc}	SDA rising edge to next SCL rising edge[3]				900	ns
t_{stp}	SCL rising edge to SDA rising edge [2,3]		0.6			µs
t_w	Duration before restart[3]		1.3			µs
C_b	SCL, SDA capacitive loading[3]			10		pF

Notes:
1. Start signaling of 2-wire interface
2. Stop signaling of 2-wire interface
3. Guaranteed by design

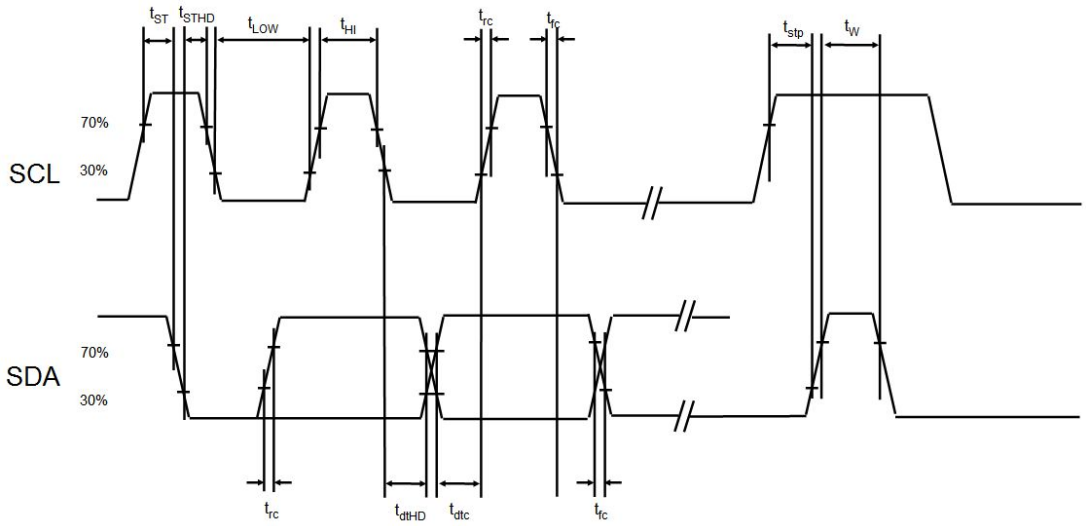


Figure 1 2-Wire Serial Control Interface Timing Diagram

Table 8 3-Wire Interface Timing Characteristics

(Vcc = 2.7 ~ 3.6 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.0V and T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK}	bus clock frequency				2.5	MHz
t_{HI}	SCL high time		25			ns
t_{LOW}	SCL low time		25			ns
ts	SEB and SDA falling edge to clock rising edge[1]		20			ns
t_h	Data holding time[1]		10			ns
t_{tr}	SCL rising edge to SDA output valid[1]	Only in read mode	2		25	ns
t_{ed}	SCL rising edge to SDA output high Z[1]		2		25	ns

Notes:
1. Guaranteed by design

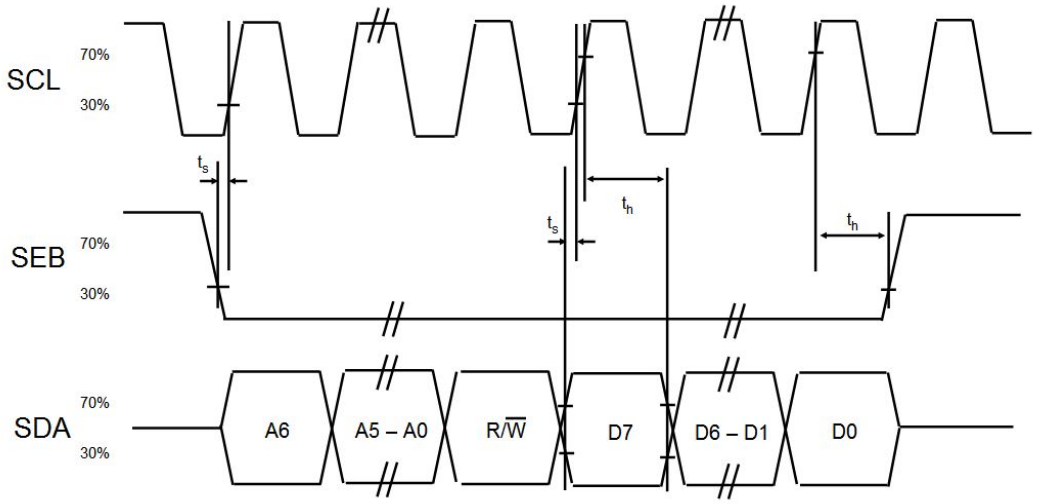


Figure 2 3-Wire Serial Control Interface Write Timing Diagram

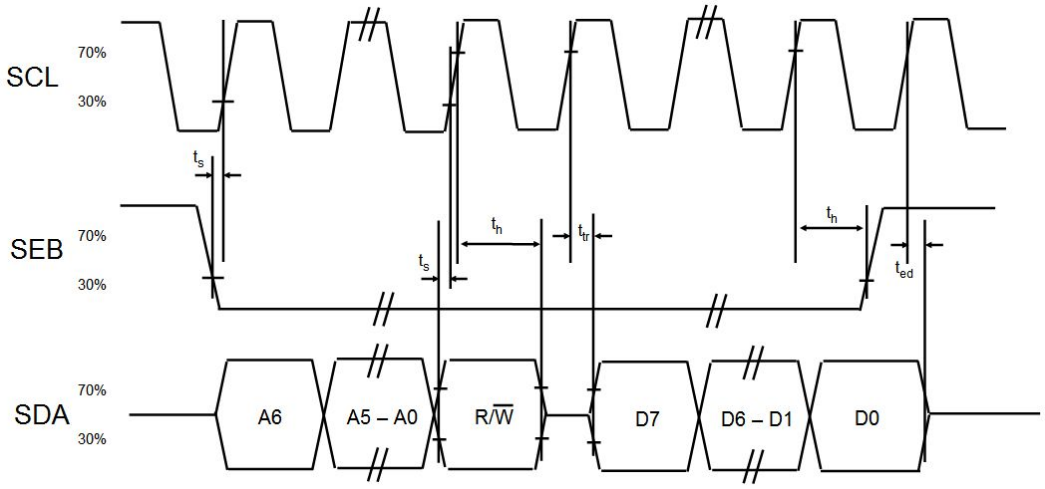


Figure 3 3-Wire Serial Control Interface Read Timing Diagram

4. FUNCTIONAL DESCRIPTION

The QN8000 is a low power, highly integrated stereo FM transmitter. It has integrated VGA, pre-emphasis, MPX encoder, pilot tone generator, PLL based modulator, power amplifier and RF BPF. Fully on chip calibration circuitry makes it tuning-free during system integration. QN8000 supports US, Europe, China and Japan FM broadcast band. It can be tuned continuously within 76MHz ~ 108MHz in 100 KHz step. QN8000 supports 2-wire, 3-wire serial and parallel (static GPIO) control interface.

AUDIO INTERFACE

QN8000 has a highly flexible single ended audio interface. The audio signal is AC coupled into chip with 3dB corner frequency less than 50Hz. It has 4 different input impedances and 21dB adjustable gain range (in 3dB step) to optimize the SNR and linearity for the input audio signal. The impedance and gain setting are controlled through control interface.

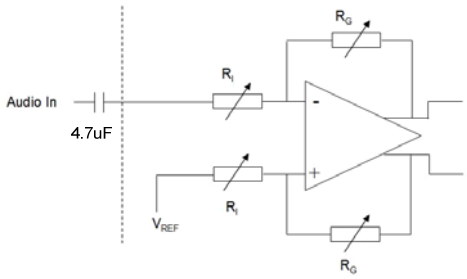


Figure 4 Audio Input Interface

The input impedance of the circuit can be calculated as

$$Z_i = R_i \times (\frac{G}{G+2} + 1)$$

Where G is the voltage gain.

PRE-EMPHASIS

QN8000 supports 2 pre-emphasis time constant, 75μs and 50μs. It is programmable through control interface. Pre-emphasis is used to enhance high frequency components of the audio signal such that at the receiver side, it will not suffer from the noise amplification due to FM demodulation. To suppress the high frequency noise, the pre-emphasis is followed by a lowpass filter.

A limiter circuit is also implemented to control the signal level. The limiter will also provide a one-bit saturation indicator signal through control interface.

MPX

Stereo signal is generated by MPX circuit. It combines the left and right channel signal in the following way:

$$m(t) = [L(t) + R(t)] + [L(t) - R(t)]\cos(2\pi ft + 2\theta_0) + \alpha\cos(\pi ft + \theta_0)$$

Here, L(t) and R(t) correspond to the audio signals on left and right channel respectively, f = 38 KHz. θ is the initial phase of pilot tone and α is the magnitude of pilot tone. In mono mode, only the L+R signal is transmitted. The 19KHz pilot tone is generated in MPX circuit which contributes 9% of peak modulation.

PLL & MODULATOR

The modulator is open loop PLL based. External loop filter is used due to narrow loop bandwidth. The modulator has a peak frequency deviation of 75KHz in stereo transmission and 22.5KHz in MONO case.

By programming channel index CH[8:0], the RF channel can be set to any frequency between 76 MHz ~ 108 MHz in 100KHz step. The channel index and RF frequency has the following relationship:

FRF = 76 + 0.1 x Channel Index

Where FRF is the RF frequency in MHz.

QN8000 has an integrated 7.6MHz crystal driver. Alternatively, QN8000 can be programmed to use an external 7.6MHz clock.

POWER AMPLIFIER

The QN8000 can deliver up to 117 dBμV output power to an external antenna and/or matching network. A RF VGA provides 20 dB output power control range in 5dB steps, which can be programmed through the serial control interface. An integrated RF bandpass filter ensures optimal output spectrum purity.

5. CONTROL INTERFACE PROTOCOL

The QN8000 supports 2-wire, 3-wire serial interfaces, as well as simple 4-bit parallel (static GPIO) interface which does not require an MCU. The interface selection is controlled by pin MOD and GSL. MOD pin will determine whether 2-wire or 3-wire serial interface will be used. MOD = HIGH selects 3 wire bus and LOW selects 2 wire bus. GSL is the parallel interface selection pin. GSL = HIGH selects parallel (static GPIO) interface. GSL = HIGH overrides the selection of MOD pin.

2-Wire Serial Control Interface

The 2-wire (L2) bus is a simple bi-directional bus interface. The bus requires only serial data (SDA) and serial clock (SCL) signals. The bus is 8-bit oriented. Each device is recognized with a unique address. A third line (SEB) is used to choose device address configuration. SEB = LOW selects the default address (0101011), SEB = HIGH selects register defined addressing. The L2 bus operates with a maximum frequency of 400 KHz. Data transfer to and from the QN8000 can begin when a start condition is created. This is the case if a transition from HIGH to LOW on the SDA line occurs while the SCL is HIGH. The first byte transferred represents the address of the IC plus the data direction.

A LOW LSB of this byte indicates data transmission (WRITE) while a HIGH LSB indicates data request (READ). Each data put on the SDA must be 8-bits long (Byte) and each byte sent should be acknowledged by an "ACK" bit. In case a byte is not acknowledged, the transmitter should generate a stop condition or restart the transmission. At power on all register bits are set to default value. To initialize the IC, all bytes should be transferred. If a stop condition is created before the whole transmission is completed, the remaining bytes will keep their old setting. In case a byte is not completely transferred, it will be discarded. The transfer of data bytes should be ordered from low to high, that is, the address first, then byte 1, byte 2, etc. The MSB of each byte will be send first. The IC address is 0101011. This means that the first byte to be transmitted to the QN8000 should be "56" for a WRITE operation or "57" for READ operation.

A transmission can be terminated by generating a stop condition, which is SDA transition from LOW to HIGH while SCL is HIGH.

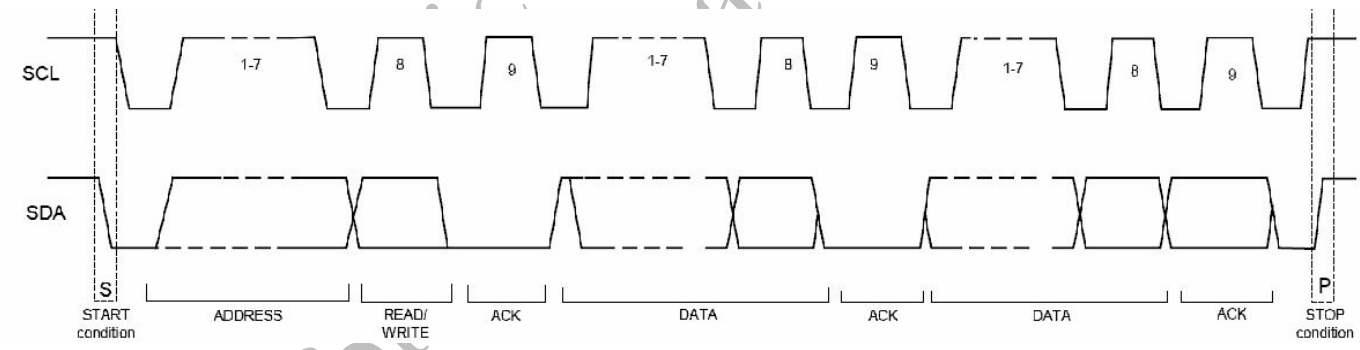


Figure 5 2-Wire Serial Control Interface Protocol

Note: A 2-wire serial write requires a block write to all register words up to and including the highest address register being accessed.

3-Wire Serial Control Interface

For 3-wire serial operation, a transfer begins when the SEB pin is set LOW on a rising SCL edge. The control word is latched internally on rising SCL edges and is 8 bits in length, comprised of a 7 bit register address A6:A0, a read/write bit (read = 1 and write = 0). The ordering of the control word is A6:A0, R/W as shown in Figure 3.

For write operations, the serial control word is followed by an 8-bit data word and is latched internally on rising SCL edges. For read operations, a bus turn-around of half a cycle is followed by an 8-bit data word shifted out on rising SCL edges. The transfer ends on the rising SCL edge after SEB is set HIGH. After the 16th data bit, a full clock with both rising and falling edge is needed to shift in the control word.

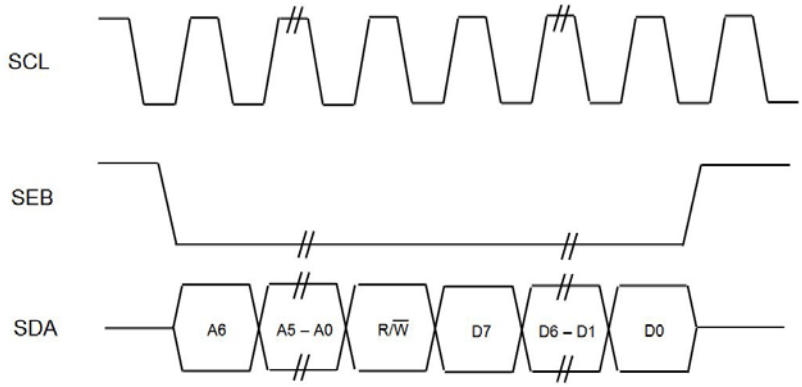


Figure 6 3-Wire Serial Control Interface Write Protocol

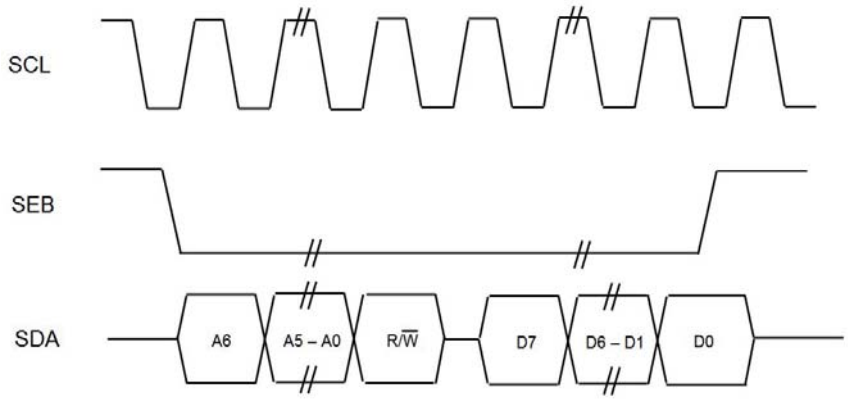


Figure 7 3-Wire Serial Control Interface Read Protocol

Parallel (static GPIO) Interface

The QN8000 also supports parallel (static GPIO) interface. If GSL = HIGH, the parallel interface will be used for control. In this mode, the MOD pin selects output power level, while SDA, SCL and SEB controls control channel and system state.

Table 9 Parallel (static GPIO) Interface Pin Function (SEB, SCL, SDA)

SEB	SCL	SDA	VALUE	COMMENT
0	0	0	Power down	Chip goes to idle mode, if within 1 min no programming, chip standby automatically
0	0	1	Channel 1	87.7 MHz
0	1	0	Channel 2	87.9 MHz
0	1	1	Channel 3	88.1 MHz
1	0	0	Channel 4	88.3 MHz
1	0	1	Channel 5	107.5 MHz
1	1	0	Channel 6	107.7 MHz
1	1	1	Channel 7	107.9 MHz

Table 10 Parallel (static GPIO) Interface Pin Function (MOD)

MOD	VALUE	COMMENT
1	High	117 dBμV max output power, with external matching network
0	Low	102 dBμV max output power, with external matching network

6. USER CONTROL REGISTERS

There are 5 user accessible control registers (00h to 03h, and 0Fh):

Table 11 User Control Registers

REGISTER	NAME	USER CONTROL FUNCTIONS
00h	SYSTEM	- Set Timeout - Transmit or Standby - Stereo or Mono
01h	CHANNEL	Sets transmit channel, 76MHz to 108MHz in 100kHz steps
02h	2WSADDR	- Select Pre-Emphasis Time Constant (50 or 75μs) - Set 2-wire serial address
03h	INBUF	- Set Transmit Output Power - Set Input Audio Gain - Set Input Audio Impedance
0Fh	XTAL	- Set crystal capacitor load - Set internal crystal oscillator current

System Control Word: 00h

Format of Word 00h: SYSTEM

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
SWRST	RECAL	TMOUT[1]	TMOUT[0]	STNBY	TXREQ	MONO	CH[8]

Description of Word 00h: SYSTEM

BIT	SYMBOL	DEFAULT	DESCRIPTION	
7	SWRST	0	Reset all registers to default values.	
			SWRST	Register values:
			0	Keep the current value.
			1	Reset to default values.
6	RECAL	0	Reset the state to initial states and recalibrate all blocks.	
			RECAL	Description:
			0	No reset. Keep the current state.
			1	Reset the state diagram. It will go through all the power up and calibration sequence.

BIT	SYMBOL	DEFAULT	DESCRIPTION	
5:4	TMOUT[1:0]	01	Time out setting for IDLE to standby state transition.	
			TMOUT[1:0]	Time out for standby (min):
			00	1
			01	3
			10	5
			11	Never
3	STNBY	0	Request immediate enter to Standby mode if the chip is in IDLE and no TXREQ is received.	
			STNBY	Modes:
			0	Non standby mode. Either idle or TX mode.
			1	Enter standby mode.
2	TXREQ	0	Transmission request.	
			TXREQ	Modes:
			0	Non TX mode. Either idle or standby.
			1	Transmit mode.
1	MONO	0	MONO or Stereo transmission.	
			MONO	Transmission mode:
			0	Stereo
			1	Mono
0	CH[8]	1	Transmitter channel index.	
			CH[8] is MSB, channel 0 is 76MHz, channel index increases monotonically with 100kHz increment each step, channel 320 corresponds to 108MHz.	

Channel Control Word

Format of Word 01h: CHANNEL

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
CH[7]	CH[6]	CH[5]	CH[4]	CH[3]	CH[2]	CH[1]	CH[0]

Description of Word 01h: CHANNEL

BIT	SYMBOL	DEFAULT	DESCRIPTION
7:0	CH[7:0]	00000000	Transmitter channel index. CH[8] is MSB. CH[0] is LSB, channel 0 is 76MHz, channel index increases monotonically with 100kHz increment each step, channel 320 corresponds to 108MHz.

2-Wire Serial Address Control Word

Format of Word 02h: 2WSADDR

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
PETC	DADD[6]	DADD[5]	DADD[4]	DADD[3]	DADD[2]	DADD[1]	DADD[0]

Description of Word 02h: 2WSADDR

BIT	SYMBOL	DEFAULT	DESCRIPTION	
7	PETC	1	Pre-emphasis time constant.	
			PETC	Pre-emphasis time constant (μs):
			0	50
			1	75
6:0	DADD[6:0]	0101011	Programmed device address when SEB=1 (if SEB=0, the default device address (0101011) is used).	
			SEB	Device address:
			0	0101011
			1	DADDR[6:0]

Input Buffer Control Word

Format of Word 03h: INBUF

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
POUT[1]	POUT[0]	RF2X	BUFG[2]	BUFG[1]	BUFG[0]	RIN[1]	RIN[0]

Description of Word 03h: INBUF

<table>
<tr><th>BIT</th><th>SYMBOL</th><th>DEFAULT</th><th colspan="6">DESCRIPTION</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">POUT[1:0]</td><td rowspan="6">11</td><td colspan="6">Transmit Power Offset from maximum (Pmax - Offset)</td></tr>
<tr><td>POUT[1:0]</td><td>RF2X</td><td colspan="3">Transmit Power Offset (dB)[1]</td></tr>
<tr><td>00</td><td>0</td><td colspan="3">-20 (min output power)</td></tr>
<tr><td>01</td><td>0</td><td colspan="3">-15</td></tr>
<tr><td>10</td><td>0</td><td colspan="3">-10</td></tr>
<tr><td>11</td><td>0</td><td colspan="3">-5</td></tr>
<tr><td>5</td><td>RF2X</td><td>1</td><td>XX</td><td>1</td><td colspan="3">0 (max output power)</td></tr>
<tr><td rowspan="11">4:2</td><td rowspan="11">BUFG[2:0]</td><td rowspan="11">011</td><td colspan="6">Input Buffer gain setting (dB), applied on both L/R channels:</td></tr>
<tr><td rowspan="2">BUFG[2:0]</td><td colspan="5">RIN[1:0]</td></tr>
<tr><td>00</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td>000</td><td>0</td><td>-6</td><td>-12</td><td>-18</td></tr>
<tr><td>001</td><td>3</td><td>-3</td><td>-9</td><td>-15</td></tr>
<tr><td>010</td><td>6</td><td>0</td><td>-6</td><td>-12</td></tr>
<tr><td>011</td><td>9</td><td>3</td><td>-3</td><td>-9</td></tr>
<tr><td>100</td><td>12</td><td>6</td><td>0</td><td>-6</td></tr>
<tr><td>101</td><td>15</td><td>9</td><td>3</td><td>-3</td></tr>
<tr><td>110</td><td>18</td><td>12</td><td>6</td><td>0</td></tr>
<tr><td>111</td><td>21</td><td>15</td><td>9</td><td>3</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">RIN[1:0]</td><td rowspan="6">01</td><td colspan="6">L/R channel input impedance, applied on both channels:</td></tr>
<tr><td>RIN[1:0]</td><td colspan="5">Input impedance (KΩ)</td></tr>
<tr><td>00</td><td colspan="5">5</td></tr>
<tr><td>01</td><td colspan="5">10</td></tr>
<tr><td>10</td><td colspan="5">20</td></tr>
<tr><td>11</td><td colspan="5">40</td></tr>
<tr><td colspan="9">Note:
1. Transmit power control accuracy +/- 1dB</td></tr>
</table>

Crystal Control Word

Format of Word 0Fh: XTAL

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
XCSEL[5]	XCSEL[4]	XCSEL[3]	XCSEL[2]	XCSEL[1]	XCSEL[0]	XISEL[1]	XISEL[0]

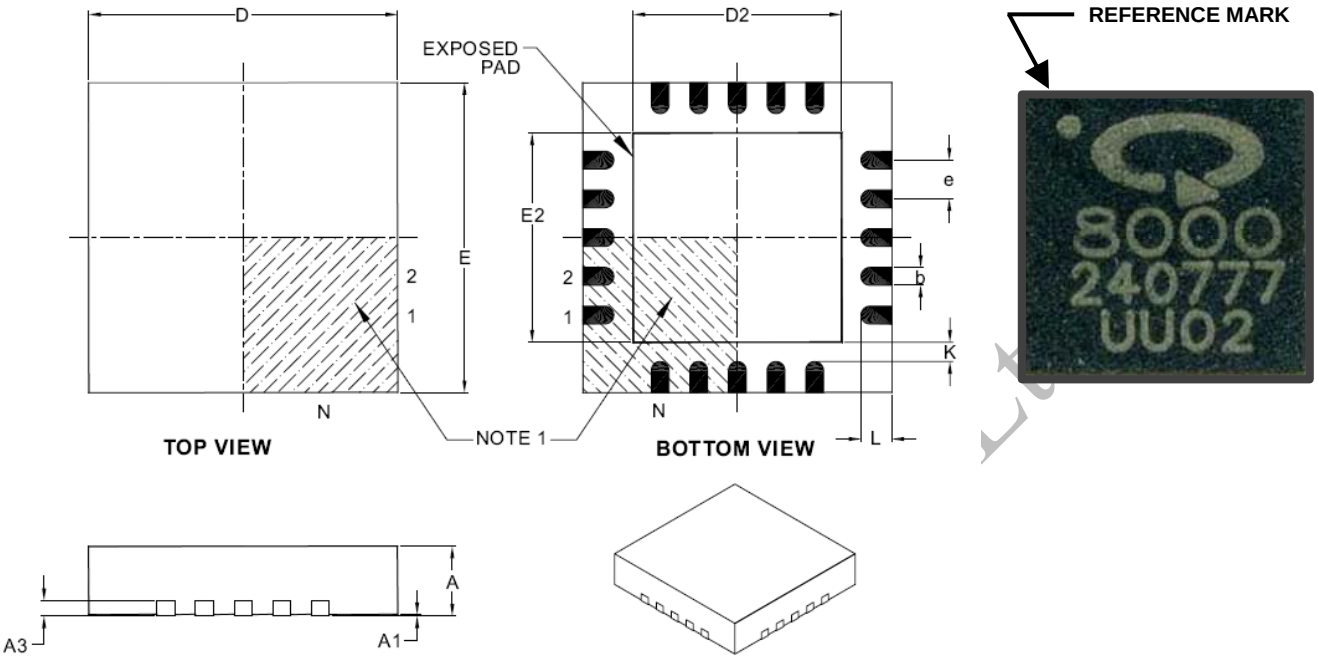
Description of Word 0Fh: XTAL

BIT	SYMBOL	DEFAULT	DESCRIPTION	
7:2	XCSEL[5:0]	100000	Crystal cap load setting. The differential cap load is: 5.76+XCSEL*0.144 pF (ie. it ranges from 5.76pF-14.8pF) Example: When XCSEL=0(min), C=5.76pF When XCSEL=63(max), C=14.832pF When XCSEL=32(default), C=10.368pF	
1:0	XISEL[1:0]	10	Crystal oscillator core current.	
			XISEL[1:0]	XTAL oscillator current (μA):
			00	30
			01	50
			10	70
			11	90

Note: Please refer to the Programmer's Guide Application Note for instructions on accessing this register via the 2-wire serial interface.

7. PACKAGE DESCRIPTION

20-Lead plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

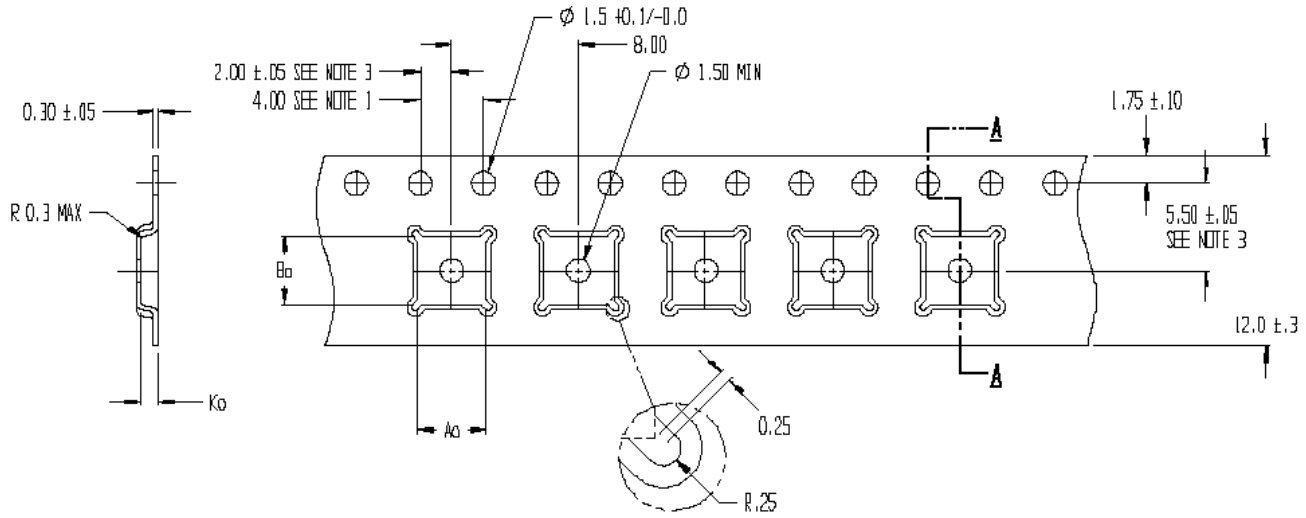


Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of pins	N		20	
Pitch	e		0.50BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00		0.05
Contact Thickness	A3		0.20REF	
Overall Width	E		4.00BSC	
Exposed Pad Width	E2	2.05	2.10	2.15
Overall Length	D		4.00BSC	
Exposed Pad Length	D2	2.05	2.10	2.15
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.50	0.55	0.60
Contact-to-Exposed Pad	K	0.40	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerance per ASME Y 14.5M.
   BSC: Basic Dimension. The theoretically exact value is shown without tolerance.
   REF: Reference Dimension, usually without tolerance, for information purpose only.

Carrier Tape Dimensions



SECTION A - A

NOTES:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA-481.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
4. $A_0 = 4.35$
   $B_0 = 4.35$
   $K_0 = 1.10$

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