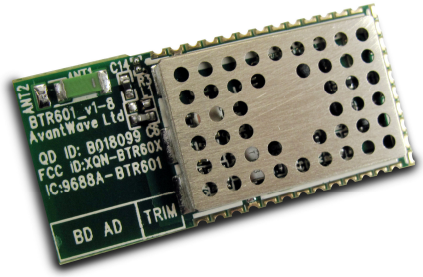
Datasheet
Bluetron™ Module
BTR602

Key Features

(photo not yet updated)



- **A small and cost effective Bluetooth® System**
- **Bluetooth® specification v2.1 +EDR compliant**
- **Class 2, up to 10-meter range**
- **Transmit RF power, up to +4dBm**
- **Receive sensitivity, up to -85dBm@BER = 0.1%**
- **Complete 2.4GHz Bluetooth® System including:**
  – Hardware: Radio, Baseband ,Crystal, MCU, Regulators & ROM
  – Standard Firmware: HCI stack 23C
- **Integrated 1.8V & 1.5V regulators (linear mode)**
- **Compact size: 28.2 mm x 15.0 mm x 2.8 mm**
- **SDIO (Bluetooth type A) & UART @4Mbps interfaces**
- **Auristream Codec (16, 24, 32, 40kbps), transmit power is minimized**
- **Built-in PCM or I2S interfaces**
- **Surface mount module for embedded applications**
- **Chip Antenna on board or External antenna design**
- **IEEE 802.11 coexistence**
- Green (RoHS & Halogen free)
- **Operating & Storage temperature within -40° C to +85° C**

Bluetooth®

QDID: B018099
FCC iD: XQN-BTR60X
IC: 9688A-BTR601

Description

Bluetron™ BTR602 module from AvantWave is a complete Bluetooth® solution for fast implementation, cutting your time-to-market. It is a short-range, compact and cost effective radio/baseband module that can be implemented in any kind of electronic devices, such as Bluetooth hands-free car kit, PDA and Mobile phone handset etc.

In standard configuration the module includes a baseband processor with on board 4M Bytes ROM memory, a radio front-end, supporting circuitry, able to connect with some higher-levels external software protocols and applications such as HSP, HFP, A2DP, AVRCP are coexisted with the external Host MCU (via I2S interface DAC codec).

The **Bluetron™ BTR602 module** is a power class 2 Bluetooth® device, and is in compliance with version 2.1 +EDR of the Bluetooth® specification. It is supplied with Bluetooth® HCI stack firmware which runs on the internal microprocessor. **Bluetron™ BTR602 module** is built on CSR BC06 QFN ROM core with ROM memory for firmware and application software storage.

Applications

- **Automotive Car Kit Applications**
- **PDAs**
- **Mobile Phones**
- **Cellular Handsets**

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Software

The lower layers of the Bluetooth stack (HCI) runs on-package. An external microcontroller is required. Bluetron™ BTR602 is integrated with a digital ADPCM low power CODEC, and interface to power management circuit.

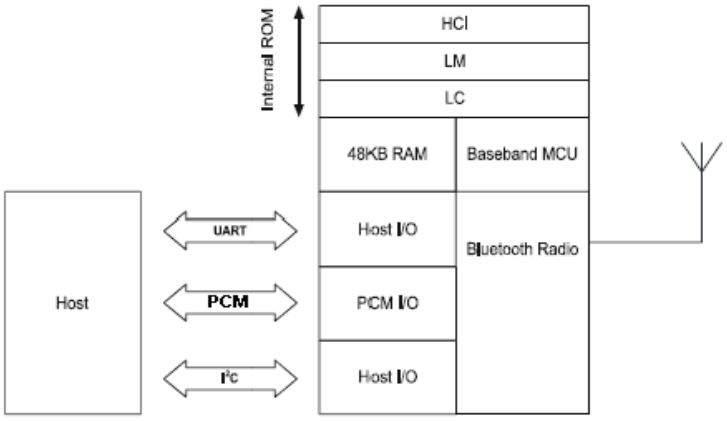

Fig. 1 System block diagram

Mechanical Specification [photo not yet updated]

Top view

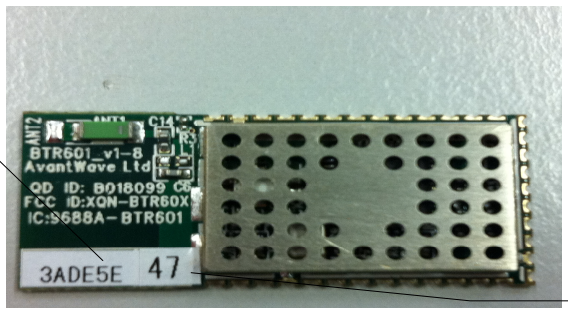

Fig. 2a module top view (15mm x 32mm)

Bottom view

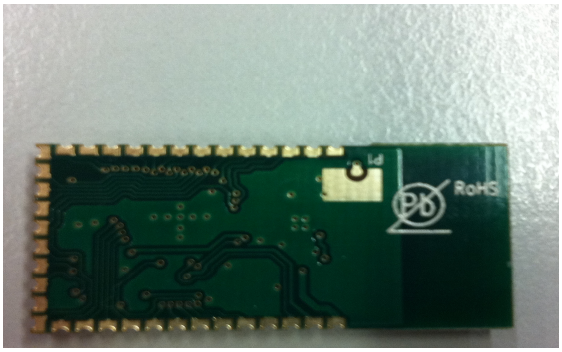

Fig. 2b module bottom view

Mechanical Drawing

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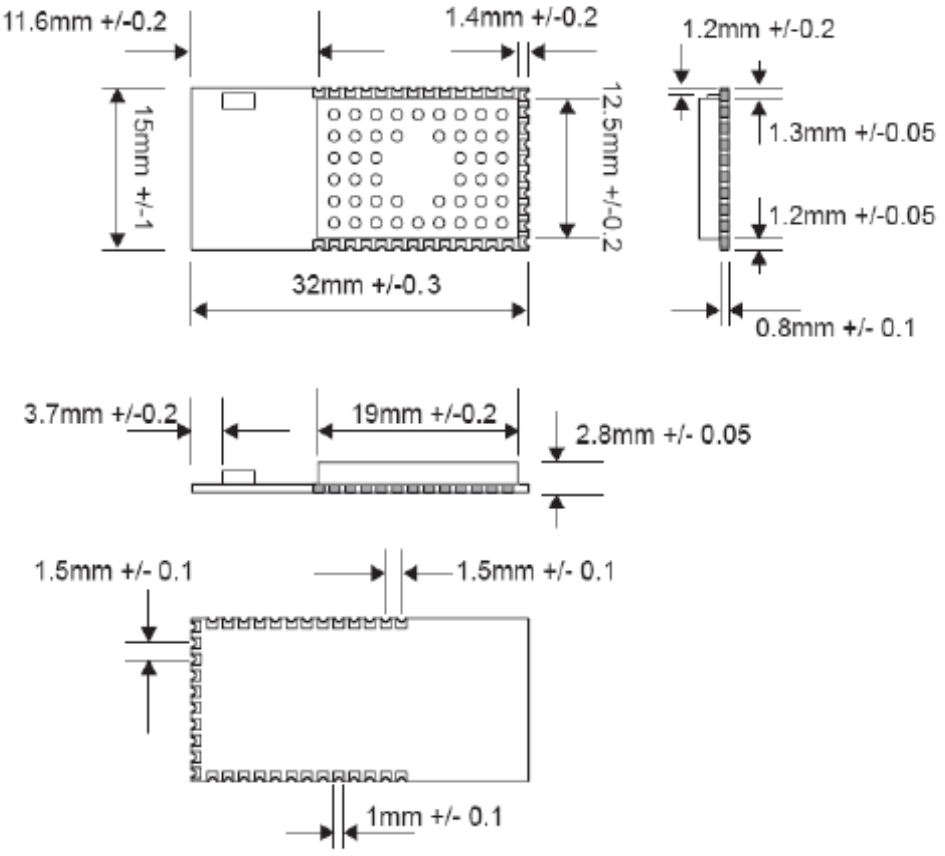

Fig. 2c Mechanical Drawing dimensions

(not yet updated)

Sectional view

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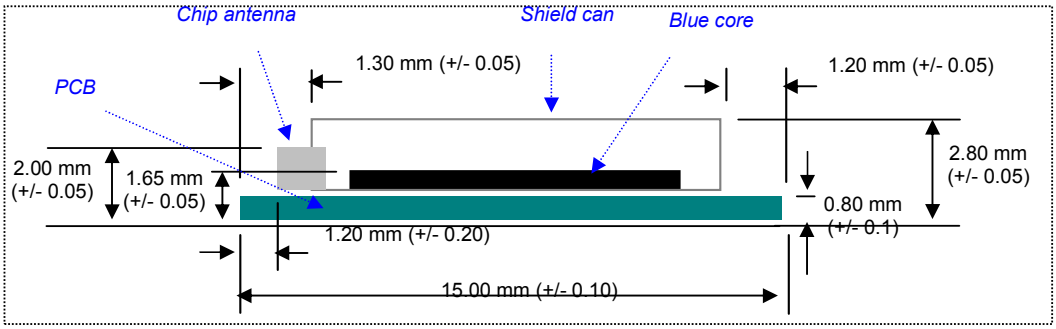


Fig. 3-1 BTR602 module side view (A)

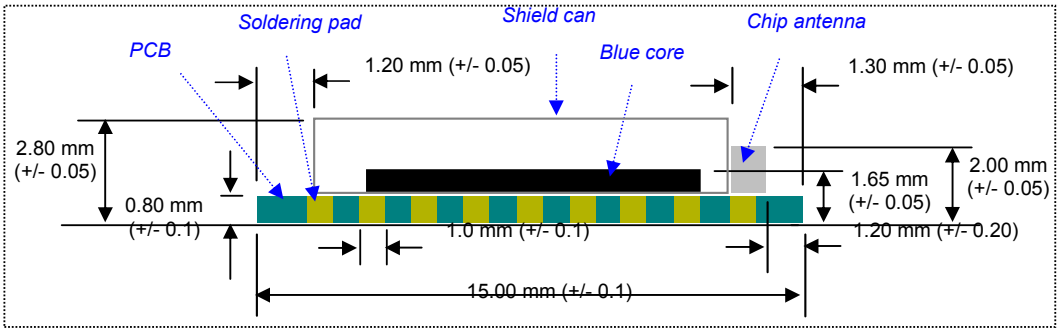


Fig. 3-2 BTR602 module side view (B)

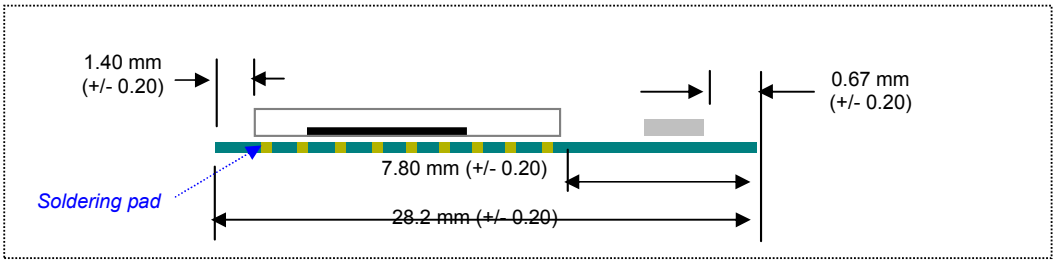
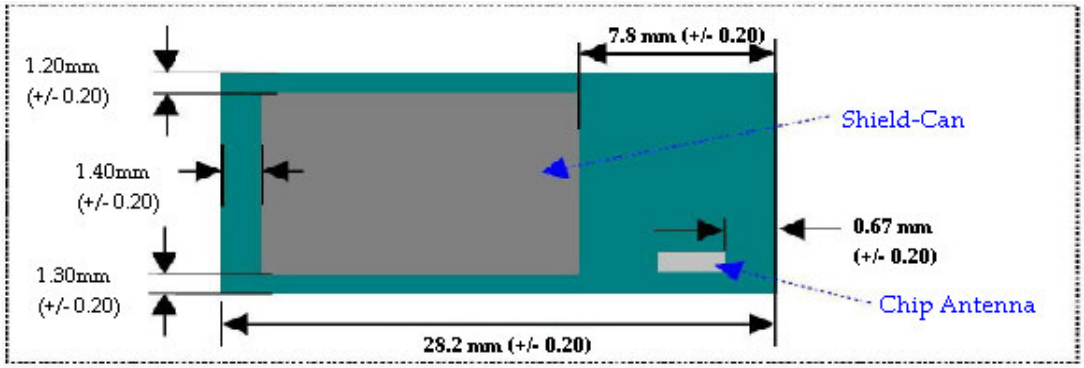


Fig. 3-3 BTR602 module side view (C)



TOP View

Fig. 3-4 BTR602 module Top view (D)

** All terminations surface finishing are coated by the Electroless Nickel immersion gold (ENIG) material, the advantages of the ENIG are good conductive, high solder-ability and excellent wettability,,etc.

Suggested Land Pattern

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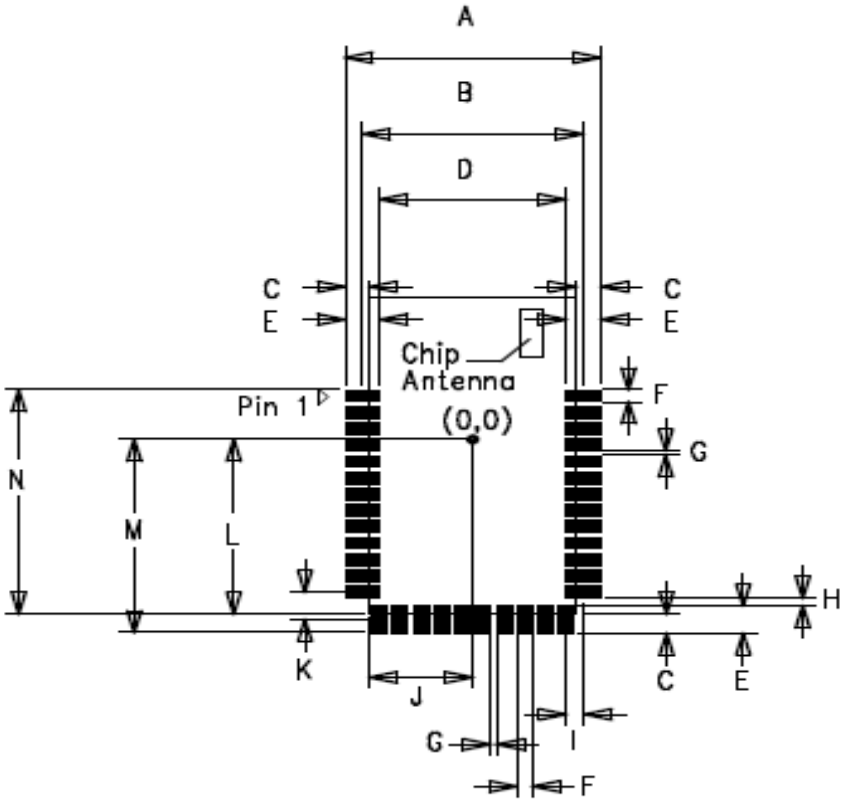

Fig.4a BTR602 module recommended PCB Land Pattern

Symbol	Dimension(mm)	Description
A	18.50	Outer width
B	16.00	Center width
C	1.75	Pad length outer from module edge
D	13.50	Inner width
E	2.50	Pad length
F	1.10	Pad width
G	0.40	Inner gap
H	0.70	Inner gap
I	1.30	Center pad to center pad
J	7.50	Module center to module edge
K	2.50	Center pad to center pad
L	16.00	Module center to module edge
M	17.70	Module center to pad edge
N	20.55	Module edge to pin1 edge

Table 1 Land Pattern Dimensions

Remark: all dimensions may have some tolerance within +/- 10%

Terminal Coating: The BTR602 module pads finishing material is flash gold over nickel (ENIG). The thickness is around 0.05 to 0.25 micron. It is the metallic surface finish plated onto the copper base by means of a chemical decomposition process

Antenna & Restricted area

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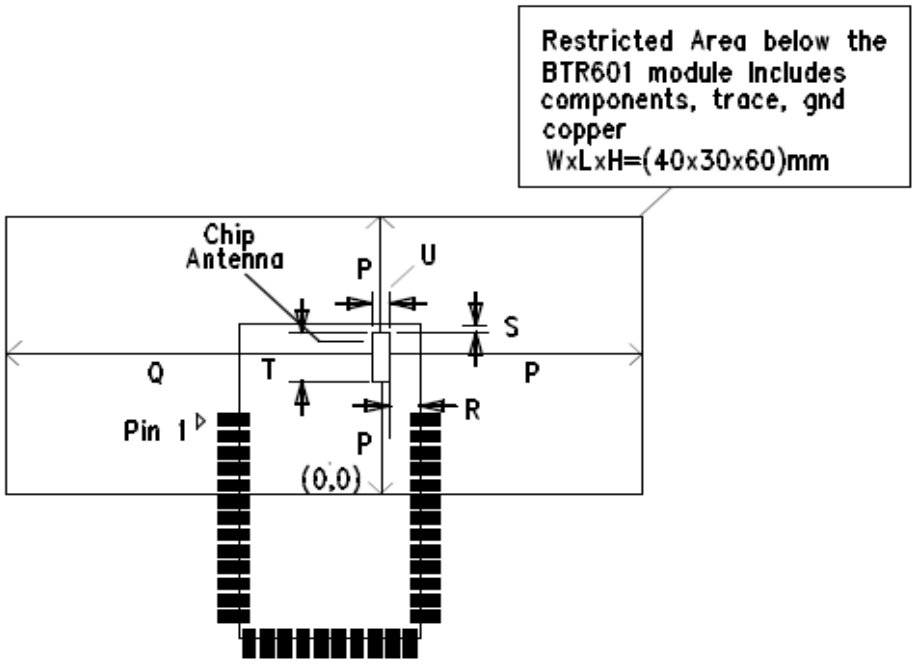

Fig.4b BTR601 module Antenna & its restricted area

Symbol	Dimension(mm)	Description
P	15.00	Antenna restricted area
Q	25.00	Antenna restricted area
R	1.0	Antenna edge to right side pcb edge
S	0.67	Antenna edge to top side pcb edge
T	4.2	Antenna pad to pad length
U	1.6	Antenna pad width

Table 2 restricted area dimensions

Restricted Area assumption: It is a reference guideline to suggest the application PCB designer about how to maximize the RF performance, generally, the restricted area should be as large as possible to attain the better performance. And the restricted area is different shape or size due to different application's PCB design. The basic concept is related to avoid obstacles around the Antenna. So, there is suggested a restricted area surround the on board Antenna with the certain dimension (>BT wavelength ~12.5cm long).
For the height of restricted area, it also depends on different applications feasibility. The height supposed to be +z/-z axis (+65mm/-65mm) in order to totally achieve as long as BT wavelength(65mm+65mm). It is a reference only but not definitely can be achieved for all applications.
For the shield can cover area(P) , it is simulate the EVB ground plane design of the Chip Antenna datasheet. The ground plane is replaced by the shield can(short to ground). The purpose is minimized the interference from/to the module.

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Pin Description

Terminal	Name	Description
1	+1.5V	+1.5V voltage supply input /output(default)
2	+1.8V	+1.8V voltage supply input/ output(default)
3	AIO[0]	Analog Programmable input/output line
4	GND	Ground pin
5	VREG_IN	voltage supply input
6	VREG_EN	Enable the high-ion LDO regulator, active high input
7	PIO[1]	Programmable input/output line
8	PIO[2]	Programmable input/output line
9	PIO[3]	Programmable input/output line
10	PIO[4]	Programmable input/output line
11	PIO[5]	Programmable input/output line
12	PIO[7]	Programmable input/output line
13	PIO[9]	Programmable input/output line
14	/Reset	Reset pin, active low input
15	GND	Ground pin
16	EEPROM_SDA	EEPROM serial address/data (input / output)
17	EEPROM_SCL	EEPROM serial clock input
18	EEPROM_WP	EEPROM write protect input
19	PCM_IN	PCM synchronous data input
20	PCM_OUT	PCM synchronous data output
21	PCM_CLK	PCM synchronous data clock input(slave)/output(master)
22	PCM_SYNC	PCM synchronous data sync input(slave)/output(master)
23	CLK_32K	32kHz external reference clock input
24	SDIO_DATA[0]	Synchronous data input/output
	CSPI_MISO	CSR SPI Master in Slave out output
	UART_TX	UART data output, active high
25	SDIO_DATA[1]	Synchronous data input/output
	CSPI_INT	CSR SPI interrupt output
	UART_RTS	UART request to send, active low output
26	SDIO_DATA[2]	Synchronous data input/output

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Terminal	Name	Description
	UART_RX	UART data input, active high
27	SDIO_DATA[3]	Synchronous data input/output
	CSPI_CS#	Chip select for CSR SPI, active low input
	UART_CTS	UART clear to send, active low input
28	SDIO_CLK	SDIO Clock input
	CSPI_CLK	CSR SPI Clock input
29	SDIO_CS	SDIO chip select to allow SDIO Accesses input
30	SDIO_CMD	SDIO data input
	CSPI_MOSI	CSPI Master out Slave in input
31	SPI_MISO	SPI Master in Slave out output
32	SPI_CLK	SPI clock input
33	SPI_CSB	Chip select for SPI, active low input
34	SPI_MOSI	SPI Master out Slave in input
35	GND	Ground pin
36	ANT	50 ohm impedance RF port input/output

Table 3 Pin Description

** CSR SPI interface is an extension of SPI interface, 8 bit command, 24 bit address, 16 bit burst length
** SDIO is a host interface that allows a SDIO host to gain access to the internal of the core.

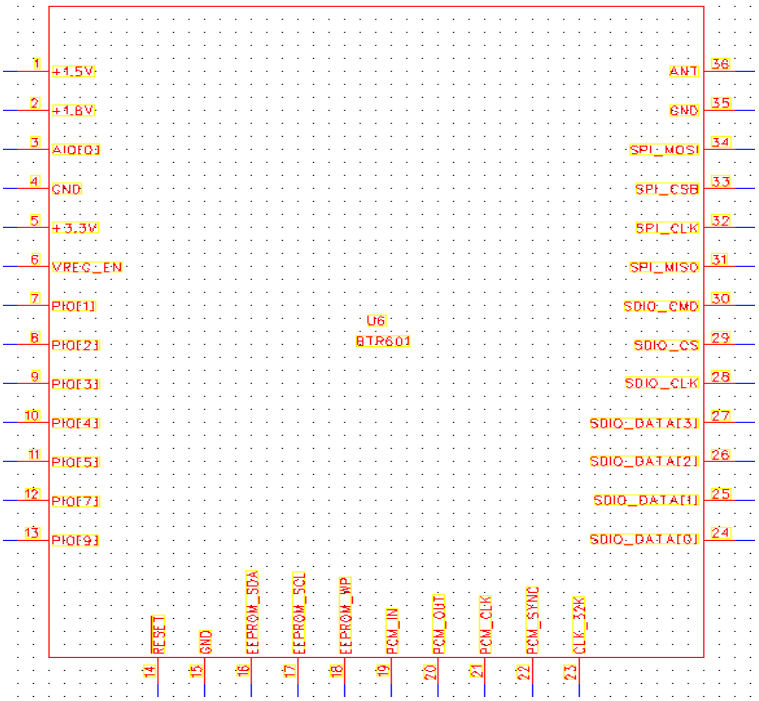

Fig. 5 BTR602 pin assignment

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Pin initial status (after reset)

Signal name	Pin #	I/O	Status under reseting (I/O)	Status under reseting (H/L/Hi-Z)	External operation	Internal PU/PD
+1.5V (default output)	1	PWR	PWR	PWR	PWR	PWR
+1.8V (output)	2	PWR	PWR	PWR	PWR	PWR
ADC[0]	3	I/O	I	Hi-Z	NC	-
GND	4	GND	GND	GND	GND	GND
VREG_IN (+3.3V)	5	PWR	PWR	PWR	up to +3.3V input connect via a decoupling capacitor to the GND	-
VREG_EN	6	I	I	H	NC	-
PIO[1]	7	I/O	I	Hi-Z	NC	programmable PU or PD
PIO[2]	8	I/O	I	Hi-Z	NC	programmable PU or PD
PIO[3]	9	I/O	I	Hi-Z (Open-drain	NC	programmable PU or PD
PIO[4]	10	I/O	I	Hi-Z	Pulldown 100k ohm	programmable PU or PD
PIO[5]	11	I/O	I	Hi-Z	NC	programmable PU or PD
PIO[7]	12	I/O	I	Hi-Z	NC	programmable PU or PD
PIO[9]	13	I/O	I	Hi-Z	NC	programmable PU or PD
/Reset	14	I	I	Hi-Z	Pullup 4k7 ohm	weak PU
GND	15	GND	GND	GND	GND	GND
EEPROM_SDA	16	I/O	I/O	Hi-Z	pull up 10k ohm (100kHz) or 1k ohm (400kHz)	NONE
EEPROM_SCL	17	I/O	I/O	Hi-Z	pullup 10k ohm	-
EEPROM_WP	18	I/O	I/O	Hi-Z	GND	-
PCM_IN	19	I	I	Hi-Z	NC	weak PD
PCM_OUT	20	O	O	Hi-Z	NC	weak PD
PCM_CLK	21	I/O	I	Hi-Z	NC	weak PD
PCM_SYNC	22	I/O	I	Hi-Z	NC	weak PD
CLK_32K	23	I	I	Hi-Z	NC	weak PD
SDIO_DATA[0]	24	I/O	I	+1.7V	NC	weak PU
CSPIMISO	24	I/O	I	+1.7V	NC	weak PU
UART_TX	24	I/O	TRI-STATE	+1.7V	Pullup 4K7 ohm	weak PU
SDIO_DATA[1]	25	I/O	I	+1.7V	NC	weak PU
CSPIINT	25	I/O	I	+1.7V	NC	weak PU
UART_RTS	25	I/O	TRI-STATE	+1.7V	-	weak PU
SDIO_DATA[2]	26	I/O	I	+1.7V	NC	weak PU
UART_RX	26	I/O	TRI-STATE	+1.7V	Pullup 4K7 ohm	weak PU
SDIO_DATA[3]	27	I/O	I	H	NC	weak PU
CSPICS#	27	I/O	I	H	NC	weak PU
UART_CTS	27	I/O	TRI-STATE	H	-	weak PU
SDIO_CLK	28	I/O	I	+1.7V	Pulldown 100k ohm	weak PU
CSPICLK	28	I/O	I	+1.7V	-	weak PU
SDIO_CS	29	I/O	I	+1.7V	-	weak PU
SDIO_CMD	30	I/O	I	+1.7V	Pulldown 100k ohm	weak PU
CSPIMOSI	30	I/O	I	+1.7V	NC	weak PU
SPIMISO	31	O	O	L	test pad (debug)	weak PD
SPICLK	32	I/O	I	H	test pad (debug)	weak PD
SPICSB	33	I/O	I	H	test pad (debug)	weak PD
SPIMOSI	34	I	I	L	test pad (debug)	weak PD
GND	35	GND	GND	GND	GND	GND
ANT	36	I/O	I/O	Hi-Z	-	NONE

Table. 4 Pin assignment initial status

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Applications Reference Circuit

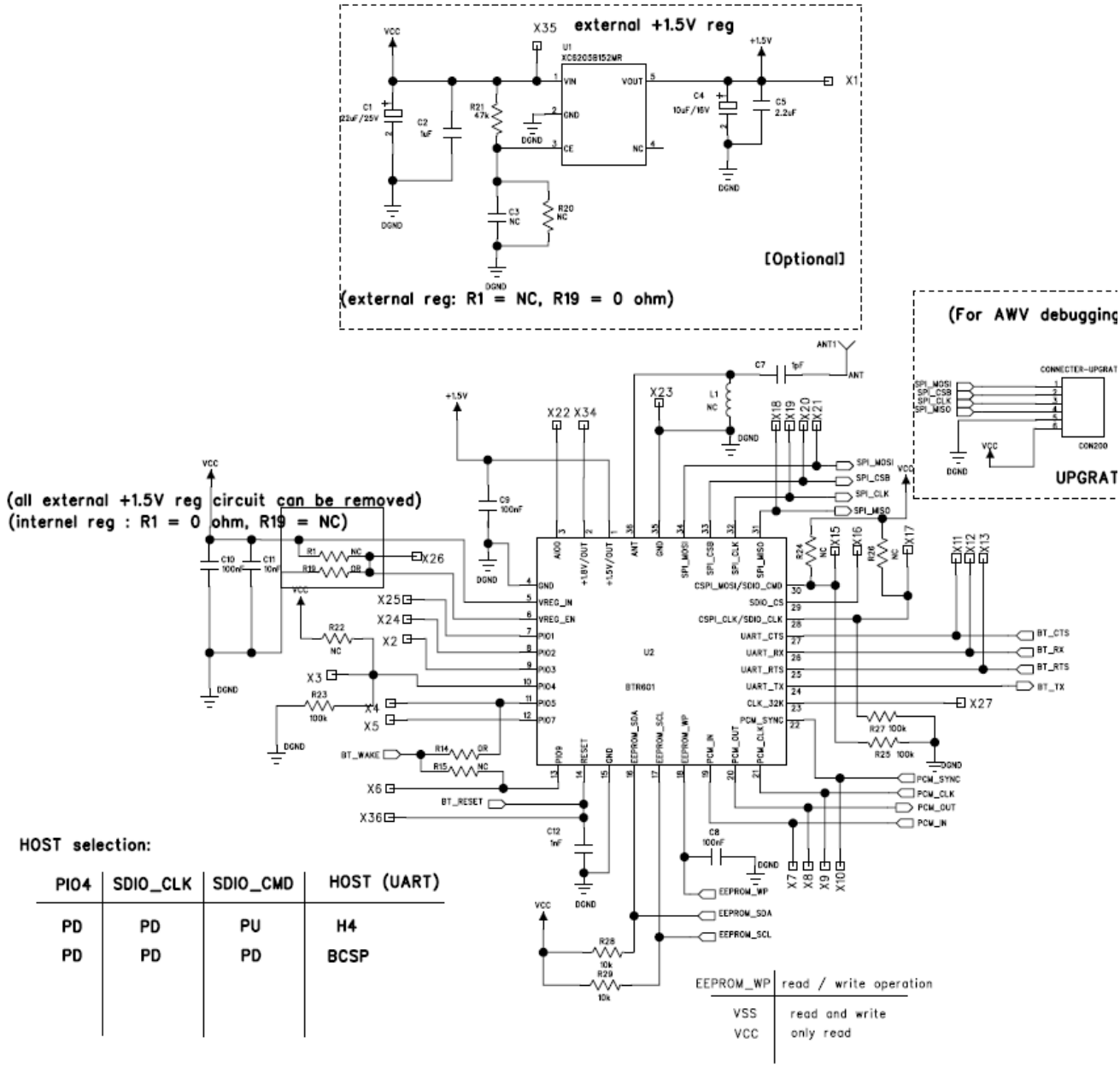

Fig.5 BTR602 module reference circuit

AIO & PIO depend on the application will be pull up or down, otherwise it will be open connection.

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General Specifications [TBC]

	Minimum	Typical	Maximum
Supply Voltage: VREG_IN	-0.4V	3.3V	4.9V
High Voltage Regulator Output (I_{load} = 70 mA)	1.7V	1.8V	1.9V
Low Voltage Regulator Output (I_{load} = 70 mA)	1.4V	1.5V	1.6V
Operating Temperature range	-40°C	25°C	85°C
Storage Temperature range	-40°C(*)	25 °C	85°C(*)
Frequency Range	2.402 GHz	2.441 GHz	2.480 GHz
Crystal Frequency	26MHz - 15ppm	26MHz	26MHz +15ppm
AFH	-	79 channels	-
Channel Bandwidth (Basic rate / Enhanced data rate)	-	1Mbps / 2 or 3Mbps	-
Internal ROM / RAM	-	4MB / 48KB	-

Table. 4 General Specifications

Remark: (*) assume all components are soldered on the module PCB, although all components can be stored in between -40 to 85°C, but not recommend to store this module in the extreme temperature before it has soldered on the application PCB. The device is turn off but the environment also in between -40 to 85°C, assume it is able to sustain the extreme temperature. All components on the module can sustain the storage temperature between -40 to 85°C. Typically, we have tested the storage temperature(-40°C or +85°C) as maximum duration is 12 hours per each time.
We have passed the high/low temperature test for operated at -40 to 85°C, and most of the components have -40 to 85°C storage temperature

RF Specifications (Basic Data Rate) [TBC]

Voltage Supplies = 1.8V (internal regulator converts to 1.5V supply domain)
Temperature = 25°C
Frequency = 2.441GHz

Receiver	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity (DH1/3/5) at 0.1% BER	-80	-84	-86	≤-70	dBm
Maximum received signal at 0.1% BER	-20	3	6	≥-20	dBm
C/I Co-channel	6	9	11	≤11	dB
C/I Adjacent channel (f = f_0 +/- 1MHz)	-7	-4	-1	<0	dB
C/I Adjacent channel (f = f_0 +/- 2MHz)	-50	-45	-40	≤-40	dB
C/I Adjacent channel (f = f_0 - 3MHz)	-60	-50	-40	≤-40	dB
C/I Adjacent channel (f = f_0 - 5MHz)	-60	-50	-40	≤-40	dB
C/I Image rejection (carrier –3MHz)	-30	-20	-10	≤-9	dB
Transmitter	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Average Output Power	-6	0	4	-6 to +4	dBm
20dB bandwidth $\|f_H - f_L\|$	900	950	1000	≤ 1000	kHz
2nd ACP (+/-2MHz)	-40	-30	-20	≤ -20	dBc
3rd ACP (+/-3MHz)	-60	-50	-40	≤ -40	dBc

Table 5 Basic Data Rate

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RF Specifications (Enhanced Data Rate) [TBC]

Voltage Supplies = 1.8V (internal regulator converts to 1.5V supply domain)
Temperature = 25°C
Frequency = 2.441GHz

Receiver	Modulation	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity (DH1/3/5) at 0.01% BER	π/4 DQPSK 8DPSK	-75 -73	-83 -78	-84 -80	≤-70	dBm
Maximum received signal at 0.1% BER	π/4 DQPSK 8DPSK	-15	0	5	≥ -20	dBm
C/I Co-channel at 0.1% BER	π/4 DQPSK 8DPSK	5 17	10 19	12 20	≤13 ≤21	dB
C/I Adjacent channel (f = f_0 +/- 1MHz)	π/4 DQPSK 8DPSK	-18 -15	-10 -5	0 5	≤0 ≤5	dB
C/I Adjacent channel (f = f_0 +/- 2MHz)	π/4 DQPSK 8DPSK	≥-30	≥-27	≥-25	≥-30 ≤-25	dB
C/I Adjacent channel (f = f_0 + 3MHz)	π/4 DQPSK 8DPSK	-40	-35	-33	≤-40 ≤-33	dB
C/I Adjacent channel (f = f_0 - 5MHz)	π/4 DQPSK 8DPSK	-40	-35	-33	≤-40 ≤-33	dB
C/I Image rejection (carrier –3MHz)	π/4 DQPSK 8DPSK	-30 -15	-20 -15	-10 0	≤-7 ≤0	dB
Transmitter		**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Average Output Power		-6	0	4	-6 to +4	dBm
Relative Transmit Power		-4	0	1	-4 to +1	dB
In-band spurious emissions	f = f_0 +/- 1MHz f = f_0 +/- 2MHz f = f_0 +/- 3MHz	-40 -45 -55	-35 ≥-34 ≥-50	-26 -20 -40	≤-26 ≤-20 ≤-40	dbm
π/4 DQPSK Modulation Accuracy	Peak DEVM	8	19	34	≤35	%
8DPSK Modulation Accuracy	Peak DEVM	10	17	25	≤25	%
EDR Differential Phase Encoding		99	99.9	100	≥99	%

Table 6 Enhanced Data Rate

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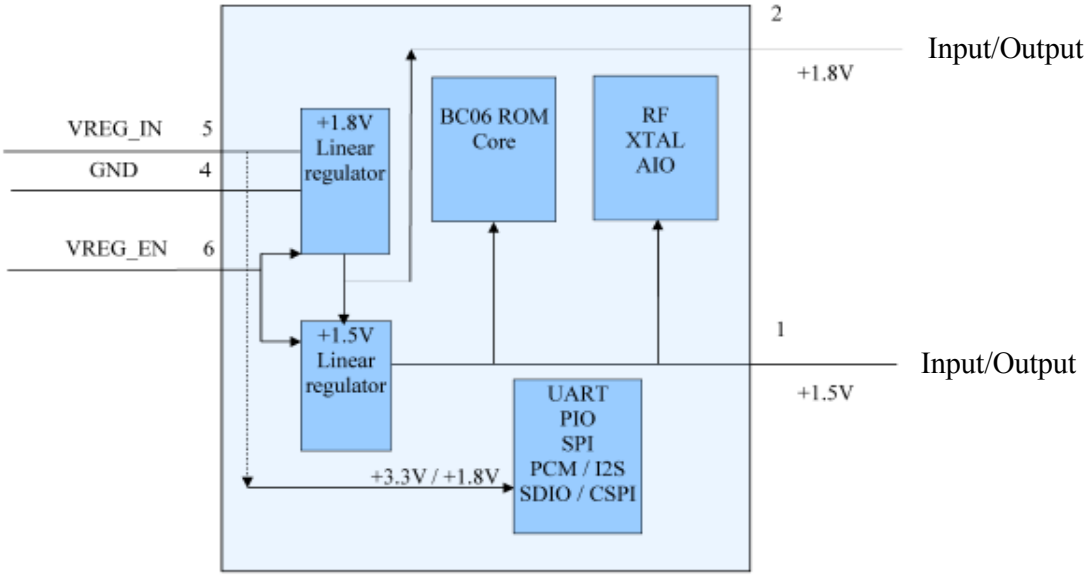

BTR601 BC06 QFN ROM Power Management Block Diagram

Fig. 6 BTR602 Power Management Block Diagram

VREG_EN (step down LDO regulator enable): Up to +4.9V dc voltage input
VREG_IN (positive supply for UART, PIOs, PCM/I2S, SPI & SDIO/CSPI) : typically +3.3V dc voltage input (can change to +1.8V dc depends on different applications)
VREG_OUT

- **option 1 (+3.3V input, +1.8V output & +1.5V output):**

=> input +3.3V to VREG_IN & VREG_EN, use the internal +1.8V & +1.5V regulator, +1.8V & 1.5V become the outputs

- option 2 (+1.8V input & +1.5V input):

=> input +1.8V to VREG_IN , use the external +1.5V input

- option 3 (+3.3V input & +1.5V input):

=> input +3.3V to VREG_IN, use the external +1.5 input

- option 4 (+1.8V input & +1.5V output):

=> input +1.8V to VREG_IN & VREG_EN, use the internal+1.8V & +1.5V regulator, +1.5V become the output, but +1.8V output may not as equal to +1.8V (-0.2V tolerance due to voltage drop.)

Remark: - If VREG_ IN to +1.8V, all the UART, PIOs, PCM/I2S, SPI & SDIO/CSPI are set to +1.8V.
- If +1.5V is output, the maximum output current is lower than 70mA.
- Option 1 is default setting, option 4 is not recommend to use.

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Power sequence (+3.3V, +1.5V & reset)

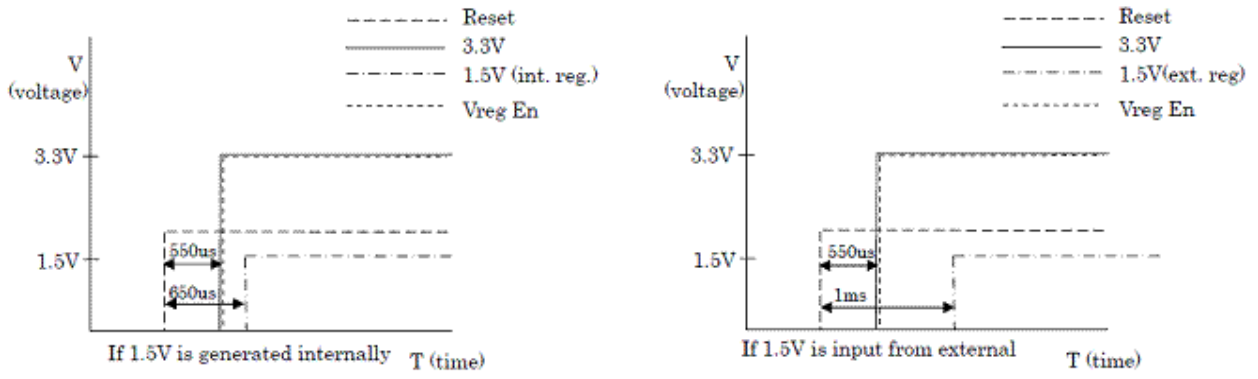

Fig. 7 initial power sequence

Sequence:

- After (Reset + 550us), +3.3V is started.
- After (Reset + 550us), VREG_EN is started
- After (Reset + 650us), +1.5V (internal regulator) is started.
- After (Reset + 1ms), +1.5V (external regulator) is started.

EEPROM Connection

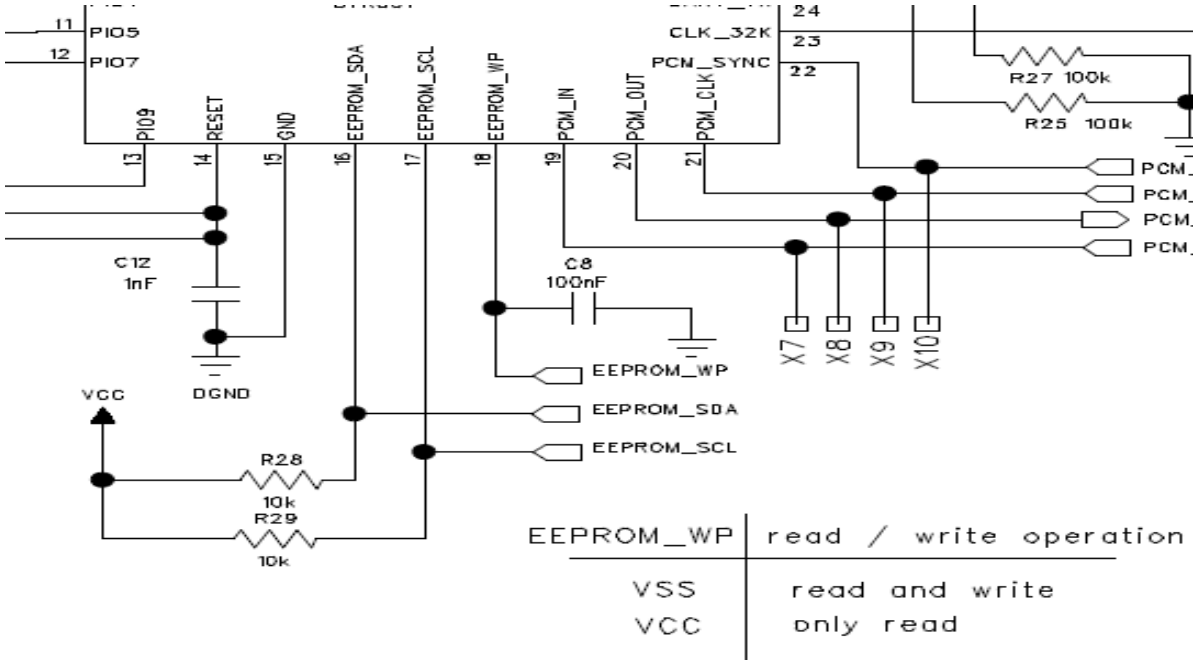

Fig. 8 EEPROM connection

Pin16 EEPROM_SDA: It is a bidirectional pin for transfer addresses and data in/out of the device, Due to the open-drain output, the I2C SDA port need a pull up resistor to Vcc (10k ohm for 100kHz, 2k ohm for 400kHz). I2C SDA bus is only able to change during I2C SCL low. Changes during I2C SCL high are reserved for indication Start and Stop bit status.

Pin17 EEPROM_SCL: I2C SCL input is assigned to synchronize the data transfer to and from the device.

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Pin18 EEPROM_WP: Write protect(WP) input pin is selected by the external device to define the EEPROM is able to write or not.
If tied it to Vss, memory operation(write/read) is enabled normally. If tied it to Vcc, write operation is disabled and read operation is enabled.

EEPROM slave address = 1010XYZ for BT address, crystal trim value and crystal frequency PSKEY storage, X is don't care bit, YZ = "00" is block select bits.

Host Interface Selections

For the protocol that is selected by the UART host interface, it is determined by the status of the SDIO_CLK and SDIO_CMD lines when sampling the PIO[4] status. Table 7 & 8 shown the host and protocol setting:

Select UART, SDIO or CSPI Host Interface by the hardware configurable method:

(PIN10) PIO	Input	Connection	Host
4	High	100k ohm to Vcc	SDIO / CSPI
4	Low	100k ohm to GND	UART

Table 7. PIO 4 selections

PIO[4] is pulled low: UART host interface is chose (default configure)
PIO[4] is pulled high: SDIO/CSPI host interface is chose.

Select UART Protocols by the hardware configurable method:

(PIN28) SDIO_CLK	Connection	(PIN30) SDIO_CMD	Connection	UART protocol
Low	100k ohm to GND	Low	100k ohm to GND	BCSP
Low	100k ohm to GND	High	100k ohm to Vcc	H4
High	100k ohm to Vcc	Low	100k ohm to GND	H4DS
High	100k ohm to Vcc	High	100k ohm to Vcc	H5

Table 8. UART protocol selections

Example
BCSP mode: SDIO_CLK and SDIO_CMD both add a 100k ohm resistor pull down to GND.
H5 mode: SDIO_CLK and SDIO_CMD both add a 100k ohm resistor pull up to Vcc.

UART connection:

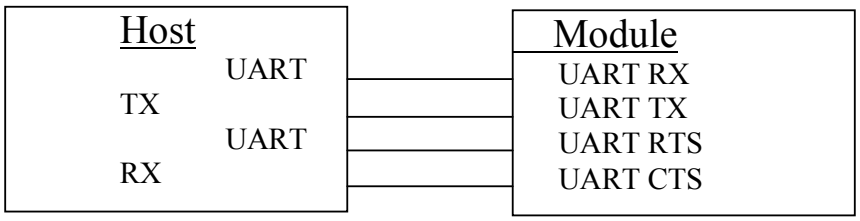

Fig. 9 UART connection method

BCSP : CSR proprietary, reliable alternative to the standard bluetooth UART Host Transport.

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H4DS : CSR proprietary, alternative to the standard bluetooth UART Host Transport, it supports deep sleep mode for low-power applications.
H4 => a transport protocol for bluetooth HCI packets over UART, the name came from bluetooth spec. appendix H4.
H5 => a three-wire protocol, presumably based on CSR's BCSP protocol.

UART operation : Set the hardware configurable pins (PIO4, SDIO_CLK & SDIO_CMD), if hardware configurable selection is BCSP transport(PIO4 is low, SDIO_CLK is low & SDIO_CMD is low), the baudrate is auto detected. The UART connection method is referent to fig. 8.

- UART_RX and UART_TX transmit data between the BTR602 module and external host. UART_RX should pull up to Vcc via a 10k ohm resistor. UART_TX is already internal pull up. UART_CTS & UART_RTS is hardware flow control (default is NC).

e.g default BCSP(0x0806) is configured to 8bit length, no hardware flow control, even parity bit. The parameter details can refer to the Appendix 1. The other default transport settings (H4, H4DS & H5 parameter) please refer to the Appendix1. All settings(PSKEY) can be changed by the external MCU via UART channel. Both the transports with auto detected baudrate and same connection method.

UART Settings:

Parameter		Possible values
Baud rate	minimum	1200 baud (≤2% error)
		9600 baud (≤1% error)
	maximum	4M baud (≤1% error)
Flow control		RTS / CTS or none
Parity		Odd, Even or none
Number of stop bit		1 or 2
Bits length		8

Table. 9 UART configurable value

PCM interface connections:

The module PCM interface is included the digital transmission and reception of PCM encoded audio data via the bluetooth channel. The BTR602 module is hardware ready for the PCM transceiver function, so, the processor computation power can be increased due to its overhead decreased. The module supports a bi-directional digital audio interface that streams directly into the baseband layer inside the on-chip firmware. It won't pass through the HCI protocol layer.

This PCM channel is able to send and receive the audio data from a SCO channel, it is three SCO channels can be supported by the PCM interface at any one time only.
For the PCM master, it can generate an output clock of 128, 256, 512, 1536 or 2400kHz. For the PCM slave, ,it can co-operate with an input clock up to 2400kHz. The module PCM supports 13bit or 16 bit linear,

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8-bit μ-law or A-law companding sample formats at 8k samples/s and send and receive on any three of first four slots following PCM_SYNC.

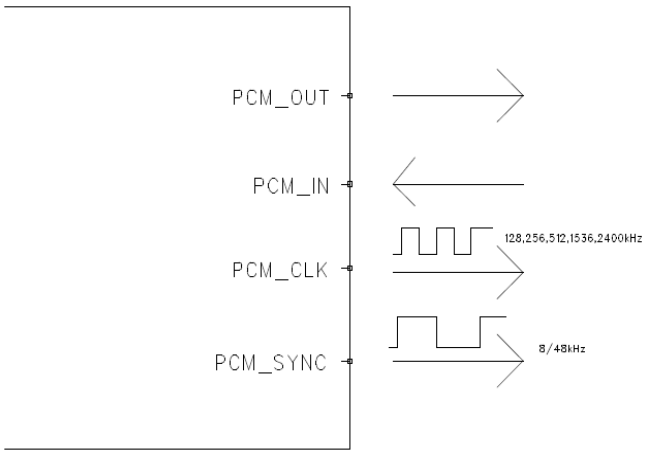

Fig. 10a) PCM interface master

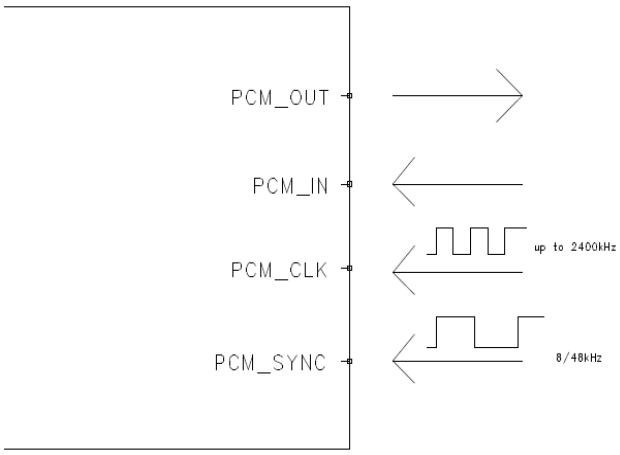

Fig. 10b) PCM interface slave

Long Frame Sync:
A clocking format which is controlled the transfer of PCM data words/samples. The rising edge of PCM_SYNC indicates the start of the PCM data. For the PCM master, PCM_SYNC & PCM_CLK are output, PCM_SYNC is 8 bits long. Besides, as PCM slave, PCM_SYNC from two continue falling edges of PCM_CLK to half the PCM_SYNC rate (62.5us long).

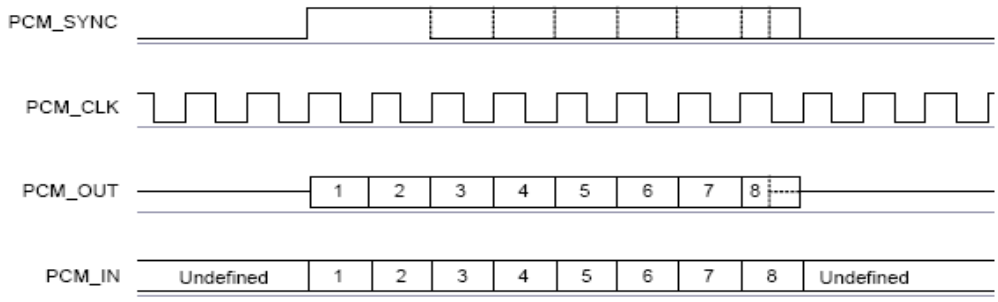

Fig. 10c) Long Frame Sync (8 bit PCM_OUT data)

Short Frame Sync:
The falling edge of PCM_SYNC indicates the start of the PCM_OUT data. PCM_SYNC is only one clock cycle duty.

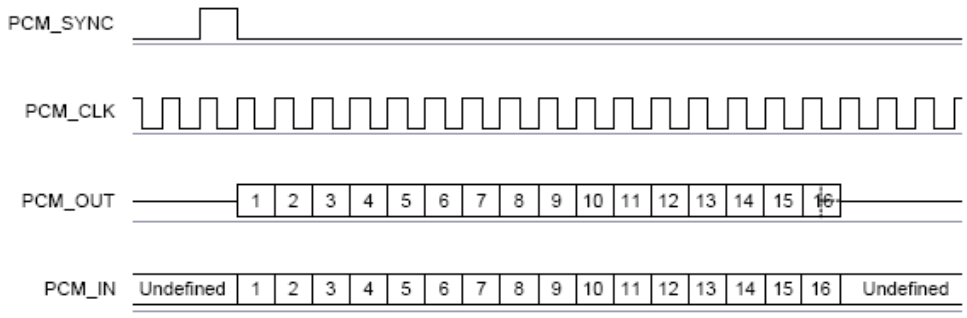

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Fig. 10d) Short Frame Sync (8 bit PCM_OUT data)

For the BTR602 module, it samples PCM_IN on the falling edge of PCM_CLK and generates PCM_OUT on the rising edge. And, PCM_OUT can be configured to be either high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

Slots and Sample Formats:
BTR602 module able to transmit and receive on any first four slots following each sync pulse. Slot periods can be either 8 or 16 clock pulses. The 8 clock cycles can only apply for the 8 bit sample formats. The 16 clock cycles can apply for 8 bit, 13 bit and 16 bit sample formats.

BTR602 module supports 13 bit linear, 16 bit linear and 8 bit μ-law or A-law sample formats. The sample rate is 8k samples/s. In case 16 bit slots are used, there are 3 or 8 unused bits in each slot will be filled with sign extension , padded with zero or a programmable 3 bit audio attenuation which is compatible with some Motorola CODEC.

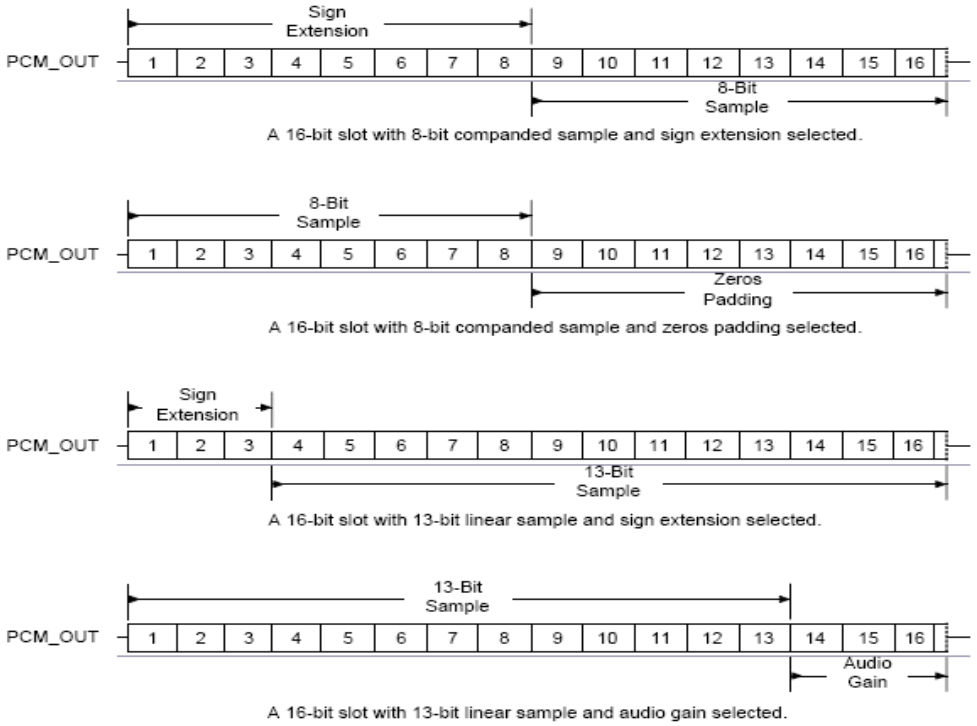

Fig. 10e) 16 bit slot length and sample formats

Symbol	Parameter		Min	Typ	Max	Unit
fmclk	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Table. 24	128	256	512	kHz
		48MHz DDS generation. Selection of frequency is programmable . See Table. 23 and page 20	2.9	3	3.1	kHz
-	PCM_SYNC frequency for SCO connection		4	8	8	kHz
tmclkh [a]	PCM_CLK high	4MHz DDS generation	980	990	1000	ns

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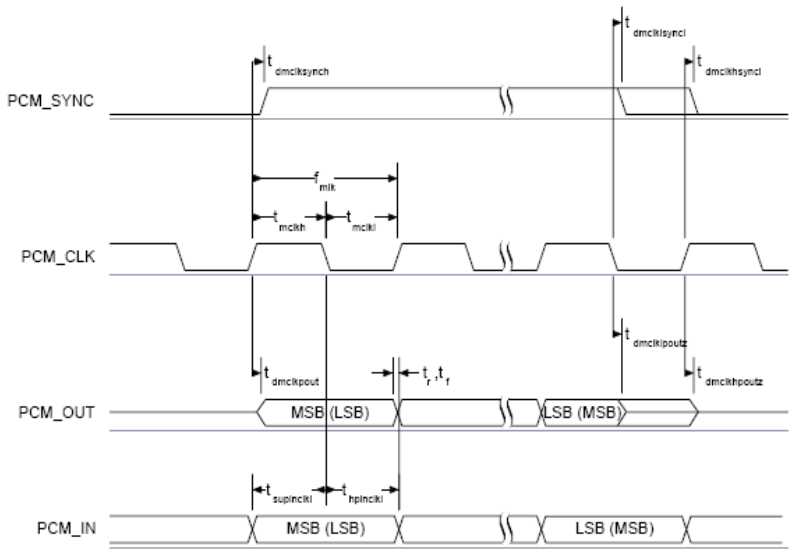
tmclkl [(a)]	PCM_CLK low	4MHz DDS generation	730	740	750	ns
-	PCM_CLK jitter	48MHz DDS generation	10	15	21	ns
tmclksynch	Delay time from PCM_CLK high to PCM_SYNC high		10	15	20	ns
tmclkpout	Delay time from PCM_CLK high to valid PCM_OUT		10	15	20	ns
tmclklsyncl	Delay time from PCM_CLK low to PCM_SYNC low		10	15	20	ns
tmclkhsyncl	Delay time from PCM_CLK high to PCM_SYNC low		10	15	20	ns
tmclklpoutz	Delay time from PCM_CLK low to PCM_OUT high impedance		10	15	20	ns
tmclkhpoutz	Delay time from PCM_CLK high to PCM_OUT high impedance		10	15	20	ns
tsupinclkl	Set-up time for PCM_IN valid to PCM_CLK low		30	35	40	ns
thpinclkl	Set-up time for PCM_CLK low to PCM_IN invalid		10	15	20	ns

Table. 10a) PCM Master Timing



ig. 10f) PCM Master Timing Long Frame Sync

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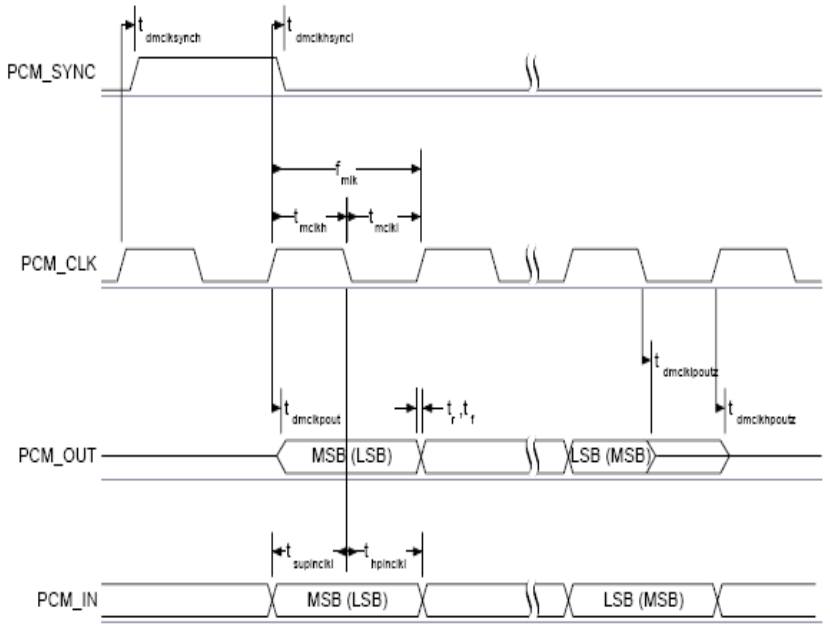

Fig. 10g) PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
fmclk	PCM_CLK frequency (slave mode: input)	64	512	2048	kHz
tclkh	PCM_CLK high time	200	300	400	ns
tclkl	PCM_CLK low time	200	300	400	ns
thclksynch	hold time from PCM_CLK low to PCM_SYNC high	30	50	70	ns
tsusclksynch	Set-up time for PCM_SYNC high to PCM_CLK low	30	50	70	ns
tdpout	Delay time from PCM_SYNC or PCM_CLK that is later, to valid PCM_OUT data (Long Frame Sync only)	15	20	20	ns
tdsclkhpout	Delay time from CLK high to PCM_OUT valid data	15	20	20	ns
tdpoutz	Delay time from PCM_SYNC or PCM_CLK that is later, to valid PCM_OUT data line high impedance	15	20	20	ns
tsupinclkl	Set-up time for PCM_IN valid to PCM_CLK low	30	40	50	ns
thpinclkl	Set-up time for PCM_CLK low to PCM_IN invalid	30	40	50	ns

Table. 10b) PCM Slave Timing

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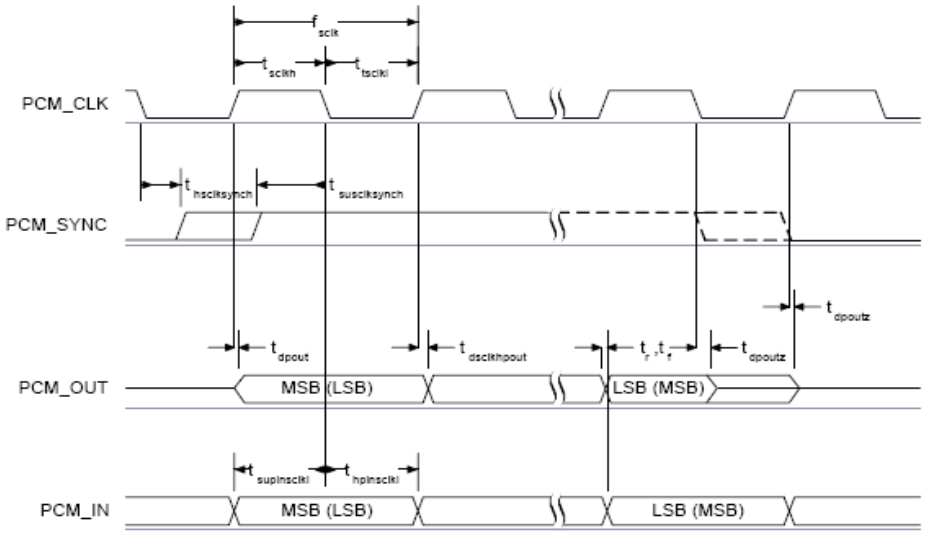

Fig. 10h) PCM Slave Timing Long Frame Sync

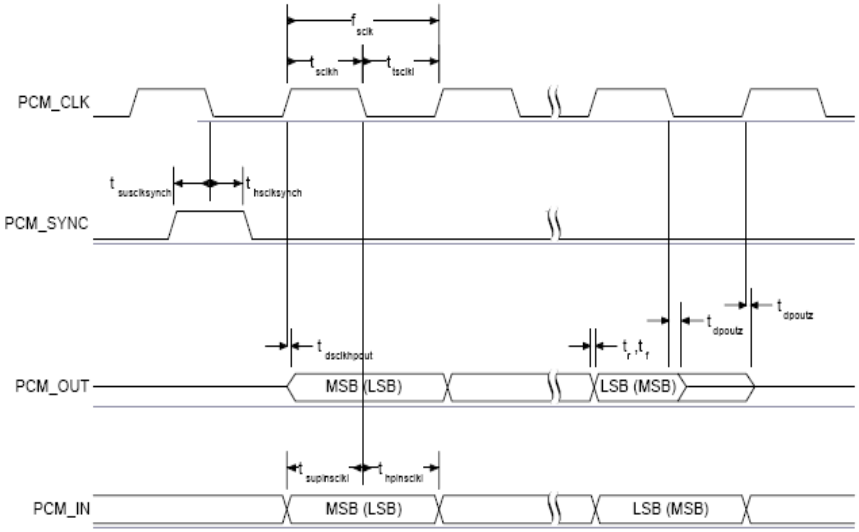

Fig. 10i) PCM Slave Timing Short Frame Sync

PCM_CLK and PCM-SYNC generation:

- Generating these by DDS from the Core internal 4MHz clock. It is limited the PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz
- Generating these by DDS from an internal 48MHz clock. Set bit via 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. For the long frame sync, the length of PCM_SYNC maybe either 8 or 16 bit cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

PCM_CLK frequency(internal 48MHz clock) formula:

f = (CNT_RATE / CNT_LIMIT) x 24MHz

PCM_SYNC frequency relevant to PCM_CLK (PCM_SYNC_MULT = 0)

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f = PCM_CLK / (SYNC_LIMIT x 8)

PCM_SYNC frequency relevant to PCM_CLK (PCM_SYNC_MULT = 1)

f = PCM_CLK / SYNC_LIMIT

CNT_RATE, CNT_LIMIT and SYNC_LIMIT all are set by PSKEY_PCM_LOW_JITTER_CONFIG. For example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW _JITTER_CONFIG to 0x08080177.

PCM configuration refer to the Appendix 4.

I^{2}S interface connections:

The BTR602 module digital audio interface provided the I^{2}S, left-justified or right justified. It is the same pins which shares with the PCM channel. So, the active digital audio interface is either PCM or I^{2}S at the same time.

PCM interface	I^{2}S interface
PCM _OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table. 10a) PCM & I2S interfaces pin assignment

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I2S interface (WS, SCK, SD_OUT):

Table. 11 shown the values for the PSKEY_DIGITAL_AUDIO_CONFIG how to configure the digital audio interface. i e. to configure an I^2S interface with 16 bit SD data set PSKEY_DIGITAL_CONFIG to 0x0406.

Bit	Mask	Name	Description
D[0]	0x0001	CONFIG_JUSTIFY_FORMAT	0 for left justified, 1 for right justified.
D[1]	0x0002	CONFIG_LEFT_JUSTIFY_DELAY	For left justified formats: 0 is MSB of SD data occurs in the first SCLK period following WS transition. 1 is MSB of SD data occurs in the second SCLK period.
D[2]	0x0004	CONFIG_CHANNEL_POLARITY	For 0, SD data is left channel when WS is high. For 1 SD data is right channel.
D[3]	0x0008	CONFIG_AUDIO_ATTEN_EN	For 0, 17 bit SD data is rounded down to 16 bits. For 1, the audio attenuation defined in CONFIG_AUDIO_ATTEN is applied over 24 bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0.
D[7:4]	0x00F0	CONFIG_AUDIO_ATTEN	Attenuation in 6 dB steps.
D[9:8]	0x0300	CONFIG_JUSTIFY_RESOLUTION	Resolution of data on SD_IN, 00=16 bit, 01=20 bit, 10=24 bit, 11=Reserved. This is required for right justified format and with left justified LSB first.
D[10]	0x0400	CONFIG_16_BIT_CROP_EN	For 0, 17 bit SD_IN data is rounded down to 16 bits. For 1 only the most significant 16 bits of data are received.

Table. 10b) I2S interface configurable PSKEY

BC06 Master mode I2c(PSKEY_DIGITAL_AUDIO_CONFIG): 0x0006

=> D[1] & D[2] is 1, others are 0

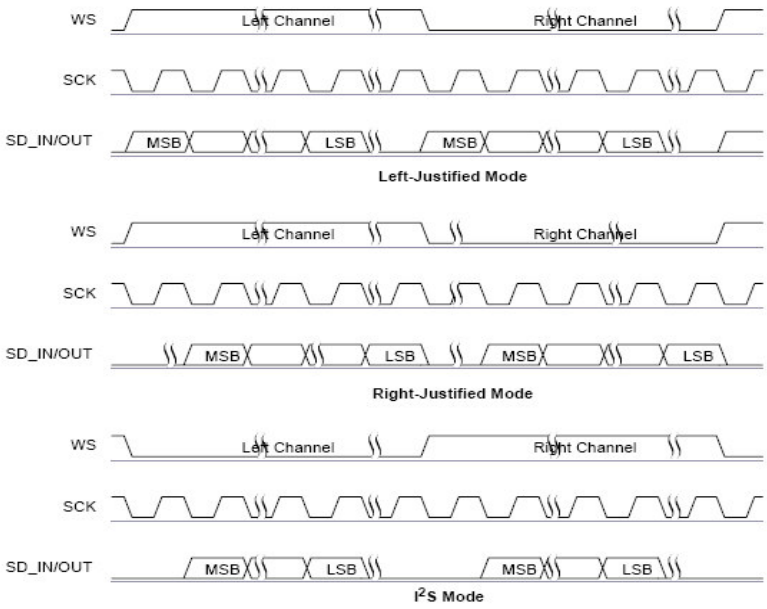

Fig. 11a) BTR602 module digital audio interface modes

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Symbol	Parameer	Min	Typ	Max	Unit
-	Clock frequency (SCK)	1.5	3	6.2	MHz
-	L/R clock (WS)	24	48	96	kHz
topd	SCK to SD_OUT delay	20	200	400	ns
tspd	SCK to WS delay	20	100	200	ns
tisu	SD_IN to SCK set up time	20	200	400	ns
tih	SD_IN to SCK hold time	10	200	450	ns

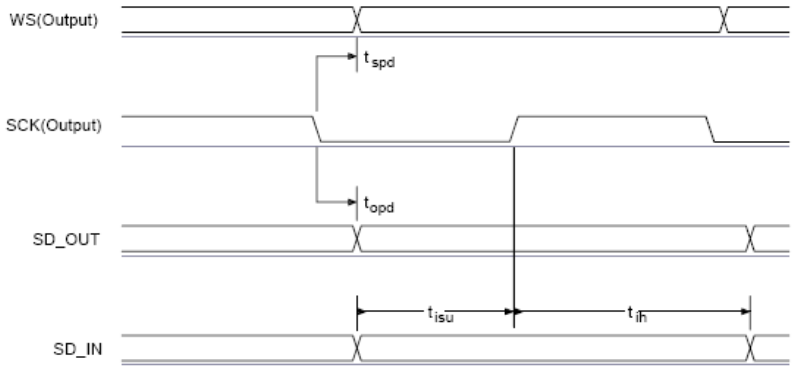

Fig. 11b) Digital Audio Interface Master Timing

Table 10c) Digital audio interface master timing (Data Output)

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK frequency	1	3	6.2	MHz
-	WS frequnecy	16	48	96	kHz
tch	SCK high time	80	340	600	ns
tcl	SCK low time	80	350	650	ns
topd	SCK to SD_OUT delay	20	50	150	ns
tssu	WS to SCK set-up time	20	100	500	ns
tsh	WS to SCK hold time	20	200	600	ns

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tisu	SD_IN to SCK set-up time	20	100	400 ns
tih	SD_IN to SCK hold time	20	100	400 ns

Table. 10d) Digital Audio Interface Slave Timing

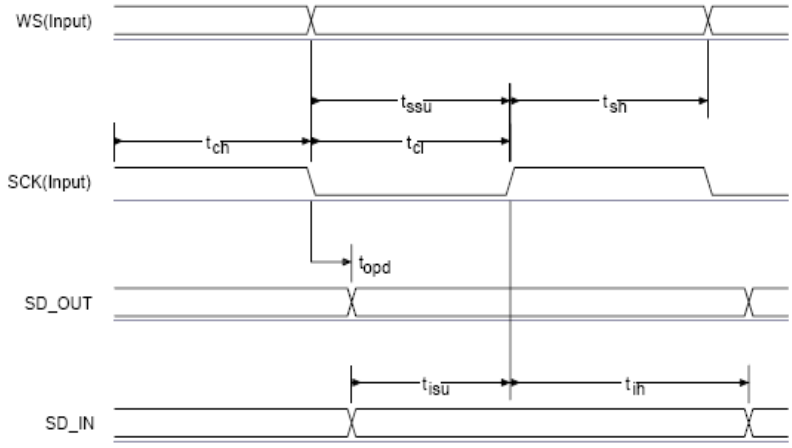

Fig. 11c) Digital audio Interface Slave Timing

Test equipment system diagram

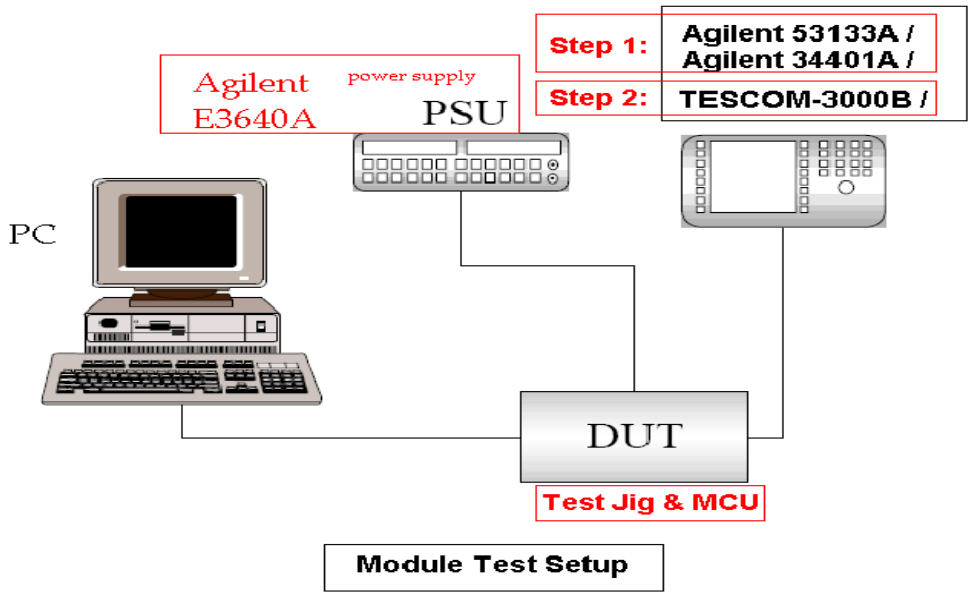

Fig. 13 RF test setup configure

Step 1:

(a) Stick the bar code label on the shield can, scan the bar code label for the unique BT address

(b) Setup the PC & Test Fixture, connect the COM port & +8V power supply unit

(c) Insert the BT module into the Fixture

(d) Download the RF & basic PSKEY to the module via UART interface

(e) Start the crystal trim, use the software program to trim the crystal value and log to a text file with the unique BT ID. Put the unique BD addr label on the BTR602 module.

(f) Check the PIOs, AIO, +1.8V output, UART & SPI by the software testing program

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(g) Log and record the results into the text file

Step 2:
(h) Scan the bar code label for the unique BT address
(i) Start the conductive RF test and log the result to a text file (refer to AWV Conductive RF Test)
(j) Log and record the results into the text file
Step 3:
(k) Scan the bar code label for the unique BT address
(l) Write the PSKEYs (unique BT address, crystal trim value & crystal frequency) into the EEPROM
(m) Check the EEPROM by the external MCU to verify the written PSKEYs are corrected or not, put the crystal trim value label on the BTR602 module

Step 4:
(n) Scan the bar code label for the unique BT address
(o) visual check the BTR602 module and read the EEPROM value to confirm that it is matched between the BD addr label and EEPROM information per each module. Failed module will be collected and analyzed by the engineers.
(p) Log and record the MP products into the text file before deliver out

Power Consumption [TBC]

Referent current consumption(different HCI settings):

Voltage Supplies = 1.8V (internal regulator converts to 1.5V supply domain)
Temperature = 25°C
Frequency = 2.441GHz

Mode	Average	Peak	Unit
SCO connection HV3 (30ms interval sniff mode)(slave)	16	25	mA
SCO connection HV3 (30ms interval sniff mode)(Master)	17	27	mA
SCO connection HV3 (no sniff mode)(slave)	23	30	mA
SCO connection HV1 (Slave)	37	40	mA
SCO connection HV1 (Master)	37	40	mA
ACL data transfer 115.2kbps UART (Master)	9	15	mA
ACL data transfer 115.2kbps UART (slave)	17	20	mA
ACL data transfer 921kbps UART (Master or slave)	30	37	mA
ACL connection, sniff mode 40ms interval, 38.4kbps UART	1.6	5	mA
ACL connection, sniff mode 1.28s interval, 38.4kbps UART	0.2	2	mA
Parked Slave, 1.28s beacon interval, 38.kpbs UART	0.28	1	mA
Standby Mode (Connected to host, no RF activity)	40	150	µA
Reset (RESET high or RESETB low)	39	120	µA

Table. 13 HCI current consumption

Measured current consumption(overall):

Voltage Supplies =1.8V (internal regulator converts to 1.5V supply domain)
Temperature = 25°C
Frequency = 2.402GHz to 2.480GHz (hopping)

- standby current consumption: ~ 0.8mA
- pairing current consumption: ~ 35mA

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- A2DP audio streaming connected current consumption: ~ 45mA
- Headset/Handsfree connected current consumption: ~ 40mA

Remark: connect to PC via UART interface with the IVT software tool, HCI module can perform some different BT profiles function like A2DP, SPP, HID & HS/HF,,etc when connected to the IVT software tool.

Electrical Characteristics [TBC]

ESD Precautions:

The BTR602 module should be applied ESD handling precautions during PCBA manufacturing proceed.

Absolute Maximum Ratings:

Storage Temperature		Min	Max	Unit
Core Supply	+1.5V supply rail	-0.4	1.6	V
IO volage	+3.3V supply rail	-0.4	3.6	V
Supply voltage	+1.5V internal regulator input	-0.4	2.6	V
	+1.8V internal regulator input, VREG_EN	-0.4	4.9	V
Other terminal voltages		Vss – 0.4	Vdd + 0.4	V

Recommended Operating Conditions:

Operating Temperature Range		Min	Max	Unit
Core Supply	+1.5V supply rail	1.4	1.6	V
IO volage	+3.3V supply rail	1.7	3.6	V

+3.3V Linear Regulator Conditions:

Normal Operation	Min	Typ	Max	Unit
Input voltage	2.7	3.3	4.9	V
Output voltage (I = 70mA, Vdd =+3.3V)	1.7	1.8	1.9	V
Temperature coefficient	-250	0	250	ppm/°C
Output noise (freq. Range 100Hz to 100kHz, reg. Output connected to 100nF and 10uF 2.2 ohm ESR capacitors)	0	0.5	1	mV rms
Load regulation (I = 70mA)	40	45	50	mV/A

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Settling time (1mA to 70mA pulse load, reg. Output connected to 100nF and 10uF 2.2 ohm ESR capacitors)	30	50	100	µS
Maximum output current	60	70	75	mA
Minimum load current	5	8	15	µA
Quiescent current (excluding load, I < 1mA)	30	40	60	µA
Deep Sleep Mode Operation				
Quiescent current (excluding load, I < 100µA)	10	13	21	µA
Standby Mode				
Quiescent current	1.5	2.5	3.3	µA

+1.8V Linear Regulator Conditions:

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.7	1.8	2.6	V
Output voltage (I = 70mA, Vdd =+1.7V)	1.4	1.5	1.6	V
Temperature coefficient	-250	0	250	ppm/^{o}C
Output noise (freq. Range 100Hz to 100kHz, reg. Output connected to 100nF and 10uF 2.2 ohm ESR capacitors)	0	0.5	1	mV rms
Load regulation (I = 70mA)	40	45	50	mV/A
Settling time (1mA to 70mA pulse load, reg. Output connected to 100nF and 10uF 2.2 ohm ESR capacitors)	30	50	100	µS
Maximum output current	60	70	75	mA
Minimum load current	5	8	15	µA
Quiescent current (excluding load, I < 1mA)	50	90	150	µA
Deep Sleep Mode Operation				
Quiescent current (excluding load, I < 100µA)	6	10	17	µA

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Standby Mode				
Quiescent current	1.5	2.5	3.3	µA

Digital part:

Digital Terminals	Min	Typ	Max	Unit
Input Voltage Levels				
Input logic level low	-0.4	0	0.25xVdd	V
Input logic level high	0.7xVdd	2.5	Vdd+0.3	V
Output Voltage Levels				
Output logic level low (I = 4mA)	0	0	0.12	V
Output logic level high(I = -4mA)	Vdd-0.4	Vdd-0.1	Vdd	V
Input and Tri-state Current with:				
Strong pull up	-100	-40	-10	µA
Strong pull down	10	40	100	µA
Weak pull up	-5	-1	-0.2	µA
Weak pull down	0.2	1	5	µA
I / O pad leakage current	-1	0	1	µA
Input capacitance	1	3	5	pF

Crystal frequency input (reference clock input):

Clock Source	Min	Typ	Max	Unit
Crystal Oscillator				
Crystal Frequency (250kHz per one step)	26	26	26	MHz

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Frequency tolerance (at +25°C temperature)	-15	-	+15	ppm
Digital trim range (internal capacitance at min & max value)	5	6.2	8	pF
Trim step size (internal capacitance at min & max value)	0	0.1	0.1	pF
Transconductance	2	4	4	mS
Negative resistance (xtal = 26MHz, Co = 0.76pF. Cl = 8.5pF)	870	1500	2400	ohm

Reset levels:

Power on Reser	Min	Typ	Max	Unit
+1.5V falling threshold	1.13	1.25	1.3	V
+1.5V rising threshold	1.2	1.3	1.35	V
Hysteresis	0.05	0.1	0.15	V

RSSI ADC channel:

RSSI ADC(*)		Min	Typ	Max	Unit
Resolution		10	10	10	Bits
Input voltage range (LSB size = +1.5V/1024)		0	1.5	1.6	V
Accuracy (Guaranteed monotonic)	INL	-1	0	1	LSB
	DNL	0	1	1	LSB
Offset		-4	0	4	LSB
Gain Error		-0.2	0	0.2	%
Sample rate		680	690	700	S/s
Conversion time		2.7	2.75	2.8	μs
Input Bandwidth		90	100	110	kHz

* RSSI Analogue to Digital Converter: The ADC applies fast AGC. The ADC samples the RSSI voltage on a step by step base. The front end LNA gain will be changed refer to the measured RSSI value(receive), the 1st mixer input signal with a limited range. It improves the dynamic range of the receiver, enhancing RF performance in noisy limited environments.

32kHz External Reference Clock (deep sleep mode for power saving):

32kHz External Reference Clock	Min	Typ	Max	Units
Frequency	32748	32768	32788	Hz
Frequency deviation at 25°C	0	±10	±20	ppm
Frequency deviation at -30°C to 85°C	±140	±145	±150	ppm
Input high level,square wave	0.625 x 1.5	0.625 x 1.5	0.65 x 1.5	V
Input low level, square wave	0.4 x 1.5	0.425 x 1.5	0.425 x 1.5	V

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Duty cycle square wave	30	50	70	%
Rise and fail time	30	40	50	ns

* 32kHz External Reference Clock: A 32kHz clock can be implemented to either CLK_32K or AIO[0], refer to the PSKEY_DEEP_SLEEP_EXTERNAL_CLOCK_SOURCE. Once the external clock is implemented to the analog AIO [0] pad in the 1.5V supply domain, the digital signal would be limited as +1.5V maximum driven voltage.
If 32kHz clock is under 200ppm accuracy, the enhance power saving feature can be added.
* 32kHz crystal is a optional selection (external circuitry), if seeking the power saving mode, 32kHz crystal is a must. Otherwise, it can be NC.

Solder Profiles

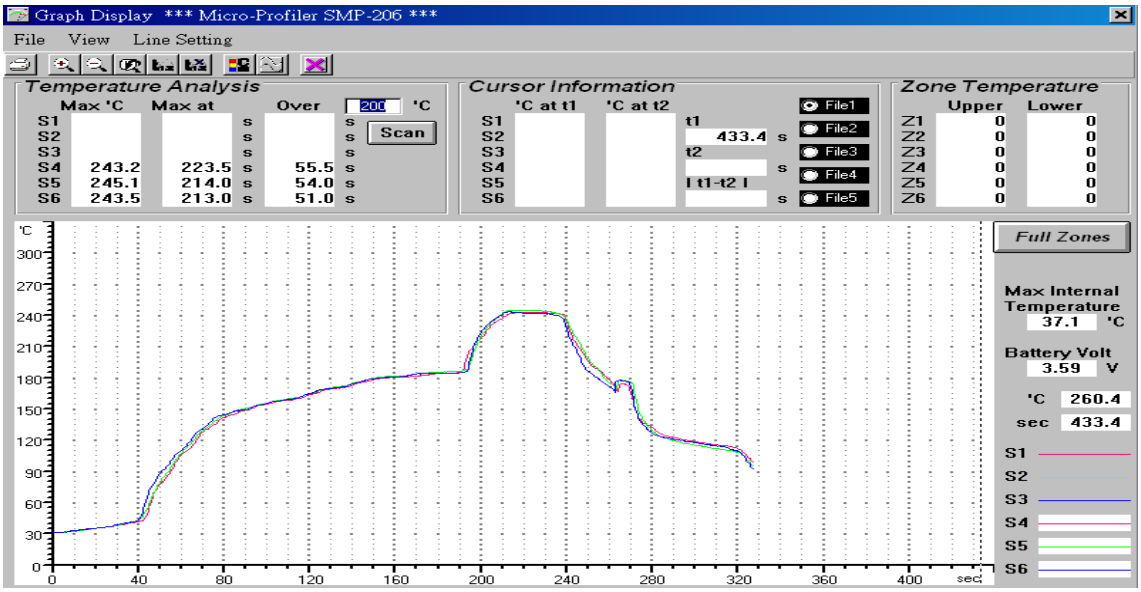
In order to setup your application, it is required to have the soldering profile which is based on various parameters.

Zone	Sensor	Description
Preheat Zone	1-2	This zone raises the temperature at a controlled rate. Generally 1~2.5°C/s.
Equilibrium Zone	3	This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone will need to be adjusted to optimize the out gassing of the flux. Generally 120~180s duration.
Reflow Zone	4	The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to inter-metallic growth which can result in a brittle joint.
Cooling Zone	5-6	The cooling rate should be fast, to keep the solder grains small which will give longer lasting joint. Generally 2~5°C/s.

Table 14. Soldering zones

** Normally, the components endure 2 times reflow & peak temperature around 255°C+/- 5°C.

Solder Re-Flow Profile for Devices with Lead-Free Solder Pads



Temperature Analysis at 200°C

Sensor	Max °C	Max at (s)	Over (s)
S4	243.2	223.5	55.5
S5	245.1	214	54
S6	243.5	213	51

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Fig. 14 Reflow soldering temperature

Hand soldering conditions:

- Maximum hand soldering points ≤ 8 (not included to remove the shield can)
- Maximum hand soldering times per each point(3~5 seconds) ≤ 4 with the solder iron temperature around 360℃ +/- 20℃

Moisture sensitivity devices caution label on MBB

This bag contains Moisture-Sensitive Devices (MSL 2)

Seal Date: DD/MM/YY

Appendix 1

Host transport configurations (PSKEY):

BCSP transport:

If PSKEY_HOST_INTERFACE selects use of BCSP then the UART's configuration register is set to the value of this PS key when it boots.

The UART configuration register is a bitfield:

Bit Meaning
0 0 => one stop bit, 1 => two stop bits.
1 0 => no parity bits, 1 => one parity bit.
2 0 => odd parity, 1 => even parity.
3 0 => h/w flow control disabled, 1 => enabled.
4 Set to 0.
5 0 => RTS deasserted, 1 => RTS asserted.
6 Set to 0.
7 0 => non-BCSP/H5 operation disabled, 1 => enabled.
8 Set to 0.
9 Set to 0.
10 Set to 0.
11 Set to 1.
12 0 => H5 operation disabled, 1 => enabled.
13 Set to 0.
14 Set to 0.
15 Set to 0.

The default value, 0x0806, selects use of BCSP mode and even parity.

In builds from HCI 18.X, this key replaces PSKEY_UART_CONFIG, PSKEY_UART_CONFIG_STOP_BITS, PSKEY_UART_CONFIG_PARITY_BIT, PSKEY_UART_CONFIG_FLOW_CTRL_EN, PSKEY_UART_CONFIG_RTS,

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PSKEY_UART_CONFIG_NON_BCSP_EN.

H4 transport:

If PSKEY_HOST_INTERFACE selects use of H4 then the UART's configuration register is set to the value of this PS key when it boots.
The UART configuration register is a bitfield and shares its format with PSKEY_UART_CONFIG_BCSP:

Bit Meaning
0 0 => one stop bit, 1 => two stop bits.
1 0 => no parity bits, 1 => one parity bit.
2 0 => odd parity, 1 => even parity.
3 0 => h/w flow control disabled, 1 => enabled.
4 Set to 0.
5 0 => RTS deasserted, 1 => RTS asserted.
6 Set to 0.
7 0 => non-BCSP/H5 operation disabled, 1 => enabled.
8 Set to 0.
9 Set to 0.
10 Set to 0.
11 Set to 1.
12 0 => H5 operation disabled, 1 => enabled.
13 Set to 0.
14 Set to 0.
15 Set to 0.

The default value, 0x08a8, selects use of hardware flow control, as required by the H4 specification.

In builds from HCI 18.X, this key replaces PSKEY_UART_CONFIG, PSKEY_UART_CONFIG_STOP_BITS, PSKEY_UART_CONFIG_PARITY_BIT, PSKEY_UART_CONFIG_FLOW_CTRL_EN, PSKEY_UART_CONFIG_RTS, PSKEY_UART_CONFIG_NON_BCSP_EN.

H4DS transport:

If PSKEY_HOST_INTERFACE selects use of H4DS then the UART's configuration register is set to the value of this PS key when the system boots.

The UART configuration register is a bitfield:

Bit Meaning
0 0 => one stop bit, 1 => two stop bits.
1 0 => no parity bits, 1 => one parity bit.
2 0 => odd parity, 1 => even parity.
3 0 => h/w flow control disabled, 1 => enabled.

4 Set to 0.
5 0 => RTS deasserted, 1 => RTS asserted.
6 Set to 0.
7 0 => non-BCSP/H5 operation disabled, 1 => enabled.
8 Set to 0.
9 Set to 0.
10 Set to 0.
11 Set to 1.
12 0 => H5 operation disabled, 1 => enabled.
13 Set to 0.
14 Set to 0.
15 Set to 0.

The default value, 0x08a8, selects use of hardware flow control, as required by the H4 (sic) specification.

H5 transport:

If PSKEY_HOST_INTERFACE selects use of H5 then the UART's configuration register is set to the value of this pskey when it boots.

The UART configuration register is a bitfield:

Bit Meaning
0 0 => one stop bit, 1 => two stop bits.
1 0 => no parity bits, 1 => one parity bit.
2 0 => odd parity, 1 => even parity.
3 0 => h/w flow control disabled, 1 => enabled.
4 Set to 0.
5 0 => RTS deasserted, 1 => RTS asserted.
6 Set to 0.
7 0 => non-BCSP/H5 operation disabled, 1 => enabled.
8 Set to 0.
9 Set to 0.
10 Set to 0.
11 Set to 1.
12 0 => H5 operation disabled, 1 => enabled.
13 Set to 0.
14 Set to 0.
15 Set to 0.

(The "H5" host transport protocol is properly known as the "Three Wire Uart Transport Layer", but is commonly known as H5 within CSR.)

In builds from HCI 18.X, this key replaces PSKEY_UART_CONFIG, PSKEY_UART_CONFIG_STOP_BITS, PSKEY_UART_CONFIG_PARITY_BIT, PSKEY_UART_CONFIG_FLOW_CTRL_EN, PSKEY_UART_CONFIG_RTS, PSKEY_UART_CONFIG_NON_BCSP_EN.

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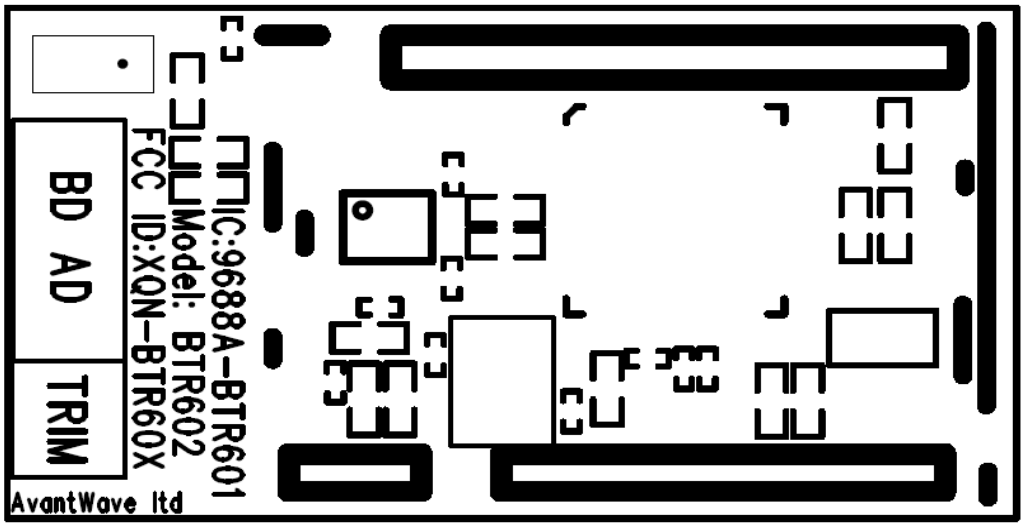
Appendix 2 [TBC]



BTR602 module silkscreen photos:

Fig. 15 BTR602 module top layer silkscreen

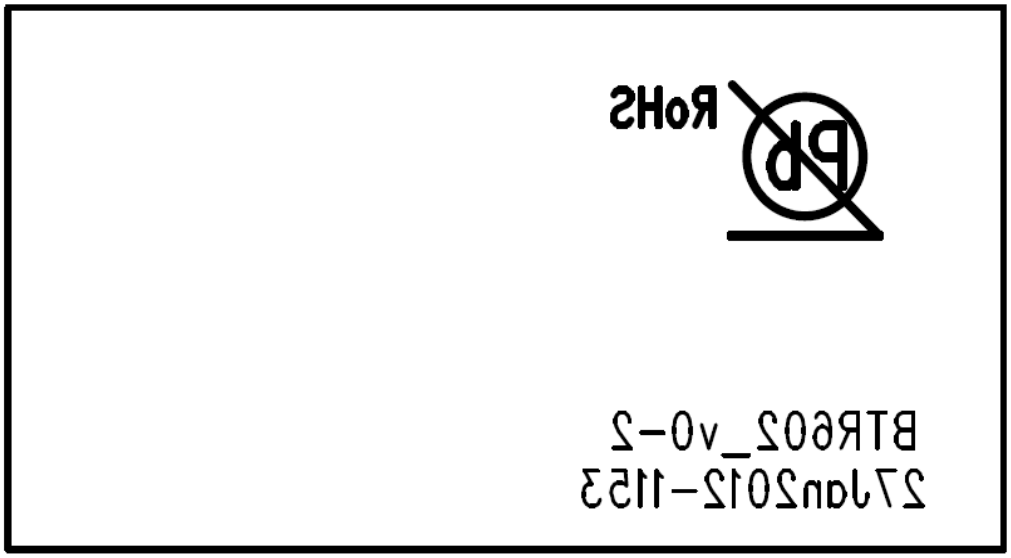


Fig. 16 BTR602 module bottom layer silkscreen

BTR602 approval certification ID:

- QD ID: BXXXXXX (Bluetooth SIG qualified design ID), XXXXXX = 018099

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- FCC ID: XXX-product code, Federal Communications Commission Identification, an FCC ID has 2 elements. The first is a three-character Grantee Code which begins with a alphabetic character and does not contain 1s or 0s. The FCC permanently assigns this code to a company for authorization of radio frequency equipment. It represents the Grantee or Applicant and each manufacturer has its unique Grantee Code. The second FCC ID element is the Product Code, which can include hyphens and dashes. An FCC ID is proof that the equipment and its manufacturer complies with the FCC-specified technical standards.
- IC: Industry Canada, certification of equipment means only that the equipment has met the requirements of the noted specification. License applications, where application to use certified equipment, are acted on accordingly by the issuing office and will depend on the existing radio environment, service and location of operation. This certification is issued on condition that the holder complies and will continue to comply with the requirements of the radio standards specifications and procedures issued by the Department(IC).

The certification number is made up of a Company Number (CN) assigned by Industry Canada's Certification and Engineering Bureau followed by the Unique Product Number (UPN), assigned by the applicat.
IC: XXXXXX-YYYYYYYYYYY
Model: project code
9688A-BTR60X (is the certification number)
XXXXXX is the CN assigned bt Industry Canada, made of at most 6 alphanumneric character (A-Z, 0-9), including a letter at the end of the CN to distinguish between different company addresses;
YYYYYYYYYYY is the UPN assigned by the applicant, made of at most 11 alphanumneric characters (A-Z, 0-9); and the letters "IC" are to indicate the Industry Canada certification numnber, but are not part of the certification number.
Model: BTR602 (is the company project code)

Dimension outline:

[TBC]

Fig. 17 BTR602 module terminals & shapes of parts

Appendix 3

BTR 602 EEPROM Data ReadPacketFormat from EEPROM to PC

Aim:
Since there are some Bluetooth Configuration Parameter(BT address, Crystal Trim, Crystal Frequency) are required to read from EEPROM to PC through UART as a confirmation in production.
This document will interpret the packet format in how to Send Packet Cmd to MCU for reading the EEPROM data

Communication Port: UART, 38400,8N1

All Send Packet Cmd (BT address, Crystal Trim, Crystal Frequency) contain 10 bytes data and receiving 8 bytes EEPROM data.

- BT address

Send Packet Cmd:

0xf0,	//Header
0x00,	//EEPROM Address
0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,	//dummy
C_ CHKSUM	//checksum

ps: C_CHKSUM =0xff - (0xf0+0x00+0x00+0x00+0x00+0x00+0x00+0x00+ 0x00 +0x00) & 0x00ff;

Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09

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Data	0xf0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	C_CHKSUM

Table. 15 BT address send packet command

Receive Packet Cmd:
It will contains 8 bytes(i.e EEPROM address 0-7) to show the Bluetooth address

Receive Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Data	BT address(NAP_0)	BT address(NAP_1)	BT address(UAP)	BT address(LAP_0)	BT address(LAP_1)	BT address(LAP_2)	0x00(dummy)	C_CHKSUM(Rec)

Table. 16 BT address receive packet command

ps: C_CHKSUM(Rec) =0xff - (BT address(NAP_0)+BT address(NAP_1)+BT address(UAP)+BT address(LAP_0)+BT address(LAP_1)+BT address(LAP_2)+0x00) & 0x00ff;

e.g. read bluetooth address cmd, and suppose bluetooth address is 0008-e0-123456
Send : f0 00 00 00 00 00 00 00 0f
Receive : 00 08 e0 12 34 56 00 7b

- ## Crystal Frequency

Send Packet Cmd:

0xf0	//Header
0x08,	//EEPROM Address
0x00, 0x00,0x00, 0x00,0x00,0x00,0x00,	//dummy
C_CHKSUM	//checksum

ps: C_CHKSUM =0xff – (0xf0+0x08+0x00+0x00+0x00+0x00+0x00+0x00+0x00+0x00) & 0x00ff;

Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09
Data	0xf0	0x08	0x00	0x00	0x00	0x00	0x00	0x00	0x00	C_CHKSUM

Table. 17 Crystal frequency send packet command

Receive Packet Cmd:
It will contains 8 bytes(i.e EEPROM address 8-15) to show the Crystal Frequency

Receive Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Data	C_CRYFREQ_HIGHER_BYTE	C_CRYFREQ_LOWER_BYTE	0x00	0x00	0x00	0x00	0x00	C_CHKSUM(Rec)

Table. 18 Crystal frequency receive packet command

ps: C_CHKSUM(Rec) =0xff - (C_CRYFREQ_HIGHER_BYTE+C_CRYFREQ_LOWER_BYTE+0x00+0x00+0x00+ 0x00 +0x00) & 0x00ff;

e.g. read the crystal frequency and suppose its value is 16Mhz
Send : f0 08 00 00 00 00 00 00 07
Receive : 3e 80 00 00 00 00 41

- ## Crystal Trim Value

Send Packet Cmd:

0xf0	//Header
0x10,	//EEPROM Address
0x00,0x00,0x00, 0x00,0x00,0x00,0x00,	//dummy
C_CHKSUM	//chksum

ps: C_CHKSUM =0xff -(0xf0+0x10+0x00+0x00+0x00+0x00+0x00+0x00+0x00 +0x00) & 0x00ff;

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Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09
Data	0xf0	0x10	0x00	0x00	0x00	0x00	0x00	0x00	0x00	C_CHKSUM

Table. 19 Crystal trim value send packet command

Receive Packet Cmd:
It will contains 8 bytes(i.e EEPROM address 16-23) to show the Crystal Trim

Receive Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Data	C_CRYTRIM	0x00	0x00	0x00	0x00	0x00	0x00	C_CHKSUM(Rec)

Table. 20 Crystal trim value receive packet command

ps: C_CHKSUM(Rec) =0xff - (C_CRYTRIM+0x00+0x00+0x00+0x00+ 0x00 +0x00) & 0x00ff;

e.g. read the crystal trim and suppose its value is 29
Send : f0 10 00 00 00 00 00 00 ff
Receive : 1d 00 00 00 00 00 00 e2

Appendix 4

PCM configuration:

- default PCM configure: PSKEY_PCM_CONFIG32 is 0x00800000.

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit
CNT_RATE	[23:16]	Sets PCM_CLK count rate
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK

Table. 25 PSKEY_PCM_LOW_JITTER_CONFIG description

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Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 = master mode with internal generation of PCM_CLK and PCM_SYNC. 1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 = long frame sync (rising edge indicates start of frame). 1 = short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = sign-extension.
LSB_FIRST_EN	5	0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples.
TX_TRISTATE_EN	6	0 = drive PCM_OUT continuously. 1 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active. 1 = tri-state PCM_OUT after rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC while keeping PCM_CLK running. Some CODECS use this to enter a low power state.
GCI_MODE_EN	9	1 = enable GCI mode.
MUTE_EN	10	1 = force PCM_OUT to 0.
48M_PCM_CLK_GEN_EN	11	0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48MHz clock.
LONG_LENGTH_SYNC_EN	12	0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
PCM_SYNC_MULT	12	0 = Sync limit = SYNC_LIMIT x 8. 1 = SYNC_LIMIT.
-	[20:16]	Set to 0b00000.

Table. 26 PSKEY_PCM_CONFIG32 Description

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Appendix 5 [TBC]

Tray and module size:

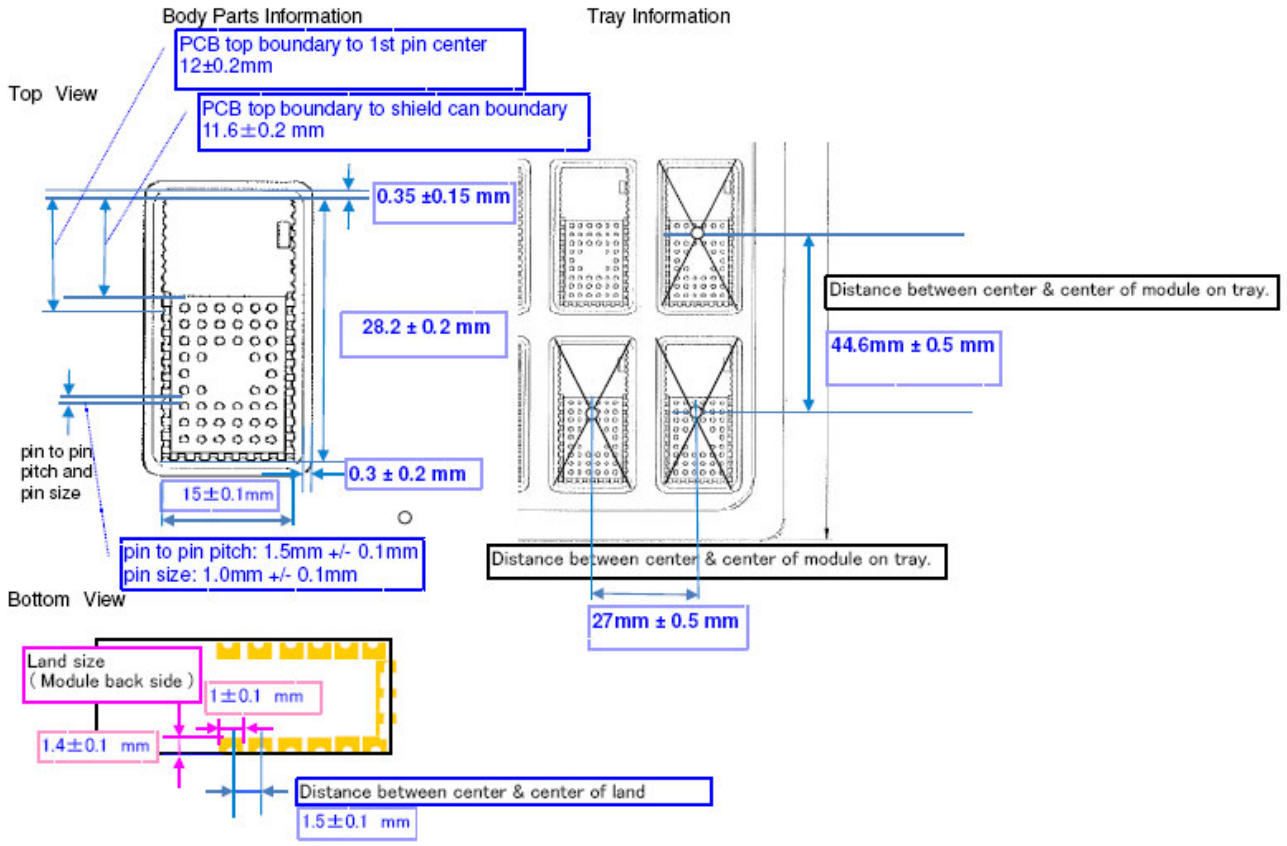

Fig. 18 a) module top & bottom view on the tray

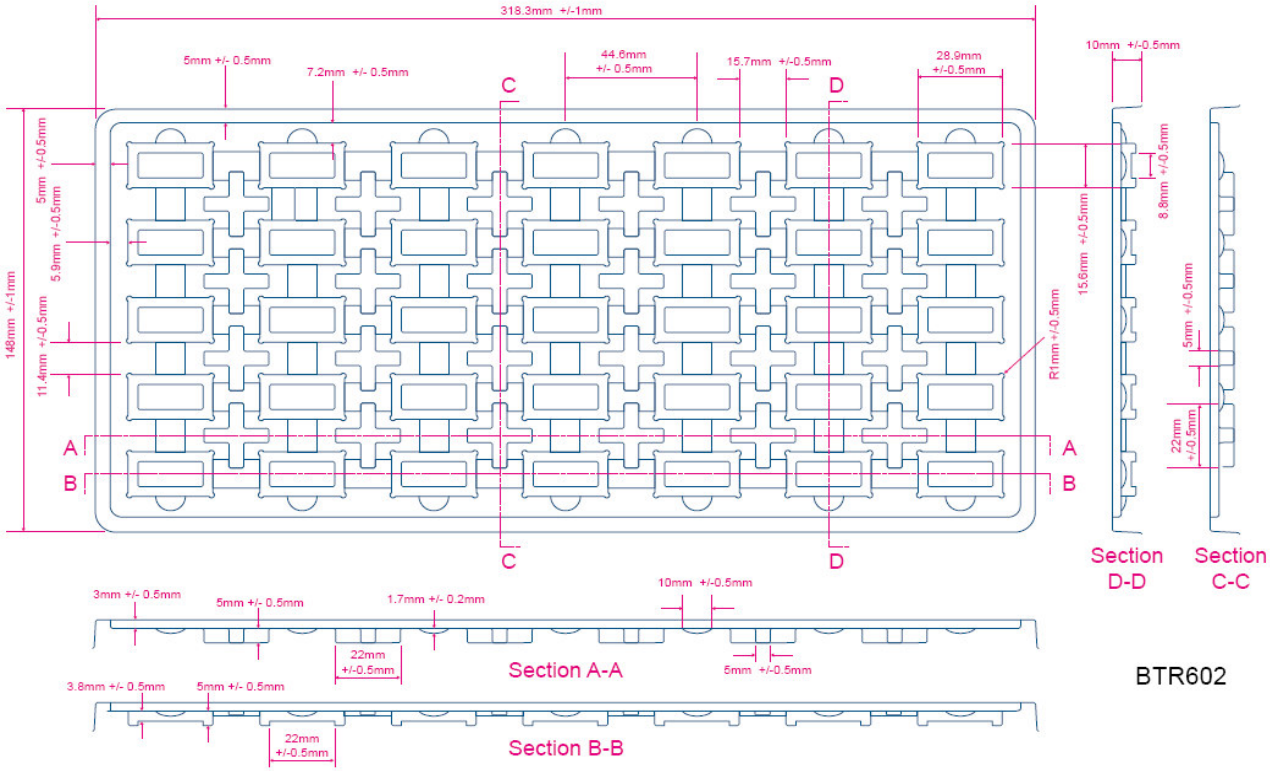

Fig. 18 b) tray dimensions

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Appendix 6 [TBC]

Label sticking

1. Refer to the BTR602 module golden sample in the SMT department, each worker can clearly know that what is the exact label sticking position.
2. In the Manufacturing Instruction (MI), it included two module photos to show out the position of bluetooth address and crystal trim value, Basically, those labels should be on the proper position that is point out at the MI.

Place the bluetooth address label within the "BD AD" white barrier.

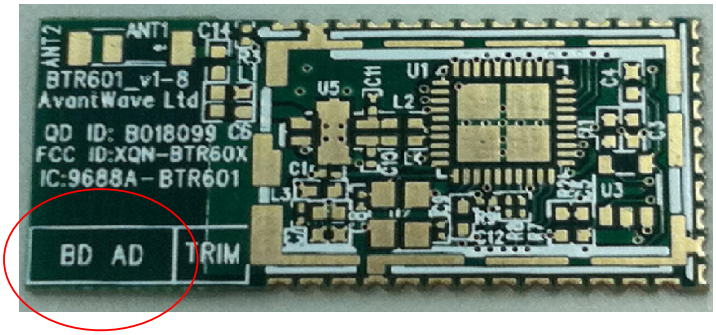

Fig. 19a bluetooth address label

Place the crystal trim value label within the "TRIM" white barrier.

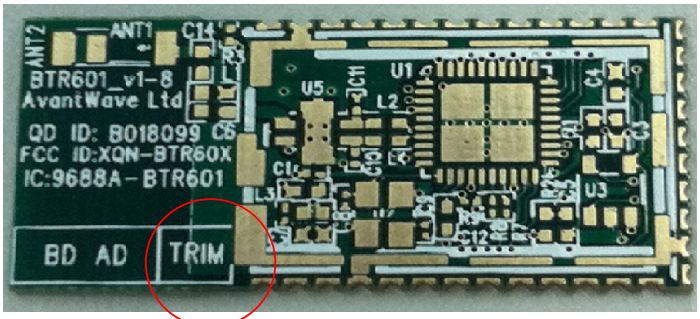

Fig. 19b crystal trim value label

Visual Check

1. Compare to the golden sample
2. After the testing procedure step 4, the worker will check the labels position are correct or not. If the label on the wrong position, the worker should be sticking again to meet the golden sample standard.

The stickers are compliant with RoHS standard self-adhesive label. The material of the label is mainly art paper.

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Appendix 7 [TBC]

Repaired module notification:

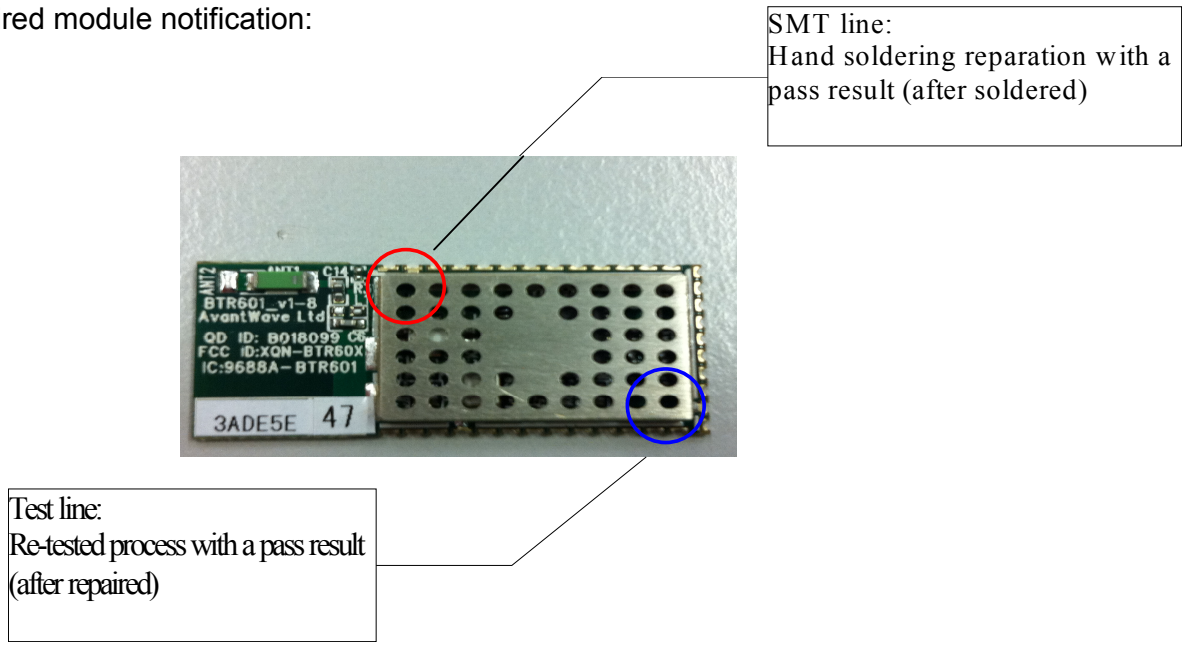

Fig. 20 repaired module marking point

mark standard

SMT line: red dot with around 3mm diameter

Testing line: blue dot with around 3mm diameter

marker type: Pilot Super Color Marker SCA-B or Pilot V Super Color (BeGreen) permanent marker SCA-VSC-MC (Chisel)

Remarks
Specifications subject to change without notice. All other trademarks mentioned are the property of their respective owners. This document shows outlined specification only. Please contact AvantWave upon evaluation and integration.

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FCC Compliance statements

Changes or modifications not expressly approved by the party responsible for compliance
could void the user's authority to operate the equipment.

This device complies with Part 15 of the FCC Rules.
Operation is subject to the following two conditions:
(1) this device may not cause harmful interference, and
(2) this device must accept any interference received,
including interference that may cause undesired operation

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.
If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
--Reorient or relocate the receiving antenna.
--Increase the separation between the equipment and receiver.
--Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
--Consult the dealer or an experienced radio/TV technician for help.

RF Radiation Exposure Information
Since the radiated output power of this device is far below the FCC radio frequency exposure limits, it is not subject to routine RF exposure evaluation
as per Section 2.1093 of the rules.

LABEL OF THE END PRODUCT:
The final end product must be labeled in a visible area with the following " Contains TX FCC ID: XQN-BTR60X".
If the size of the end product is larger than 8x10cm, then the following FCC part 15.19 statement has to also be available on the label:
This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions:
(1) this device may not cause harmful interference and
(2) this device must accept any interference received, including interference that may cause undesired operation.

IC statements

LABEL OF THE END PRODUCT:
The final end product must be labeled in a visible area with the following "Contains TX IC: 9688A-BTR601".

This Class B digital apparatus complies with Canadian ICES-003.
Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause
interference, and (2) this device must accept any interference, including interference that may cause
undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux

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appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions
suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit
accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en
compromettre le fonctionnement.

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