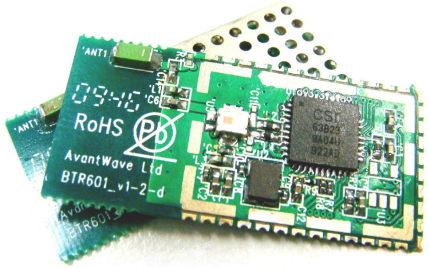
Datasheet
Bluetron™ Module
BTR601

Key Features

- **A small and cost effective Bluetooth® System**
- **Bluetooth® specification v2.1 +EDR compliant**
- **Class 2, up to 10-meter range**
- **Transmit RF power, up to +4dBm0**
- **Receive sensitivity, up to -85dBm@BER = 0.1%**
- **Complete 2.4GHz Bluetooth® System including:**
  - Hardware: Radio, Baseband ,Crystal, MCU, Regulators & ROM
  - Standard Firmware: HCI stack 23C
- **Integrated 1.8V & 1.5V regulators (linear mode)**
- **Compact size: 32.0 mm x 15.0 mm x 2.85 mm**
- **SDIO (Bluetooth type A) & UART @4Mbps interfaces**
- **Auristream Codec (16, 24, 32, 40kbps), transmit power is minimized**
- **Built-in PCM or I2S interfaces**
- **Surface mount module for embedded applications**
- **Chip Antenna on board or External antenna design**
- **IEEE 802.11 coexistence**
- **Green (RoHS & Halogen free)**
- **Operating & Storage temperature within -40° C to +85° C**



Bluetooth®

Description

Bluetron™ BTR601 module from AvantWave is a complete Bluetooth® solution for fast implementation, cutting your time-to-market. It is a short-range, compact and cost effective radio/baseband module that can be implemented in any kind of electronic devices, such as Bluetooth hands-free car kit, PDA and Mobile phone handset etc.

In standard configuration the module includes a baseband processor with on board 4M Bytes ROM memory, a radio front-end, supporting circuitry, able to connect with some higher-levels external software protocols and applications such as HSP, HFP, A2DP, AVRCP are coexisted with the external Host MCU (via I2S interface DAC codec).

The **Bluetron™ BTR601 module** is a power class 2 Bluetooth® device, and is in compliance with version 2.1 +EDR of the Bluetooth® specification. It is supplied with Bluetooth® HCI stack firmware which runs on the internal microprocessor. **Bluetron™ BTR601 module** is built on CSR BC06 QFN ROM core with ROM memory for firmware and application software storage.

Applications

- **Automotive Car Kit Applications**
- **PDAs**
- **Mobile Phones**
- **Cellular Handsets**

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Software

The lower layers of the Bluetooth stack (HCI) runs on-package. An external microcontroller is required. Bluetron™ BTR601 is integrated with a digital ADPCM low power CODEC, and interface to power management circuit.

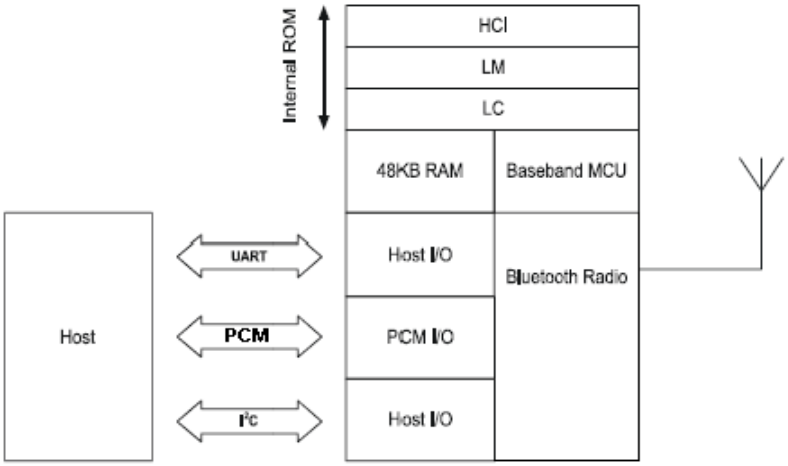

Fig. 1 System block diagram

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Mechanical Specification

Suggested Land Pattern:

Top view

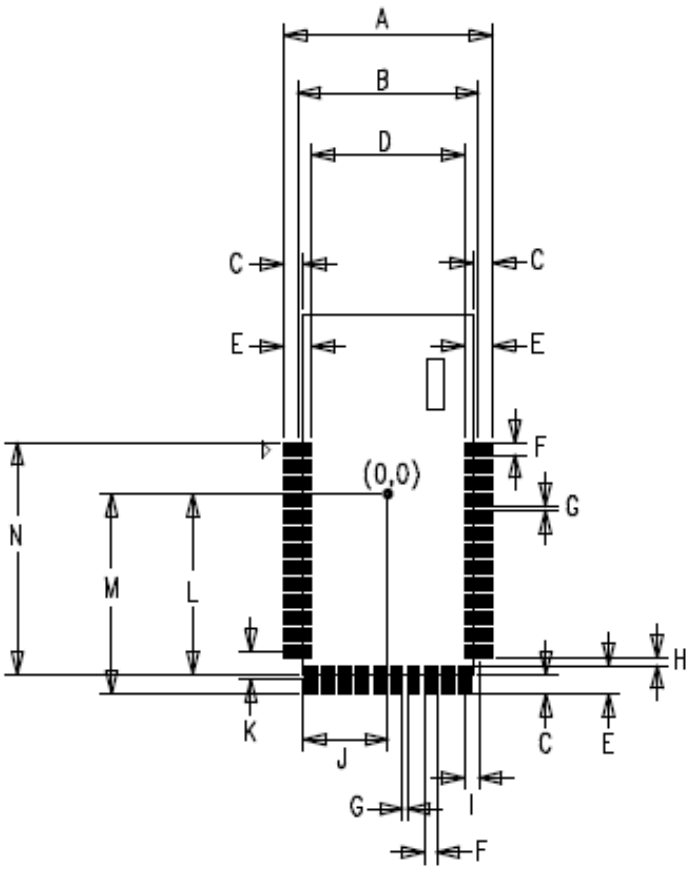

Fig.2 BTR601 module recommended PCB Land Pattern

Symbol	Dimension(mm)	Description
A	18.50	Outer width
B	16.00	Center width
C	1.75	Pad length outer from module edge
D	13.50	Inner width
E	2.50	Pad length
F	1.10	Pad width
G	0.40	Inner gap
H	0.70	Inner gap
I	1.30	Center pad to center pad
J	7.50	Module center to module edge
K	2.50	Center pad to center pad
L	16.00	Module center to module edge
M	17.70	Module center to pad edge
N	20.55	Module edge to pin1 edge

Table 1 Land Pattern Dimensions

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Sectional view

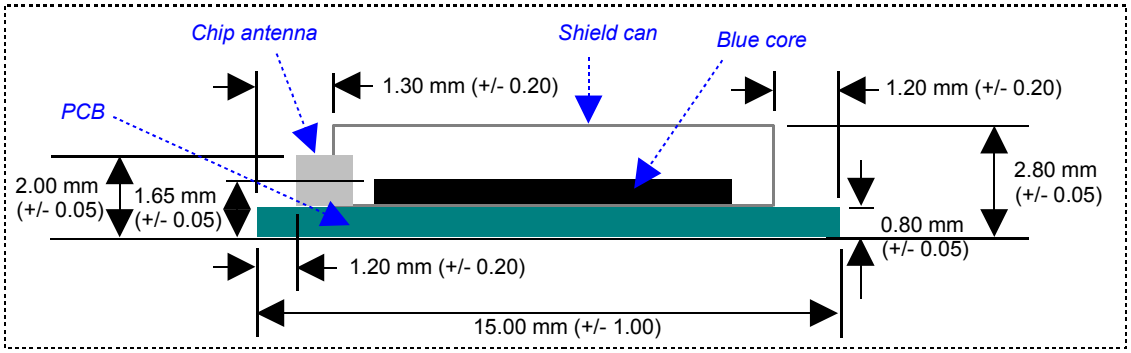

Fig. 3-1 side view (A)

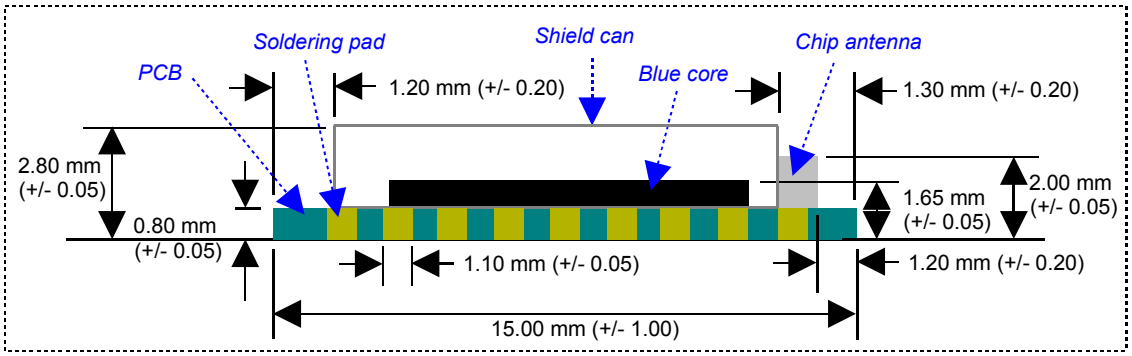

Fig. 3-2 side view (B)

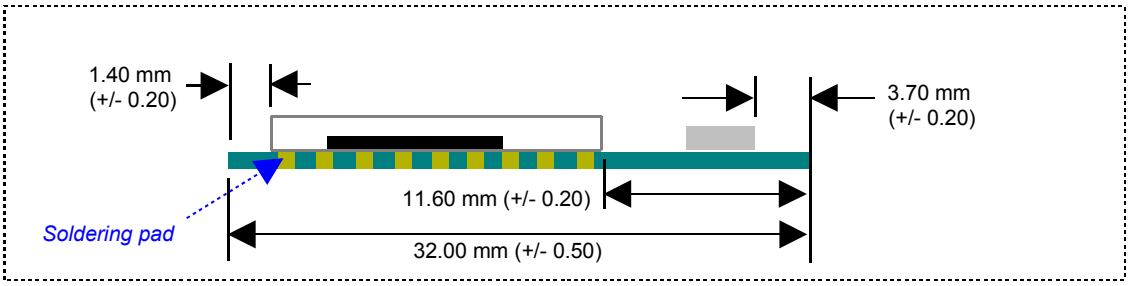

Fig. 3-3 side view (C)

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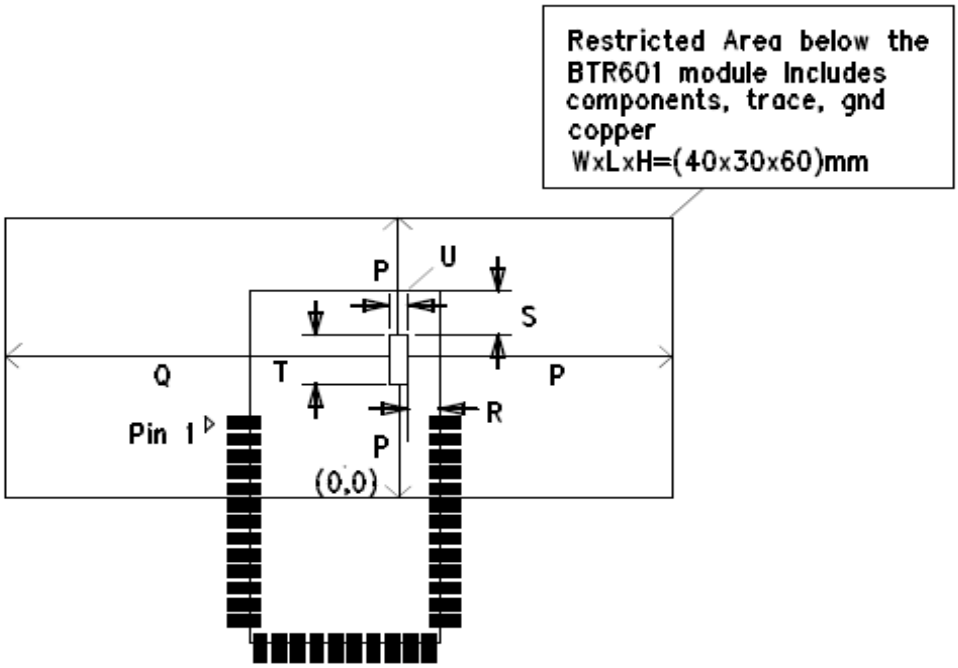

Fig.4 BTR601 module Antenna & its restricted area

Symbol	Dimension(mm)	Description
P	15.00	Antenna restricted area
Q	25.00	Antenna restricted area
R	1.0	Antenna edge to right side pcb edge
S	3.3	Antenna edge to top side pcb edge
T	4.2	Antenna pad to pad length
U	1.6	Antenna pad width

Table 2 restricted area dimensions

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Pin Assignment

Terminal	Name	Description
1	+1.5V	+1.5V voltage supply output
2	+1.8V	+1.8V voltage supply output
3	AIO[0]	Analog Programmable input/output line
4	GND	Ground pin
5	VREG_IN	voltage supply input
6	VREG_EN	Enable the high-ion LDO regulator, active high
7	PIO[1]	Programmable input/output line
8	PIO[2]	Programmable input/output line
9	PIO[3]	Programmable input/output line
10	PIO[4]	Programmable input/output line
11	PIO[5]	Programmable input/output line
12	PIO[7]	Programmable input/output line
13	PIO[9]	Programmable input/output line
14	/Reset	Reset pin, active low
15	GND	Ground pin
16	EEPROM_SDA	EEPROM serial address/data (input / output)
17	EEPROM_SCL	EEPROM serial clock input
18	EEPROM_WP	EEPROM write protect input
19	PCM_IN	PCM synchronous data input
20	PCM_OUT	PCM synchronous data output
21	PCM_CLK	PCM synchronous data clock
22	PCM_SYNC	PCM synchronous data sync
23	CLK_32K	32kHz external reference clock
24	SDIO_DATA[0]	Synchronous data input/output
	CSPI_MISO	CSPI data output
	UART_TX	UART data output, active high
25	SDIO_DATA[1]	Synchronous data input/output
	CSPI_INT	CSPI data input
	UART_RTS	UART request to send, active low
26	SDIO_DATA[2]	Synchronous data input/output

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Terminal	Name	Description
	UART_RX	UART data input, active high
27	SDIO_DATA[3]	Synchronous data input/output
	CSPI_CS#	Chip select for CSPI, active low
	UART_CTS	UART clear to send, active low
28	SDIO_CLK	SDIO Clock
	CSPI_CLK	CSPI Clock
29	SDIO_CS	SDIO chip select to allow SDIO Accesses
30	SDIO_CMD	SDIO data input
	CSPI_MOSI	CSPI data input
31	SPI_MISO	SPI data output
32	SPI_CLK	SPI clock
33	SPI_CSB	Chip select for SPI, active low
34	SPI_MOSI	SPI data input
35	GND	Ground pin
36	ANT	50 ohm impedance RF port

Table 3 Pin Description

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Reference Circuit

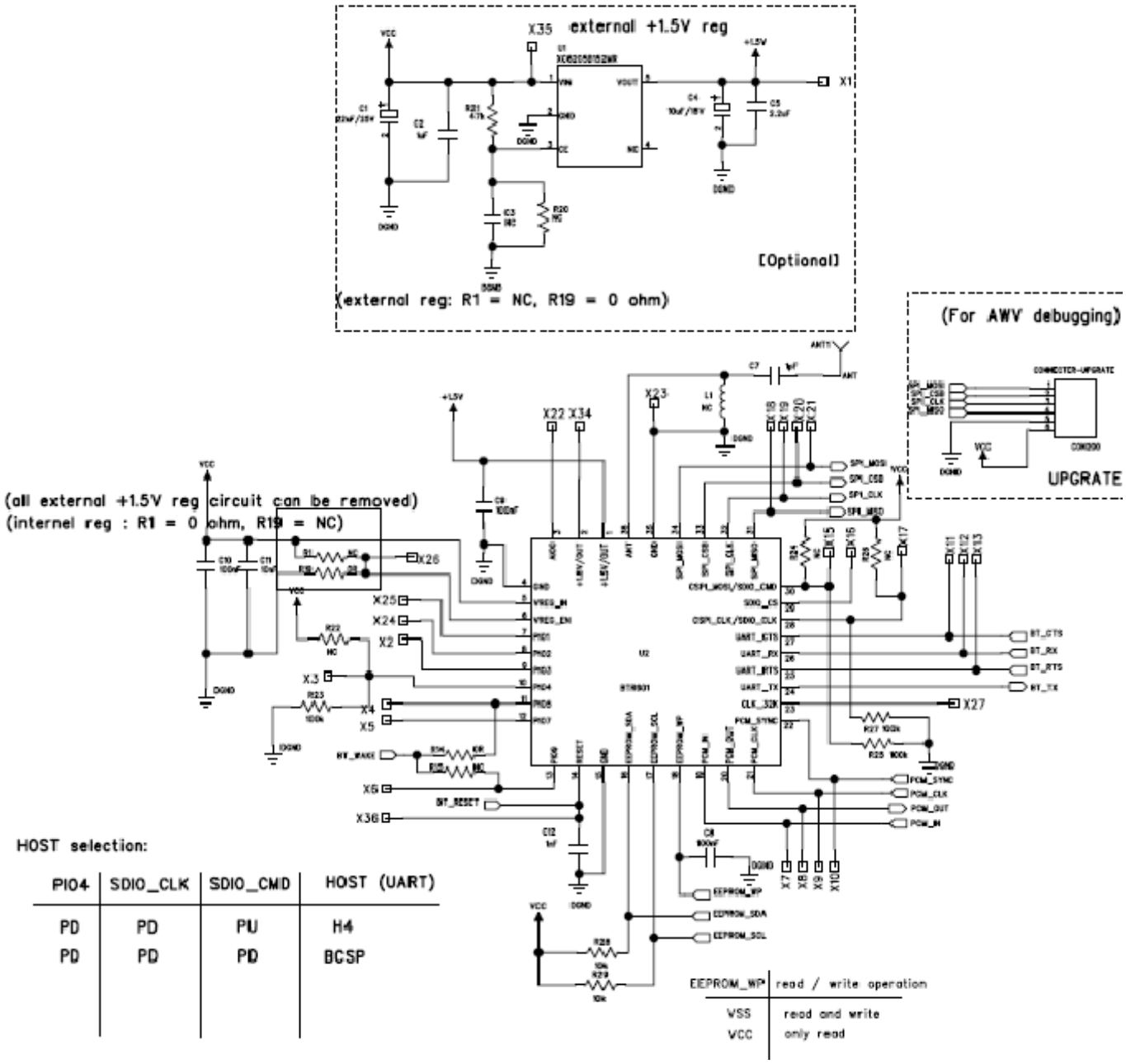

Fig.5 BTR601 module reference cicuit

AIO & PIO depend on the application will be pull up or down, otherwise it will be open connection.

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General Specifications

	Minimum	Typical	Maximum
Supply Voltage: VREG_IN	-0.4V	3.3V	4.9V
High Voltage Regulator Output (I_{load} = 70 mA)	1.7V	1.8V	1.9V
Low Voltage Regulator Output (I_{load} = 70 mA)	1.4V	1.5V	1.6V
Operating Temperature range	-40°C	25°C	85°C
Storage Temperature range	-40°C(*)	25 °C	85°C(*)
Frequency Range	2.402 GHz	2.441 GHz	2.480 GHz
Crystal Frequency	14.4MHz	26MHz	26MHz
AFH	-	79 channels	-
Channel Bandwidth (Basic rate / Enhanced data rate)	-	1Mbps / 2 or 3Mbps	-
Internal ROM / RAM	-	4MB / 48KB	-

Table 4 General Specifications

Remark: (*) assume all components are soldered on the module PCB, although all components can be stored in between -40 to 85°C, but not recommend to store this module in the extreme temperature before it has soldered on the application PCB. The device is turn off but the environment also in between -40 to 85°C, assume it is able to sustain the extreme temperature. Most of the components on the module can sustain the storage temperature between -40 to 85°C.

We have passed the high/low temperature test for operated at -40 to 85°C, and most of the components have -40 to 85°C storage temperature

RF Specifications (Basic Data Rate)

Voltage Supplies = 1.5V
Temperature = 25°C
Frequency = 2.441GHz

Receiver	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity (DH1/3/5) at 0.1% BER	-	-84	-86	≤-70	dBm
Maximum received signal at 0.1% BER	-	3	-	≥-20	dBm
C/I Co-channel		9	-	≤11	dB
C/I Adjacent channel (f = f_0 +/- 1MHz)	-	-4	-	<0	dB
C/I Adjacent channel (f = f_0 +/- 2MHz)	-	-40	-	≤-40	dB
C/I Adjacent channel (f = f_0 - 3MHz)	-	-45	-	≤-40	dB
C/I Adjacent channel (f = f_0 - 5MHz)	-	-45	-	≤-40	dB
C/I Image rejection (carrier –3MHz)	-	-20	-	≤-9	dB
Transmitter	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Average Output Power	-	0	4	-6 to +4	dBm
20dB bandwidth	-	950	-	≤ 1000	kHz
2nd ACP (+/-2MHz)	-	-35	-	≤ -20	dBc
3rd ACP (+/-3MHz)	-	-55	-	≤ -40	dBc

Table 5 Basic Data Rate

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RF Specifications (Enhanced Data Rate)

Voltage Supplies = 1.5V
Temperature = 25°C
Frequency = 2.441GHz

Receiver	Modulation	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity (DH1/3/5) at 0.01% BER	π/4 DQPSK 8DPSK	-	-83 -78	-	⩽-70	dBm
Maximum received signal at 0.1% BER	π/4 DQPSK 8DPSK	-	0	-	-20	dBm
C/I Co-channel at 0.1% BER	π/4 DQPSK 8DPSK		10 19	-	⩽13 ⩽21	dB
C/I Adjacent channel (f = f_0 +/- 1MHz)	π/4 DQPSK 8DPSK	-	-10 -5	-	⩽0 ⩽5	dB
C/I Adjacent channel (f = f_0 +/- 2MHz)	π/4 DQPSK 8DPSK	-	⩾-40	-	⩾-30 ⩽-25	dB
C/I Adjacent channel (f = f_0 + 3MHz)	π/4 DQPSK 8DPSK	-	-45	-	⩽-40 ⩽-33	dB
C/I Adjacent channel (f = f_0 - 5MHz)	π/4 DQPSK 8DPSK	-	-45	-	⩽-40 ⩽-33	dB
C/I Image rejection (carrier –3MHz)	π/4 DQPSK 8DPSK	-	-20 -15	-	⩽-7 ⩽0	dB
Transmitter		**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Average Output Power		-	0	4	-6 to +4	dBm
Relative Transmit Power		-	0		-4 to +1	dB
In-band spurious emissions	f = f_0 +/- 1MHz f = f_0 +/- 2MHz f = f_0 +/- 3MHz	- - -	-35 ⩾-34 ⩾-50	- - -	⩽-26 ⩽-20 ⩽-40	dbm
π/4 DQPSK Modulation Accuracy	Peak DEVM	-	19	-	⩽35	%
8DPSK Modulation Accuracy	Peak DEVM	-	17	-	⩽25	%
EDR Differential Phase Encoding		99	No errors	-	⩾99	%

Table 6 Enhanced Data Rate

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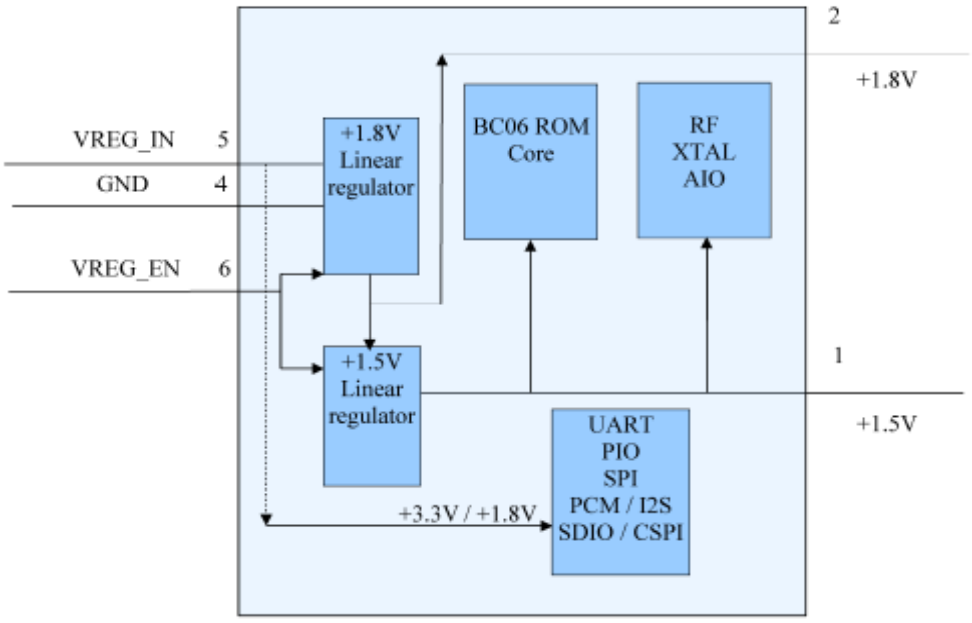
Power Control & Regulation



BTR601 BC06 QFN ROM Power Management Block Diagram

Fig. 6

VREG_EN (step down LDO regulator enable): Up to +4.9V dc voltage input
VREG_IN (positive supply for UART, PIOs, PCM/I2S, SPI & SDIO/CSPI) : typically +3.3V dc voltage input (can change to +1.8V dc depends on different applications)
VREG_OUT

•option 1 (+3.3V input, +1.8V output & +1.5V output):

=> input +3.3V to VREG_IN & VREG_EN, use the internal +1.8V & +1.5V regulator, +1.8V & 1.5V become the outputs

• option 2 (+1.8V input & +1.5V input):
=> input +1.8V to VREG_IN , use the external +1.5V input
•option 3 (+3.3V input & +1.5V input):
=> input +3.3V to VREG_IN, use the external +1.5 input
•option 4 (+1.8V input & +1.5V output):

=> input +1.8V to VREG_IN & VREG_EN, use the internal+1.8V & +1.5V regulator, +1.5V become the output, but +1.8V output may not as equal to +1.8V (-0.2V tolerance due to votlage drop.)

Remark: - If VREG_ IN to +1.8V, all the UART, PIOs, PCM/I2S, SPI & SDIO/CSPI are set to +1.8V.
- If +1.5V is output, the maximum output current is lower than 70mA.
- Option 1 is default setting, option 4 is not recommend to use.

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Power sequence (+3.3V, +1.5V & reset)

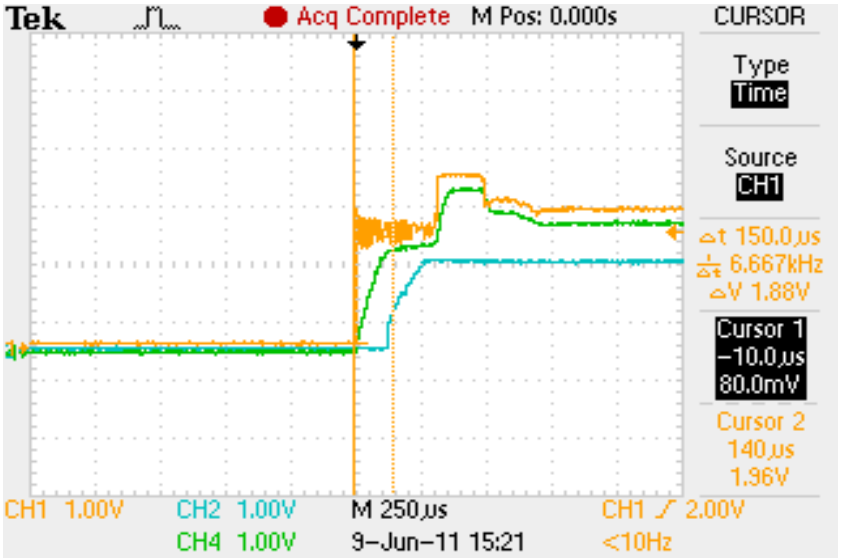

Fig. 7 initial power sequence

CH1 is +3.3V, VREG_EN
CH2 is +1.5V
CH4 is RESET#

Sequence: CH1 => CH4 => CH2

EEPROM Connection

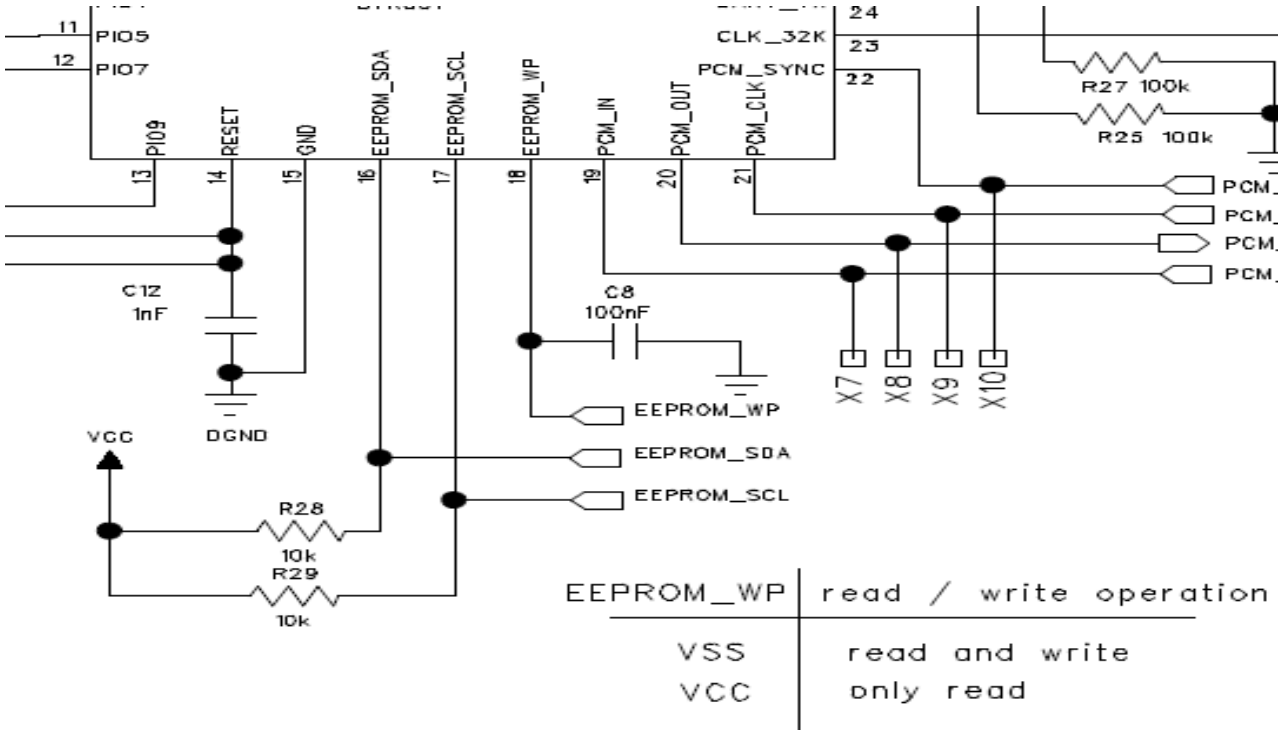

Fig. 8 EEPROM connection

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Pin16 EEPROM_SDA: It is a bidirectional pin for transfer addresses and data in/out of the device, Due to the open-drain output, the SDA port need a pull up resistor to Vcc (10k ohm for 100kHz, 2k ohm for 400kHz). SDA bus is only able to change during SCL low. Changes during SCL high are reserved for indication Start and Stop bit status.

Pin17 EEPROM_SCL: SCL input is assigned to synchronize the data transfer to and from the device.

Pin18 EEPROM_WP: Write protect(WP) input pin is selected by the external device to define the EEPROM is able to write or not.
If tied it to Vss, memory operation(write/read) is enabled normally. If tied it to Vcc, write operation is disabled and read operation is enabled.

Host Interface Selections

Select UART, SDIO or CSPI Host Interface by the hardware configurable method:

(PIN10) PIO	Input	Connection	Host
4	High	100k ohm to Vcc	SDIO / CSPI
4	Low	100k ohm to GND	UART

Table 7. PIO 4 selections

Select UART Protocols by the hardware configurable method:

(PIN28) SDIO_CLK	Connection	(PIN30) SDIO_CMD	Connection	UART protocol
Low	100k ohm to GND	Low	100k ohm to GND	BCSP
Low	100k ohm to GND	High	100k ohm to Vcc	H4
High	100k ohm to Vcc	Low	100k ohm to GND	H4DS
High	100k ohm to Vcc	High	100k ohm to Vcc	H5

Table 8. UART protocol selections

UART connection:

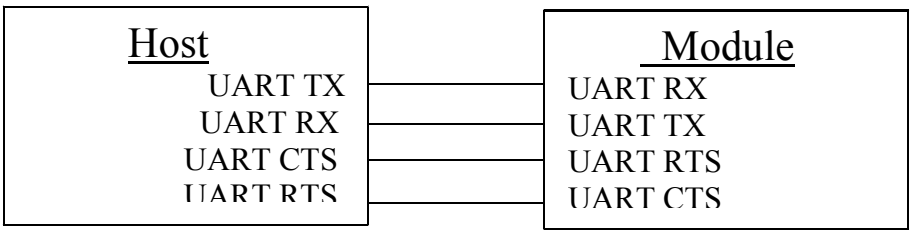

Fig. 9 UART connection method

BCSP => CSR proprietary, reliable alternative to the standard bluetooth UART Host Transport.
H4DS => CSR proprietary, alternative to the standard bluetooth UART Host Transport, it supports deep sleep mode for low-power applications.
H4 => a transport protocol for bluetooth HCI packets over UART, the name came from bluetooth spec appendix H4.

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H5 => a three-wire protocol, presumably based on CSR's BCSP protocol.

UART operation => Set the hardware configurable pins (PIO4, SDIO_CLK & SDIO_CMD), if hardware configurable selection is BCSP transport(PIO4 is low, SDIO_CLK is low & SDIO_CMD is low), the baudrate is auto detected. The UART connection method is referent to fig. 8.
=> UART_RX should pull up to Vcc via a 10k ohm resistor. UART_TX is already internal pull up. UART_CTS & UART_RTS is NC.

e.g default BCSP(0x0806) is configured to 8bit length, no hardware flow control, even parity bit. The parameter details can refer to the Appendix 1. The other default transport settings (H4, H4DS & H5 parameter) please refer to the Appendix1. All settings(PSKEY) can be changed by the external MCU via UART channel. Both the transports with auto detected baudrate and same connection method.

UART Settings:

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table. 9 UART configurable value

PCM or I2S interface connections:

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table. 10 PCM & I2S interfaces pin assignment

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I2S interface (WS, SCK, SD_OUT):

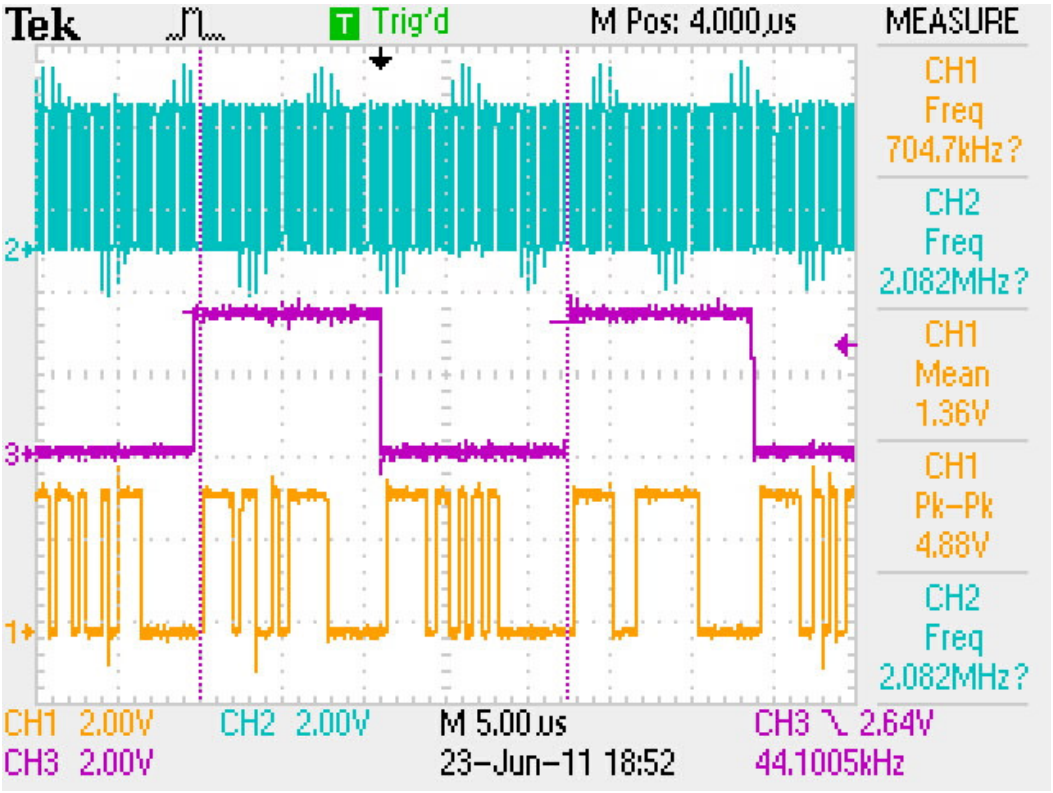

Fig. 10 I2S interface waveform

ch1 => data
ch2 => bit clcok
ch3 => L/R clock => 44.1kHz

Remark: audio source is iphone3Gs, a MP3 song.

Bit	Mask	Name	Description
D[0]	0x0001	CONFIG_JUSTIFY_FORMAT	0 for left justified, 1 for right justified.
D[1]	0x0002	CONFIG_LEFT_JUSTIFY_DELAY	For left justified formats: 0 is MSB of SD data occurs in the first SCLK period following WS transition. 1 is MSB of SD data occurs in the second SCLK period.
D[2]	0x0004	CONFIG_CHANNEL_POLARITY	For 0, SD data is left channel when WS is high. For 1 SD data is right channel.
D[3]	0x0008	CONFIG_AUDIO_ATTEN_EN	For 0, 17 bit SD data is rounded down to 16 bits. For 1, the audio attenuation defined in CONFIG_AUDIO_ATTEN is applied over 24 bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0.
D[7:4]	0x00F0	CONFIG_AUDIO_ATTEN	Attenuation in 6 dB steps.
D[9:8]	0x0300	CONFIG_JUSTIFY_RESOLUTION	Resolution of data on SD_IN, 00=16 bit, 01=20 bit, 10=24 bit, 11=Reserved. This is required for right justified format and with left justified LSB first.
D[10]	0x0400	CONFIG_16_BIT_CROP_EN	For 0, 17 bit SD_IN data is rounded down to 16 bits. For 1 only the most significant 16 bits of data are received.

Table. 11 I2S interface configurable PSKEY

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BC06 Master mode I2c(PSKEY_DIGITAL_AUDIO_CONFIG): 0x0006

=> D[1] & D[2] is 1, others are 0

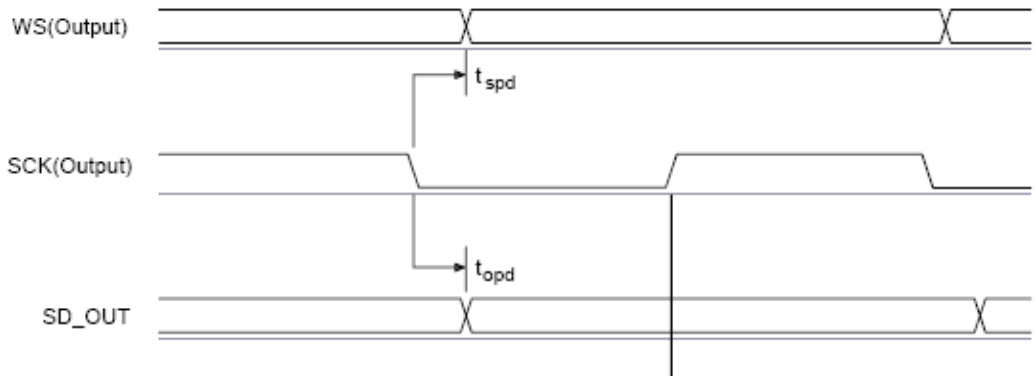

Fig. 11 CSR BC06 ROM I2s master mode timing diagram

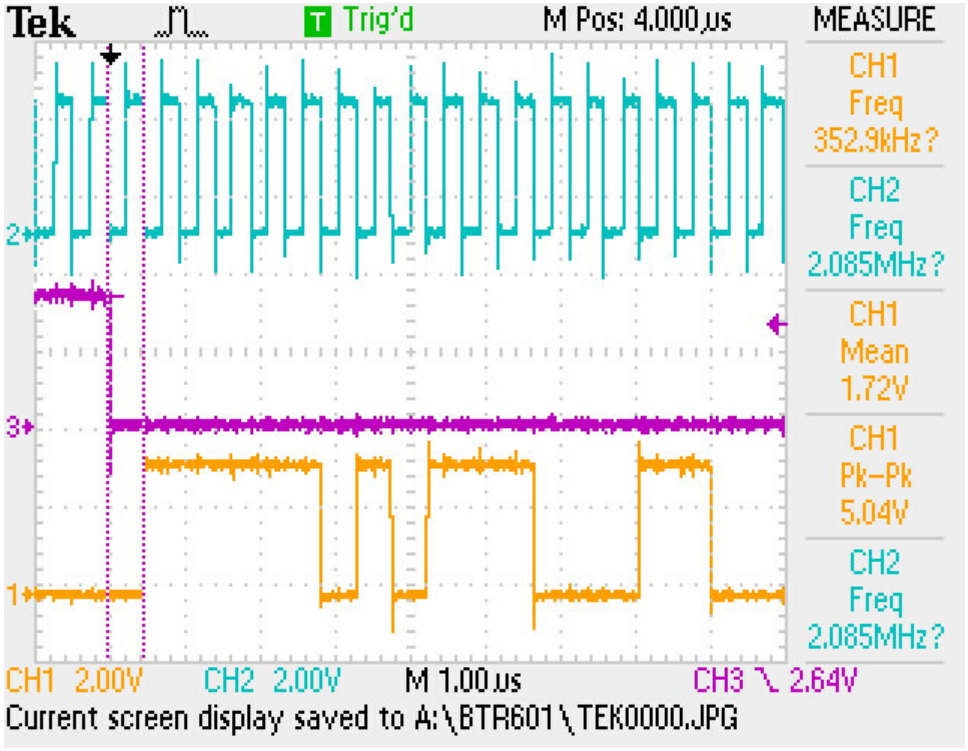

Fig. 12 Actual I2s master mode timing diagram(L/R clock rising edge trigger)

ch1 => data
ch2 => bit clcok (WS)
ch3 => L/R clock (SCK) => 44.1kHz

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Symbol	Parameer	Typ	Max	Unit
-	Clock frequency (SCK)	-	6.2	MHz
-	L/R clock (SCK)	-	96	kHz
t_{opd}	SCK to data delay	400	-	ns
t_{spd}	SCK to WS delay	200	-	ns

Table 12 Digital audio interface master timing (Data Output)

Test equipment system diagram

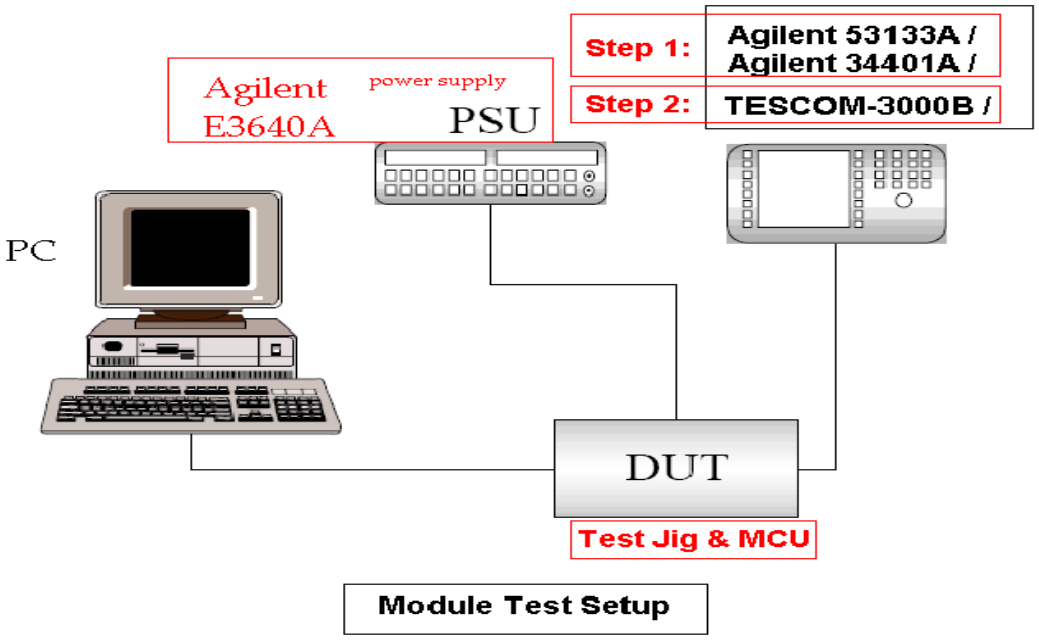

Fig. 13 RF test setup configure

Step 1:

(a) Setup the PC & Test Fixture, connect the COM port & +8V power supply unit
(b) Insert the BT module into the Fixture
(c) Download the RF & basic PSKEY to the module via UART interface
(d) Start the crystal trim, use the software program to trim the crystal value and log to a text file with the unique BT ID. Put the unique BD addr label on the BTR601 module.
(e) Check the PIOs, AIO, +1.8V output, UART & SPI by the software testing program
(f) Log and record the results into the text file

Step 2:

(g) Start the conductive RF test and log the result to a text file (refer to AWV Conductive RF Test
(h) Log and record the results into the text file

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Step 3:
(I) Write the PSKEYs (unique BT address, crystal trim value & crystal frequency) to the EEPROM
(j) Check the EEPROM by the external MCU to verify the written PSKEYs are corrected or not, put the crystal trim value label on the BTR601 module
(k) Log and record the MP products into the text file before deliver out

Step 4:
(l) visual check the BTR601 module and read the EEPROM value to confirm it is matched between the BD addr label and EEPROM information per each module.

Power Consumption

Referent current consumption(different HCI settings):

Voltage Supplies =1.8V
Temperature = 25°C
Frequency = 2.441GHz

Mode	Average	Peak	Unit
SCO connection HV3 (30ms interval sniff mode)(slave)	16	-	mA
SCO connection HV3 (30ms interval sniff mode)(Master)	17	-	mA
SCO connection HV3 (no sniff mode)(slave)	23	-	mA
SCO connection HV1 (Slave)	37	-	mA
SCO connection HV1 (Master)	37	-	mA
ACL data transfer 115.2kbps UART (Master)	9	-	mA
ACL data transfer 115.2kbps UART (slave)	17	-	mA
ACL data transfer 921kbps UART (Master or slave)	30	-	mA
ACL connection, sniff mode 40ms interval, 38.4kbps UART	1.6	-	mA
ACL connection, sniff mode 1.28s interval, 38.4kbps UART	0.2	-	mA
Parked Slave, 1.28s beacon interval, 38.kpbs UART	0.28	-	mA
Standby Mode (Connected to host, no RF activity)	40	-	µA
Reset (RESET high or RESETB low)	39	-	µA

Table. 13 HCI current consumption

Measured current consumption(overall):

Voltage Supplies =1.8V
Temperature = 25°C
Frequency = 2.402GHz to 2.480GHz (hopping)

•standby current consumption: ~ 0.8mA
•pairing current consumption: ~ 35mA
•A2DP audio streaming connected current consumption: ~ 45mA
•Headset/Handsfree connected current consumption: ~ 40mA

Remark: connect to PC via UART interface with the IVT software tool, HCI module can perform some different BT profiles function like A2DP, SPP, HID & HS/HF,,etc when connected to the IVT software tool.

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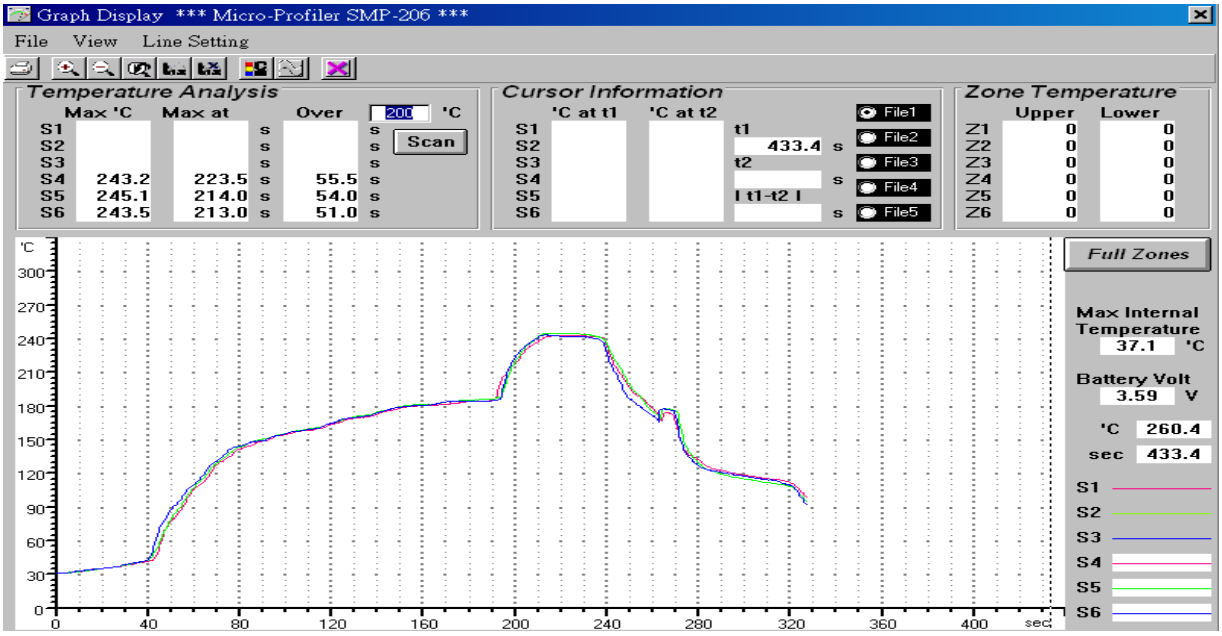
Solder Profiles

In order to setup your application, it is required to have the soldering profile which is based on various parameters.

Zone	Sensor	Description
Preheat Zone	1-2	This zone raises the temperature at a controlled rate. Generally 1~2.5°C/s.
Equilibrium Zone	3	This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone will need to be adjusted to optimize the out gassing of the flux. Generally 120~180s duration.
Reflow Zone	4	The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to inter-metallic growth which can result in a brittle joint.
Cooling Zone	5-6	The cooling rate should be fast, to keep the solder grains small which will give longer lasting joint. Generally 2~5°C/s.

Table 14. Soldering zones

Solder Re-Flow Profile for Devices with Lead-Free Solder Pads



Temperature Analysis at 200°C

Sensor	Max °C	Max at (s)	Over (s)
S4	243.2	223.5	55.5
S5	245.1	214	54
S6	243.5	213	51

Fig. 14 Reflow soldering temperature

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Storage Recommendations

Baking conditions:
125 +/- 5 °C, 24 hours, 1 time
The products should be baked on the heat resistant baking tray inside the heat oven, because the module's tray are not heat resistant.
After opening the packing, the products should be stored at 5 to 30 °C & ~65 %RH and the products should be used/mounted within 24 hours. If the products are exposed more than 24 hours after opening the packing, its should be baked under the above baking conditions (125 +/- 5 °C).

Storage conditions:
▪The products should be stored without opening the packing and the room temperature between 5 and 30 °C and humidity between 30 and 70 % RH. Products should be used within 4 to 6 months after reception.
▪The products can't be stored in corrosive gas.
▪Solder-ability should be promised before use if the products are stored for less than 6 months.
▪Don't excess the mechanical shock, drop the products(without packing) over 20cm height and sticking the packing materials by any sharp object.

Appendix 1

Host transport configurations (PSKEY):

BCSP transport:

If PSKEY_HOST_INTERFACE selects use of BCSP then the UART's configuration register is set to the value of this PS key when it boots.

The UART configuration register is a bitfield:

Bit Meaning
0 0 => one stop bit, 1 => two stop bits.
1 0 => no parity bits, 1 => one parity bit.
2 0 => odd parity, 1 => even parity.
3 0 => h/w flow control disabled, 1 => enabled.
4 Set to 0.
5 0 => RTS deasserted, 1 => RTS asserted.
6 Set to 0.
7 0 => non-BCSP/H5 operation disabled, 1 => enabled.
8 Set to 0.
9 Set to 0.
10 Set to 0.
11 Set to 1.
12 0 => H5 operation disabled, 1 => enabled.

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13 Set to 0.
14 Set to 0.
15 Set to 0.

The default value, 0x0806, selects use of BCSP mode and even parity.

In builds from HCI 18.X, this key replaces PSKEY_UART_CONFIG, PSKEY_UART_CONFIG_STOP_BITS, PSKEY_UART_CONFIG_PARITY_BIT, PSKEY_UART_CONFIG_FLOW_CTRL_EN, PSKEY_UART_CONFIG_RTS, PSKEY_UART_CONFIG_NON_BCSP_EN.

H4 transport:

If PSKEY_HOST_INTERFACE selects use of H4 then the UART's configuration register is set to the value of this PS key when it boots.

The UART configuration register is a bitfield and shares its format with PSKEY_UART_CONFIG_BCSP:

Bit Meaning
0 0 => one stop bit, 1 => two stop bits.
1 0 => no parity bits, 1 => one parity bit.
2 0 => odd parity, 1 => even parity.
3 0 => h/w flow control disabled, 1 => enabled.
4 Set to 0.
5 0 => RTS deasserted, 1 => RTS asserted.
6 Set to 0.
7 0 => non-BCSP/H5 operation disabled, 1 => enabled.
8 Set to 0.
9 Set to 0.
10 Set to 0.
11 Set to 1.
12 0 => H5 operation disabled, 1 => enabled.
13 Set to 0.
14 Set to 0.
15 Set to 0.

The default value, 0x08a8, selects use of hardware flow control, as required by the H4 specification.

In builds from HCI 18.X, this key replaces PSKEY_UART_CONFIG, PSKEY_UART_CONFIG_STOP_BITS, PSKEY_UART_CONFIG_PARITY_BIT, PSKEY_UART_CONFIG_FLOW_CTRL_EN, PSKEY_UART_CONFIG_RTS, PSKEY_UART_CONFIG_NON_BCSP_EN.

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H4DS transport:

If PSKEY_HOST_INTERFACE selects use of H4DS then the UART's configuration register is set to the value of this PS key when the system boots.

The UART configuration register is a bitfield:

Bit Meaning
0 0 => one stop bit, 1 => two stop bits.
1 0 => no parity bits, 1 => one parity bit.
2 0 => odd parity, 1 => even parity.
3 0 => h/w flow control disabled, 1 => enabled.
4 Set to 0.
5 0 => RTS deasserted, 1 => RTS asserted.
6 Set to 0.
7 0 => non-BCSP/H5 operation disabled, 1 => enabled.
8 Set to 0.
9 Set to 0.
10 Set to 0.
11 Set to 1.
12 0 => H5 operation disabled, 1 => enabled.
13 Set to 0.
14 Set to 0.
15 Set to 0.

The default value, 0x08a8, selects use of hardware flow control, as required by the H4 (sic) specification.

H5 transport:

If PSKEY_HOST_INTERFACE selects use of H5 then the UART's configuration register is set to the value of this pskey when it boots.

The UART configuration register is a bitfield:

Bit Meaning
0 0 => one stop bit, 1 => two stop bits.
1 0 => no parity bits, 1 => one parity bit.
2 0 => odd parity, 1 => even parity.
3 0 => h/w flow control disabled, 1 => enabled.
4 Set to 0.
5 0 => RTS deasserted, 1 => RTS asserted.
6 Set to 0.
7 0 => non-BCSP/H5 operation disabled, 1 => enabled.

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8 Set to 0.
9 Set to 0.
10 Set to 0.
11 Set to 1.
12 0 => H5 operation disabled, 1 => enabled.
13 Set to 0.
14 Set to 0.
15 Set to 0.

(The "H5" host transport protocol is properly known as the "Three Wire Uart Transport Layer", but is commonly known as H5 within CSR.)

In builds from HCI 18.X, this key replaces PSKEY_UART_CONFIG, PSKEY_UART_CONFIG_STOP_BITS, PSKEY_UART_CONFIG_PARITY_BIT, PSKEY_UART_CONFIG_FLOW_CTRL_EN, PSKEY_UART_CONFIG_RTS, PSKEY_UART_CONFIG_NON_BCSP_EN.

Appendix 2

BTR601 module silkscreen photos:

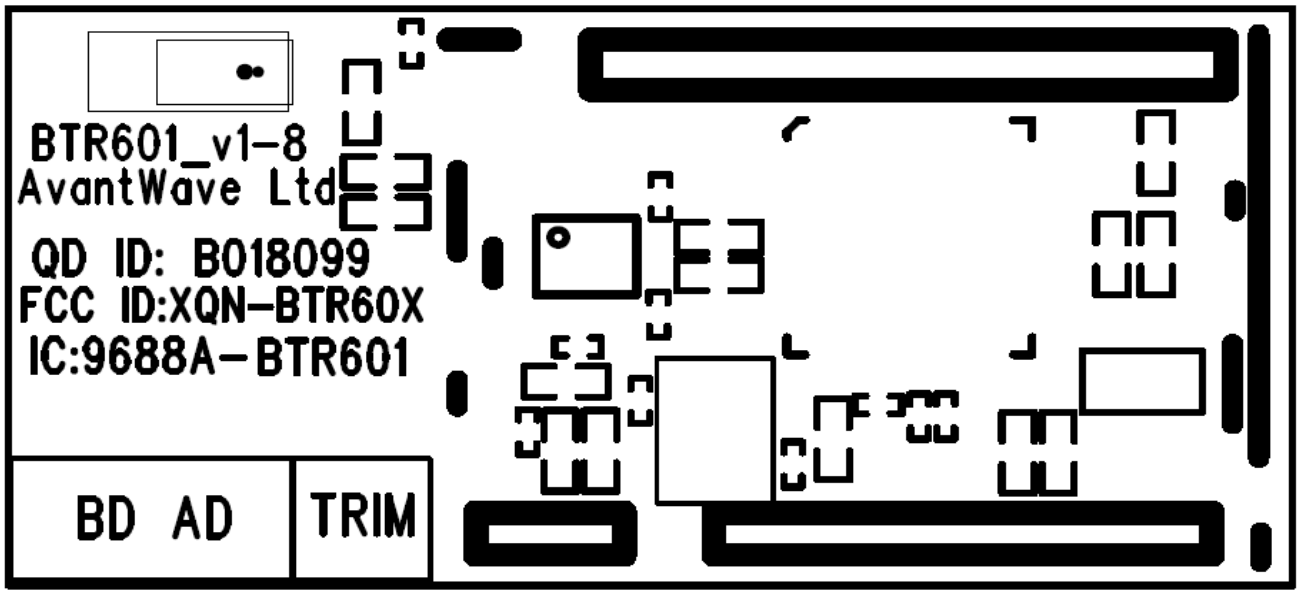

Fig. 15 BTR601 module top layer silkscreen

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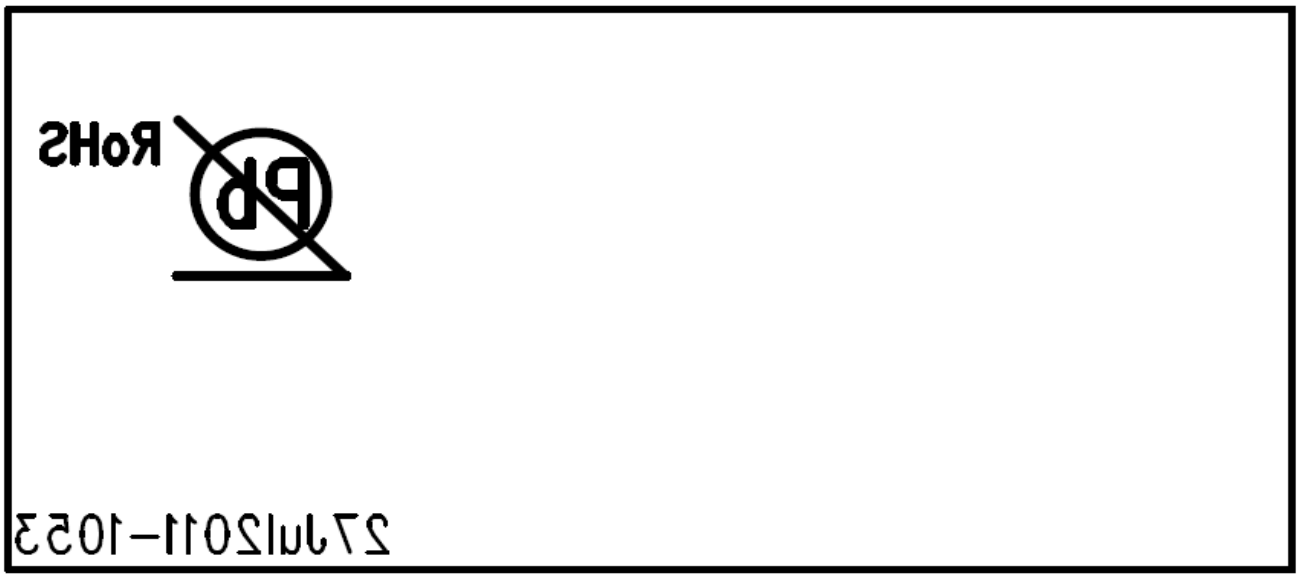
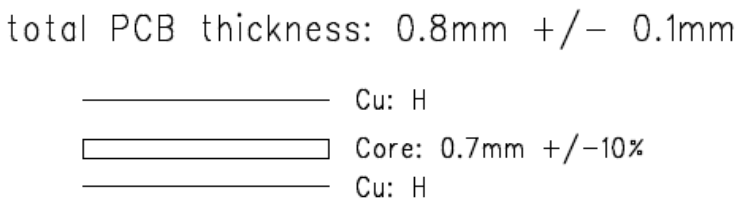


Fig. 16 BTR601 module bottom layer silkscreen

Dimension outline:



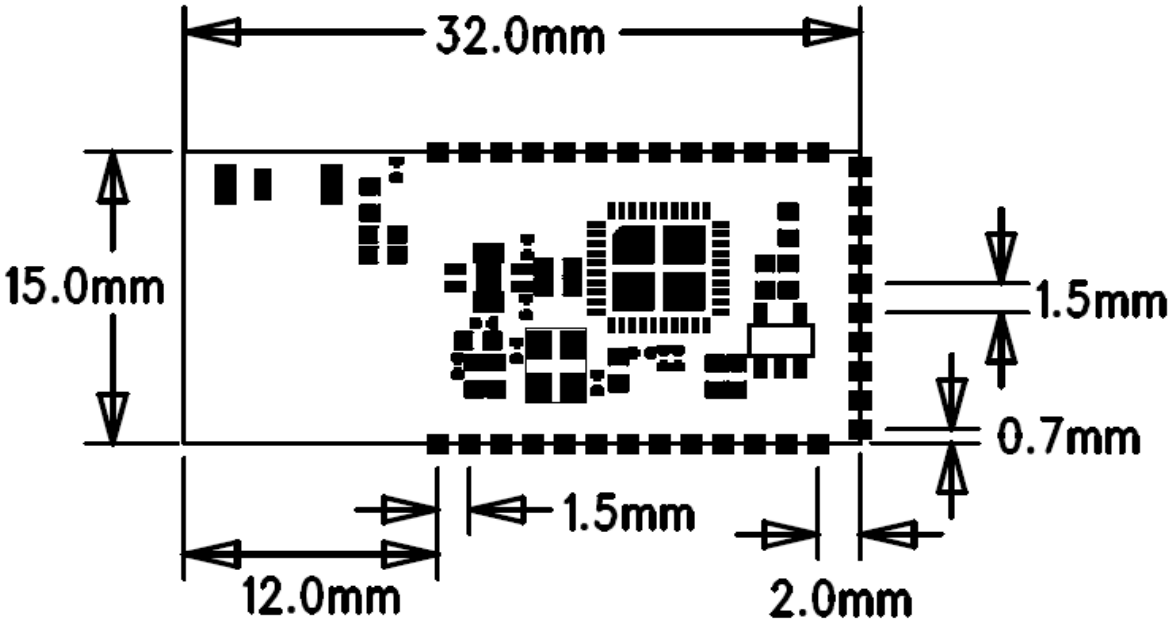


Fig. 17 BTR601 module terminals & shapes of parts

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Appendix 2

BTR 601 EEPROM Data ReadPacketFormat from EEPROM to PC

Aim:
Since there are some Bluetooth Configuration Parameter(BT address, Crystal Trim, Crystal Frequency) are required to read from EEPROM to PC through UART as a confirmation in production.
This document will interpret the packet format in how to Send Packet Cmd to MCU for reading the EEPROM data

Communication Port: UART, 38400,8N1

All Send Packet Cmd (BT address, Crystal Trim, Crystal Frequency) contain 10 bytes data and receiving 8 bytes EEPROM data.

BT address:

Send Packet Cmd:

```
0xf0,                                   //Header
0x00,                                   //EEPROM Address
0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,  //dummy
C_ CHKSUM                               //checksum
```

ps: C_CHKSUM =0xff - (0xf0+0x00+0x00+0x00+0x00+0x00+0x00+0x00+ 0x00 +0x00) & 0x00ff;

Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09
Data	0xf0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	C_CHKSUM

Table. 15 BT address send packet command

Receive Packet Cmd:
It will contains 8 bytes(i.e EEPROM address 0-7) to show the Bluetooth address

Receive Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Data	BT address(NAP_0)	BT address(NAP_1)	BT address(UAP)	BT address(LAP_0)	BT address(LAP_1)	BT address(LAP_2)	0x00(dummy)	C_CHKSUM(Rec)

Table. 16 BT address receive packet command

ps: C_CHKSUM(Rec) =0xff - (BT address(NAP_0)+BT address(NAP_1)+BT address(UAP)+BT address(LAP_0)+BT address(LAP_1)+BT address(LAP_2)+0x00) & 0x00ff;

e.g. read bluetooth address cmd, and suppose bluetooth address is 0008-e0-123456
Send : f0 00 00 00 00 00 00 00 00 0f
Receive : 00 08 e0 12 34 56 00 7b

Crystal Frequency

Send Packet Cmd:

```
0xf0                                    //Header
    0x08,                               //EEPROM Address
    0x00, 0x00,0x00, 0x00,0x00,0x00,0x00,  //dummy
    C_CHKSUM                            //checksum
```

ps: C_CHKSUM =0xff – (0xf0+0x08+0x00+0x00+0x00+0x00+0x00+0x00+0x00+0x00) & 0x00ff;

Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09
Data	0xf0	0x08	0x00	0x00	0x00	0x00	0x00	0x00	0x00	C_CHKSUM

Table. 17 Crystal frequency send packet command

Receive Packet Cmd:
It will contains 8 bytes(i.e EEPROM address 8-15) to show the Crystal Frequency

Receive Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07

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Data	C_CRYFREQ_HIGHER_BYTE	C_CRYFREQ_LOWER_BYTE	0x00	0x00	0x00	0x00	0x00	C_CHKSUM(Rec)

Table. 18 Crystal frequency receive packet command

ps: C_CHKSUM(Rec) =0xff - (C_CRYFREQ_HIGHER_BYTE+C_CRYFREQ_LOWER_BYTE+0x00+0x00+0x00+ 0x00 +0x00) & 0x00ff;

e.g. read the crystal frequency and suppose its value is 16Mhz
Send : f0 08 00 00 00 00 00 00 07
Receive : 3e 80 00 00 00 00 41

▪Crystal Trim

Send Packet Cmd:

```
0xf0                                        //Header
0x10,                                       //EEPROM Address
        0x00,0x00,0x00, 0x00,0x00,0x00,0x00,        //dummy
        C_CHKSUM                                    //chksum

        ps: C_CHKSUM =0xff -(0xf0+0x10+0x00+0x00+0x00+0x00+0x00+0x00 +0x00) & 0x00ff;
```

Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09
Data	0xf0	0x10	0x00	0x00	0x00	0x00	0x00	0x00	0x00	C_CHKSUM

Table. 19 Crystal trim value send packet command

Receive Packet Cmd:
It will contains 8 bytes(i.e EEPROM address 16-23) to show the Crystal Trim

Receive Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Data	C_CRYTRIM	0x00	0x00	0x00	0x00	0x00	0x00	C_CHKSUM(Rec)

Table. 20 Crystal trim value receive packet command

ps: C_CHKSUM(Rec) =0xff - (C_CRYTRIM+0x00+0x00+0x00+0x00+ 0x00 +0x00) & 0x00ff;

e.g. read the crystal trim and suppose its value is 29
Send : f0 10 00 00 00 00 00 00 ff
Receive : 1d 00 00 00 00 00 00 e2

▪Pio Set1

Send Packet Cmd:

```
0xf0                                        //Header
0x18,                                       //EEPROM Address
        0x00,0x00,0x00, 0x00,0x00,0x00,0x00,        //dummy
        C_CHKSUM                                    //chksum

        ps: C_CHKSUM =0xff -(0xf0+0x18+0x00+0x00+0x00+0x00+0x00+0x00 +0x00) & 0x00ff;
```

Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09
Data	0xf0	0x18	0x00	0x00	0x00	0x00	0x00	0x00	0x00	C_CHKSUM

Table. 21 PIO set1 send packet command

Receive Packet Cmd:
It will contains 8 bytes(i.e EEPROM address 24-31) to show the Pio Set1

Receive Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Data	C_PIO_MASK	C_PIO_MASK_1	C_PIO_DIR_0	C_PIO_DIR_1	0x00	0x00	0x00	C_CHKSUM(Rec)

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	_0							

Table. 22 PIO set1 receive packet command

ps: C_CHKSUM(Rec) =0xff - (C_PIO_MASK_0+C_PIO_MASK_1+C_PIO_DIR_0+C_PIO_DIR_1+0x00+ 0x00 +0x00) & 0x00ff;

e.g. read the Pio Set1 and suppose its value is ffef(C_PIO_MASK),ffef(C_PIO_DIR)
Send : f0 18 00 00 00 00 00 00 f7
Receive : ff ef ff ef 00 00 00 1b

▪Pio Set2

Send Packet Cmd:
0xf0 //Header
0x20, //EEPROM Address
0x00,0x00,0x00, 0x00,0x00,0x00,0x00,0x00, //dummy
C_CHKSUM //chksum

ps: C_CHKSUM =0xff -(0xf0+0x20+0x00+0x00+0x00+0x00+0x00+0x00+0x00 +0x00) & 0x00ff;

Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09
Data	0xf0	0x20	0x00	0x00	0x00	0x00	0x00	0x00	0x00	C_CHKSUM

Table. 23 PIO set2 send packet command

Receive Packet Cmd:
It will contains 8 bytes(i.e EEPROM address 32-39) to show the Pio Set2

Receive Packet byte	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Data	C_PIO_LVL_0	C_PIO_LVL_1	C_PIO_BIAS_0	C_PIO_BIAS_1	0x00	0x00	0x00	C_CHKSUM(Rec)

Table. 24 PIO set2 receive packet command

ps: C_CHKSUM(Rec) =0xff - (C_PIO_LVL_0+C_PIO_LVL_1+C_PIO_BIAS_0+C_PIO_BIAS_1+0x00+ 0x00 +0x00) & 0x00ff;

e.g. read the Pio Set1 and suppose its value is 0000(C_PIO_LVL),0000(C_PIO_BIAS)
Send : f0 20 00 00 00 00 00 00 ef
Receive : 00 00 00 00 00 00 00 ff

Remarks
Specifications subject to change without notice. All other trademarks mentioned are the property of their respective owners. This document shows outlined specification only. Please contact AvantWave upon evaluation and integration.

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FCC Compliance statements

Changes or modifications not expressly approved by the party responsible for compliance
could void the user's authority to operate the equipment.

This device complies with Part 15 of the FCC Rules.
Operation is subject to the following two conditions:
(1) this device may not cause harmful interference, and
(2) this device must accept any interference received,
including interference that may cause undesired operation

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.
If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
--Reorient or relocate the receiving antenna.
--Increase the separation between the equipment and receiver.
--Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
--Consult the dealer or an experienced radio/TV technician for help.

RF Radiation Exposure Information
Since the radiated output power of this device is far below the FCC radio frequency exposure limits, it is not subject to routine RF exposure evaluation
as per Section 2.1093 of the rules.

LABEL OF THE END PRODUCT:
The final end product must be labeled in a visible area with the following " Contains TX FCC ID: XQN-BTR60X".
If the size of the end product is larger than 8x10cm, then the following FCC part 15.19 statement has to also be available on the label:
This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions:
(1) this device may not cause harmful interference and
(2) this device must accept any interference received, including interference that may cause undesired operation.

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