LEXI-R10 series

LTE Cat 1bis modules

System integration manual

Abstract

This document describes the features and the integration of the ultra-small LEXI-R10 series cellular modules. These modules are a complete and cost-efficient solution offering multi-band LTE Cat 1bis data transmissions in the ultra-compact LEXI form factor.

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This document applies to the following products:

Product name	Type number
LEXI-R10001D	LEXI-R10001D-01B-00
LEXI-R10011D	LEXI-R10011D-01B-00
LEXI-R10401D	LEXI-R10401D-00B-00
	LEXI-R10401D-01B-00
LEXI-R10801D	LEXI-R10801D-00B-00
	LEXI-R10801D-00B-01
	LEXI-R10801D-01B-00

For firmware versions, notification documents, and product status, see the data sheet [1].

Contents

1 System description

1.1 Overview

LEXI-R10 series are the world's smallest LTE Cat 1bis modules in the ultra-small LEXI LGA form factor (16.0 x 16.0 mm, 133-pin), featuring medium capacity data connectivity (up to 10 Mbit/s downlink, and up to 5 Mbit/s uplink) with very low energy consumption.

Thanks to connectivity to ubiquitous LTE Cat 1 networks, LEXI-R10 series modules are ideally suited to a wide range of value-oriented applications that require medium data speed and superior coverage. Typical applications are asset tracking, telematics, healthcare, and wearables.

LEXI-R10 series modules support multi-band LTE radio access technology, and come in the following product variants to reduce logistics complexity:

- LEXI-R10001D data-only LTE Cat 1bis module for global use, with a comprehensive set of bands supported, and all relevant regulatory and conformance approvals.
- LEXI-R10011D data-only LTE Cat 1bis module for global use, with the most comprehensive set of bands supported, and all relevant regulatory, conformance, Mobile Network Operator approvals.
- LEXI-R10401D data-only LTE Cat 1bis module, an ideal solution for use in North America region, with relevant supported bands and regulatory, conformance, Mobile Network Operator approvals.
- LEXI-R10801D data-only LTE Cat 1bis module, an ideal solution for use in Europe, Middle East, Africa, Brazil and Asia-Pacific regions, with relevant supported bands and regulatory approvals.

LEXI-R10 series modules are qualified according to u-blox qualification policy based on the AEC-Q104 standard, for operation in harsh environments and in very compact designs.

Model	Regions	Radio Access Technology			Interfaces						Features																	Grade		
		LTE category	LTE FDD bands	LTE TDD bands	UARTs	USB	I2C	SIM	GPIOs	Digital audio (I2S)	Secure boot and updates	CellLocate®	Wi-Fi scan	PSM	eDRX	Embedded TCP/IP, UDP/IP	Embedded HTTP, HTTPS	Embedded FTP, FTPS	Embedded TLS, DTLS	Embedded MQTT	Dual stack IPv4 / IPv6	SNTP	FW update via serial (FOAT)	FW update Over the Air (FOTA)	Backup/Restore	Antenna dynamic tuning	Antenna and SIM detection	Standard	Professional	Automotive
LEXI-R10001D	Global	1bis	1,2,3,4,5 7,8,12,13 20,28,66	34 38,39 40,41	●	●	○	●	●	●	●	●	●	●	●	●	●	■	●	●	●	●	●	●	●	●	●		●	
LEXI-R10011D	Global	1bis	1,2,3,4,5 7,8,12,13 20,25,28,66	34 38,39 40,41	●	●	○	●	●	●	●	●	●	●	●	●	●	■	●	●	●	●	●	●	●	●	●		●	
LEXI-R10401D	Americas	1bis	2,4,5 12,13,14 66,71		●	●	○	●	●	●	●	●	●	●	●	●	●	■	●	●	●	●	●	●	●	●	●		●	
LEXI-R10801D	EMEA APAC Brazil	1bis	1,3,5 7,8 20,28		●	●	○	●	●	●	●	●	●	●	●	●	●	■	●	●	●	●	●	●	●	●	●		●	

● = Supported ■ = Supported by "01B" product version onwards ○ = HW-ready

Table 1: LEXI-R10 series main features summary

Table 2 summarizes cellular radio access technologies characteristics and features of the modules.

	LEXI-R10001D	LEXI-R10011D	LEXI-R10401D	LEXI-R10801D
Protocol stack	3GPP Release 14	3GPP Release 14	3GPP Release 14	3GPP Release 14
Radio Access Technology	LTE Cat 1bis	LTE Cat 1bis	LTE Cat 1bis	LTE Cat 1bis
LTE FDD operating bands	Band 1 (2100 MHz) Band 2 (1900 MHz) Band 3 (1800 MHz) Band 4 (1700 MHz) Band 5 (850 MHz) Band 7 (2600 MHz) Band 8 (900 MHz) Band 12 (700 MHz) Band 13 (700 MHz) Band 20 (800 MHz) Band 28 (700 MHz) Band 66 (1700 MHz)	Band 1 (2100 MHz) Band 2 (1900 MHz) Band 3 (1800 MHz) Band 4 (1700 MHz) Band 5 (850 MHz) Band 7 (2600 MHz) Band 8 (900 MHz) Band 12 (700 MHz) Band 13 (700 MHz) Band 20 (800 MHz) Band 25 (1900 MHz) Band 28 (700 MHz) Band 66 (1700 MHz)	Band 2 (1900 MHz) Band 4 (1700 MHz) Band 5 (850 MHz) Band 12 (700 MHz) Band 13 (700 MHz) Band 14 (700 MHz) Band 66 (1700 MHz) Band 71 (600 MHz)	Band 1 (2100 MHz) Band 3 (1800 MHz) Band 5 (850 MHz) Band 7 (2600 MHz) Band 8 (900 MHz) Band 20 (800 MHz) Band 28 (700 MHz)
LTE TDD operating bands	Band 34 (2000 MHz) Band 38 (2600 MHz) Band 39 (1900 MHz) Band 40 (2300 MHz) Band 41 (2600 MHz)	Band 34 (2000 MHz) Band 38 (2600 MHz) Band 39 (1900 MHz) Band 40 (2300 MHz) Band 41 (2600 MHz)		
LTE Power class	Class 3 (23 dBm)	Class 3 (23 dBm)	Class 3 (23 dBm)	Class 3 (23 dBm)
Data rate	LTE category 1bis: up to 10.3 Mbit/s DL, up to 5.2 Mbit/s UL	LTE category 1bis: up to 10.3 Mbit/s DL, up to 5.2 Mbit/s UL	LTE category 1bis: up to 10.3 Mbit/s DL, up to 5.2 Mbit/s UL	LTE category 1bis: up to 10.3 Mbit/s DL, up to 5.2 Mbit/s UL

Table 2: LEXI-R10 series modules cellular characteristics summary

☞ SIM with IMSI MCC values from 300 to 400 are not allowed to operate with the LEXI-R10001D and LEXI-R10801D: when a SIM with such IMSI MCC is used, an error "SIM not powered on" is returned and the SIM is powered off.

Table 3 summarizes Wi-Fi receiver scan capabilities of the modules.

	LEXI-R10 series
IEEE standard	802.11 b/g/n with DSSS (Direct-Sequence Spread Spectrum) beacon
Operating band	2.4 GHz, all 14 channels
Channel bandwidth	20 MHz
Modulation	DBPSK (Differential Binary Phase Shift Keying) at 1 Mbit/s DQPSK (Differential Quadrature Phase Shift Keying) at 2 Mbit/s

Table 3: LEXI-R10 series Wi-Fi receiver main characteristics

☞ Some DSSS PHY scrambler initialization vectors are not supported. This information is normally not specified by Wi-Fi Access Points manufacturers. If a specific Wi-Fi AP must be found, it is recommended to test the compatibility of the AP with LEXI-R10 series modules in advance.

1.2 Architecture

Figure 1 summarizes the internal architecture of the modules, described more in details below.

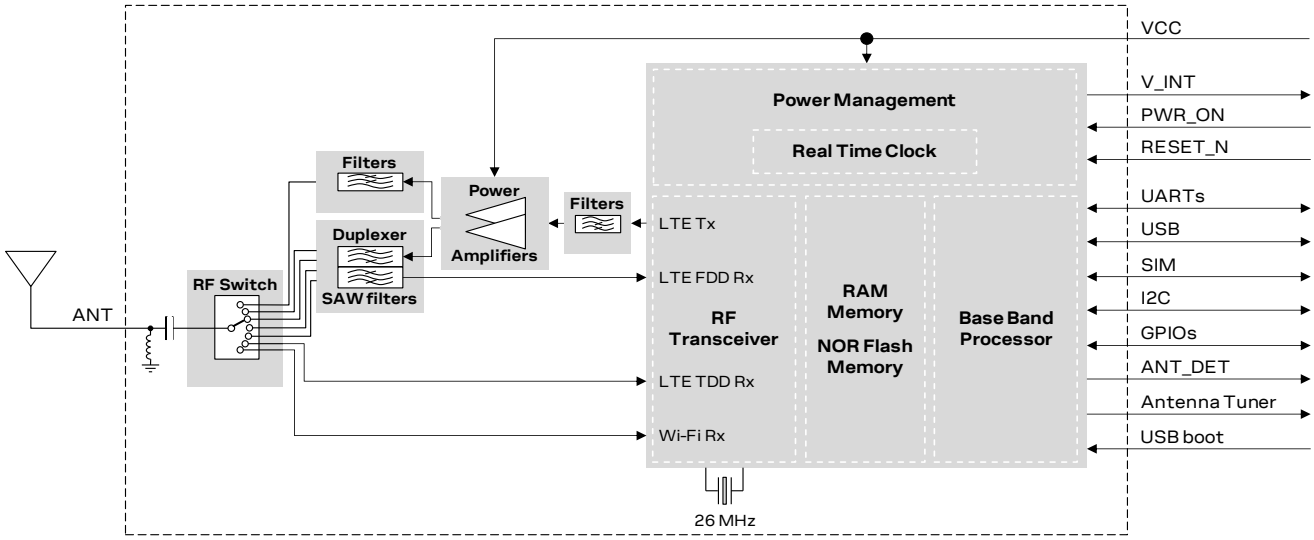

Figure 1: LEXI-R10 series modules' simplified block diagram

RF section

The RF section is composed of the following main elements:

- RF switch connecting the antenna port (**ANT**) to the suitable RF LTE Tx paths, RF LTE Rx paths, and the RF Wi-Fi Rx path
- Power Amplifiers amplifying the LTE Tx signal modulated and pre-amplified by the RF transceiver
- RF filters along the Tx and Rx signal paths providing RF filtering (Duplexer SAW filters for LTE FDD RF paths, other filters for LTE TDD and Wi-Fi RF paths)
- RF transceiver, performing modulation, up-conversion and pre-amplification of baseband signals for transmission, and performing down-conversion and demodulation of RF signals for reception
- 26 MHz crystal oscillator generating the reference clock signal for the RF transceiver and the baseband system, when the related system is in active mode or connected mode

Baseband and power management section

The baseband and power management section, is composed of the following main elements:

- On-chip modem processor, vector signal processor, with dedicated hardware assistance for signal processing and system timing
- On-chip modem processor, with interfaces control functions
- On-chip voltage regulators to derive all the internal or external (**V_SIM**, **V_INT**) supply voltages from the module supply input **VCC**
- On-chip RAM memory and NOR flash memory
- On-chip oscillator to provide the clock reference in ultra-low power deep-sleep mode

1.3 Pin-out

Table 4 lists the pin-out of the LEXI-R10 series modules, with pins grouped by function.

Function	Name	No	ID	I/O	Description	Remarks
Power	VCC	40-42	A12-14	I	Module supply input	VCC supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for functional description and requirements. See section 2.2.1 for external circuit design-in.
	GND	1,3,50,52, 53,56-61, 64-70, 73-79, 82-88, 91-97, 100-106, 109-115, 116-124, 125-133	B1,D1,A4,A2, C3,C7-11,C13, E6-11,E13, F6-11,F13, G6-11,G13, H6-11,H13, J6-11,J13, K6-11,K13, L3,L5-11,L13, N3,N5-11,N13	N/A	Ground	GND pins are internally connected each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1 for functional description. See section 2.2.1 for external circuit design-in.
	V_INT	43	A11	O	Generic digital interfaces supply output	V_INT = 1.8 V (typical) generated by internal regulator when the module is switched on, outside the ultra-low power deep-sleep mode. See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in. Provide test point for diagnostic purposes.
System	PWR_ON	27	P15	I	Power-on/off input	Internal pull-up resistor. See section 1.6.1 / 1.6.2 for functional description. See section 2.3.1 for external circuit design-in. Provide test point for FW update or diagnostic.
	RESET_N	28	N15	I	Reset input	Internal pull-up resistor. See section 1.6.3 for functional description. See section 2.3.1 for external circuit design-in. Provide test point for FW update or diagnostic.
Antenna	ANT	51	A3	I/O	RF antenna I/O	50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and application device compliance with required certification schemes. See section 1.7.1 for functional description and requirements. See section 2.4 for external circuit design-in.
	ANT_DET	49	A5	I	Antenna detection	ADC for antenna presence detection function. See section 1.7.2 for functional description. See section 2.4.3 for external circuit design-in.
SIM	VSIM	33	H15	O	SIM supply output	Supply output for external SIM / UICC. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_IO	32	J15	I/O	SIM data	Data input/output for external SIM / UICC. Internal pull-up to VSIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_CLK	31	K15	O	SIM clock	Clock output for external SIM / UICC See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_RST	30	L15	O	SIM reset	Reset output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.

Function	Name	No	ID	I/O	Description	Remarks
UART	RXD	4	E1	O	UART data output	Primary UART circuit 104 (RxD) in ITU-T V.24, for AT commands, data, Mux, FW update or Diagnostic See section 1.9.2 for functional description. See section 2.6.1 for external circuit design-in. Provide test point for FW update and diagnostic, if the USB interface is used by the host processor.
	TXD	5	F1	I	UART data input	Primary UART circuit 103 (TxD) in ITU-T V.24, for AT commands, data, Mux, FW update or Diagnostic Internal active pull-up to V_INT. See section 1.9.2 for functional description. See section 2.6.1 for external circuit design-in. Provide test point for FW update and diagnostic, if the USB interface is used by the host processor.
	CTS	6	G1	O	UART clear to send output	Primary UART circuit 106 (CTS) in ITU-T V.24. See section 1.9.2 for functional description. See section 2.6.1 for external circuit design-in.
	RTS	7	H1	I	UART request to send input	Primary UART circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to V_INT. See section 1.9.2 for functional description. See section 2.6.1 for external circuit design-in.
	DSR	11	M1	O / I	UART data set ready output / AUX UART request to send input	Primary UART circuit 107 (DSR) in ITU-T V.24, configurable as auxiliary UART RTS input. See section 1.9.2 for functional description. See section 2.6.1 for external circuit design-in.
	RI	10	L1	O / O	UART ring indicator output / AUX UART clear to send output	Primary UART circuit 125 (RI) in ITU-T V.24, configurable as auxiliary UART CTS output. See section 1.9.2 for functional description. See section 2.6.1 for external circuit design-in.
	DTR	9	K1	I / I	UART data terminal ready input / AUX UART data input	Primary UART circuit 108/2 (DTR) in ITU-T V.24, configurable as auxiliary UART TxD data input (for AT commands, data, or Diagnostic). Internal active pull-up to V_INT. See section 1.9.2 for functional description. See section 2.6.1 for external circuit design-in. Provide test point for diagnostic, if the USB and main UART are used by the host processor.
	DCD	8	J1	O / O	UART data carrier detect output / AUX UART data output	Primary UART circuit 109 (DCD) in ITU-T V.24, configurable as auxiliary UART RxD data output (for AT commands, data, or Diagnostic). See section 1.9.2 for functional description. See section 2.6.1 for external circuit design-in. Provide test point for diagnostic, if the USB and main UART are used by the host processor.

Function	Name	No	ID	I/O	Description	Remarks
USB	USB_D-	20	R8	I/O	USB Data Line D-	USB available for AT commands, data, Ethernet over USB, FW update and diagnostic. 90 Ω nominal differential impedance. Pull-up/down / series resistors as per USB specs [5] are integrated and shall not be provided externally. See section 1.9.3 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for FW update and diagnostic, if the UARTs are used by the host processor.
	USB_D+	21	R9	I/O	USB Data Line D+	USB available for AT commands, data, Ethernet over USB, FW update and diagnostic. 90 Ω nominal differential impedance. Pull-up/down / series resistors as per USB specs [5] are integrated and shall not be provided externally. See section 1.9.3 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for FW update and diagnostic, if the UARTs are used by the host processor.
	USB_BOOT	48	A6	I	Force USB boot	Input to force FW update over USB. Active high. See section 1.9.3 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for FW update, if the UART interfaces are used by the host processor.
I2C	SCL	12	N1	O	I2C bus clock line	I2C not supported by current product versions' FW. Fixed open drain. Internal pull-up to V_INT: no need external pull-up. See section 1.9.4 for functional description. See section 2.6.3 for external circuit design-in.
	SDA	13	P1	I/O	I2C bus data line	I2C not supported by current product versions' FW. Fixed open drain. Internal pull-up to V_INT: no need external pull-up. See section 1.9.4 for functional description. See section 2.6.3 for external circuit design-in.
GPIO	GPIO1	14	R2	I/O	GPIO	Pin with alternatively configurable functions, in the V_INT supply domain (1.8 V typ.). See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO2	15	R3	I/O	GPIO	Pin with alternatively configurable functions, in the "always-on" supply domain (1.8 V typ.), including module status indication function, event / ring indicator function, etc. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO3	16	R4	I/O	GPIO	Pin with alternatively configurable functions, in the "always-on" supply domain (1.8 V typ.), including deep sleep mode control / wake-up, fastest memory-safe emergency shutdown, etc. See sections 1.6.1 / 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO4	17	R5	I/O	GPIO	Pin with alternatively configurable functions, in the "always-on" supply domain (1.8 V typ.), including module status indication function, event / ring indicator function, etc. See section 1.10 for functional description. See section 2.7 for external circuit design-in.

Function	Name	No	ID	I/O	Description	Remarks
	GPIO5	18	R6	I/O	GPIO	Pin with alternatively configurable functions, in the V_INT supply domain (1.8 V typ.). See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO6	29	M15	I/O	GPIO	Pin with alternatively configurable functions, in the “always-on” supply domain (1.8 V typ.), including deep sleep mode control / wake-up, fastest memory-safe emergency shutdown, external SIM card physical presence detection, etc. See sections 1.6.1 / 1.8.2 / 1.10 for functional description See sections 2.5 / 2.7 for external circuit design-in.
	GPIO7	23	R11	I/O	GPIO	Pin with alternatively configurable functions, in the V_INT supply domain (1.8 V typ.). See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO8	24	R12	I/O	GPIO	Pin with alternatively configurable functions, in the V_INT supply domain (1.8 V typ.). See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO9	25	R13	I/O	GPIO	Pin with alternatively configurable functions, in the V_INT supply domain (1.8 V typ.). See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO10	26	R14	I/O	GPIO	Pin with alternatively configurable functions, in the V_INT supply domain (1.8 V typ.). See section 1.10 for functional description. See section 2.7 for external circuit design-in.
Antenna tuning	RFCTRL1	45	A9	O	RF GPIO for antenna tuner	Optional output for antenna dynamic tuning. See section 1.11 for functional description. See section 2.4.4 for external circuit design-in.
	RFCTRL2	44	A10	O	RF GPIO for antenna tuner	Optional output for antenna dynamic tuning. See section 1.11 for functional description. See section 2.4.4 for external circuit design-in.
Reserved	RSVD	2,19,22 34,35, 36,37, 38,39, 46,47, 54,55, 62,63, 71,72, 80,81, 89,90, 98,99, 107,108	C1,R7,R10, G15,F15, E15,D15, C15, B15, A8,A7, C5,C6, E3,E5, F3, F5, G3,G5, H3,H5, J3,J5, K3,K5	N/A	Reserved pin	Leave unconnected. See sections 1.12 and 2.8.

Table 4: LEXI-R10 series modules pin definition, grouped by function

1.4 Operating modes

LEXI-R10 series modules have several operating modes. The main operating modes are summarized in Table 5 and described in detail below, providing general guidelines for operation.

General status	Operating mode	Description
Power-down	**Not-powered mode**	**VCC** supply is not present or below operating range: the module is switched off.
	Power-off mode	**VCC** supply is within operating range and the module is switched off.
Normal Operation	**Deep-sleep mode**	Module processor main operating clock is switched off. The internal power management unit (including **V_INT** and **VSIM** supply output) and the other parts (including processor, transceiver, etc.) are switched off, keeping RTC running, keeping the state of the "always-on" GPIOs, and keeping wake-up capability over **PWR_ON** pin or over configured "always-on" GPIO pin. The module is temporarily not ready to communicate with an external device by means of the application interfaces as configured to reduce the power consumption to the minimum possible. See Table 6 for the description of the 3 levels of the ultra-low power deep-sleep mode.
	Active mode	Module processor runs in normal operating mode. The internal power management unit and other related parts run to provide normal operating functionality. The module is ready to communicate with an external device by means of the application interfaces.
	Connected mode	Transmission and/or reception of RF signals is in progress with the module processor running in normal operating mode. The internal power management unit and other related parts run to provide normal operating functionality. The module is ready to communicate with an external device by means of the application interfaces.

Table 5: LEXI-R10 series modules operating modes description summary

The initial operating mode of LEXI-R10 series modules is the one with **VCC** supply not present or below the operating range: the modules are switched off in not-powered mode.

Once a valid **VCC** supply is applied to the LEXI-R10 series modules, they remain switched off in the power-off mode. Then the proper toggling of the **PWR_ON** input line is necessary to trigger the switch-on routine of the modules that subsequently enter the active mode.

LEXI-R10 series modules are ready to operate when in active mode: the available communication interfaces are functional and the module can accept and respond to AT commands according to the operations executed, entering connected mode upon RF signal reception / transmission.

LEXI-R10 series modules switch from active mode to the ultra-low power deep-sleep mode whenever possible if the low power configuration is enabled by the dedicated +UPSV AT command. The switch from active to deep-sleep mode may occur with different timings according to the specific +UPSV AT command setting, and according to the concurrent activities executed by the module.

LEXI-R10 series modules may automatically enter the ultra-low power deep-sleep mode also after entering the User Equipment (UE) power saving mode (PSM) feature defined in 3GPP Rel.13, whenever possible, if no other concurrent activities are executed by the module and if PSM is enabled by the dedicated +CPSMS / +UCPSMS AT commands. The PSM can last for different time periods according to the T3412 periodic TAU timer set by the network.

Once the modules enter the ultra-low power deep-sleep mode, the available communication interfaces are not functional: a wake-up event is necessary to trigger the wake-up routine of the modules that subsequently enter back into the active mode. The wake-up event may consists of a low level applied at the **PWR_ON** input pin, or, in case of +UPSV=5 low power configuration, a rising edge applied at the **GPIO3** or **GPIO6** input pin configured with the module wake-up and low power mode control function

by the +UGPIOC AT command, or, in case the USB interface is used and it is suspended, via USB resume procedure.

The deep-sleep mode consists of the three levels of ultra-low power modes described in Table 6.

Operating mode	Sub-state	Description
Deep-sleep mode	**Sleep-1 (Minimum deep-sleep)**	Volatile configurations (as PPP and UART multiplexer) are held. USB resume and remote wake-up are available.
	Sleep-2 (Medium deep-sleep)	PPP and UART multiplexer configurations are lost. USB resume and remote wake-up are not available.
	Hibernate (Maximum deep-sleep)	Using USB interface, achievable only with <usb_allow_sleep> = 1. Using UART interface, achievable only with AT+UUSBCONF = 99.

Table 6: LEXI-R10 series modules different levels of ultra-low power deep-sleep operating mode description

LEXI-R10 series modules can be gracefully switched off by the +CPWROFF AT command, or by proper toggling of the **PWR_ON** input.

Figure 2 summarizes the transition between the different operating modes.

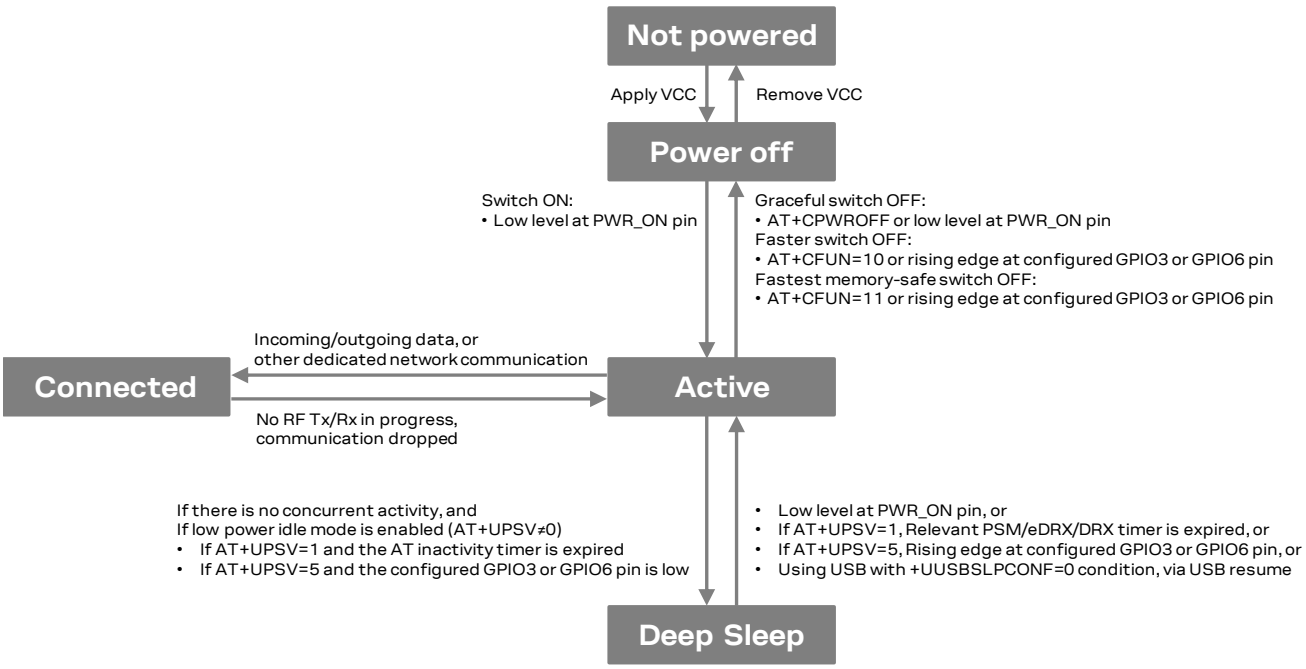

Figure 2: LEXI-R10 series modules operating modes transitions

- For more details about the operating modes, in particular the ones related with power saving, and for general guidelines for operation, see the LEXI-R10 series application development guide [3].
- For indicative current consumption figures of the modules, see the LEXI-R10 series data sheet [1].
- For the description of the related AT commands, see the AT commands manual [2].

1.5 Supply interfaces

1.5.1 Module supply input (VCC)

1.5.1.1 Overview

The modules must be supplied via the three **VCC** pins that represent the module power supply input.

Voltage must be stable, because during operation, the current drawn by the LEXI-R10 series modules through the **VCC** pins can vary by several orders of magnitude, depending on the operating mode and state, from the default active mode available at the switch-on as default factory-programmed setting of the module (see section 1.5.1.4), up to the LTE connected mode (see section 1.5.1.3), and down to the ultra-low power deep sleep mode (see section 1.5.1.5).

LEXI-R10 series are designed to have low power requirements, but it is important that the system power supply circuit can withstand with adequate safe design margin the maximum current during transmission at maximum RF power level (see the LEXI-R10 series data sheet [1]).

The internal baseband Power Management Unit, fed from the **VCC** supply input pins as illustrated in Figure 1 or in Figure 3, integrates voltage regulators generating all internal supply voltages needed by the module for its intended operations, including supply voltage for:

- The generic digital interfaces, as the UART interfaces (see 1.9.2), the I2C interface (see 1.9.4), the antenna dynamic tuner interface (see 1.11), some of the GPIOs (see 1.10), which supply voltage is available at the **V_INT** output pin (see 1.5.2),
- The digital pins in the “always-on” supply voltage domain, that are some of the GPIOs (see 1.10), which supply voltage is not available on a pin of the module, and which is always enabled when the module is switched on, even when the module is in the ultra-low power deep-sleep mode,
- The USB interface, which is in dedicated supply domain (see 1.9.3),
- The SIM interface, which supply voltage is available at the **VSIM** output pin (see 1.8.1),
- The power-on / power-off and the reset inputs, which are in dedicated supply domains (see 1.6),
- Other internal sub-systems, as for example the internal flash memory, which supply voltage is not available on a pin of the module.

Figure 3 provides a simplified block diagram of LEXI-R10 series modules internal **VCC** supply routing.

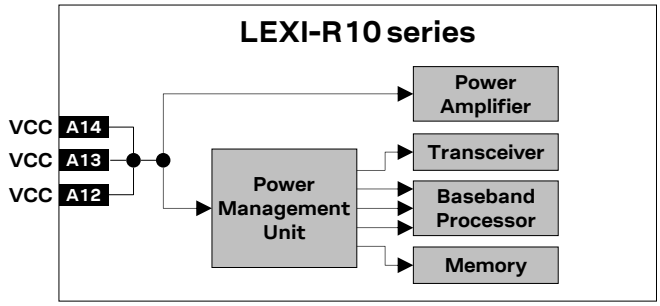

Figure 3: Block diagram of LEXI-R10 series modules internal VCC supply routing

1.5.1.2 VCC supply requirements

Table 7 summarizes the requirements for the VCC modules supply. See section 2.2.1 for suggestions to correctly design a **VCC** supply circuit compliant with the requirements listed in Table 7.

⚠ The supply circuit affects the RF compliance of the device integrating LEXI-R10 series modules with applicable required certification schemes as well as antenna circuit design. RF performance is optimized by fulfilling the requirements summarized in the Table 7.

Item	Requirement	Remark
VCC nominal voltage	Within **VCC** operating range: 3.3 V / 4.5 V	RF performance is optimized when **VCC** voltage is inside the operating range limits.
VCC voltage during normal operation	Within **VCC** operating range: 3.3 V / 4.5 V	**VCC** voltage must be above the operating range minimum limit to switch-on the module and to avoid possible switch-off of the module. Operation above **VCC** operating range is not recommended and may affect device reliability.
VCC current	Support with adequate margin the highest averaged **VCC** current consumption value in connected mode conditions specified in the LEXI-R10 series data sheet [1]	The maximum average current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and supply voltage. For a safe design margin, use a **VCC** supply source that can deliver double the typical average **VCC** current consumption at maximum Tx power, normal ambient temperature and normal voltage condition shown in the LEXI-R10 series data sheet [1].
VCC voltage ripple during Tx	Noise in the supply pins must be minimized	High supply voltage ripple values during RF transmissions in connected mode directly affect the RF compliance with the applicable certification schemes.

Table 7: VCC modules supply requirements

1.5.1.3 VCC consumption in LTE connected mode

During an LTE connection, LEXI-R10 series modules may transmit and receive simultaneously due to the frequency division duplex (FDD) mode of operation available with the LTE radio access technology, or the LEXI-R10001D module may also transmit and receive alternatively due to the time division duplex (TDD) mode of operation supported by this module on some bands (see Table 2).

Transmission and reception may last differently depending on the amount of data to be transmitted and received, depending on the specific scheduling in use, and according to the LTE connected mode discontinuous reception (cDRX) capability supported by the modules, allowing suspension while there is no traffic between the network and module.

The current consumption during transmission depends on the output RF power, which may vary from less than -40 dBm up to roughly +23 dBm, as it is always regulated by the cellular network (the current base station), according to 3GPP specifications.

For detailed consumption values in LTE connected mode, see LEXI-R10 series data sheet [1].

1.5.1.4 VCC consumption in active mode

The active mode is the state where the module is switched on and ready to communicate with an external device by means of the application interfaces (as the USB or the UART serial interfaces). The module processor core is active, and the 26 MHz reference clock frequency is used.

If low power mode configurations are disabled, as it is by default factory-programmed setting (see the AT commands manual [2], +UPSV AT command for details), the module remains in active mode.

Otherwise, if the low power mode configurations are enabled, the LEXI-R10 series modules enter the ultra-low power deep-sleep mode whenever possible.

When the module is registered to the network in active mode, the receiver is periodically activated to monitor the paging channel for paging block reception.

For detailed consumption values in active mode, see LEXI-R10 series data sheet [1].

1.5.1.5 VCC consumption in ultra-low power deep-sleep mode

LEXI-R10 series modules can automatically enter the ultra-low power deep-sleep mode whenever possible, even in-between short DRX cycles, if the functionality is enabled by the AT+UPSV command. For further details about the available setting and guidelines, see the AT commands manual [2] and the application development guide [3].

When the LEXI-R10 series modules are in ultra-low power deep-sleep mode, the main operating clock is switched off, the availability of the generic digital interfaces is temporarily suspended, while the function of the specific GPIOs in the "always-on" supply voltage domain (see 1.10) is held.

This allows a reduction the current consumption down the µA range. For detailed consumption values ultra-low power deep-sleep mode, see LEXI-R10 series data sheet [1].

1.5.2 Generic digital interfaces supply output (V_INT)

The **V_INT** output pin of LEXI-R10 series modules is internally generated by a linear LDO regulator, integrated in the Power Management Unit, enabled when the modules are switched on, and outside ultra-low power deep-sleep mode that can be entered even in between short DRX cycles after having enabled the feature by AT+UPSV command.

The **V_INT** voltage domain is used internally to supply the generic digital interfaces of the module, as

- the UART interfaces (see 1.9.2),
- the I2C interface (see 1.9.4),
- the antenna dynamic tuner interface (see 1.11),
- some of the GPIOs (see 1.10).

The typical operating voltage is 1.8 V, whereas the current capability is specified in the LEXI-R10 series data sheet [1]. The **V_INT** voltage domain can be used in place of an external discrete regulator as a reference voltage rail for external components.

The **V_INT** output pin of the LEXI-R10 series modules is connected to an internal 1.8 V supply with a current capability specified in the LEXI-R10 series data sheet [1].

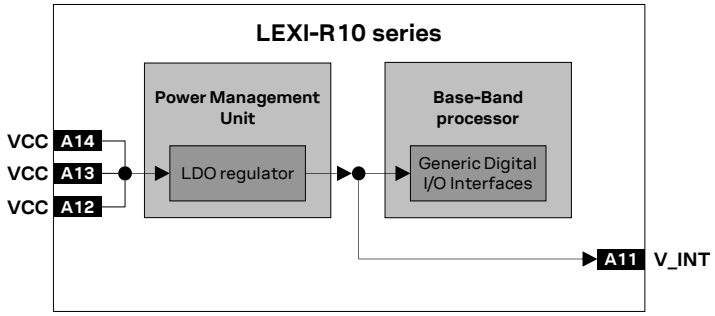

Figure 4: LEXI-R10 series interfaces supply output (V_INT) simplified block diagram

1.6 System function interfaces

1.6.1 Module power-on

When the LEXI-R10 series modules are in the not-powered mode (i.e. without a valid voltage supply present at the **VCC** module supply input), the modules' switch on can be triggered by:

- Applying a voltage supply at the **VCC** supply input within the **VCC** voltage supply operating range (see LEXI-R10 series data sheet [1], module VCC supply operating input voltage), and then forcing a low level at the **PWR_ON** input pin for a valid time (see LEXI-R10 series data sheet [1], module switch on from power off mode).

When the LEXI-R10 series modules are in the power-off mode (i.e. switched off, but with a valid voltage present at the **VCC** module supply input), the modules' switch on can be triggered by:

- Forcing a low level at the **PWR_ON** input pin for a valid time (see LEXI-R10 series data sheet [1], module switch on from power off mode).

When the LEXI-R10 series modules are in ultra-low power deep-sleep mode, the modules' wake-up can be triggered by:

- Forcing a low level at the **PWR_ON** input pin for a valid time (see LEXI-R10 series data sheet [1], module wake-up from deep sleep mode), or
- In +UPSV=5 condition, applying a rising edge at the **GPIO3** or the **GPIO6** input pin, which are in the "always-on" supply domain, appropriately configured by AT+UGPIOC command (see section 1.10, module wake-up and low power mode control).
- Using USB interface with +UUSBSLPCONF=0 condition, via USB resume procedure

The **PWR_ON** input pin is equipped with an internal active pull-up resistor, in a dedicated internal supply domain available when a valid voltage supply at the **VCC** supply input, within the **VCC** voltage supply operating range, is present. Detailed characteristics with voltages and timings are described in the LEXI-R10 series data sheet [1].

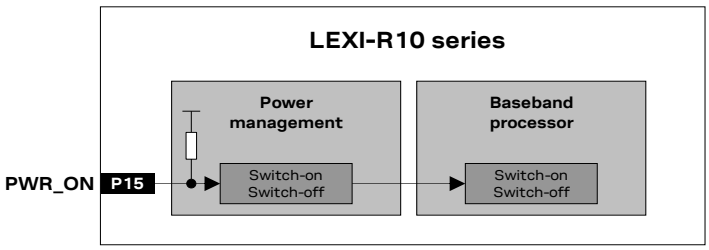

Figure 5: PWR_ON input pin description

Figure 6 shows the module switch-on sequence from the not-powered mode, with following phases:

- The external power supply is applied to the **VCC** module pins.
- The **PWR_ON** line goes high due to internal pull-up.
- The **PWR_ON** pin is set low for a valid time.
- The **RESET_N** line goes high due to internal pull-up.
- All the generic digital pins are tri-stated until the switch-on of their supply source (**V_INT**).
- The internal reset signal is held low: the baseband core and all digital pins are held in reset state.
- When the internal reset signal is released, any digital pin is set in the correct sequence from the reset state to the default operational configured state. The duration of this phase differs within generic digital interfaces and USB interface due to host / device enumeration timings.
- The module is ready to operate after all interfaces are configured.

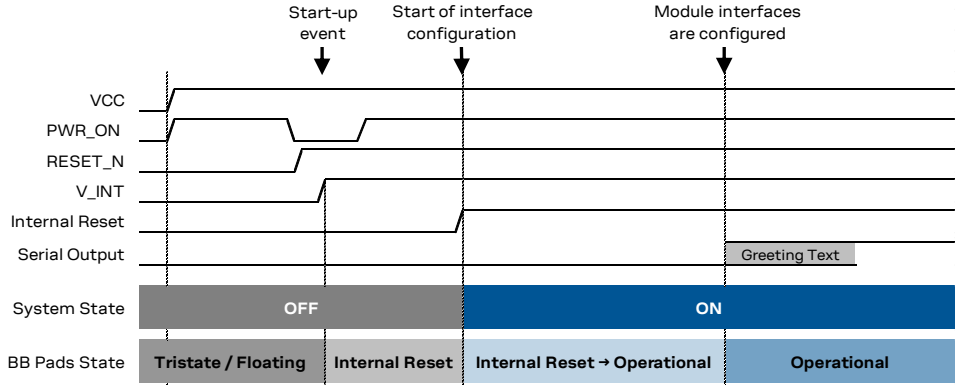

Figure 6: LEXI-R10 series switch-on sequence description

The Internal Reset signal is not available on a module pin, but it is highly recommended to monitor:

- The **V_INT** pin, to sense the start of the LEXI-R10 series module switch-on sequence
- The greeting text configured on the serial interface (see AT commands manual [2], +CSGT AT command), to signal that the module is ready to operate

Before the LEXI-R10 series module is ready to operate, the host application processor should not send any AT command over AT communication interfaces of the module.

The duration of the LEXI-R10 series modules switch-on routine can largely vary depending on the application / network settings and the concurrent module activities.

It is highly recommended to avoid an abrupt removal of the **VCC** supply, or forcing an abrupt emergency reset by asserting the **RESET_N** input, during the boot sequence of the module.

1.6.2 Module power-off

The proper graceful switch off procedure of the LEXI-R10 series modules, with storage of the current parameter settings in module's non-volatile memory and a clean network detach, can be triggered by:

- AT+CPWROFF command (see the LEXI-R10 series AT commands manual [2]), or
- Forcing a low level at the **PWR_ON** input pin for a valid time period (for detailed characteristics, see LEXI-R10 series data sheet [1], module graceful switch off)

☞ The graceful shutdown must be started as indicated above, and then a proper **VCC** supply must be held at least until the end of the modules' internal switch-off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module.

A faster emergency switch-off procedure of the modules, with storage of current parameter settings in the module's non-volatile memory, but without a clean network detach, can be triggered by:

- AT+CFUN=10 command (see the LEXI-R10 series AT commands manual [2]), or
- Forcing a rising edge at the GPIO input pin configured with the faster power-off function (see section 1.10, faster power-off).

The fastest memory-safe emergency switch off procedure of the LEXI-R10 series modules, inhibiting further operations in the non-volatile flash memory, without executing the storage of the current parameter settings, and without executing a clean network detach, can be triggered by:

- AT+CFUN=11 command (see the LEXI-R10 series AT commands manual [2]), or
- Forcing a rising edge at the GPIO input pin configured with the memory-safe power-off function (see section 1.10, memory-safe power-off).

☞ The graceful shutdown procedure must be preferred to any emergency power-off procedures, which shall be used for emergency only.

An abrupt under-voltage shutdown occurs on LEXI-R10 series modules when the **VCC** module supply is removed. If this occurs, it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory or to perform the clean network detach.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during LEXI-R10 series modules normal operations. It is highly recommended to start the graceful shutdown, and then held a proper **VCC** supply voltage at least until the end of the internal switch-off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module.

☞ If an abrupt power removal is unavoidable, it is recommended to apply a rising edge to the GPIO pin configured with the memory-safe power-off function as soon as the power failure in the supply source is detected, placing a low-ESR 470 mF capacitor at the **VCC** supply input to let the module complete the memory-safe emergency power-off.

Figure 7 and Figure 8 show the LEXI-R10 series modules switch-off sequence started by means of the AT+CPWROFF command and by the **PWR_ON** input pin respectively, with the following phases:

- When the +CPWROFF AT command is sent, or when a low pulse is applied at the **PWR_ON** input pin with appropriate time duration (see the LEXI-R10 series data sheet [1]), the module starts the switch-off routine.
- Then, if the +CPWROFF AT command has been sent, the module replies OK on the AT interface: the switch-off routine is in progress.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the necessary internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**).
- Then, the module remains switched off as long as a switch-on event does not occur (applying a low level to **PWR_ON** input), and it enters not-powered mode if the **VCC** supply is removed.

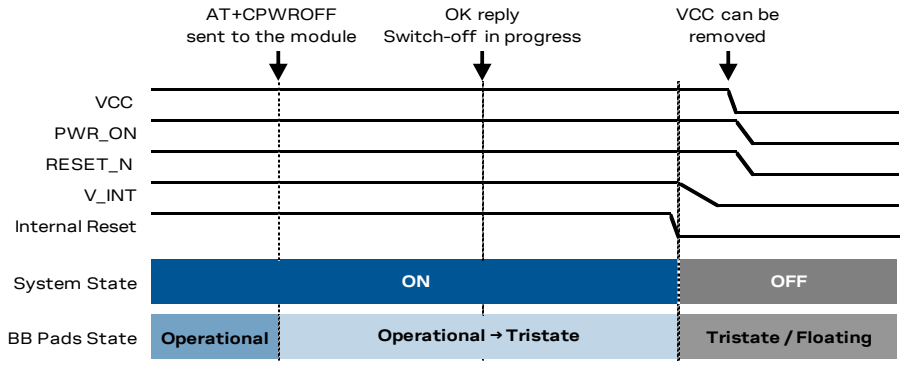

Figure 7: LEXI-R10 series modules switch-off sequence by AT+CPWROFF command

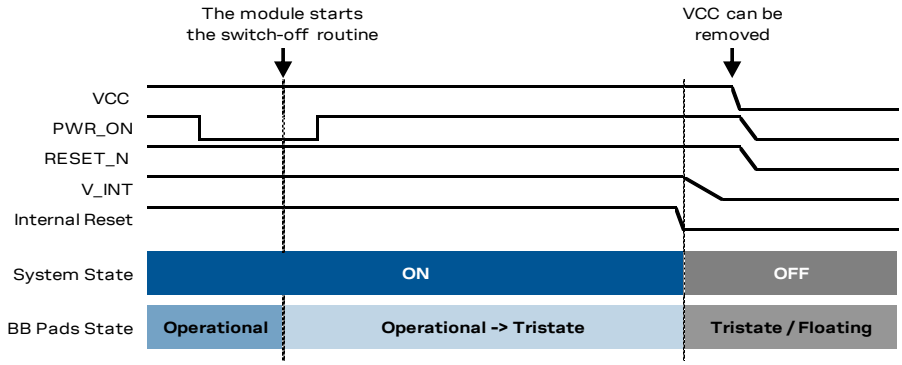

Figure 8: LEXI-R10 series modules switch-off sequence by PWR_ON pin

☞ The Internal Reset signal is not available on a module pin, but it is highly recommended to monitor:

- The **V_INT** pin, or
- The UART break condition,

to detect the end of the LEXI-R10 series module switch-off sequence

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply before the end of the module switch-off sequence, which occurs when the **V_INT** supply output is switched off.

☞ The duration of each phase in the LEXI-R10 series modules switch-off routines can largely vary depending on the application / network settings and the concurrent module activities.

1.6.3 Module reset

The graceful reset of LEXI-R10 series modules, performing storage of the current parameter settings in module's non-volatile memory and a clean network detach before the reboot, can be triggered by:

- AT+CFUN=16 command (see the LEXI-R10 series AT commands manual [2] for detailed options).

An abrupt emergency reset is triggered on LEXI-R10 series modules, with shutdown followed by a reboot of the internal power management unit, without storage of current parameter settings and without a clean network detach, when:

- A low level is applied on the **RESET_N** pin for a valid time period (see LEXI-R10 series data sheet [1], module abrupt emergency reset / reboot).

☞ It is highly recommended to avoid an abrupt hardware reset of the module by forcing a low level on the **RESET_N** input during modules normal operation: the abrupt HW reset shall be performed only if reset or shutdown via AT commands fails, or if the module does not reply to a specific AT command after a time period longer than the one defined in the AT commands manual [2].

The **RESET_N** input pin is directly connected to the power management unit IC, with an integrated pull-up to an internal supply domain, in order to perform an abrupt hardware reset when asserted for a specific time period. Asserting the **RESET_N** input pin causes an abrupt shutdown of the internal power management unit with integrated regulators for the related voltage domains internally generated. Detailed electrical characteristics with voltages and timings for the **RESET_N** input are described in the LEXI-R10 series data sheet [1].

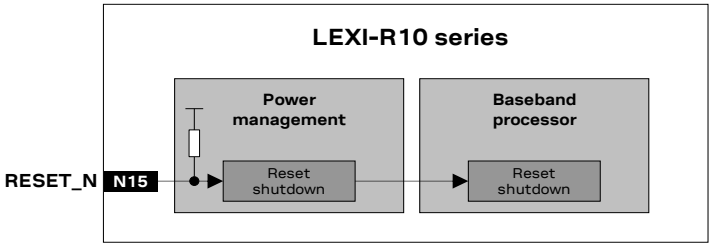

Figure 9: RESET_N input pin description

1.7 Antenna interface

1.7.1 Antenna RF interface (ANT)

LEXI-R10 series modules provide an RF interface for connecting the external antenna. The **ANT** pin represents the RF input/output for transmission and reception of cellular RF signals, as well as the RF input for reception of Wi-Fi RF signals.

The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the antenna system through a 50 Ω transmission line to allow clear RF transmission and reception.

1.7.1.1 Antenna RF interface requirements

Table 8 summarizes the requirements for the antenna RF interface. See section 2.4.1 for suggestions to correctly design antennas circuits compliant with these requirements.

⚠ The antenna circuits affect the RF compliance of the device integrating LEXI-R10 series modules with applicable required certification schemes (for more details see section 4). RF performance is optimized by fulfilling the antenna RF interface requirements summarized in Table 8.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT** port.
Frequency range	See the LEXI-R10 series data sheet [1]	The required frequency range of the antenna connected to **ANT** port depends on the operating bands of the used cellular module and the used mobile network.
Return loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the **ANT** port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as Total Radiated Power (TRP) and the Total Isotropic Sensitivity (TIS), specified by applicable related certification schemes.
Maximum gain	According to radiation exposure limits	The power gain of an antenna is the radiation efficiency multiplied by the directivity: the gain describes how much power is transmitted in the direction of peak radiation to that of an isotropic source. The maximum gain of the antenna connected to **ANT** port must not exceed the herein stated value to comply with regulatory agencies radiation exposure limits. For additional info see section 4.
Input power	> 24 dBm (> 0.25 W)	The antenna connected to the **ANT** port must support with adequate margin the maximum power transmitted by the modules.

Table 8: Tx/Rx antenna RF interface requirements

1.7.2 Antenna detection interface (ANT_DET)

The antenna detection is based on ADC measurement. The **ANT_DET** pin is an Analog to Digital Converter (ADC) provided to sense the antenna presence.

The antenna detection function provided by the **ANT_DET** pin is an optional feature that can be implemented only if the application requires it. The antenna detection is forced by the +UANTR AT command. See the AT commands manual [2] for more details on this feature.

The **ANT_DET** pin generates a DC current (for detailed characteristics see the LEXI-R10 series data sheet [1]) and measures the resulting DC voltage, thus determining the resistance from the antenna connector provided on the application board to GND. So, the requirements to achieve antenna detection functionality are the following:

- An RF antenna assembly with a built-in resistor (diagnostic circuit) must be used.
- An antenna detection circuit must be implemented on the application board.

See section 2.4.3 for antenna detection circuit on application board and diagnostic circuit on antenna assembly design-in guidelines.

1.8 SIM interface

1.8.1 SIM interface

LEXI-R10 series modules provide a SIM interface on the **VSIM**, **SIM_IO**, **SIM_CLK**, **SIM_RST** pins to connect an external SIM card or UICC chip. External 1.8 V and 3.0 V SIM card/chip types are supported.

1.8.2 SIM detection interface

The **GPIO6** pin of LEXI-R10 series modules is a 1.8 V digital pin in the “always-on” supply domain, which can be configured as an external interrupt to detect the SIM card presence (see section 1.10). This detection of an external SIM card presence is an optional feature, not necessarily required to be implemented by connecting the pin to the mechanical switch of a SIM card holder as described in section 2.5, properly configuring the digital levels:

- Low logic level at **GPIO6** input pin is recognized as SIM card not present
- High logic level at **GPIO6** input pin is recognized as SIM card present

For more details, see the AT commands manual [2], +UGPIOC and +UDCONF=50 AT commands.

1.9 Data communication interfaces

1.9.1 Overview

LEXI-R10 series modules provide the following serial interfaces for communications with the external host application processor:

- UART interfaces, described in section 1.9.2, configurable as
    - 8-wire main UART interface, as module default factory-programmed AT+USIO=0 setting, with data input/output lines, HW flow control input/output lines and modem status and control lines (**DTR**, **DSR**, **DCD** and **RI** functions), or
    - 4-wire main UART interface and 4-wire auxiliary UART interface, as alternative AT+USIO=1 and/or AT+USIO=5 setting of the module, with data input/output lines and HW flow control input/output lines only, with the auxiliary UART lines over the **DTR**, **DSR**, **DCD** and **RI** pins

- USB interface, described section 1.9.3, configurable in the following ways:
  - 2 ports for AT / data communication and 1 port for diagnostic, as default factory-programmed AT+UUSBCONF=0 setting of the module
  - RNDIS / CDC-ECM for Ethernet-over-USB, 2 ports for AT / data communication and 1 port for diagnostic, as alternative AT+UUSBCONF=4 setting of the module
  - Disabled, as alternative AT+UUSBCONF=99 setting of the module

Additionally, LEXI-R10 series modules provide the following serial interface for communications with external devices:

- I2C interface, described in section 1.9.4, is not supported by the FW of current product versions.

Using both the UART and the USB interfaces for communication with the external host application processor is uncommon, even if possible.

The UART interface only, or the USB interface only, is in general intended to be used depending on the application use-case requirements as following:

- the UART interface, as 8-wire main UART, or as 4-wire main UART and 4-wire auxiliary UART, is recommended to be used in case of low power requirements, because the minimum possible consumption of the module, in the ultra-low power deep-sleep mode as well as in the other operating modes, is achievable using the UART interface with USB disabled.
- the USB interface is recommended to be used in case of high data rate requirement, because the 480 Mb/s max baud rate of the USB makes the interface capable of sustaining the 10 Mb/s LTE Cat 1bis max data rate, while the UART max baud rate is 3 Mb/s.

In case only one interface is used for communication with the external host application processor (either the UART interface only, or the USB interface only), we recommed the following:

- In case only the UART interface is used, disable the USB by AT+UUSBCONF=99 command, and provide test-points to **USB_D+**, **USB_D-** and **USB_BOOT** pins for FW update and diagnostic.
- In case only the USB interface is used, disable the UART HW flow control by AT+UUARTCONF command, and provide test-points to UART **TXD** and **RXD** pins for FW update and to the auxiliary UART **DCD** and **DTR** pins for diagnostic purposes.

For more details about the mentioned AT commands, see the AT commands manual [2].

1.9.2 UART interfaces

1.9.2.1 UART features

LEXI-R10 series modules include a main primary UART interface (UART) in the **V_INT** supply domain, with settings configurable by dedicated AT commands (for more details, see the AT commands manual [2]), supporting:

- AT commands communication
- Data communication
- Multiplexer protocol functionality (see section 1.9.2.3)
- FW update by FOAT
- FW update by u-blox EasyFlash tool

Some of the characteristics of the main primary UART interface (UART) are the following:

- 8-wire serial port with RS-232 functionality conforming to ITU-T V.24 recommendation [6], with CMOS compatible signal levels (0 V for low data bit / ON state, 1.8 V for high data bit / OFF state)
  - Data lines (**RXD** as data output, **TXD** as data input)
  - HW flow control lines (**CTS** as flow control output, **RTS** as flow control input)
  - Modem status and control lines (**DTR** input, **DSR** output, **DCD** output, **RI** output)[1]

☞ UART signal names of the cellular modules conform to the ITU-T V.24 recommendation [6]: e.g. **TXD** line represents data transmitted by the DTE (host processor output) and received by the DCE (module input).

☞ It is recommended to provide accessible test points directly connected to the main primary UART interface **RXD** data output and **TXD** data input pins, for FW update purposes, in case the USB interface is used for the communication with the host application processor.

LEXI-R10 series modules include an auxiliary second UART interface (AUX UART) in the **V_INT** supply domain, which can be enabled as alternative function, in a mutually exclusive way, over the **DTR**, **DSR**, **DCD** and **RI** pins of the main primary UART interface, with settings configurable by dedicated AT commands (for more details, see the AT commands manual [2]), supporting:

- AT commands communication
- Data communication
- FW update by FOAT
- Diagnostic trace logging

Some of the characteristics of the auxiliary second UART interface (AUX UART) are the following:

- 4-wire serial port with RS-232 functionality conforming to ITU-T V.24 recommendation [6], with CMOS compatible signal levels (0 V for low data bit / ON state, 1.8 V for high data bit / OFF state)
  - Data lines (**DCD** as data output, **DTR** as data input)
  - HW flow control lines (**RI** as flow control output, **DSR** as flow control input)

☞ It is recommended to provide accessible test points directly connected to the auxiliary UART interface **DCD** data output and **DTR** data input pins, for diagnostic purposes, in case the USB interface is used for the communication with the host application processor.

UART interfaces are by default configured in AT command mode: the module waits for AT command instructions and interprets all the characters received as commands to execute:

- AT commands according to 3GPP TS 27.007 [7], 3GPP TS 27.005 [8], 3GPP TS 27.010 [9]
- u-blox AT commands (see the AT commands manual [2])

The default baud rate is 115200 b/s, while the default frame format is 8N1 (8 data bits, no parity, 1 stop bit: see Figure 10). Other baud rates, up to 3 Mbit/s, can be configured by dedicated AT command (see the AT commands manual [2]).

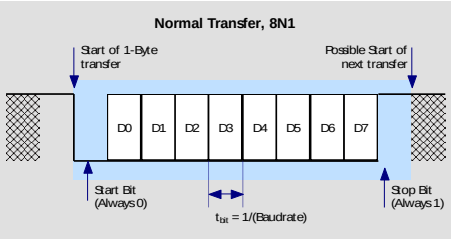

Figure 10: UART 8N1 frame format (8 data bits, no parity, 1 stop bit)

[1] **DTR**, **DSR**, **DCD** and **RI** pins can be alternatively configured, in mutually exclusive way, as second auxiliary UART interface (UART AUX). The Ring Indicator (RI) function can be alternatively configured over GPIO (see section 1.10).

1.9.2.2 UART and power saving

The power saving configuration is controlled by the AT+UPSV command (for description see the AT commands manual [2], for further details and guidelines see the application development guide [3]).

The low power mode configurations are by default disabled, as per factory-programmed setting of the AT+UPSV command. In this scenario, LEXI-R10 series modules have the UART interfaces available to communicate with an external host processor.

If the low power mode configurations are enabled by the AT+UPSV command, the LEXI-R10 series modules can enter the ultra-low power deep-sleep mode whenever possible, even very frequently, as in-between short DRX cycles.

When the ultra-low power deep sleep mode is entered, all the lines in **V_INT** supply domain go low, including all the lines of the UART interfaces, as the data lines, the hardware flow control lines and the Ring Indicator line, because the **V_INT** supply domain of the UART interfaces is switched off.

When LEXI-R10 series modules are in ultra-low power deep sleep mode, the external host processor may see a low level at the module HW flow control output (the **CTS** pin) due to:

- The HW flow control output function (indicating the CTS line “on” state), or
- The deep sleep mode status (with the UART in the “off” state)

The external host processor can monitor the UART break condition at the **RXD** data output of the module, or can monitor the **V_INT** output of the module, to determine if

- The HW flow control is low due to deep sleep mode (with **V_INT** “off”), or
- The HW flow control is low due to its HW flow control function (with **V_INT** “on”)

Additionally, LEXI-R10 series modules include some GPIO pins in the “always-on” supply domain (see section 1.10), that keep their function available in ultra-low power deep sleep mode. These always-on GPIOs can be used to

- Wake-up and control the low power mode of the module once enabled by AT+UPSV=5 command
- Monitor the module status indication: “low” if the module is switched off, “high” if the module is in any other mode (deep sleep, active, or connected)
- Get the Ring Indicator / URC notifications even in ultra-low power deep sleep mode

The following Figure 11 show an illustrative diagram of the UART interfaces’ behavior with the power saving configurations enabled.

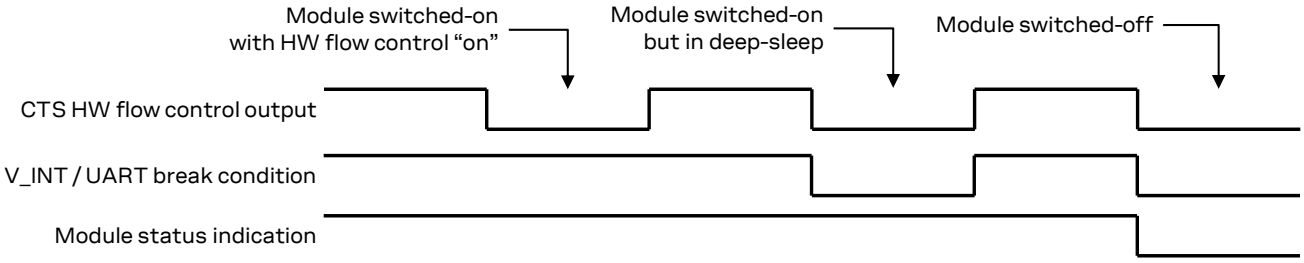

Figure 11: LEXI-R10 series illustrative behavior of the UART and “always-on” GPIO with power saving configurations enabled

1.9.2.3 UART multiplexer protocol

LEXI-R10 series modules include multiplexer functionality as per 3GPP TS 27.010 [9], on the primary UART physical link. This is a data link protocol which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows a number of simultaneous sessions over the primary UART physical link.

1.9.3 USB interface

1.9.3.1 USB features

LEXI-R10 series modules include a high-speed USB 2.0 interface, in dedicated supply domain, with a maximum 480 Mb/s data rate according to the USB 2.0 specification [5]. The module itself acts as a USB device and can be connected to any compatible USB host. The USB interface include multiple virtual serial ports to support various functions such as:

- AT commands communication
- Data communication
- FW update by FOAT
- FW update by u-blox EasyFlash tool
- Diagnostic trace logging
- Ethernet over USB

LEXI-R10 series modules provide the following USB lines:

- the **USB_D+** / **USB_D-** lines, carrying the USB data and signaling
- the **USB_BOOT** input pin to enable the FW update over the USB interface.

☞ The **USB_BOOT** input pin must be set high, at the 1.8 V voltage level of the **V_INT** supply output, to enable the FW update over the USB interface at the boot of the module, using the u-blox EasyFlash tool to execute the FW update. Only if the **USB_BOOT** pin is left floating (unconnected), or it is set low (grounded), the modules can boot in normal operating mode.

☞ If the USB interface is enabled, the module does not enter the ultra-low power deep-sleep mode.

☞ It is recommended to provide accessible test points directly connected to the **USB_D+** and **USB_D-** pins, as well as to the **USB_BOOT** pin, for FW update and for diagnostic purposes, in case the UART interfaces are used for the communication with the host application processor.

The USB profile of LEXI-R10 series modules identifies itself by dedicated VID (Vendor ID) and PID (Product ID) combination, included in the USB device descriptor following USB 2.0 specifications [5].

Using the default USB configuration (+UUSBCONF=0) with 2 CDC-ACM for AT commands and data, and 1 CDC-ACM for diagnostic, the USB VID and PID are the following:

- VID = 0x1546, PID = 0x1301

Using the Ethernet over USB configuration (+UUSBCONF=4,"RNDIS") with 2 CDC-ACM for AT and data, 1 CDC-ACM for diagnostic, and 1 RNDIS, the USB VID and PID are the following:

- VID = 0x1546, PID = 0x1302

Using the Ethernet over USB configuration (+UUSBCONF=4,"ECM") with 2 CDC-ACM for AT and data, 1 CDC-ACM for diagnostic, and 1 CDC-ECM, the USB VID and PID are the following:

- VID = 0x1546, PID = 0x1303

1.9.4 I2C interface

☞ The I2C interface is not supported by the FW of the “00B” and “01B” product versions.

LEXI-R10 series modules include an I2C-bus compatible interface (**SDA**, **SCL** lines) in the **V_INT** supply domain, available to communicate with external I2C devices: the LEXI-R10 series module acts as an I2C host which can communicate with I2C devices in accordance with the I2C bus specifications [10].

The **SDA** and **SCL** pins have internal pull-up to **V_INT**, so there is no need of additional pull-up resistors on the external application board.

1.10 General purpose input / output

LEXI-R10 series modules include ten GPIO pins which can be configured to provide custom functions as summarized in Table 9 (for more details, see AT commands manual [2], +UGPIOC AT command).

Note that the GPIO pins are in two different supply domains:

- The **GPIO1**, **GPIO5**, **GPIO7**, **GPIO8**, **GPIO9** and **GPIO10** pins are in the **V_INT** supply domain as the other generic digital interfaces (the UART interfaces, the I2C interface, and the antenna dynamic tuner interface), meaning that their function is not available when the module is in ultra-low power deep-sleep mode, with the generic digital interface supply (**V_INT**) switched off,
- The **GPIO2**, **GPIO3**, **GPIO4** and **GPIO6** pins are in the "always-on" supply domain, meaning that their function is available also when the module is in ultra-low power deep-sleep mode, with the generic digital interface supply (**V_INT**) switched off.

Function	Description	Default GPIO	Configurable GPIOs
General purpose output	Output to set the high or the low digital level	--	All
General purpose input	Input to sense high or low digital level	--	All
Network status indication	Output indicating cellular network status: registered, data transmission, no service	--	GPIO1, GPIO2, GPIO4, GPIO5, GPIO7, GPIO8, GPIO9, GPIO10
Module status indication	Output indicating module status: low when switched off, high when in deep-sleep, idle, active, or connected mode	--	GPIO2, GPIO4
SIM card detection	Input for external SIM card physical presence detection, to optionally enable / disable the SIM interface in case the SIM hot insertion function is enabled by AT+UDCONF=50	--	GPIO6
Ring indicator	Output providing events indicator (as the UART RI line)	--	GPIO1, GPIO2, GPIO4, GPIO5, GPIO7, GPIO8, GPIO9, GPIO10
Module wake-up and low power mode control	Input to wake-up and control the low power mode of the module once enabled by AT+UPSV command	--	GPIO3, GPIO6
Faster power-off	Input with internal pull-down to trigger a faster emergency shutdown (as AT+CFUN=10) by applying a rising edge	--	GPIO3, GPIO6
Memory-safe power-off	Input with internal pull-down to trigger the fastest memory-safe emergency shutdown (as AT+CFUN=11) by applying a rising edge	--	GPIO3, GPIO6
Pin disabled	Tri-state with an internal active pull-up enabled	GPIO1	GPIO1
	Tri-state with an internal active pull-down enabled	GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, GPIO9, GPIO10	GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, GPIO9, GPIO10

Table 9: LEXI-R10 series modules GPIO custom functions configuration

1.11 Antenna dynamic tuner interface

LEXI-R10 series modules include two digital output pins (**RFCTRL1** and **RFCTRL2**), in the **V_INT** supply domain, that can be configured, as optional feature, to control in real time an external antenna tuning IC, changing their output value dynamically according to the specific actual RF band in use by the module. Table 10 shows the default factory-programmed configuration that can be changed by dedicated AT command.

RFCTRL1	RFCTRL2	LEXI-R10401D frequency band in use	LEXI-R10801D frequency band in use
0	0	B2, B4, B12, B13, B14, B66, Wi-Fi	B1, B3, B7, B28, Wi-Fi
0	1	B5	B5, B20
1	0	-	B8
1	1	B71	-

Table 10: LEXI-R10 series modules antenna dynamic tuning truth table (default factory-programmed configuration)

1.12 Reserved pins (RSVD)

LEXI-R10 series modules include pins reserved for future use, marked as **RSVD**, which can all be left unconnected on the application board.

2 Design-in

2.1 Overview

For an optimal integration of the LEXI-R10 series modules in the final application board, follow the design guidelines stated in this section.

Every application circuit must be suitably designed to ensure the correct functionality of the relative interface, but a number of points require greater attention during the design of the application device.

The following list provides a rank of importance in the application design, starting from the highest relevance:

1. Module antenna connection: **ANT** pin.
   Cellular antenna circuit directly affects the RF compliance of the device integrating a LEXI-R10 series module with applicable certification schemes. Follow the suggestions provided in the relative section 2.4 for the schematic and layout design.

2. Module supply: **VCC** and **GND** pins.
   The supply circuit affects the RF compliance of the device integrating a LEXI-R10 series module with the applicable required certification schemes as well as the antenna circuit design. Very carefully follow the suggestions provided in the relative section 2.2.1 for the schematic and layout design.

3. SIM interface: **VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST** pins.
   Accurate design is required to ensure SIM functionality reducing the risk of RF coupling. Carefully follow the guidelines provided in relative section 2.5 for schematic and layout design.

4. System functions: **PWR_ON** and **RESET_N** pins.
   Accurate design is required to ensure that the voltage level is well defined during operation. Carefully follow the guidelines provided in relative section 2.3 for schematic and layout design.

5. Other digital interfaces: UART, USB, I2C, GPIOs, and reserved pins.
   Accurate design is required to ensure correct functionality and reduce the risk of digital data frequency harmonics coupling. Follow the suggestions provided in sections 2.6.1, 2.6.2, 2.6.3, 2.7 and 2.8 for the schematic and layout design.

6. Other supplies: **V_INT** generic digital interfaces supply.
   Accurate design is required to ensure correct functionality. Follow the suggestions provided in the corresponding section 2.2.2 for the schematic and layout design.

☞ It is recommended to follow the specific design guidelines provided by each manufacturer of any external part selected for the application board integrating the u-blox cellular modules.

2.2 Supply interfaces

2.2.1 Module supply (VCC)

2.2.1.1 General guidelines for VCC supply circuit selection and design

All the available **VCC** pins have to be connected to the external supply minimizing the power loss due to series resistance.

GND pins are internally connected. Application design shall connect all the available pads to solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

LEXI-R10 series modules must be sourced through the **VCC** pins with a suitable DC power supply that should meet the following prerequisites to comply with the modules **VCC** requirements summarized in Table 7.

The appropriate DC power supply can be selected according to the application requirements (see Figure 12) between the different possible supply sources types, which most common ones are the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery

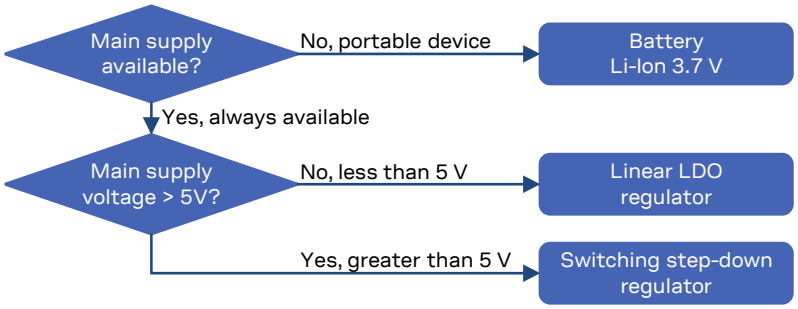

Figure 12: VCC supply concept selection

The switching step-down regulator is the typical choice when primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the operating supply voltage of LEXI-R10 series. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. See section 2.2.1.2 for design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less or equal than 5 V). In this case, the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. See section 2.2.1.3 for design-in.

If LEXI-R10 series modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided. See sections 2.2.1.4, 2.2.1.5, 2.2.1.6 and 2.2.1.7 for specific design-in.

Keep in mind that the use of rechargeable batteries requires the implementation of a suitable charger circuit, which is not included in the modules. The charger circuit needs to be designed to prevent over-voltage on **VCC** pins, and it should be selected according to the application requirements. A DC/DC switching charger is the typical choice when the charging source has a high nominal voltage (e.g. ~12 V), whereas a linear charger is the typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source, then a suitable charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery. See sections 2.2.1.6 and 2.2.1.7 for specific design-in.

An appropriate primary (not rechargeable) battery can be selected considering the maximum current specified in the LEXI-R10 series data sheet [1] during connected mode, considering that primary cells might have weak power capability. See section 2.2.1.5 for specific design-in.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can result as mutually exclusive.

The selected regulator or battery must be able to support with adequate margin the highest averaged current consumption value specified in the LEXI-R10 series data sheet [1].

The following sections highlight some design aspects for each of the supplies listed above providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 7.

2.2.1.2 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail source to the **VCC** value is high, since switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.8 V value of the **VCC** supply.

The characteristics of the switching regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 7:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum current consumption occurring during transmissions at the maximum power, as specified in the LEXI-R10 series data sheet [1].
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **High switching frequency:** for best performance and for smaller applications it is recommended to select a switching frequency ≥ 600 kHz (since L-C output filter is typically smaller for high switching frequency). The use of a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be carefully evaluated since this can produce noise in the **VCC** profile and therefore negatively impact modulation spectrum performance.
- **PWM mode operation**: it is preferable to select regulators with Pulse Width Modulation (PWM) mode. While in connected mode, the Pulse Frequency Modulation (PFM) mode and PFM/PWM modes transitions must be avoided to reduce noise on **VCC** voltage profile. Switching regulators can be used that are able to switch between low ripple PWM mode and high ripple PFM mode, provided that the mode transition occurs when the module changes status from the active mode to connected mode. It is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold.

Figure 13 and the components listed in Table 11 show an example of a high reliability power supply circuit for the LEXI-R10 series modules, where the module **VCC** input is supplied by a step-down switching regulator capable of delivering with adequate safe margin the highest current specified in the LEXI-R10 series data sheet [1], with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz.

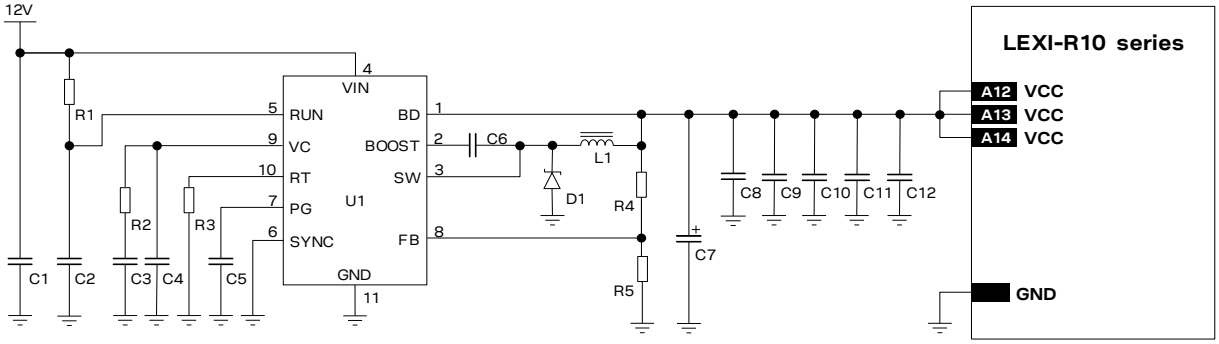

Figure 13: Example of high reliability VCC supply circuit for LEXI-R10 series modules, using a step-down regulator

Reference	Description	Part number - Manufacturer
C1	10 µF capacitor ceramic X7R 5750 15% 50 V	Generic manufacturer
C2	10 nF capacitor ceramic X7R 0402 10% 16 V	Generic manufacturer
C3	680 pF capacitor ceramic X7R 0402 10% 16 V	Generic manufacturer
C4	22 pF capacitor ceramic C0G 0402 5% 25 V	Generic manufacturer
C5	10 nF capacitor ceramic X7R 0402 10% 16 V	Generic manufacturer
C6	470 nF capacitor ceramic X7R 0603 10% 25 V	Generic manufacturer
C7	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C8	100 nF capacitor ceramic X7R 16 V	GRM155R71C104KA01 - Murata
C9	10 nF capacitor ceramic X7R 16 V	GRM155R71C103KA01 - Murata
C10	82 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 - Murata
C11	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E150JA01 - Murata
C12	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
D1	Schottky diode 40 V 3 A	MBRA340T3G - ON Semiconductor
L1	10 µH inductor 744066100 30% 3.6 A	744066100 - Wurth Electronics
R1	470 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	15 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R3	22 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R4	390 kΩ resistor 0402 1% 0.063 W	Generic manufacturer
R5	100 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
U1	Step-down regulator MSOP10 3.5 A 2.4 MHz	LT3972IMSE#PBF - Linear Technology

Table 11: Components for high reliability VCC supply circuit for LEXI-R10 series modules, using a step-down regulator

☞ See section 2.2.1.9, particularly Figure 21 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

Figure 14 and the components listed in Table 12 show an example of a low cost power supply circuit suitable for the LEXI-R10 series modules, where the module **VCC** is supplied by a step-down switching regulator capable of delivering with adequate safe margin the highest current specified in LEXI-R10 series data sheet [1], transforming a 12 V supply input.

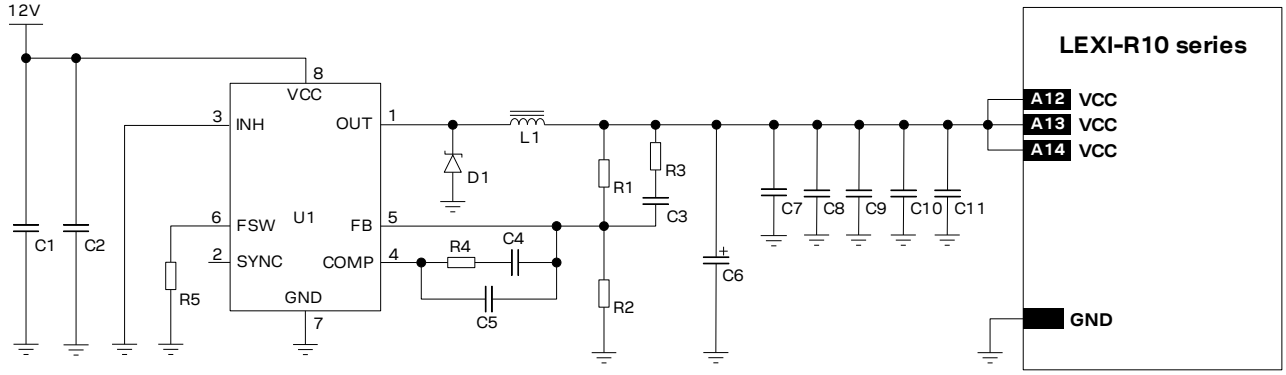

Figure 14: Example of low cost VCC supply circuit for LEXI-R10 series modules, using a step-down regulator

Reference	Description	Part number - Manufacturer
C1	22 µF capacitor ceramic X5R 1210 10% 25 V	Generic manufacturer
C2	220 nF capacitor ceramic X7R 0603 10% 25 V	Generic manufacturer
C3	5.6 nF capacitor ceramic X7R 0402 10% 50 V	Generic manufacturer
C4	6.8 nF capacitor ceramic X7R 0402 10% 50 V	Generic manufacturer
C5	56 pF capacitor ceramic C0G 0402 5% 50 V	Generic manufacturer
C6	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C7	100 nF capacitor ceramic X7R 16 V	GRM155R71C104KA01 - Murata
C8	10 nF capacitor ceramic X7R 16 V	GRM155R71C103KA01 - Murata
C9	82 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 - Murata
C10	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E150JA01 - Murata
C11	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
D1	Schottky diode 25V 2 A	STPS2L25 – STMicroelectronics
L1	5.2 µH inductor 30% 5.28A 22 mΩ	MSS1038-522NL – Coilcraft
R1	4.7 kΩ resistor 0402 1% 0.063 W	Generic manufacturer
R2	910 Ω resistor 0402 1% 0.063 W	Generic manufacturer
R3	82 Ω resistor 0402 5% 0.063 W	Generic manufacturer
R4	8.2 kΩ resistor 0402 5% 0.063 W	Generic manufacturer
R5	39 kΩ resistor 0402 5% 0.063 W	Generic manufacturer
U1	Step-down regulator 8-VFQFPN 3 A 1 MHz	L5987TR – ST Microelectronics

Table 12: Suggested components for low cost VCC circuit for LEXI-R10 series modules, using a step-down regulator

☞ See section 2.2.1.9, particularly Figure 21 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.3 Guidelines for VCC supply circuit design using LDO linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail source and the **VCC** value is low. The linear regulators provide high efficiency when transforming a 5 V DC supply to a voltage value within the module **VCC** normal operating range.

The characteristics of the Low Drop-Out (LDO) linear regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 7:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum current consumption occurring during a transmission at the maximum Tx power, as specified in the LEXI-R10 series data sheet [1].
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the rated range (i.e. check the voltage drop from the maximum input voltage to the minimum output voltage to evaluate the power dissipation of the regulator).

Figure 15 and the components listed in Table 13 show an example of a high reliability power supply circuit for LEXI-R10 series modules, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering with adequate safe margin the highest current specified in LEXI-R10 series data sheet [1], with an appropriate power handling capability. The regulator described in this example supports a wide input voltage range, and it includes internal circuitry for reverse battery protection, current limiting, thermal limiting and reverse current protection.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range (e.g. ~4.1 V). This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.

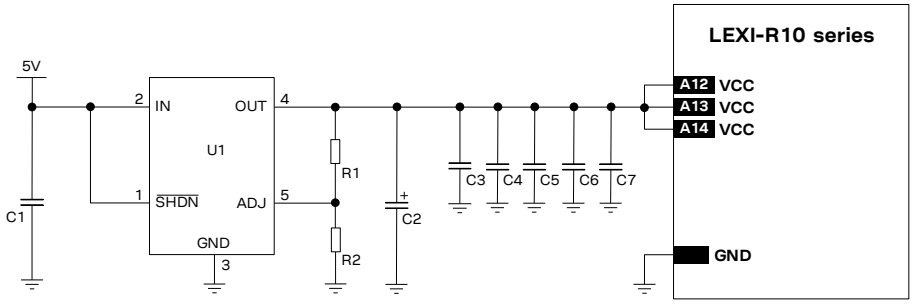

Figure 15: Example of high reliability VCC supply circuit for LEXI-R10 series modules, using an LDO linear regulator

Reference	Description	Part number - Manufacturer
C1	10 µF capacitor ceramic X5R 0603 20% 6.3 V	Generic manufacturer
C2	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C3	100 nF capacitor ceramic X7R 16 V	GRM155R71C104KA01 - Murata
C4	10 nF capacitor ceramic X7R 16 V	GRM155R71C103KA01 - Murata
C5	82 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 - Murata
C6	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E150JA01 - Murata
C7	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
R1	9.1 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	3.9 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
U1	LDO linear regulator ADJ 3.0 A	LT1764AEQ#PBF - Linear Technology

Table 13: Suggested components for high reliability VCC circuit for LEXI-R10 series modules, using an LDO regulator

☞ See the section 2.2.1.9, and in particular Figure 21 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

Figure 16 and the components listed in Table 14 show an example of a low cost power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the specified highest current, with an appropriate power handling capability. The regulator described in this example supports a limited input voltage range and it includes internal circuitry for current and thermal protection.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module VCC normal operating range (e.g. ~4.1 V). This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.

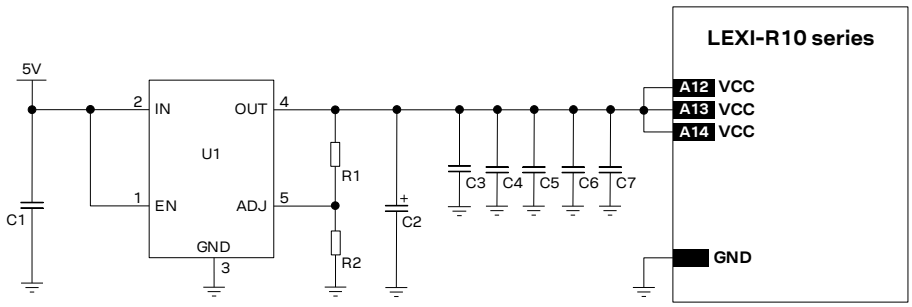

Figure 16: Example of low cost VCC supply circuit for LEXI-R10 series modules, using an LDO linear regulator

Reference	Description	Part number - Manufacturer
C1	10 µF capacitor ceramic X5R 0603 20% 6.3 V	Generic manufacturer
C2	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C3	100 nF capacitor ceramic X7R 16 V	GRM155R71C104KA01 - Murata
C4	10 nF capacitor ceramic X7R 16 V	GRM155R71C103KA01 - Murata
C5	82 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 - Murata
C6	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E150JA01 - Murata
C7	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
R1	27 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	4.7 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
U1	LDO linear regulator ADJ 3.0 A	LP38501ATJ-ADJ/NOPB - Texas Instrument

Table 14: Suggested components for low cost VCC supply circuit for LEXI-R10 series modules, using an LDO linear regulator

☞ See the section 2.2.1.9, and in particular Figure 21 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.4 Guidelines for VCC supply circuit design using a rechargeable battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 7:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its related output circuit connected to the **VCC** pins must be capable of delivering the maximum current occurring during a transmission at maximum Tx power, as specified in the LEXI-R10 series data sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a **VCC** voltage drop below the operating range summarized in Table 7 during Tx bursts.

2.2.1.5 Guidelines for VCC supply circuit design using a primary battery

The characteristics of a primary (non-rechargeable) battery connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 7:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its related output circuit connected to the **VCC** pins must be capable of delivering the maximum current consumption occurring during a transmission at maximum Tx power, as specified in LEXI-R10 series data sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a **VCC** voltage drop below the operating range summarized in Table 7 during transmit bursts.

2.2.1.6 Guidelines for external battery charging circuit

LEXI-R10 series modules do not have an on-board charging circuit. Figure 17 provides an example of a battery charger design, suitable for applications that are battery powered with a Li-Ion (or Li-Polymer) cell.

In the application circuit, a rechargeable Li-Ion (or Li-Polymer) battery cell, that features the correct pulse and DC discharge current capabilities and the appropriate DC series resistance, is directly connected to the **VCC** supply input of the module. Battery charging is completely managed by the battery charger IC, which from a USB power source (5.0 V typ.), linearly charges the battery in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current.
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor.
- **Constant voltage**: when the battery voltage reaches the regulated output voltage, the battery charger IC starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor or when the charging timer reaches the factory set value.

Using a battery pack with an internal NTC resistor, the battery charger IC can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

The battery charger IC, as linear charger, is more suitable for applications where the charging source has a relatively low nominal voltage (~5 V), so that a switching charger is suggested for applications

where the charging source has a relatively high nominal voltage (e.g. ~12 V, see section 2.2.1.7 for the specific design-in).

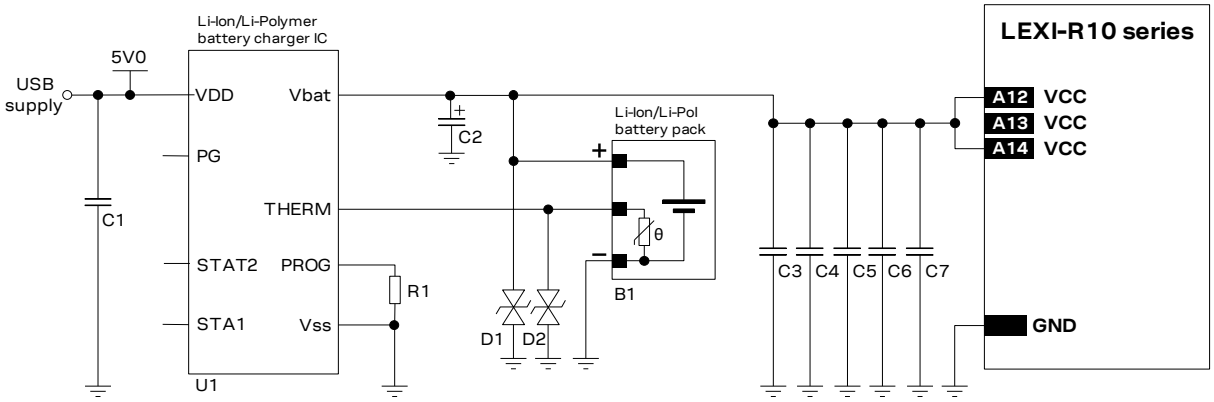

Figure 17: Li-Ion (or Li-Polymer) battery charging application circuit

Reference	Description	Part number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 470 Ω NTC	Generic manufacturer
C1	1 µF capacitor ceramic X7R 16 V	Generic manufacturer
C2	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C3	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
C4	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
C5	82 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 - Murata
C6	10 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C7	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2	Low capacitance ESD protection	CG0402MLE-18G - Bourns
R1	10 kΩ resistor 0.1 W	Generic manufacturer
U1	Single cell Li-Ion (or Li-Polymer) battery charger IC	MCP73833 - Microchip

Table 15: Suggested components for the Li-Ion (or Li-Polymer) battery charging application circuit

☞ See section 2.2.1.9, particularly Figure 21 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.7 Guidelines for external charging and power path management circuit

Application devices where both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as a possible supply source, should implement a suitable charger / regulator with integrated power path management function to supply the module and the whole device while simultaneously and independently charging the battery.

Figure 18 reports a simplified block diagram circuit showing the working principle of a charger / regulator with integrated power path management function. This component allows the system to be powered by a permanent primary supply source (e.g. ~12 V) using the integrated regulator, which simultaneously and independently recharges the battery (e.g. 3.7 V Li-Pol) that represents the back-up supply source of the system. The power path management feature permits the battery to supplement the system current requirements when the primary supply source is not available or cannot deliver the peak system currents.

A power management IC should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 7:

- High efficiency internal step down converter, with characteristics as indicated in section 2.2.1.2
- Low internal resistance in the active path Vout – Vbat, typically lower than 50 mΩ
- High efficiency switch mode charger with separate power path control

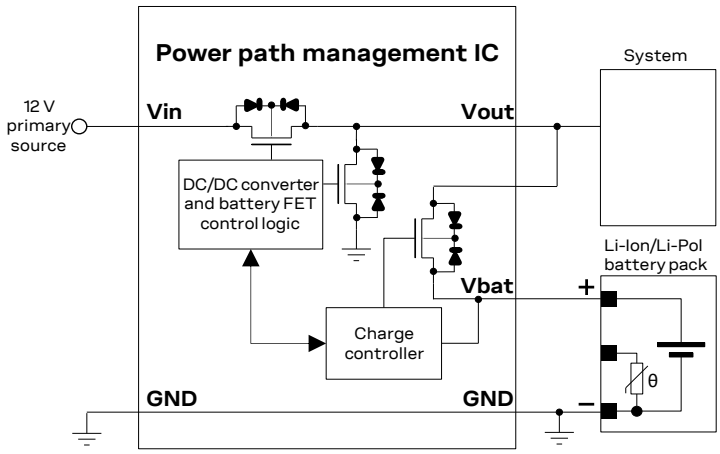

Figure 18: Charger / regulator with integrated power path management circuit block diagram

Figure 19 and the parts listed in Table 16 provide an application circuit example where the MPS MP2617H switching charger / regulator with integrated power path management function provides the supply to the cellular module. At the same time it also concurrently and autonomously charges a suitable Li-Ion (or Li-Polymer) battery with the correct pulse and DC discharge current capabilities and the appropriate DC series resistance according to the rechargeable battery recommendations described in section 2.2.1.4.

The MP2617H IC constantly monitors the battery voltage and selects whether to use the external main primary supply / charging source or the battery as supply source for the module, and starts a charging phase accordingly.

The MP2617H IC normally provides a supply voltage to the module regulated from the external main primary source allowing immediate system operation even under missing or deeply discharged battery: the integrated switching step-down regulator is capable to provide up to 3 A output current with low output ripple and fixed 1.6 MHz switching frequency in PWM mode operation. The module load is satisfied in priority, then the integrated switching charger will take the remaining current to charge the battery.

Additionally, the power path control allows an internal connection from battery to the module with a low series internal ON resistance (40 mΩ typical), in order to supplement additional power to the module when the current demand increases over the external main primary source or when this external source is removed.

Battery charging is managed in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current.
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for the application.
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the current is progressively reduced until the charge termination is done. The charging process ends when the charging current reaches the 10% of the fast-charge current or when the charging timer reaches the value configured by an external capacitor.

Using a battery pack with an internal NTC resistor, the MP2617H can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Several parameters as the charging current, the charging timings, the input current limit, the input voltage limit, the system output voltage can be easily set according to the specific application requirements, as the actual electrical characteristics of the battery and the external supply / charging source: suitable resistors or capacitors must be accordingly connected to the related pins of the IC.

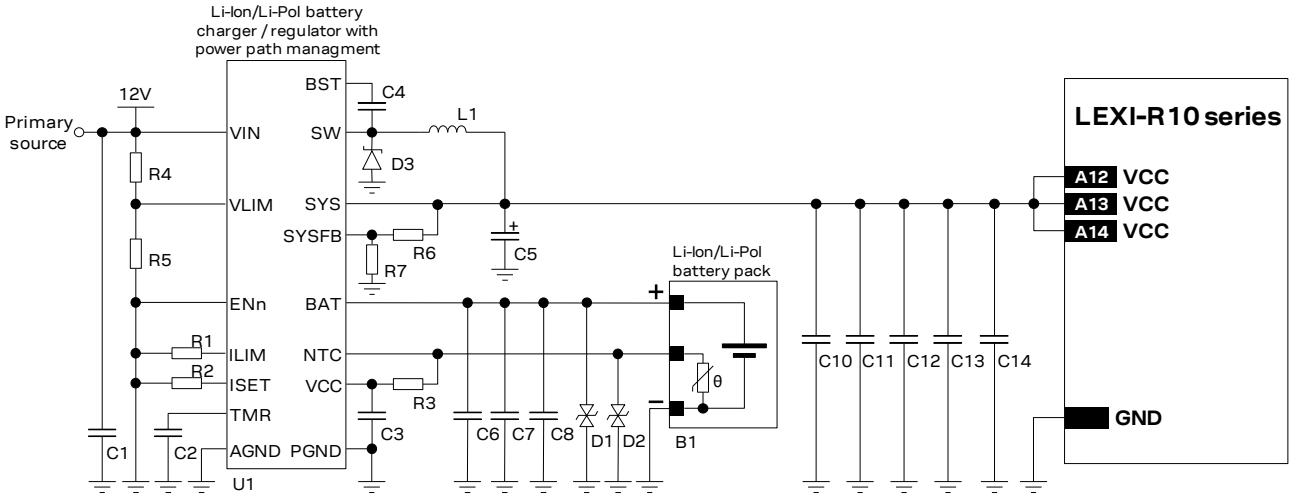

Figure 19: Li-Ion (or Li-Polymer) battery charging and power path management application circuit

Reference	Description	Part number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 10 kΩ NTC	Generic manufacturer
C1, C6	22 µF capacitor ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C2, C4, C10	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C3	1 µF capacitor ceramic X7R 0603 10% 25 V	GRM188R71E105KA12 - Murata
C5	330 µF capacitor tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C7, C12	82 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 - Murata
C8, C13	15 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C11	10 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C14	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
D1, D2	Low capacitance ESD protection	CG0402MLE-18G - Bourns
D3	Schottky diode 40 V 3 A	MBRA340T3G - ON Semiconductor
R1, R3, R5, R7	10 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
R2	1.05 kΩ resistor 0402 1% 0.1 W	Generic manufacturer
R4	22 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
R6	26.5 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
L1	2.2 µH inductor 7.4 A 13 mΩ 20%	SRN8040-2R2Y - Bourns
U1	Li-Ion/Li-Polymer battery DC/DC charger / regulator with integrated power path management function	MP2617H - Monolithic Power Systems (MPS)

Table 16: Suggested components for battery charging and power path management application circuit

☞ See the section 2.2.1.9, and in particular Figure 21 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.8 Guidelines for removing VCC supply

Removing the **VCC** power supply may be useful to further minimize the current consumption when LEXI-R10 series modules are switched off, even if this is not really needed considering the extremely low consumption of the LEXI-R10 series modules when they are switched off (see LEXI-R10 series data sheet [1] for module current consumption figures).

The **VCC** supply source can be removed using an appropriate low-leakage load switch or p-channel MOSFET controlled by the application processor as shown in Figure 20, given that the external switch has provided:

- Ultra-low leakage current (for example, less than 1 µA), to minimize the current consumption
- Very low $R_{DS(ON)}$ series resistance (for example, less than 50 mΩ), to minimize voltage drops
- Adequate maximum drain current (see the LEXI-R10 series data sheet [1] for module current consumption figures)

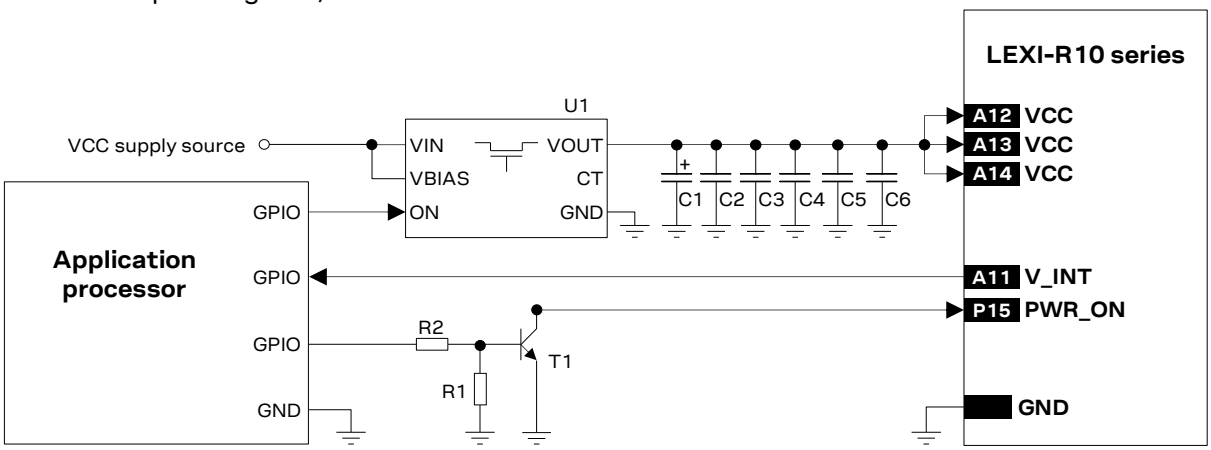

Figure 20: Example of application circuit for VCC supply removal

Reference	Description	Part number - Manufacturer
C1	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C2	10 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C4	82 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 - Murata
C5	15 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C6	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
R1, R3	47 kΩ resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R2	10 kΩ resistor 0402 5% 0.1 W	RC0402JR-0710KL - Yageo Phycomp
T1	NPN BJT transistor	BC847 - Infineon
U1	Ultra-low resistance load switch	TPS22967 - Texas Instruments

Table 17: Components for VCC supply removal application circuit

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during LEXI-R10 series normal operations: the **VCC** supply can be removed only after **V_INT** goes low, indicating that the module has entered deep-sleep Power Saving Mode or power-off mode.

☞ See the section 2.2.1.9, and in particular Figure 21 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.9 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The series resistance of the supply lines (connected to the modules **VCC** and **GND** pins) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize losses.

Three pins are allocated to **VCC** supply connection. Several pins are designated for **GND** connection. It is recommended to correctly connect all of them to supply the module minimizing series resistance.

To reduce voltage ripple and noise, improving RF performance especially if the application device integrates an internal antenna, place the following bypass capacitors near the **VCC** pins:

- 82 pF 0402 ceramic capacitor with Self-Resonant Frequency in the 800/900 MHz range
- 15 pF 0402 ceramic capacitor with Self-Resonant Frequency in the 1800/1900 MHz range
- 8.2 pF 0402 ceramic capacitor with Self-Resonant Frequency in the 2500/2600 MHz range
- 10 nF 0402 ceramic capacitor, to filter digital logic noise from clocks and data sources
- 100 nF 0402 ceramic capacitor, to filter digital logic noise from clocks and data sources

An additional capacitor is recommended to avoid undershoot and overshoot at the start and at the end of RF transmission:

- 100 µF low ESR capacitor (e.g Kemet T520B107M006ATE015)

An additional series ferrite bead is recommended for additional RF noise filtering, in particular if the application device integrates an internal antenna:

- Ferrite bead specifically designed for EMI suppression in GHz band (as Murata BLM18EG221SN1), placed as close as possible to the **VCC** pins of the module, implementing the circuit described in Figure 21, to filter out EMI in all the cellular bands

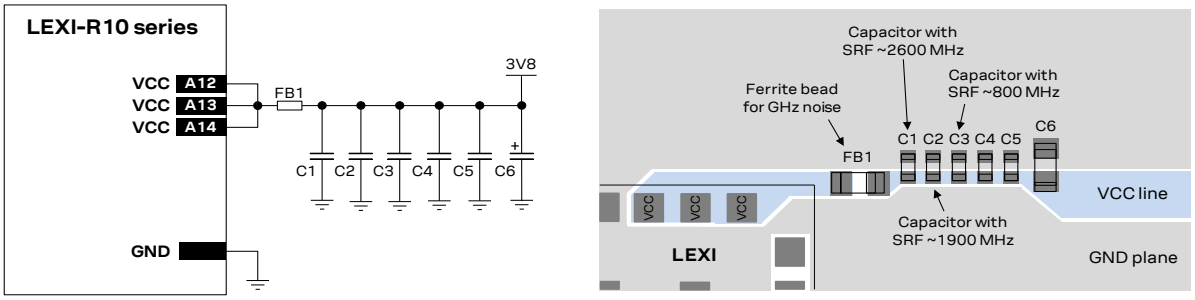

Figure 21: Suggested design to reduce ripple / noise on VCC, highly recommended when using an integrated antenna

Reference	Description	Part number - Manufacturer
C1	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
C2	15 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
C3	82 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 - Murata
C4	10 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C6	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
FB1	Chip ferrite bead EMI filter for GHz band noise 220 Ω at 100 MHz, 260 Ω at 1 GHz, 2000 mA	BLM18EG221SN1 - Murata

Table 18: Suggested components to reduce ripple / noise on VCC

☞ The necessity of each part depends on the specific design, but it is recommended to provide all the parts described in Figure 21 / Table 18 if the application device integrates an internal antenna.

☞ ESD sensitivity rating of the **VCC** supply pins is 1 kV (HBM). Higher protection level can be required if the line is externally accessible on the application board, e.g. if accessible battery connector is directly connected to the supply pins. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible point.

2.2.1.10 Guidelines for VCC supply layout design

Good connection of the module **VCC** pins with DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source.
- **VCC** connection must be as wide as possible and as short as possible.
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided.
- **VCC** connection must be routed through a PCB area separated from RF lines / parts, sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between the **VCC** track and other signal routing.
- **VCC** connection must be routed as far as possible from the antenna, in particular if embedded in the application device: see Figure 22.
- Coupling between **VCC** and digital lines, especially USB, must be avoided.
- The tank bypass capacitor with low ESR for current spikes smoothing described in section 2.2.1.9 should be placed close to the **VCC** pins; if the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize **VCC** track length, otherwise consider using separate capacitors for DC-DC converter and module tank capacitor.
- The bypass capacitors in the pF range described in Figure 21 and Table 18 should be placed as close as possible to the **VCC** pins, where the **VCC** line narrows close to the module input pins, improving the RF noise rejection in the band centered on the self-resonant frequency of the pF capacitors: this is highly recommended if the application device integrates an internal antenna.
- Since **VCC** input provide the supply to RF power amplifiers, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal; this is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the LEXI-R10 series modules in the worst case.
- Shielding of switching DC-DC converter circuit, or at least the use of shielded inductors for the switching DC-DC converter, may be considered since all switching power supplies may potentially generate interfering signals as a result of high-frequency high-power switching.
- If **VCC** is protected by transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the module, preferably closer to the DC source (otherwise protection function may be compromised).

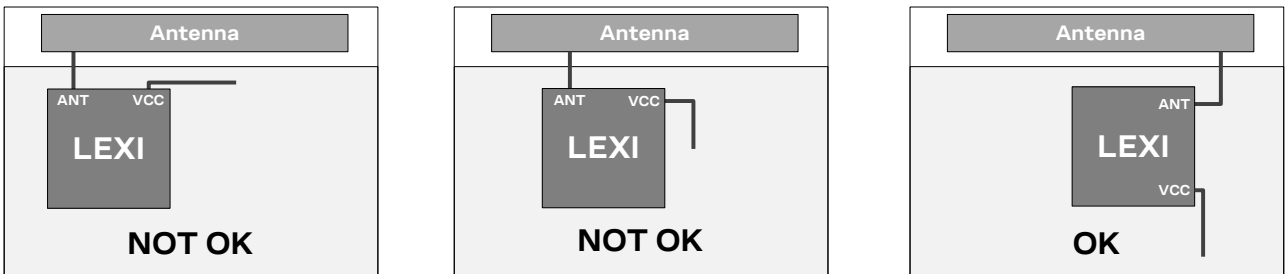

Figure 22: VCC line routing guideline for designs integrating an embedded antenna

2.2.1.11 Guidelines for grounding layout design

Good connection of the module **GND** pins with application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with application board solid GND layer; it is strongly recommended that each **GND** pad surrounding **VCC** pins have one or more dedicated via down to the application board solid ground layer.
- The **VCC** supply current flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source.
- It is recommended to implement one layer of the application board as ground plane as wide as possible.
- If the application board is a multilayer PCB, then all the board layers should be filled with GND plane as much as possible and each GND area should be connected together with complete via stack down to the main ground layer of the board; use as many vias as possible to connect the ground planes.
- Provide a dense line of vias at the edges of each ground area, in particular along RF and high speed lines.
- If the whole application device is composed by more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the different PCBs.
- Good grounding of **GND** pads also ensures thermal heat sink; this is critical during connection, when the real network commands the module to transmit at maximum power: correct grounding helps prevent module overheating.

2.2.2 Generic digital interfaces supply output (V_INT)

2.2.2.1 Guidelines for V_INT circuit design

LEXI-R10 series modules provide the **V_INT** generic digital interfaces 1.8 V supply output, which can be mainly used to:

- Indicate when the module is switched on and it is not in the ultra-low power deep-sleep mode (as described in sections 1.6.1, 1.6.2)
- Pull-up SIM detection signal (see section 2.5 for more details)
- Supply voltage translators to connect 1.8 V module generic digital interfaces to 3.0 V devices (e.g. see 2.6.1)
- Enable external voltage regulators providing supply for external devices

☞ Do not apply loads which might exceed the maximum available current from **V_INT** supply (see LEXI-R10 series data sheet [1]) as this can cause malfunctions in internal circuitry.

☞ **V_INT** can only be used as an output: do not connect any external supply source on **V_INT**.

☞ ESD sensitivity rating of the **V_INT** supply pin is 1 kV (HBM). Higher protection level could be required if the line is externally accessible, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG) close to accessible point.

☞ It is recommended to monitor the **V_INT** pin to sense the end of the internal switch-off sequence of LEXI-R10 series modules: **VCC** supply can be removed only after **V_INT** goes low.

☞ It is highly recommended to provide direct access to the **V_INT** pin on the application board by an accessible test point directly connected to the **V_INT** pin, for firmware upgrade and/or for diagnostic purposes.

2.3 System functions interfaces

2.3.1 Module PWR_ON input

2.3.1.1 Guidelines for PWR_ON circuit design

LEXI-R10 series **PWR_ON** input is equipped with an internal active pull-up resistor; an external pull-up resistor is not required and should not be provided.

If connecting the **PWR_ON** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection should be provided close to the accessible point, as described in Figure 23 and Table 19.

☞ ESD sensitivity rating of the **PWR_ON** pin is 1 kV (HBM). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to the pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to the accessible point.

An open drain or open collector output is suitable to drive the **PWR_ON** input from an application processor, as described in Figure 23.

☞ **PWR_ON** input line should not be driven high, as it may cause start up issues.

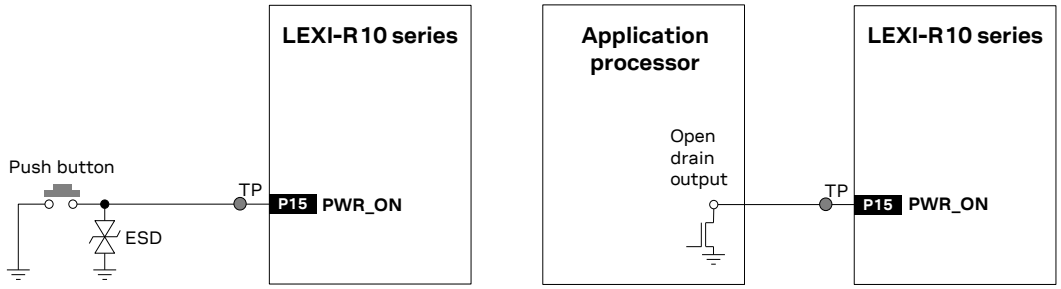

Figure 23: PWR_ON application circuits using a push button and an open drain output of an external processor

Reference	Description	Remarks
ESD	CT0402S14AHSG - EPCOS	Varistor array for ESD protection

Table 19: Example ESD protection component for the PWR_ON application circuit

☞ It is highly recommended to provide direct access to the **PWR_ON** pin on the application board by an accessible test point directly connected to the **PWR_ON** pin, for firmware upgrade and/or for diagnostic purposes.

2.3.1.2 Guidelines for PWR_ON layout design

The **PWR_ON** circuit requires careful layout since it is the sensitive input available to switch on and switch off the LEXI-R10 series modules. It is required to ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request.

2.3.2 Module RESET_N input

2.3.2.1 Guidelines for RESET_N circuit design

LEXI-R10 series **RESET_N** input is equipped with an internal active pull-up resistor; an external pull-up resistor is not required and should not be provided.

If connecting the **RESET_N** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection should be provided close to the accessible point, as described in Figure 24 and Table 20.

ESD sensitivity rating of the **RESET_N** pin is 1 kV (HBM). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to the pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to the accessible point.

An open drain or open collector output is suitable to drive the **RESET_N** input from an application processor, as described in Figure 24.

RESET_N input line should not be driven high, as it may cause start up issues.

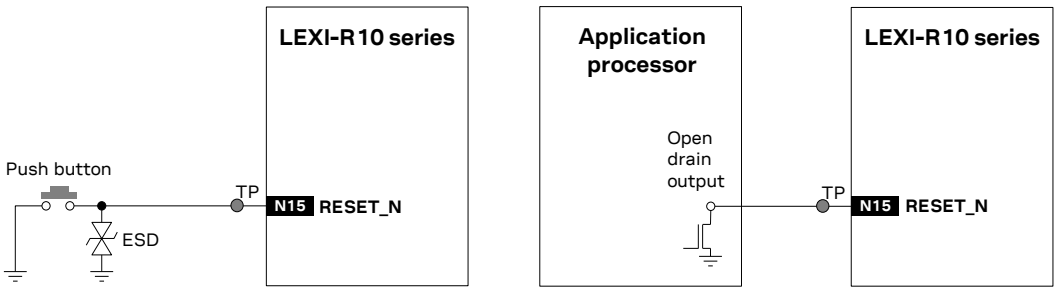

Figure 24: RESET_N application circuits using a push button and an open drain output of an external processor

Reference	Description	Remarks
ESD	CT0402S14AHSG - EPCOS	Varistor array for ESD protection

Table 20: Example ESD protection component for the RESET_N application circuit

It is highly recommended to provide direct access to the **RESET_N** pin on the application board by an accessible test point directly connected to the **RESET_N** pin, for firmware upgrade and/or for diagnostic purposes.

2.3.2.2 Guidelines for RESET_N layout design

The **RESET_N** circuit requires careful layout since it is the sensitive input available to reset / reboot the LEXI-R10 series modules. It is required to ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request.

2.4 Antenna interface

LEXI-R10 series modules provide an RF interface for connecting the external antenna: the **ANT** pin represents the RF input/output for the transmission and the reception of LTE RF signals, and for the reception of Wi-Fi RF signals.

The **ANT** pin has 50 Ω nominal characteristic impedance and must be connected to the external antenna system through 50 Ω transmission line to allow clean transmission / reception of RF signals.

2.4.1 Antenna RF interface (ANT)

2.4.1.1 Guidelines for ANT pin RF connection design

A clean transition between the **ANT** pad and the application PCB must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the **ANT** pad:

- On a multilayer PCB, the whole layer stack below the RF connections should be free of digital lines.
- Increase GND keep-out (i.e. clearance, a void area) at least up to 500 µm around the **ANT** pad on the top layer of the application PCB, to reduce parasitic capacitance to ground, as described in the left picture in Figure 25.
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT** pad if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as described in the right picture in Figure 25.

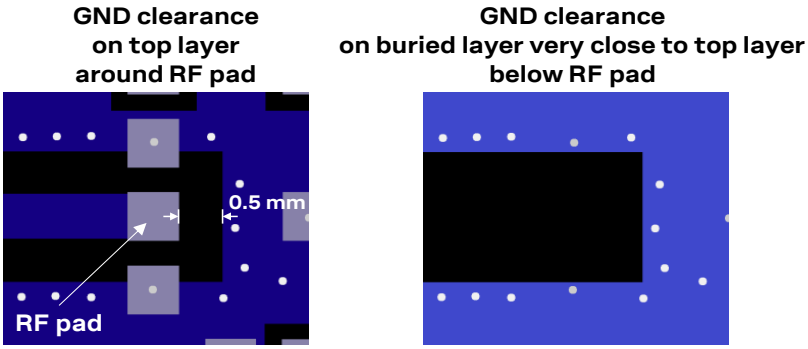

Figure 25: GND keep-out area on top layer around RF pad and on very close buried layer below RF pad (ANT)

☞ See section 2.4.1.5 for the description of the antenna trace design implemented on the u-blox host printed circuit board used for conformity assessment of LEXI-R10 series surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc.

2.4.1.2 Guidelines for RF transmission lines design

Any RF transmission line, such as the ones from the **ANT** pad up to the related antenna connector or up to the related internal antenna pad, must be designed so that the characteristic impedance is as close as possible to 50 Ω.

RF transmission lines can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit board.

Figure 26 and Figure 27 provide two examples of suitable 50 Ω coplanar waveguide designs. The first example of RF transmission line can be implemented in case of 4-layer PCB stack-up herein described, and the second example of RF transmission line can be implemented in case of 2-layer PCB stack-up herein described.

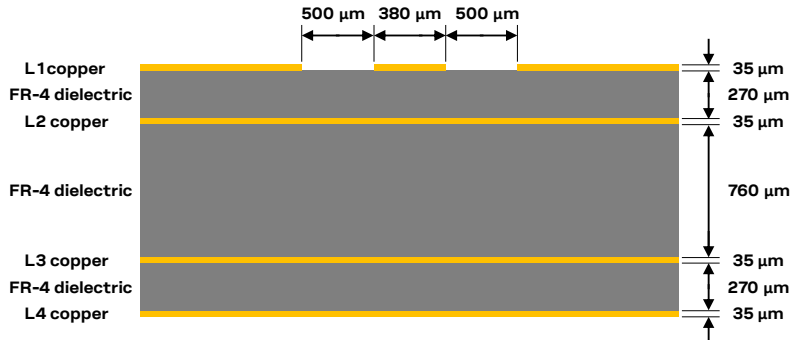

Figure 26: Example of 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

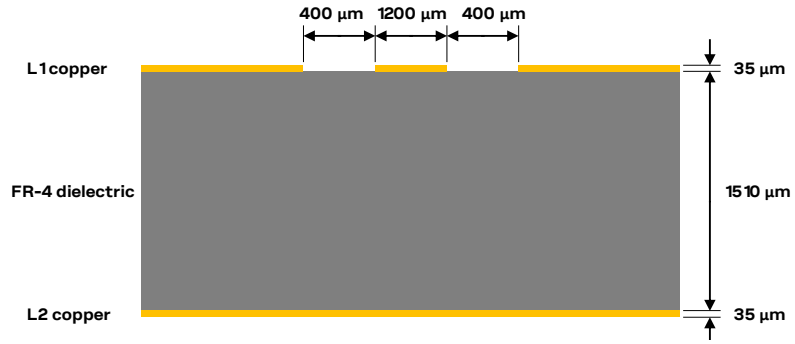

Figure 27: Example of 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB stack-up, then the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like Avago / Broadcom AppCAD (https://www.broadcom.com/appcad) taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the transmission line width must be chosen due to:

- The thickness of the transmission line itself (e.g. 35 µm in the example of Figure 26 / Figure 27).
- The thickness of the dielectric material between the top layer (where the line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 26).
- The dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 26 and Figure 27).
- The gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 26 and 400 µm in Figure 27).

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the width of the line, use the “Coplanar Waveguide” model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for transmission lines:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB.
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of component present on the RF transmission lines, if top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground.
- The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND.
- Add GND stitching vias around transmission lines, as described in Figure 28.
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough vias on the adjacent metal layer, as described in Figure 28.

- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as USB).
- Avoid stubs on the transmission lines.
- Avoid signal routing in parallel to transmission lines or crossing the transmission lines on buried metal layer.
- Do not route microstrip lines below discrete component or other mechanics placed on top layer.

Two examples of a suitable RF circuit design for the **ANT** pin are illustrated in Figure 28, where the antenna detection circuit is not implemented (if the antenna detection function is required by the application, follow the guidelines for circuit and layout implementation detailed in section 2.4.3):

- In the first example shown on the left, the **ANT** pin is directly connected to an SMA connector by a suitable 50 Ω transmission line, designed with the appropriate layout.
- In the second example shown on the right, the **ANT** pin is connected to an SMA connector by means of a suitable 50 Ω transmission line, designed with the appropriate layout, with an additional low pass filter to attenuate the radiated spurious emissions in the range of frequency higher than the operating frequency range of the LEXI-R10 series modules.

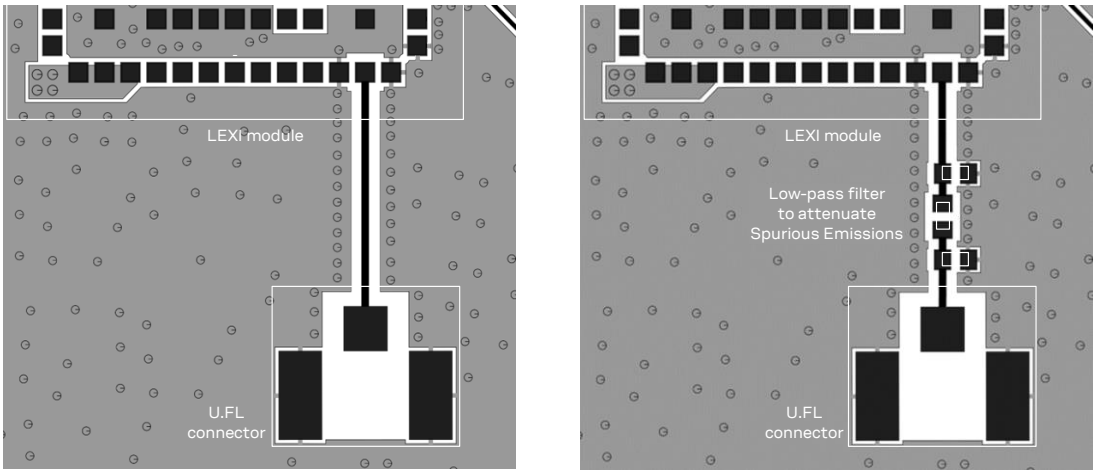

Figure 28: Example of circuit and layout for ANT RF circuits on the application board

See section 2.4.1.5 for the description of the antenna trace design implemented on the u-blox host printed circuit board used for conformity assessment of LEXI-R10 series surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc.

2.4.1.3 Guidelines for RF termination design

The RF termination must provide a characteristic impedance of 50 Ω as well as the RF transmission line up to the RF termination, to match the characteristic impedance of **ANT** port.

However, real antennas do not have a perfect 50 Ω load on all the supported frequency bands. So to reduce as much as possible any performance degradation due to antenna mismatching, the RF termination must provide optimal return loss (or VSWR) figures over all the operating frequencies, as summarized in Table 8.

If an external antenna is used, the antenna connector represents the RF termination on the PCB:

- Use a suitable 50 Ω connector providing a clean PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer's recommended layout, for example:
  - SMA Pin-Through-Hole connectors require a GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to the annular pads of the four GND posts.
  - U.FL surface mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads, as shown in Figure 28 / Figure 29.

- Cut out the GND layer under the RF connector and close to any buried vias, to remove stray capacitance and thus keep the RF line at 50 Ω, e.g. the active pad of U.FL connector needs to have a GND keep-out (i.e. clearance, a void area) at least on the first inner layer to reduce parasitic capacitance to ground.

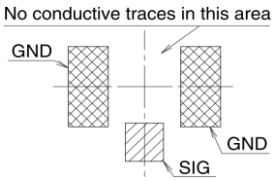

Figure 29: U.FL surface mounted connector mounting pattern layout

If an integrated antenna is used, the integrated antenna represents the RF termination. The following guidelines should be followed:

- Use an antenna designed by an antenna manufacturer providing the best possible return loss.
- Provide a ground plane large enough according to the relative integrated antenna requirements: the ground plane of the application PCB can be reduced down to a minimum size that must be similar to one quarter of wavelength of the minimum radiated frequency, as numerical example:
  Frequency = 617 MHz → Wavelength ≅ 48 cm → Minimum GND plane size ≅ 12 cm
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including the PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, the antenna may require a tuning to comply with all the applicable required certification schemes; it is recommended to consult the antenna manufacturer for antenna matching design-in guidelines relative to the custom application.

Additionally, these recommendations regarding the antenna system placement must be followed:

- Do not place the antennas within a closed metal case.
- Do not place the cellular antenna in close vicinity to the end user since the emitted radiation in human tissue is restricted by regulatory requirements.
- Place the antennas as far as possible from VCC supply line and related parts (see also Figure 22), from high-speed digital lines (as USB) and from any possible noise source.
- Place the antenna far from sensitive analog systems or employ countermeasures to reduce EMC or EMI issues.
- Be aware of interaction between co-located RF systems since the LTE transmitted power may interact or affect the performance of companion systems as a GNSS receiver (see section 2.4.2 for further details and design-in guidelines regarding cellular / GNSS RF coexistence).

☞ See section 2.4.1.5 for the description of the antenna trace design implemented on the u-blox host printed circuit board used for conformity assessment of LEXI-R10 series surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc.

2.4.1.4 General guidelines for antenna selection and design

The antenna is the most critical component to be evaluated. Designers must take care of the antenna from all perspective at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating the modules with all the applicable requirements depends on antenna radiating performance.

Cellular antennas are typically available as:

- External antennas (e.g. linear monopole):
  - External antennas basically do not imply physical restriction to the design of the PCB where the LEXI-R10 series module is mounted.
  - The radiation performance mainly depends on the antennas: it is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected to have minimum insertion losses: additional insertion loss will be introduced by low quality or long cable; large insertion loss reduces both transmit and receive radiation performance.
  - A high quality 50 Ω RF connector provides clean PCB-to-RF-cable transition: we recommend to strictly follow layout and cable termination guidelines gave by the connector manufacturer.
- Integrated antennas (e.g. PCB antennas such as patches or ceramic SMT elements):
  - Internal integrated antennas imply physical restriction to the design of the PCB: integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna; its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that needs to be radiated, given that the orientation of the ground plane relative to the antenna element must be considered. As numerical example, the PCB physical restriction can be considered as following:

    Frequency = 617 MHz → Wavelength ~48 cm → Minimum GND plane size ~12 cm
  - Radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage: antennas should be selected with optimal radiating performance according to the mechanical specifications of the PCB and the whole product.
  - It is recommended to select a custom antenna designed by an antennas manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide); the antenna design process should begin at the start of the whole product design process.
  - It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
  - Further to the custom PCB and product restrictions, antennas may require tuning to obtain the required performance for compliance with all the applicable required certification schemes: it is recommended to consult the antenna manufacturer for the design-in guidelines for antenna matching relative to the custom application.

In both cases, selecting external or internal antennas, these recommendations should be observed:

- Select an antenna providing optimal return loss / VSWR / efficiency figure over all the operating cellular frequencies.
- Select an antenna providing the worst possible return loss / VSWR / efficiency figure in the GNSS frequency band, to optimize the RF coexistence between the cellular and the GNSS systems (see section 2.4.2 for further details and guidelines regarding cellular / GNSS RF coexistence).
- Select an antenna providing appropriate gain figure (i.e. combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity do not exceed the regulatory limits, such as FCC United States (see 4.2), ISED Canada (see 4.3), CE Europe (see 4.4), etc.

☞ For examples of antennas intended to be surface-mounted on the device integrating the module, examples of antennas with cable and connector intended to be placed off-board inside the device integrating the module, and examples of antennas intended to be mounted outside the device integrating the module, please contact the u-blox office or sales representative nearest you.

2.4.1.5 Antenna trace design used for LEXI-R10 series modules' type approvals

Overview

The conformity assessment of u-blox LEXI-R10 series LGA surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc. has been carried out with the modules mounted on a u-blox host printed circuit board with a 50 Ω grounded coplanar waveguide designed on it, herein referenced as "antenna trace design", implementing the connection from the **ANT** pad of the module up to a 50 Ω SMA connector for external antenna and/or RF cable access.

☞ Manufacturers of mobile or fixed devices incorporating LEXI-R10 series modules are authorized to use the FCC United States Grants and ISED Canada Certificates of the modules for their own final host products if, as per FCC KDB 996369, the antenna trace design implemented on the host PCB is electrically equivalent to the antenna trace design implemented on the u-blox host PCB used for regulatory type approvals of the modules, described in this section.

☞ In case of antenna trace design change, an FCC Class II Permissive Change and/or ISED Class IV Permissive Change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID and/or the ISED Multiple Listing (new application) procedure followed by an FCC C2PC and/or ISED C4PC application.

Antenna trace design used for LEXI-R10401D and LEXI-R10801D modules' type approvals

The antenna trace design is implemented as illustrated in Figure 30 on the u-blox host PCB used for the LEXI-R10401D and LEXI-R10801D modules, using the parts listed in Table 21, with the support of the additional optional antenna detection capability.

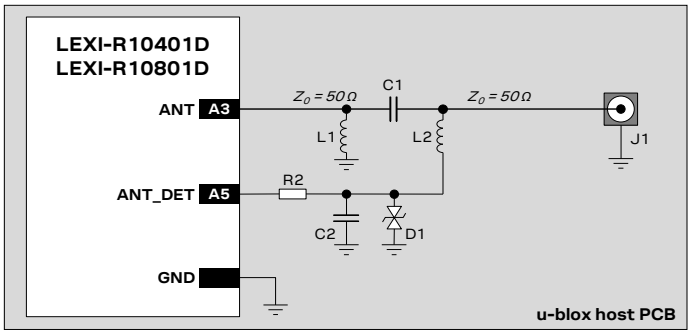

Figure 30: Antenna trace design implemented on the u-blox host PCB used for LEXI-R10401D and LEXI-R10801D modules

Reference	Description	Part number – Manufacturer
C1	47 pF capacitor ceramic C0G 0201 2% 50 V	GRM0335C1H470GA01 – Murata
C2	39 pF capacitor ceramic C0G 0201 5% 50 V	GRM0332C1H390JA01 – Murata
D1	Low capacitance ESD protection	CG0402MLE-18G – Bourns
L1	39 nH multilayer inductor 0402 (SRF ~1 GHz)	Not Installed
L2	82 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS82NJ02B – Murata
R2	10 kΩ resistor 0402 1% 0.063 W	Generic manufacturer
J1	SMA connector 50 Ω through hole jack	SMA6251A1-3GT50G-50 – Amphenol

Table 21: Parts in use on the u-blox host PCB for the antenna trace design used for LEXI-R10401D / LEXI-R10801D modules

The u-blox host printed circuit board used for the LEXI-R10401D and LEXI-R10801D modules has a structure of 6 copper layers with 35 µm thickness (1 oz/ft^2) for all the layers except for the two inner buried layers, having 18 µm thickness (1/2 oz/ft^2), using FR4 dielectric substrate material with 4.3 typical permittivity and 0.013 typical loss tangent at 1 GHz.

The top layer layout of the u-blox host PCB used for the LEXI-R10401D and LEXI-R10801D modules is described in Figure 31, implementing the RF antenna trace designed as a 50 Ω grounded coplanar

waveguide, with ~24 mm length from the pad designed to accommodate the **ANT** pad of the module up to the pad designed to accommodate the SMA RF connector for an external cellular antenna and/or RF coaxial cable.

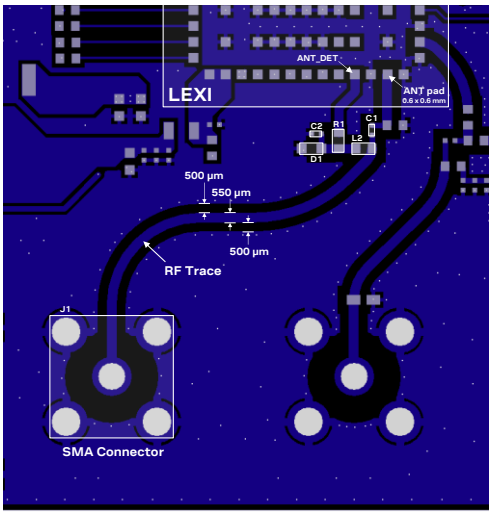

Figure 31: Top layer (L1) layout of the u-blox host PCB with the antenna RF trace design for LEXI-R10401D / LEXI-R10801D

The PCB stack-up structure of the 6-layer u-blox host printed circuit board used for the LEXI-R10401D and LEXI-R10801D modules is illustrated in Figure 32.

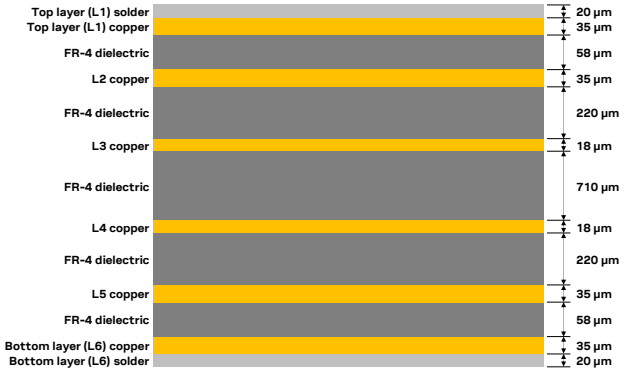

Figure 32: Stack-up structure of the u-blox host PCB for LEXI-R10401D / LEXI-R10801D modules

Considering that the thickness of the dielectric material from the top layer to the buried layer is less than 200 µm, GND keep-out is implemented on the buried metal layer area below the **ANT** pad and the antenna RF trace as illustrated in Figure 33 in the host printed circuit board used for LEXI-R10401D and LEXI-R10801D modules.

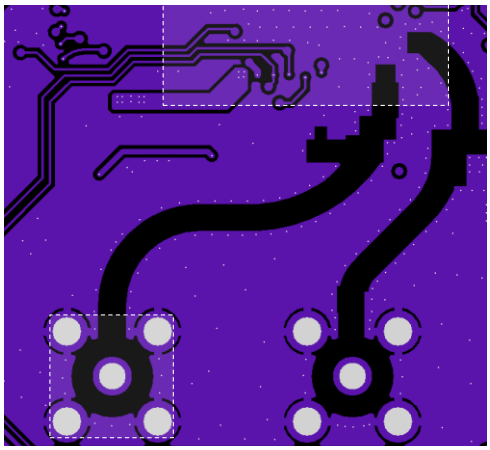

Figure 33: Buried layer (L2) of the u-blox host PCB for LEXI-R10401D / LEXI-R10801D, below the antenna RF trace design

Antenna trace design used for LEXI-R10001D and LEXI-R10011D modules' type approvals

The antenna trace design is implemented as illustrated in Figure 34 on the u-blox host PCB used for the LEXI-R10001D and LEXI-R10011D modules, using the parts listed in Table 22.

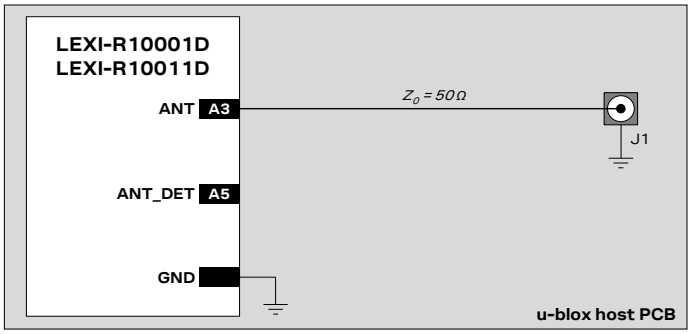

Figure 34: Antenna trace design implemented on the u-blox host PCB used for LEXI-R10001D / LEXI-R10011D modules

Reference	Description	Part number – Manufacturer
J1	SMA connector 50 Ω through hole jack	SMA6251A1-3GT50G-50 – Amphenol

Table 22: Parts in use on the u-blox host PCB for the antenna trace design used for LEXI-R10001D / LEXI-R10011D modules

The u-blox host printed circuit board used for the LEXI-R10001D and LEXI-R10011D modules has a structure of 4 copper layers with 35 µm thickness (1 oz/ft^2) for all the layers, using FR4 dielectric substrate material with 4.3 typical permittivity and 0.013 typical loss tangent at 1 GHz.

The top layer layout of the u-blox host PCB used for the LEXI-R10001D and LEXI-R10011D modules is described in Figure 35, implementing the RF antenna trace designed as a 50 Ω grounded coplanar waveguide, with ~18 mm length from the pad designed to accommodate the **ANT** pad of the module up to the pad designed to accommodate the SMA RF connector for an external cellular antenna and/or RF coaxial cable.

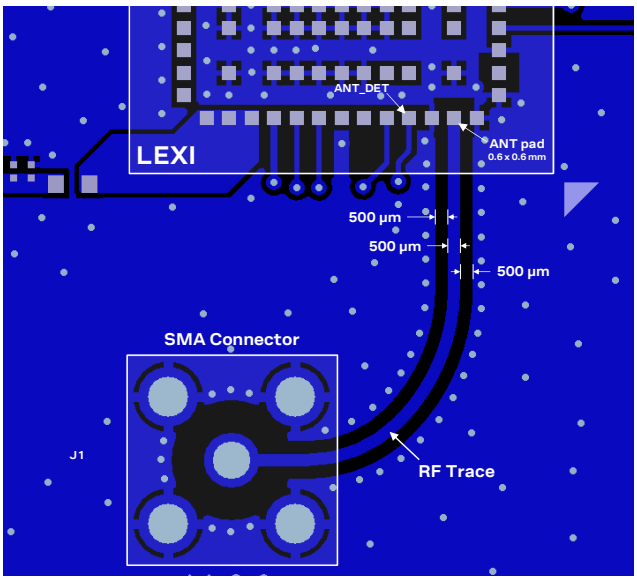

Figure 35: Top layer (L1) layout of the u-blox host PCB with the antenna RF trace design for LEXI-R10001D / LEXI-R10011D

The PCB stack-up structure of the 4-layer u-blox host printed circuit board used for the LEXI-R10001D and LEXI-R10011D modules is illustrated in Figure 36.

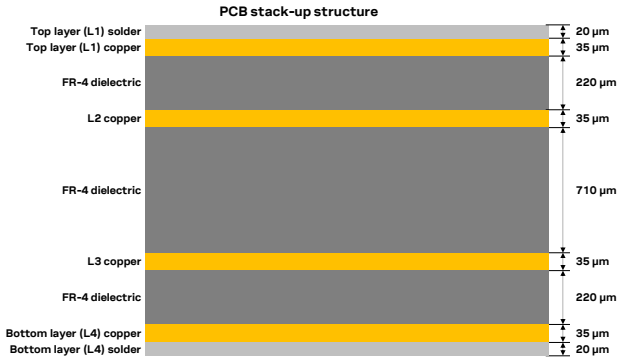

Figure 36: Stack-up structure of the u-blox host PCB for LEXI-R10001D / LEXI-R10011D modules

Considering that the thickness of the dielectric material from the top layer to the buried layer is more than 200 µm, GND keep-out is not implemented on the buried metal layer area below the **ANT** pad and the antenna RF trace as shown in Figure 37 in the host printed circuit board used for LEXI-R10001D and LEXI-R10011D modules.

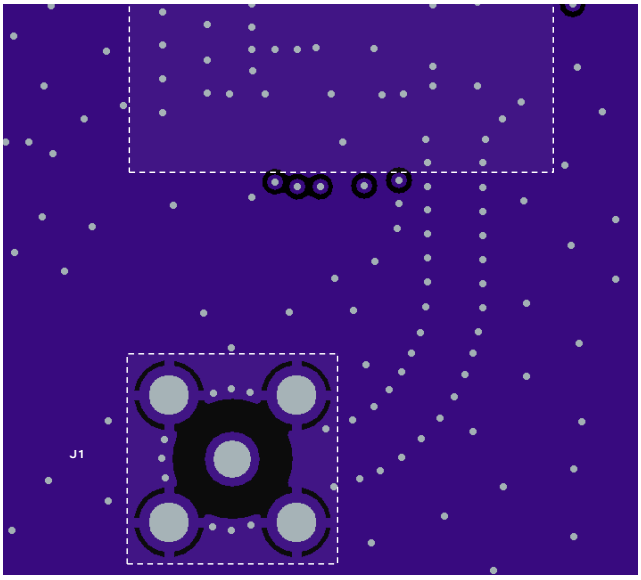

Figure 37: Buried layer (L2) of the u-blox host PCB for LEXI-R10001D / LEXI-R10011D, below the antenna RF trace design

Additional considerations

Guidelines to design an equivalent proper connection for the **ANT** pad are available in section 2.4.1.1. Guidelines to design an equivalent proper 50 Ω transmission line are available in section 2.4.1.2. Guidelines to design a proper equivalent 50 Ω termination are available in section 2.4.1.3, with further guidelines for cellular antenna selection and design available in section 2.4.1.4. Guidelines to design a proper equivalent (optional) antenna detection circuit are available in section 2.4.3.

The 50 Ω characteristic impedance of the antenna trace design on a host printed circuit board can be verified using a Vector Network Analyzer, as done on the u-blox host PCB, with calibrated RF coaxial cable soldered at the pad corresponding to RF input/output of the module and with the transmission line terminated to a 50 Ω load at the 50 Ω SMA connector.

Compliance of the design with regulatory rules and specifications defined by the FCC, ISED, RED, etc. can be verified using a radio communication tester (callbox) as the Rohde & Schwarz CMW500, or any equivalent equipment for multi-technology signaling conformance tests.

2.4.2 Cellular and GNSS RF coexistence

Overview

Desensitization or receiver blocking is a form of electromagnetic interference where a radio receiver is unable to detect a weak signal that it may otherwise be able to receive when there is no interference.

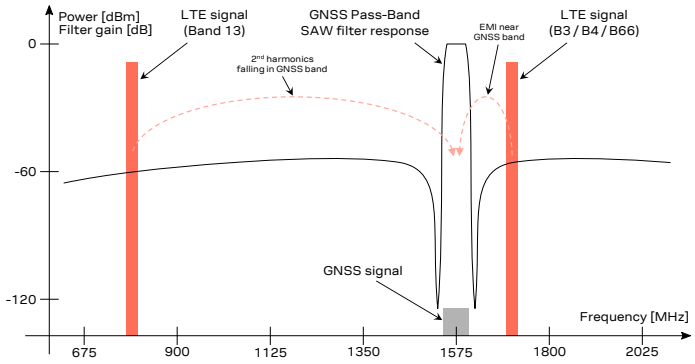

Figure 38: EMI due to Tx in LTE B3, B4, B66 low channels (1710 MHz) adjacent to GNSS frequency range (1561 to 1610 MHz), or due to Tx in LTE B13 high channels (787 MHz) with harmonics falling into the GNSS frequency range

Jamming signals may come from in-band and out-of-band frequency sources. In-band jamming is caused by signals with frequencies falling within the GNSS frequency range, while the out-of-band jamming is caused by very strong signals adjacent to the GNSS frequency range so that part of the strong signal power may leak at the input of the GNSS receiver and/or block GNSS reception.

If not properly taken into consideration, in-band and out-band jamming signals may cause a reduction in the carrier-to-noise power density ratio (C/No) of the GNSS satellites.

In-band interference

In-band interference signals are typically caused by harmonics from displays, switching converters, micro-controllers and bus systems. Moreover, considering for example the second harmonic of the LTE band 13 high channel transmission frequency (787 MHz) is exactly within the GPS operating band (1575.42 MHz ± 1.023 MHz). Therefore, depending on the board layout and the transmit power, the highest channel of LTE band 13 is the channel that has the greatest impact on the C/No reduction.

Countermeasures against in-band interference include:

- Maintaining a good grounding concept in the design
- Ensuring proper shielding of the different RF paths
- Ensuring proper impedance matching of RF traces
- Placing the GNSS antenna away from noise sources
- Add a notch filter along the GNSS RF path, just after the antenna, at the frequency of the jammer

Out-of-band interference

Out-of-band interference is caused by signal frequencies that are different from the GNSS, the main sources being cellular or other transmitters. For example, the lowest channels in LTE band 3, 4 or 66 at 1710 MHz might affect the reception of GLONASS satellites at 1602 MHz ± 8 MHz. The LTE signal is outside the GNSS band, but provided that the power received by the GNSS subsystem at 1710 MHz is high enough, blocking and leakage effects may appear reducing once again the C/No.

Countermeasures against out-of-band interference include:

- Maintaining a good grounding concept in the design.
- Keeping the GNSS and cellular antennas more than the quarter-wavelength (of the minimum Tx frequency) away from each other. If for layout or size reasons this requirement cannot be met, then the antennas should be placed orthogonally to each other and/or on different side of the PCB.

- Selecting a cellular antenna providing the worst possible return loss / VSWR / efficiency figure in the GNSS frequency band: the lower is the cellular antenna efficiency between 1561 MHz and 1610 MHz, the higher is the isolation between the cellular and the GNSS systems.
- Ensuring at least 15 – 20 dB isolation between antennas in the GNSS band by implementing the most suitable placement for the antennas, considering in particular the related radiation diagrams of the antennas: better isolation results from antenna patterns with radiation lobes in different directions considering the GNSS frequency band.
- Adding a GNSS pass-band SAW filter along the GNSS RF line, providing very large attenuation in the cellular frequency bands.

Countermeasures for small devices

Further countermeasures are generally not required using LEXI-R10 series modules, which integrate a band-pass SAW filter along each LTE FDD RF path, improving the isolation with GNSS by design.

The actual isolation may be limited due to small device dimensions, so that adding an external GNSS stop-band SAW filter along the cellular RF line may be considered. The filter shall provide very low attenuation in the cellular frequency bands (see examples in Table 23), but note that adding such external SAW filter along the cellular RF line must be carefully evaluated, because the additional insertion loss of such filter may affect the cellular TRP and/or TIS RF figures.

Manufacturer	Part number	Description
Qualcomm RF360	B8666	GNSS (L1) SAW extractor filter, 1.7 x 1.3 mm
Qualcomm RF360	B8939	GNSS (L1) SAW extractor filter, 1.5 x 1.1 mm
Murata	SADAC1G56AB0E0A	GNSS (L1) SAW extractor filter, 1.5 x 1.1 mm
TST	TE0123A	GPS (1575.42MHz) SAW band-stop filter, 3.0 x 3.0 mm

Table 23: Examples of GNSS band-stop SAW filters

Additional considerations

Note that high-power transmission occurs very infrequently according to the Tx power distribution shown in the GSMA official document TS.09 [11]. Therefore, careful PCB layout, antenna selection and placement should be sufficient to ensure accurate GNSS reception.

For an example of successful RF coexistence between u-blox cellular, GNSS and short-range products in a small form factor, refer to the u-blox B36 blueprint [18] illustrated in Figure 39.

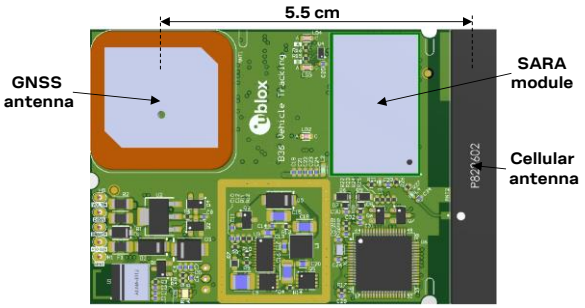

Figure 39: PCB top rendering for the u-blox B36 blueprint with annotated distance between cellular and GNSS antennas

2.4.3 Antenna detection interface (ANT_DET)

2.4.3.1 Guidelines for ANT_DET circuit design

Figure 40 and Table 24 describe the recommended schematic / components for the optional antenna detection circuit that must be provided on the application board and for the diagnostic circuit that must be provided on the antenna's assembly to achieve antenna detection functionality.

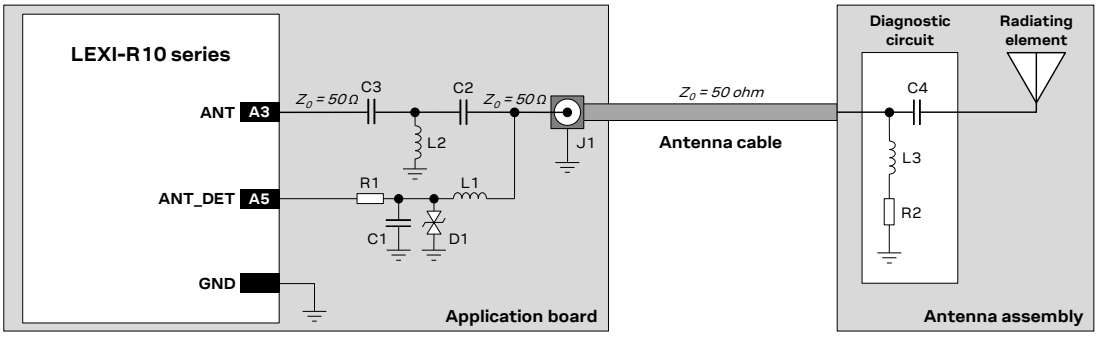

Figure 40: Suggested schematic for antenna detection circuit on application PCB and diagnostic circuit on antenna assembly

Reference	Description	Part number - Manufacturer
C1	27 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H270J - Murata
C2	33 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H330J - Murata
D1	Very low capacitance ESD protection	PESD0402-140 - Littelfuse
L1	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ resistor 0402 1% 0.063 W	RK73H1ETTP1002F - KOA Speer
J1	SMA connector 50 Ω through hole jack	SMA6251A1-3GT50G-50 - Amphenol
C3	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150J - Murata
L2	39 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HN39NJ02 - Murata
C4	22 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1H220J - Murata
L3	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R2	15 kΩ resistor for diagnostics	Generic manufacturer

Table 24: Suggested parts for antenna detection circuit on application PCB and diagnostic circuit on antennas assembly

The antenna detection circuit and diagnostic circuit shown in Figure 40 / Table 24 are here explained:

- When detection is forced by the +UANTR AT command, the **ANT_DET** pin generates a DC current measuring the resistance (R2) from the antenna connector (J1) on the application PCB to GND.
- DC blocking capacitors are needed at the **ANT** pin (C2) and at the antenna radiating element (C4) to decouple the DC current generated by the **ANT_DET** pin.
- Choke inductors with a Self-Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT_DET** pin (L1) and in series at the diagnostic resistor (L3), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Resistor on the **ANT_DET** path (R1) is needed for the measurements by +UANTR AT command.
- Additional components (C1 and D1 in Figure 40) are provided as **ANT_DET** pin as ESD protection.
- Additional high pass filter (C3 and L2 in Figure 40) is provided as ESD immunity improvement.
- The **ANT** pin must be connected to the antenna connector by means of a transmission line with nominal characteristics impedance as close as possible to 50 Ω.

The DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 40, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no mean to distinguish between a defect on antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self-Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example, considering an antenna with 15 kΩ built-in resistor, the resistance value evaluated from the antenna connector on the application PCB to GND is reported by the AT+UANTR command, and:

- Reported values close to the used diagnostic resistor nominal value (for example from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is correctly connected.
- Values close to the measurement range maximum limit (approximately 50 kΩ) or an open-circuit "over range" report (see the AT commands manual [2]) means that that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit (1 kΩ) highlights a short to GND at antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an unclean connection, a damaged antenna or incorrect value of the antenna diagnostics resistor.
- Reported value could differ from the real resistance value of the resistor mounted inside the antenna assembly due to cable length / capacitance and the used measurement method.

☞ If the antenna detection function is not required by the customer application, the **ANT_DET** pin can be left not connected and the **ANT** pin can be directly connected to the antenna connector by means of a 50 Ω transmission line as described in Figure 28.

2.4.3.2 Guidelines for ANT_DET layout design

Figure 41 describes the recommended layout for the antenna detection circuit to be provided on the application board to achieve antenna detection functionality, implementing the recommended schematic described in the previous Figure 40 and Table 24:

- The **ANT** pin must be connected to the antenna connector by means of a 50 Ω transmission line, implementing the design guidelines described in section 2.4.1 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at **ANT** pin (C2) must be placed in series to the 50 Ω RF line.
- The **ANT_DET** pin must be connected to the 50 Ω transmission line by means of a sense line.
- Choke inductor in series at the **ANT_DET** pin (L1) must be placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to the **ANT_DET** pin.
- The additional components (R1, C1 and D1) are provided as **ANT_DET** ESD protection.
- The additional high pass filter (C3 and L2) is provided as ESD immunity improvement.

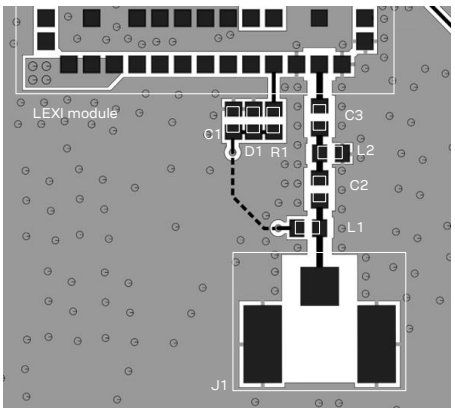

Figure 41: Suggested layout for antenna detection circuit on application board

2.4.4 Antenna dynamic tuner interface

LEXI-R10 series modules include two output pins (**RFCTRL1** and **RFCTRL2**) that can be configured, as optional feature, to change their output value dynamically according to the actual RF band in use by the module. These pins, paired with an external antenna tuner IC or RF switch, can be used to:

- Tune antenna impedance to reduce power losses due to mismatch
- Tune antenna aperture to improve total antenna efficiency
- Select the optimal antenna for each operating band

Figure 42 shows application circuits examples implementing impedance tuning and aperture tuning. The module controls an RF switch that is responsible for selecting the appropriate matching element for the operating band. Table 25 reports suggested parts for the SP4T RF switch.

In Figure 42(a), tuning the antenna impedance optimizes the power delivered into the antenna by dynamically adjusting the RF impedance seen by **ANT** pin of LEXI-R10 series module. By creating a tuned matching network for each operating band, the total radiated power (TRP) and the total isotropic sensitivity (TIS) metrics are improved.

In Figure 42(b), antenna aperture tuning enables higher antenna efficiency over a wide frequency range. The dynamically tunable components are added to the antenna structure itself, thereby modifying the effective electrical length of the radiating element. Thus, the resonant frequency of the antenna is shifted into the module's operating frequency band. Aperture tuning optimizes radiation efficiency, insertion loss, isolation, and rejection levels of the antenna.

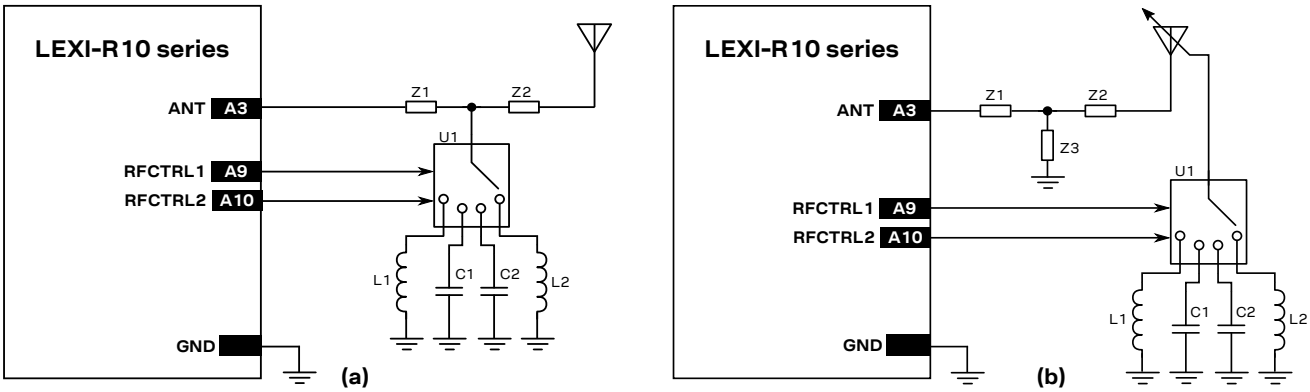

Figure 42: Examples of schematics for antenna dynamic impedance tuning (a) and aperture tuning (b).

Refer to the antenna datasheet and/or manufacturer for proper values of matching components Z1, Z2, Z3, L1, L2, C1, C2. These components should have low losses to avoid degrading the radiating efficiency of the antenna, thereby hindering the positive effects of dynamic tuning.

Manufacturer	Part number	Description
Peregrine Semiconductor	PE42442	30..6000 MHz UltraCMOS SP4T RF switch
Peregrine Semiconductor	PE613050	5..3000 MHz UltraCMOS SP4T RF switch
Peregrine Semiconductor	PE42440	50..3000 MHz UltraCMOS SP4T RF switch
Skyworks Solutions	SKY13626-685LF	400..3800 MHz SP4T high-power RF switch
Skyworks Solutions	SKY13380-350LF	20..3000 MHz SP4T high-power RF switch
KYOCERA AVX	EC646	100..3000 MHz ultra-small SP4T RF switch
KYOCERA AVX	EC686-3	100..3000 MHz ultra-low R_{ON} SP4T RF switch
Qorvo	RF1654A	100..2700 MHz SP4T RF switch
Infineon	BGSA14GN10	100..6000 MHz SP4T RF switch for antenna tuning applications

Table 25: Examples of RF switches for antenna dynamic tuning

2.5 SIM interface

2.5.1 Guidelines for SIM circuit design

2.5.1.1 Guidelines for SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC), which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the LTE network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221 as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP/SWP (Other function) → It can be left not connected
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1, C2, C3, C5, C6, C7) or 8 contacts, also including the auxiliary contacts C4 and C8. Only 6 contacts are required and must be connected to the module SIM interface.

Removable SIM cards are suitable for applications requiring a change of SIM card during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins relative to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided. Select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature is required by the custom application, otherwise a connector without integrated mechanical presence switch can be selected.

Surface-Mounted UICC / SIM chip contact mapping (M2M UICC Form Factor) is defined by the ETSI TS 102 671 as:

- Case pin 8 = UICC contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Case pin 7 = UICC contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Case pin 6 = UICC contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Case pin 5 = UICC contact C4 = AUX1 (Aux. contact) → It must be left not connected
- Case pin 1 = UICC contact C5 = GND (Ground) → It must be connected to **GND**
- Case pin 2 = UICC contact C6 = VPP/SWP (Other) → It can be left not connected
- Case pin 3 = UICC contact C7 = I/O (Data I/O) → It must be connected to **SIM_IO**
- Case pin 4 = UICC contact C8 = AUX2 (Aux. contact) → It must be left not connected

A Surface-Mounted SIM chip has 8 contacts and can also include the auxiliary contacts C4 and C8 for other uses, but only 6 contacts are required and must be connected to the module SIM card interface as described above.

Surface-Mounted SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

2.5.1.2 Guidelines for single SIM card connection without detection

A removable SIM card placed in a SIM card holder must be connected to the SIM card interface of LEXI-R10 series modules as described in Figure 43, where the optional SIM detection feature is not implemented.

Follow these guidelines to connect the module to a SIM connector without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) on SIM supply line, close to the relative pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Littelfuse PESD0402-140) on each externally accessible SIM line, close to each relative pad of the SIM connector. ESD sensitivity rating of the SIM interface pins is 1 kV (HBM). So that, according to EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device.
- Limit capacitance and series resistance on each SIM signal to match the SIM specifications requirements (considering 50 ns is the maximum allowed rise time on clock line, 1.0 µs is the maximum allowed rise time on data and reset lines).

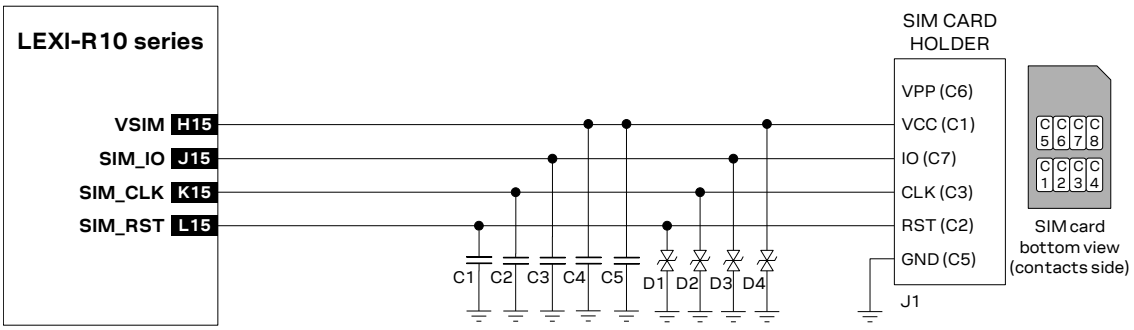

Figure 43: Application circuits for the connection to a removable SIM card, with SIM detection not implemented

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4	Very low capacitance ESD protection	PESD0402-140 - Littelfuse
J1	SIM card holder, 6 positions, without card presence switch	Generic manufacturer, as C707 10M006 136 2 - Amphenol

Table 26: Example of components for the connection to a removable SIM card, with SIM detection not implemented

2.5.1.3 Guidelines for single SIM chip connection

A Surface-Mounted SIM chip (M2M UICC Form Factor) must be connected the SIM card interface of the LEXI-R10 series modules as described in Figure 44.

Follow these guidelines to connect the module to a SIM chip without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line close to the relative pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM lines.
- Limit capacitance and series resistance on each SIM signal to match the SIM specifications (as 50 ns is the max rise time on clock line, 1.0 µs is the max rise time on data and reset lines).

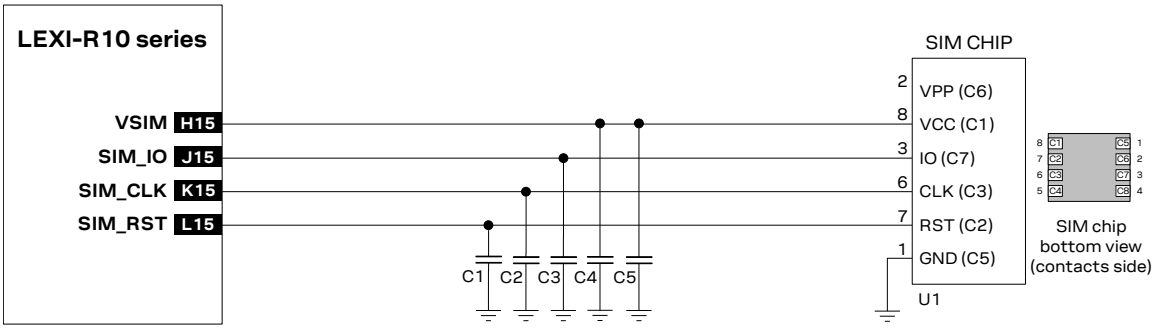

Figure 44: Application circuits for the connection to a Surface-Mounted SIM chip

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	SIM chip (M2M UICC form factor)	Generic manufacturer

Table 27: Example of components for the connection to a solderable SIM chip

2.5.1.4 Guidelines for single SIM card connection with detection

Application circuits for the connection to a single removable SIM card placed in a SIM card holder are described in Figure 45 and Figure 46, where the optional SIM card detection feature is implemented, for applications with no power saving modes use (keeping the AT+UPSV=0 default configuration) and with power saving modes use (AT+UPSV≠0 configuration) respectively.

Follow these guidelines connecting the module to a SIM connector with SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Connect one pin of the normally-open mechanical switch integrated in the SIM connector (as the SW2 pin in Figure 45 and Figure 46) to the **GPIO6** input pin in the “always-on” supply domain, providing a weak pull-down resistor (e.g. 470 kΩ, as R2 in Figure 45 and Figure 46).

- In case of applications with power saving modes not planned to be used: connect the other pin of the normally-open mechanical switch integrated in the SIM connector (SW1 pin in Figure 45) to **V_INT** 1.8 V supply output by means of a strong pull-up resistor (e.g. 1 kΩ, as R1 in Figure 45).
- In case of applications with power saving modes planned to be used: connect the other pin of the normally-open mechanical switch integrated in the SIM connector (SW1 pin in Figure 46) to a GPIO pin in the "always-on" supply domain set as output-high, as for example the **GPIO4** pin, by means of a strong pull-up resistor (e.g. 1 kΩ, as R1 in Figure 46).
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a low capacitance (i.e. less than 10 pF) ESD protection (e.g. Littelfuse PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector. ESD sensitivity rating of SIM interface pins is 1 kV (HBM), so that higher protection level may be required if the lines are externally accessible.
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface (50 ns = max rise time on **SIM_CLK**, 1.0 µs = max rise time on **SIM_IO** and **SIM_RST**).

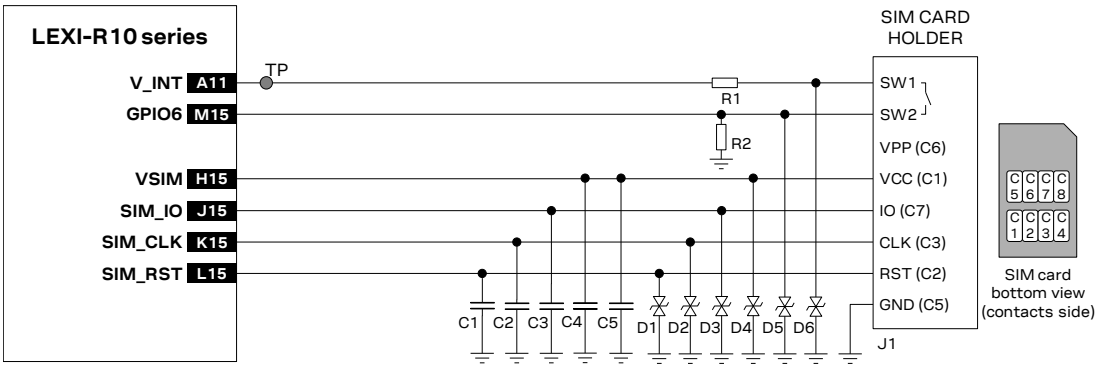

Figure 45: Application circuit to connect a removable SIM card with SIM card detection implemented, keeping AT+UPSV=0

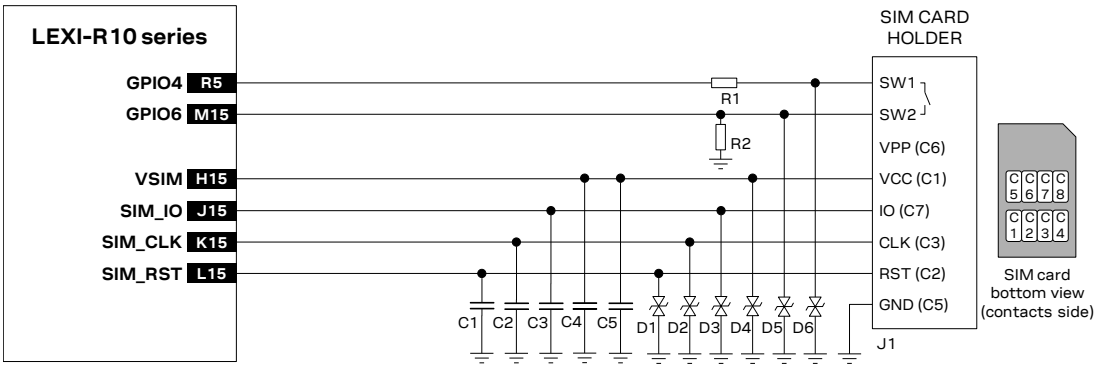

Figure 46: Application circuit to connect a removable SIM card with SIM card detection implemented, using AT+UPSV≠0

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1 – D6	Very low capacitance ESD protection	PESD0402-140 - Littelfuse
R1	1 kΩ resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
R2	470 kΩ resistor 0402 5% 0.1 W	RC0402JR-07470KL- Yageo Phycomp
J1	SIM card holder, 6 + 2 positions, with card presence switch	Generic manufacturer, as CCM03-3013LFT R102 - C&K Components

Table 28: Example of components for the connection to a removable SIM card, with SIM card detection implemented

2.5.2 Guidelines for SIM layout design

The layout of the SIM card interface lines (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**) may be critical if the SIM card is placed far away from the LEXI-R10 series modules or in close proximity to the RF antenna: these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface. It is recommended to keep the traces short and avoid coupling with RF line or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of LTE receiver channels whose carrier frequency is coincidental with harmonic frequencies. It is strongly recommended to place the RF bypass capacitors suggested in Figure 43, Figure 44, and Figure 45 near the SIM connector.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges. Add adequate ESD protection as suggested to protect module SIM pins near the SIM connector.

Limit capacitance and series resistance on each SIM signal to match the SIM specifications. The connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.

2.6 Data communication interfaces

2.6.1 UART interfaces

2.6.1.1 Guidelines for UART circuit design

Providing 1 UART with full RS-232 functionality (using the complete V.24 link)

If RS-232 compatible signal levels are needed, two different external voltage translators can be used to provide full RS-232 (9 lines) functionality: e.g. using the Texas Instruments SN74AVC8T245PW for the translation from 1.8 V to 3.3 V, and the Maxim MAX3237E for the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8 V Application Processor (DTE) is used and complete RS-232 functionality is required, then the complete 1.8 V UART of the module (DCE) should be connected to a 1.8 V DTE, as in Figure 47.

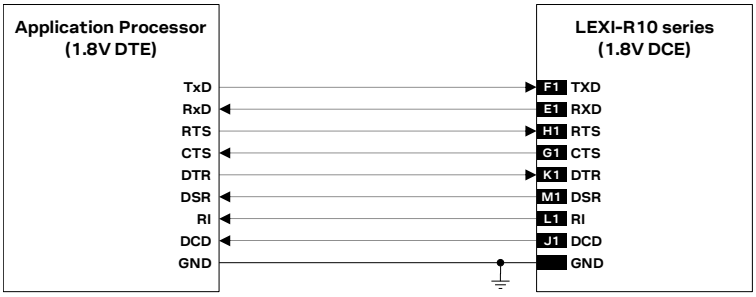

Figure 47: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 48.

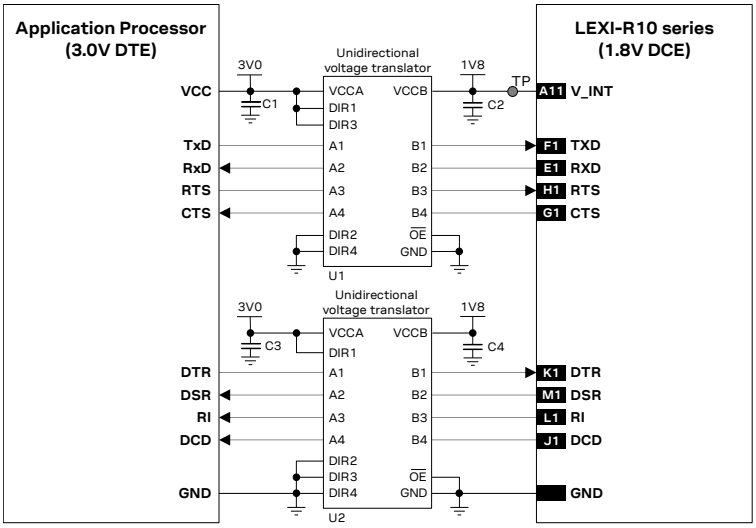

Figure 48: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1, U2	Unidirectional voltage translator	SN74AVC4T774[2] - Texas Instruments

Table 29: Component for UART application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

[2] Voltage translator providing partial power down feature so that the DTE 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with TXD, RXD, RTS and CTS lines only

If the functionality of the **DSR**, **DCD**, **RI** and **DTR** lines is not required, or the lines are not available:

- Connect the module **DTR** input to GND using a 0 Ω series resistor, since it may be useful to set **DTR** active if not specifically handled, in particular to have URCs presented over the UART interface (see the AT commands manual [2] for the &D, S0, +CNMI AT commands)
- Leave **DSR**, **DCD** and **RI** lines of the module floating, with test-point on **DCD** line for diagnostic

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard. If a 1.8 V Application Processor is used, the circuit should be implemented as described in Figure 49.

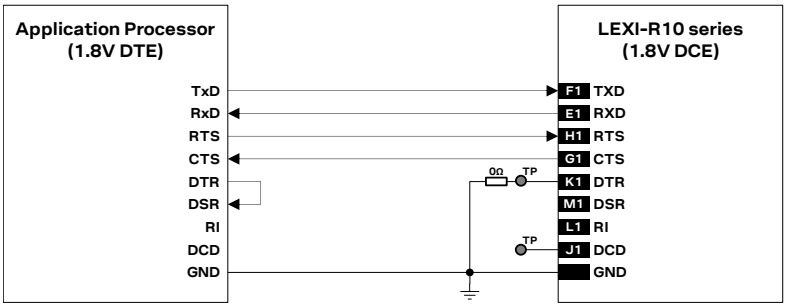

Figure 49: UART interface application circuit with partial V.24 link (5-wire) in the DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as in Figure 50.

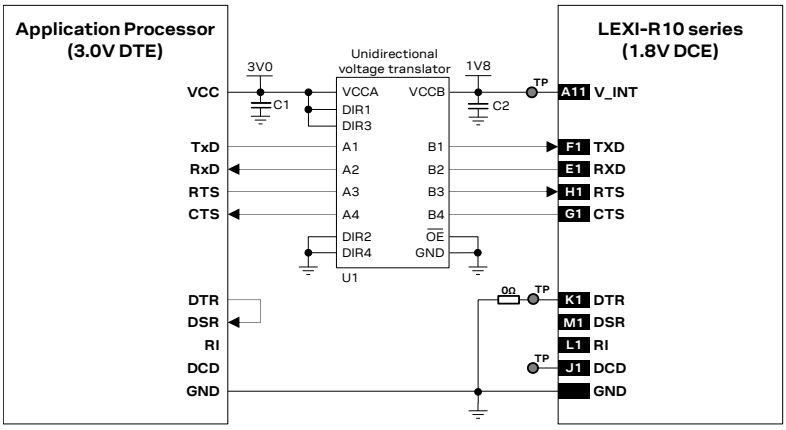

Figure 50: UART interface application circuit with a partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional voltage translator	SN74AVC4T774[4] - Texas Instruments

Table 30: UART application circuit components with a partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

[4] Voltage translator providing partial power down feature so that the DTE 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 2 UARTs with the TXD, RXD, RTS and CTS lines

LEXI-R10 series modules include an auxiliary UART interface (UART AUX), as alternative mutually exclusive function over the **DTR**, **DSR**, **DCD** and **RI** pins, with settings configurable by dedicated AT commands (see the AT commands manual [2]):

- Data lines (**DCD** as data output, **DTR** as data input)
- HW flow control lines (**RI** as flow control output, **DSR** as flow control input)

If RS-232 compatible signal levels are needed, two Maxim MAX13234E voltage level translators can be used. These chips translate voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor is used, the circuit should be implemented as described in Figure 51.

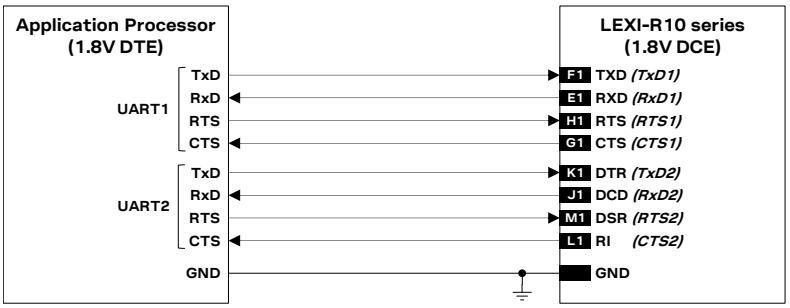

Figure 51: 2 UART interfaces application circuit with 5-wire links in DTE/DCE serial communications (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interfaces of the module (DCE) by appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as in Figure 52.

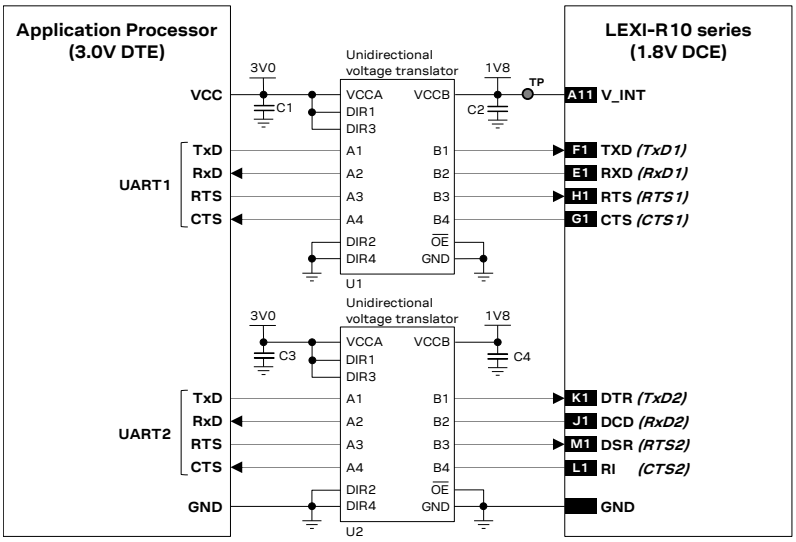

Figure 52: 2 UART interfaces application circuit with 5-wire links in DTE/DCE serial communications (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1, U2	Unidirectional voltage translator	SN74AVC4T774 [5] - Texas Instruments

Table 31: Components for 2 UARTs application circuit with 5-wire links in DTE/DCE serial communications (3.0 V DTE)

[5] Voltage translator providing partial power down feature so that the DTE 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with TXD and RXD lines only

☞ Providing the **TXD** and **RXD** lines only is not recommended if the multiplexer functionality is used: providing also at least the HW flow control (**RTS** and **CTS** lines) is recommended, and it is in particular necessary if the low power mode is enabled by +UPSV AT command.

If functionality of the **CTS**, **RTS**, **DSR**, **DCD**, **RI** and **DTR** lines is not required in the application, then:

- Connect the **RTS** input line to GND or to the **CTS** output line of the module, since the module requires **RTS** active (low electrical level) if HW flow-control is enabled (AT&K3, default setting)
- Connect the **DTR** input line to GND using a 0 Ω series resistor, because it is useful to set **DTR** active if not specifically handled, in particular to have URCs presented over the UART interface (see the AT commands manual [2], &D, S0, +CNMI AT commands)
- Leave **DSR**, **DCD** and **RI** lines of the module floating, with test-point on **DCD** line for diagnostic

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V Application Processor (DTE) is used, the circuit should be implemented as in Figure 53.

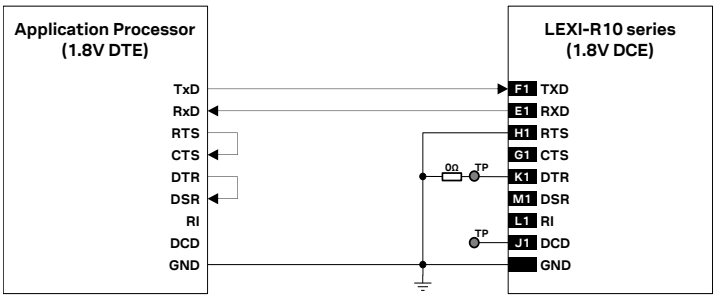

Figure 53: UART interface application circuit with a 3-wire link in the DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as in Figure 54.

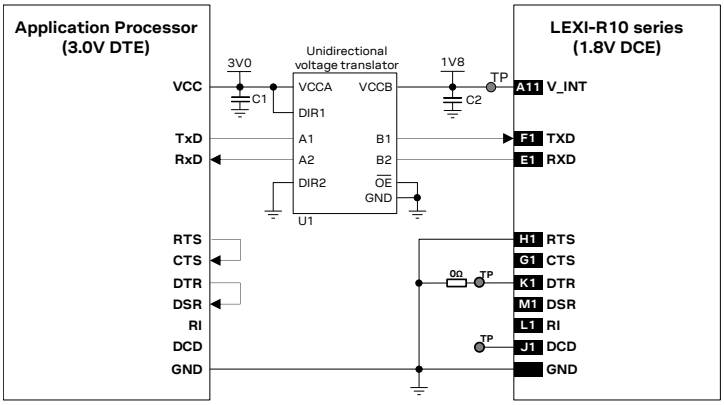

Figure 54: UART interface application circuit with a partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional voltage translator	SN74AVC2T245[6] - Texas Instruments

Table 32: UART application circuit components with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

[6] Voltage translator providing partial power down feature so that the DTE 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Additional considerations using UART and power saving modes

As indicated in section 1.9.2.2, if the power saving configurations are enabled by AT+UPSV command, LEXI-R10 series modules can enter the ultra-low power deep-sleep mode whenever possible, even very frequently, as in-between short DRX cycles, and in such case all the UART interfaces lines go low.

When the ultra-low power deep sleep mode is entered, all the lines in **V_INT** supply domain, including, as the data lines, the hardware flow control lines and the Ring Indicator line, because the **V_INT** supply domain of the UART interfaces is switched off.

☞ We recommend monitoring the UART break condition at the **RXD** data output line of the module or monitoring the **V_INT** output of the module, to determine when the ultra-low power deep sleep mode is entered.

☞ We recommend considering the use of the GPIO pins in the “always-on” supply domain (see section 1.10), to monitor the module status and to get the Ring Indicator / URC event notifications even in ultra-low power deep sleep mode

Other additional general considerations using UART

If a 3.0 V Application Processor (DTE) is used, the voltage scaling from any 3.0 V output of the DTE to the corresponding 1.8 V input of the module (DCE) can be implemented as an alternative low-cost solution, by means of an appropriate voltage divider. Consider the value of the pull-down / pull-up integrated at the inputs of the module (DCE) for the correct selection of the voltage divider resistance values.

Moreover, the voltage scaling from any 1.8 V output of the module (DCE) to the corresponding 3.0 V input of the Application Processor (DTE) can be implemented by means of appropriate non-inverting buffer with open drain output. The non-inverting buffer should be supplied by the **V_INT** supply output of the module. Consider the value of the pull-up integrated at each input of the DTE (if any) and the baud rate required by the application for the appropriate selection of the resistance value for the external pull-up biased by the application processor supply rail.

☞ ESD sensitivity rating of the UART pins is 1 kV (HBM). Higher protection levels could be required if the lines are externally accessible, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

2.6.1.2 Guidelines for UART layout design

The UART serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.2 USB interface

2.6.2.1 Guidelines for USB circuit design

USB_D+ and **USB_D-** lines carry USB serial data and signaling. The lines are set in single-ended mode for full-speed USB and in differential mode for high-speed USB signaling and data transfer.

Pull-up, pull-down and external series resistors on **USB_D+** and **USB_D-** lines as required by USB 2.0 specification [5] are part of the module USB pins driver and do not need to be externally provided.

☞ The **USB_BOOT** input pin has to be set high, at the 1.8 V voltage level of the **V_INT** supply output, to enable the FW update by means of the dedicated tool over the USB interface.

Routing the USB pins to a connector, they will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device with very low capacitance should be provided close to accessible point on the line connected to this pin, as described in Figure 55 and Table 33.

☞ USB interface pins ESD sensitivity rating is 1 kV (HBM). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ultra-low capacitance (i.e. < 1 pF) ESD protection (e.g. Littelfuse PESD0402-140 ESD protection device) on the lines connected to these pins, close to accessible points.

The USB pins of the modules can be directly connected to the USB host application processor without additional ESD protections if they are not externally accessible.

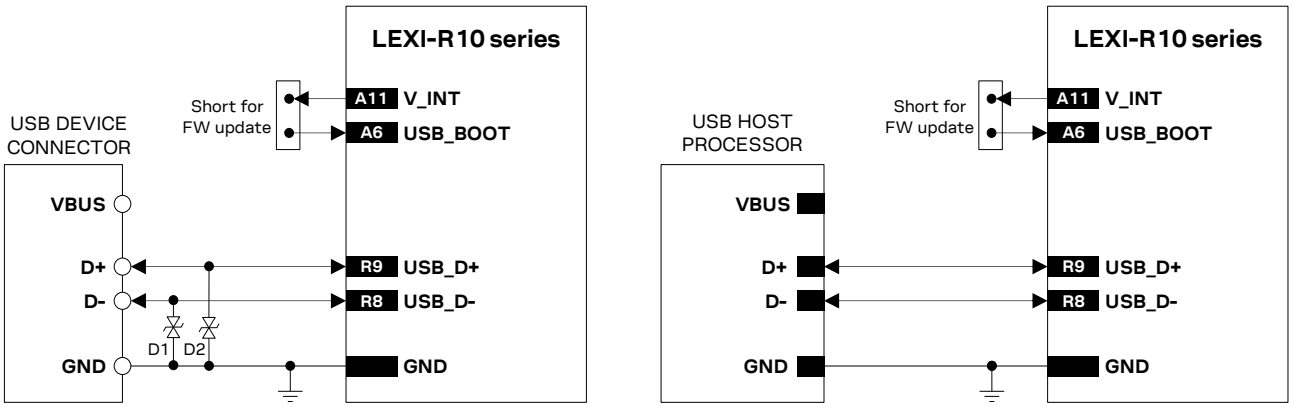

Figure 55: USB Interface application circuits for LEXI-R10 series modules

Reference	Description	Part number - Manufacturer
D1, D2	Very Low Capacitance ESD Protection	PESD0402-140 - Littelfuse

Table 33: Components for USB application circuits for LEXI-R10 series modules

2.6.2.2 Guidelines for USB layout design

The **USB_D+** / **USB_D-** lines require accurate layout design to achieve reliable signaling at the high speed data rate (up to 480 Mb/s) supported by the USB serial interface.

The same careful considerations for approriate RF transmission lines design must be taken for the design of the **USB_D+** / **USB_D-** lines.

The characteristic impedance of **USB_D+** / **USB_D-** lines is specified by the USB 2.0 specification [5]. One of the key parameters is the differential characteristic impedance applicable for the odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential.

Signal integrity may be degraded if PCB layout is not optimal, especially when USB lines are very long.

Use the following general routing guidelines to minimize signal quality problems:

- Route **USB_D+** / **USB_D-** lines as a differential pair
- Route **USB_D+** / **USB_D-** lines as short as possible
- Ensure the differential characteristic impedance (Z_0) is as close as possible to 90 Ω
- Ensure the common mode characteristic impedance (Z_{CM}) is as close as possible to 30 Ω
- Use design rules for **USB_D+** / **USB_D-** as RF transmission lines, being them coupled differential micro-strip or buried stripline: avoid stubs, abrupt change of layout, and route on clear PCB area

Figure 56 and Figure 57 provide two examples of coplanar waveguide designs with differential characteristic impedance close to 90 Ω and common mode characteristic impedance close to 30 Ω.

The first transmission line can be implemented in case of 4-layer PCB stack-up herein described, the second transmission line can be implemented in case of 2-layer PCB stack-up herein described.

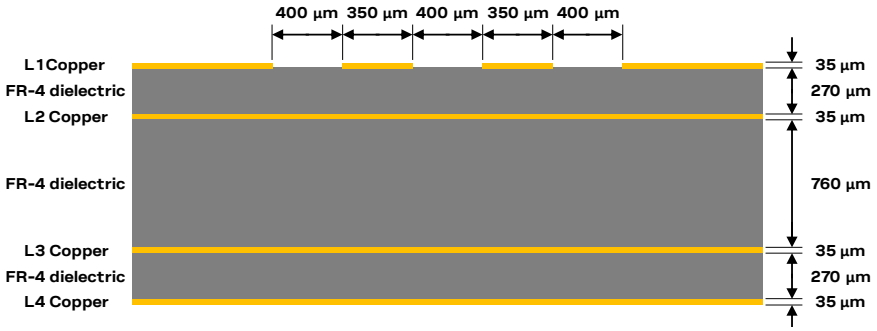

Figure 56: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 4-layer board layup

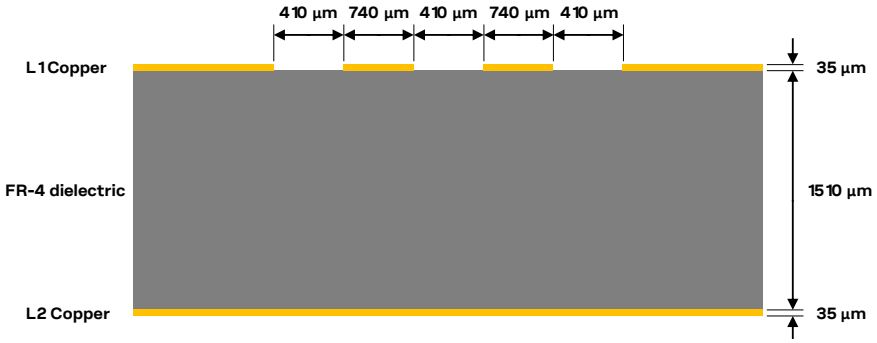

Figure 57: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 2-layer board layup

2.6.3 I2C interface

2.6.3.1 Guidelines for I2C circuit design

☞ The I2C interface is not supported by the FW of the “00B” and “01B” product versions.

The **SDA** and **SCL** pins of the module are open drain output as per I2C bus specifications [10], and they have internal pull-up resistors to the **V_INT** 1.8 V supply rail of the module, so there is no need of additional external pull-up resistors, but they can be provided according to application requirements.

☞ Capacitance and series resistance must be limited on the bus to match the I2C specifications (maximum proper rise time for **SCL** / **SDA** lines is 1.0 µs): route connections as short as possible.

☞ ESD sensitivity rating of the I2C pins is 1 kV (HBM). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible points.

2.6.3.2 Guidelines for I2C layout design

The I2C serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.7 General purpose input / output

2.7.1 Guidelines for GPIO circuit design

As indicated in section 1.10, the GPIO pins are in two different supply domains:

- **GPIO1**, **GPIO5**, **GPIO7**, **GPIO8**, **GPIO9** and **GPIO10** pins are in the **V_INT** supply domain (1.8 V typ.), meaning that their function is not available when the module is in ultra-low power deep-sleep mode enabled by AT+UPSV≠0, with the generic digital interface supply (**V_INT**) switched off;
- **GPIO2**, **GPIO3**, **GPIO4** and **GPIO6** pins are in the "always-on" supply domain (1.8 V typ.), meaning that their function is available also when the module is in ultra-low power deep-sleep mode enabled by AT+UPSV≠0, with the generic digital interface supply (**V_INT**) switched off.

In case a GPIO pin needs to be connected to a device with voltage level different than 1.8 V, as for example to a pin of the external host processor operating at 3 V:

- The **V_INT** supply output of the module can be used as reference for the voltage level translator, on the module side, used to translate the 1.8 V voltage domain of **GPIO1**, **GPIO5**, **GPIO7**, **GPIO8**, **GPIO9** and **GPIO10** pins to the 3 V voltage domain of the external device / host processor;
- A GPIO pin in the "always-on" supply domain, set as output-high, can be used as reference for the voltage level translator, on the module side, used to translate the 1.8 V voltage domain of **GPIO2**, **GPIO3**, **GPIO4** and **GPIO6** pins to the 3 V voltage domain of the external device / host processor.

A typical usage of LEXI-R10 series modules GPIOs can be the following:

- Network indication provided over **GPIO1** pin in **V_INT** supply domain (see Figure 58 and Table 34)
- Module status indication over **GPIO2** pin in "always-on" supply domain (see Figure 58, section 1.10, 1.9.2.2: "low" with module switched off, "high" with module in deep-sleep, active, connected mode)
- Low power mode control, Faster power-off, or Memory-safe power-off functions over **GPIO3** pin in "always-on" supply domain (see Figure 58, section 1.10)
- Event / URC / ring indication over **GPIO4** pin in "always-on" supply domain (see sections 1.10 and 1.9.2.2: "low" pulse to notify the event, "high" otherwise)
- SIM card detection provided over **GPIO6** pin in "always-on" supply domain (see Figure 45, Figure 46 and Table 28 in section 2.5)

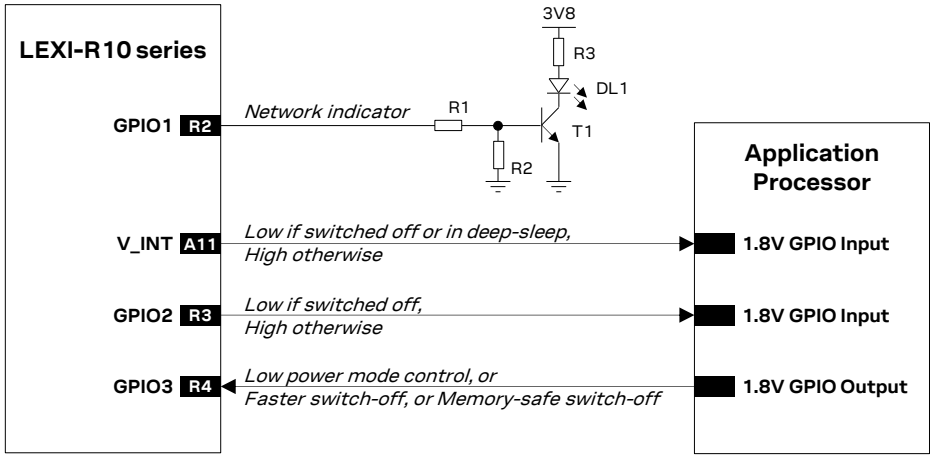

Figure 58: Application circuit example for GPIO pins providing network indication, module status indication, ultra-low power deep sleep mode control or switch-off functions

Reference	Description	Part number - Manufacturer
R1	10 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	47 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R3	820 Ω resistor 0402 5% 0.1 W	Generic manufacturer
DL1	LED red SMT 0603	LTST-C190KRKT - Lite-on Technology Corporation
T1	NPN BJT transistor	BC847 - Infineon

Table 34: Components for network indication application circuit

- Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO of LEXI-R10 series modules.
- ESD sensitivity rating of the GPIO pins is 1 kV (HBM). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible points.
- If the GPIO pins are not used, they can be left unconnected on the application board.

2.7.2 Guidelines for general purpose input/output layout design

The general-purpose inputs / outputs pins are not critical for layout.

2.8 Reserved pins (RSVD)

LEXI-R10 series modules include pins reserved for future use, marked as **RSVD**, which can all be left unconnected on the application board.

2.9 Module placement

An optimized placement allows a minimum RF line's length and closer path from DC source for **VCC**.

Make sure that the module, analog parts and RF circuits are clearly separated from any possible source of radiated energy. In particular, digital circuits can radiate digital frequency harmonics, which can produce electro-magnetic interference that affects the module, analog parts and RF circuits performance. Implement suitable countermeasures to avoid any possible EMC issue.

Make sure that the module is placed in order to keep the antenna as far as possible from **VCC** supply line and related parts (refer to Figure 22), from high speed digital lines (as USB) and from any possible noise source.

Provide enough clearance between the module and any external part: clearance of at least 0.4 mm per side is recommended to let suitable mounting of the parts.

- The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application base-board below the LEXI-R10 series modules: avoid placing temperature sensitive devices close to the module.

2.10 Module footprint and paste mask

Figure 59 describes the suggested footprint (i.e. copper mask) and paste mask layout for LEXI-R10 series modules: the proposed land pattern layout and the proposed stencil apertures layout reflect the modules pads layout described in the LEXI-R10 series data sheet [1].

The recommended thickness of the stencil for the soldering paste is 130 µm, according to application production process requirements.

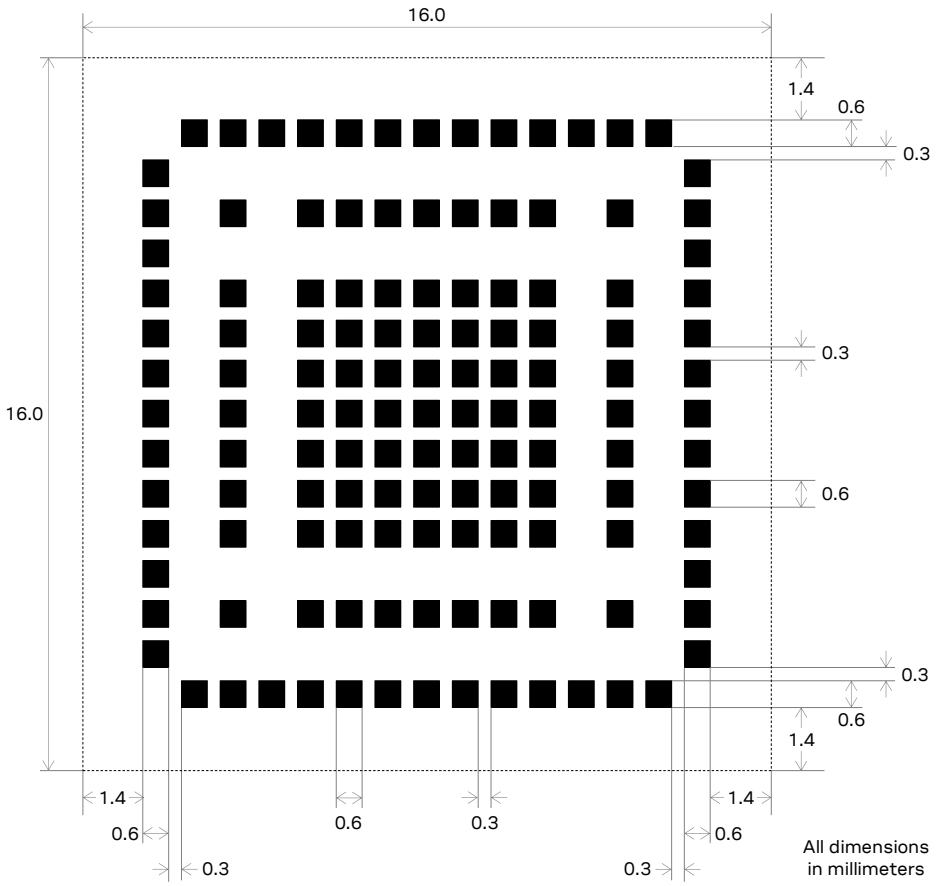

Figure 59: Suggested footprint and paste mask for LEXI-R10 series modules (application board top view)

These are recommendations only and not specifications. The exact copper, solder and paste mask geometries, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) implemented.

2.11 Thermal guidelines

The module operating temperature range is specified in the LEXI-R10 series data sheet [1].

The most critical condition concerning module thermal performance is the uplink transmission at maximum power (data upload in connected mode), when the baseband processor runs at full speed, radio circuits are all active and the RF power amplifier is driven to higher output RF power. This scenario is not often encountered in real networks (for example, see the Terminal Tx Power distribution taken from operation on a live network described in the GSMA TS.09 Document [11]); however the application should be correctly designed to cope with it.

During transmission at maximum RF power the LEXI-R10 series modules may indicatively generate ~2 W thermal power: this is an indicative value since the exact generated power strictly depends on

operating condition such as the actual antenna return loss, the transmitting frequency band, etc. The generated thermal power must be adequately dissipated through the thermal and mechanical design of the application.

The spreading of the Module-to-Ambient thermal resistance ($R_{th,M-A}$) depends on the module operating condition. The overall temperature distribution is influenced by the configuration of the active components during the specific mode of operation and their different thermal resistance toward the case interface.

☞ The Module-to-Ambient thermal resistance value and the relative increase of module temperature will differ according to the specific mechanical deployments of the module, e.g. application PCB with different dimensions and characteristics, mechanical shells enclosure, or forced air flow.

The increase of the thermal dissipation, i.e. the reduction of the Module-to-Ambient thermal resistance, will decrease the temperature of the modules internal circuitry for a given operating ambient temperature. This improves the device long-term reliability in particular for applications operating at high ambient temperature.

Recommended hardware techniques to be used to improve heat dissipation in the application:

- Connect each **GND** pin with solid ground layer of the application PCB and connect each ground area of the multilayer application PCB with complete thermal via stacked down to main ground layer.
- Provide a ground plane as wide as possible on the application board.
- Optimize antenna return loss, to optimize overall electrical performance of the module including a decrease of module thermal power.
- Optimize the thermal design of any high-power components included in the application, such as linear regulators and amplifiers, to optimize overall temperature distribution in the application.
- Select the material, the thickness and the surface of the box (i.e. the mechanical enclosure) of the application device that integrates the module so that it provides good thermal dissipation.

Beside the reduction of the Module-to-Ambient thermal resistance implemented by correct application hardware design, the increase of module temperature can be moderated by a correspondingly correct application software implementation:

- Enable low power mode configuration using the dedicated AT commands
- Enable module connected mode for a given time period and then disable it for a time period long enough to adequately mitigate the temperature increase.

2.12 Schematic for LEXI-R10 series modules integration

Figure 60 is an example of a schematic diagram where a LEXI-R10 series module is integrated into an application board using almost all available interfaces and functions.

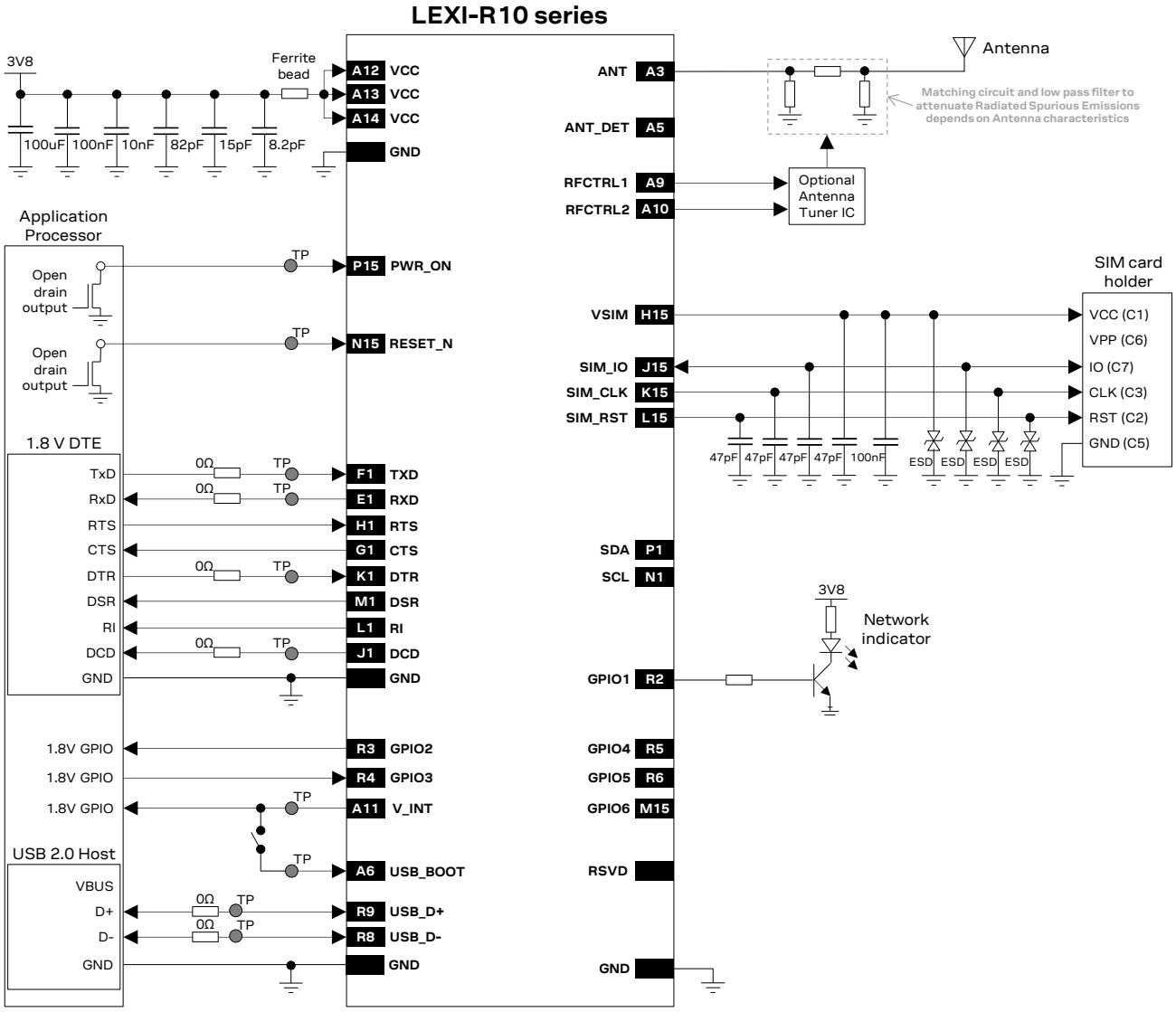

Figure 60: Example of schematic diagram to integrate a LEXI-R10 series module using almost all available interfaces

2.13 Design-in checklist

This section provides a design-in checklist.

2.13.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at **VCC** pin within the operating range limits.
- ☑ DC supply must be capable of supporting the highest peak / pulse current consumption values and the maximum averaged current consumption values in connected mode, as specified in the LEXI-R10 series data sheet [1].
- ☑ **VCC** voltage supply should be clean, with very low ripple/noise: provide the suggested bypass capacitors, in particular if the application device integrates an internal antenna.
- ☑ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply.
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested pF capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART signals direction, as the modules signal names follow the ITU-T V.24 recommendation [6].
- ☑ Capacitance and series resistance must be limited on each high speed line of the USB interface.
- ☑ It is recommended to provide accessible test points directly connected to the **V_INT**, **PWR_ON** and **RESET_N** pins for diagnostic and/or FW update purposes.
- ☑ In case the UART interfaces are used for communications with the host application processor, it is recommended to provide accessible test points directly connected to the **USB_D+**, **USB_D-** and **USB_BOOT** pins for diagnostic and/or FW update purposes.
- ☑ In case the USB interface is used for communications with the host application processor, it is recommended to provide accessible test points directly connected to the **TXD** and **RXD** pins of the main UART interface for diagnostic and/or FW update purposes.
- ☑ In case the USB and the main UART interfaces are used for communications with the host application processor, it is recommended to provide accessible test points directly connected to the **DCD** and **DTR** pins of the auxiliary UART interface for diagnostic purposes.
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ Provide adequate precautions for EMC / ESD immunity as required on the application board.
- ☑ All unused pins can be left unconnected, providing Test-Points on the relevant pins for FW update or diagnostic purposes as indicated above.

2.13.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT** port (antenna RF interface).
- ☑ Check cellular antenna trace design for regulatory compliance perspective (see section 4.2 for FCC United States, and related section 2.4.1.5).
- ☑ Ensure no coupling occurs between the RF interface and noisy or sensitive signals (SIM signals, high-speed digital lines such as USB, and other data lines).
- ☑ Optimize placement for minimum length of RF line.
- ☑ Check the footprint and paste mask designed for the LEXI-R10 series module as illustrated in section 2.10.
- ☑ **VCC** line should be enough wide and as short as possible.
- ☑ Route **VCC** supply line away from RF line / part (refer to Figure 22) and other sensitive analog lines / parts.
- ☑ The **VCC** bypass capacitors in the picoFarad range should be placed as close as possible to the **VCC** pins, in particular if the application device integrates an internal antenna.
- ☑ Ensure an optimal grounding connecting each **GND** pin with application board solid ground layer.
- ☑ Use as many vias as possible to connect the ground planes on multilayer application board, providing a dense line of vias at the edges of each ground area, in particular along RF and high speed lines.
- ☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.
- ☑ **USB_D+** / **USB_D-** traces should meet the characteristic impedance requirement (90 Ω differential and 30 Ω common mode) and should not be routed close to any RF line / part.
- ☑ Ensure appropriate RF precautions for the GNSS and cellular technologies coexistence.

2.13.3 Antenna checklist

- ☑ Antenna termination should provide 50 Ω characteristic impedance with V.S.W.R at least less than 3:1 (recommended 2:1) on operating bands in deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure compliance with any regulatory RF radiation requirement, as reported in section 4.2 for FCC United States, in section 4.3 for ISED Canada, in section 4.4 for CE Europe, etc.
- ☑ Ensure high isolation between the cellular antenna and any other antennas or transmitters present on the end device.

3 Handling and soldering

☞ No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to LEXI-R10 series reels / tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning, see the LEXI-R10 series data sheet [1] and the u-blox package information user guide [17].

3.2 Handling

The LEXI-R10 series modules are Electro-Static Discharge (ESD) sensitive devices.

⚠ Ensure ESD precautions are implemented during handling of the module.

Electro-Static Discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of LEXI-R10 series modules, using Human Body Model according to JS-001-2017 and using Charged Device Model according to JS-002-2018, is specified in LEXI-R10 series data sheet [1].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from the International Electrotechnical Commission (IEC) or the American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be considered whenever handling the LEXI-R10 series modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect the ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron).
- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in a non-ESD protected work area, implement adequate ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD-safe soldering iron.

3.3 Soldering

3.3.1 Soldering paste

"No Clean" soldering paste is strongly recommended for LEXI-R10 series modules, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper) 95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)
Melting Temperature:	217 °C
Stencil Thickness:	130 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.10.

☞ The quality of the solder joints should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type soldering oven is strongly recommended for LEXI-R10 series modules over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the ”IPC-7530A Guidelines for temperature profiling for mass soldering (reflow and wave) processes”.

Reflow profiles are to be selected according to the following recommendations.

⚠ Failure to observe these recommendations can result in severe damage to the device!

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s
  If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 – 120 s
  If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End temperature: +150 - +200 °C
  If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of +217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above +217 °C liquidus temperature: 40 - 60 s
- Peak reflow temperature: +245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s

☞ To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

⚠ Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.

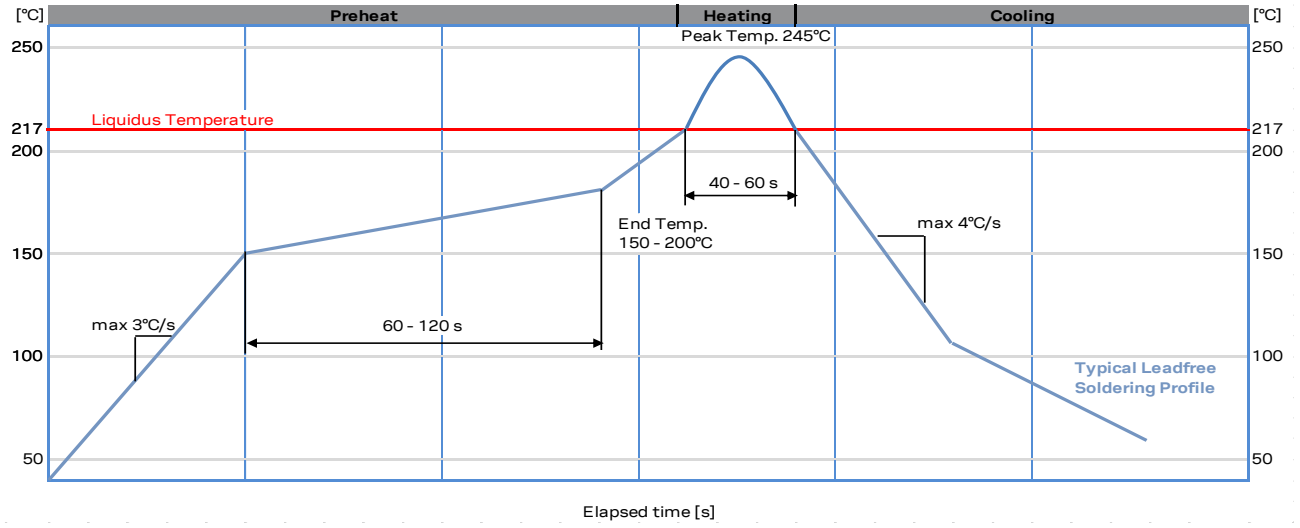

Figure 61: Recommended soldering profile

☞ The modules must not be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the module, inspect it optically to verify that it is correctly aligned and centered.

3.3.4 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results, use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.3.5 Repeated reflow soldering

Repeated reflow soldering processes and soldering the module upside-down are not recommended.

Boards with components on both sides may require two reflow cycles. In this case, the module should always be placed on the side of the board that is submitted into the last reflow cycle. The reason for this (besides others) is the risk of the module falling off due to the significantly higher weight in relation to other components.

☞ u-blox gives no warranty against damages to the LEXI-R10 series modules caused by performing more than a total of two reflow soldering processes (one reflow soldering process to mount the LEXI-R10 series module, plus one reflow soldering process to mount other parts).

3.3.6 Wave soldering

LEXI-R10 series LGA modules must not be soldered with a wave soldering process.

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. No more than one wave soldering process is allowed for a board with a LEXI-R10 series module already populated on it.

⚠ Performing a wave soldering process on the module can result in severe damage to the device!

☞ u-blox gives no warranty against damages to the LEXI-R10 series modules caused by performing more than a total of two soldering processes (one reflow soldering process to mount the LEXI-R10 series module, plus one wave soldering process to mount other THT parts on the application PCB).

3.3.7 Hand soldering

Hand soldering is not recommended.

3.3.8 Rework

Rework is not recommended.

☞ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the HF properties of the cellular modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal coating of the module will void the warranty.

3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the cellular modules before implementing this in production.

☞ Casting will void the warranty.

3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interference and noise.

☞ u-blox gives no warranty for damages to the cellular modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12 Use of ultrasonic processes

The cellular modules contain components which are sensitive to ultrasonic waves. Use of any ultrasonic processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty against damages to the modules caused by any ultrasonic processes.