REVIEW HISTORY

Revision	Department	Authors/Reviewer	Date	Description
	Engineering	Engineering Project Manager (reviewer)		
	Engineering	Reviewer1		
	Engineering	Reviewer2		
	QA	Reviewer3		
	Product marketing	Reviewer4		
	Product Management	Engineering Product manager(reviewer)		

1. PROBLEM DEFINITION

This document is Hardware Function Specification for KD-921WS

KD-921WS is an outdoor MST that can support data, video and roaming and handoff. KD-921WS need support 802.11 a/b/g radio and one (or two) 100 base ethernet interface. Through these ethernet and radio, it can provide a path between video camera and data center, or between outdoor KD-921WS router and indoor networks like KD-921WS. Or between two seperated Mesh networks.

KD-921WS is a dual radio indoor router

2. DESIGN PRINCIPLES

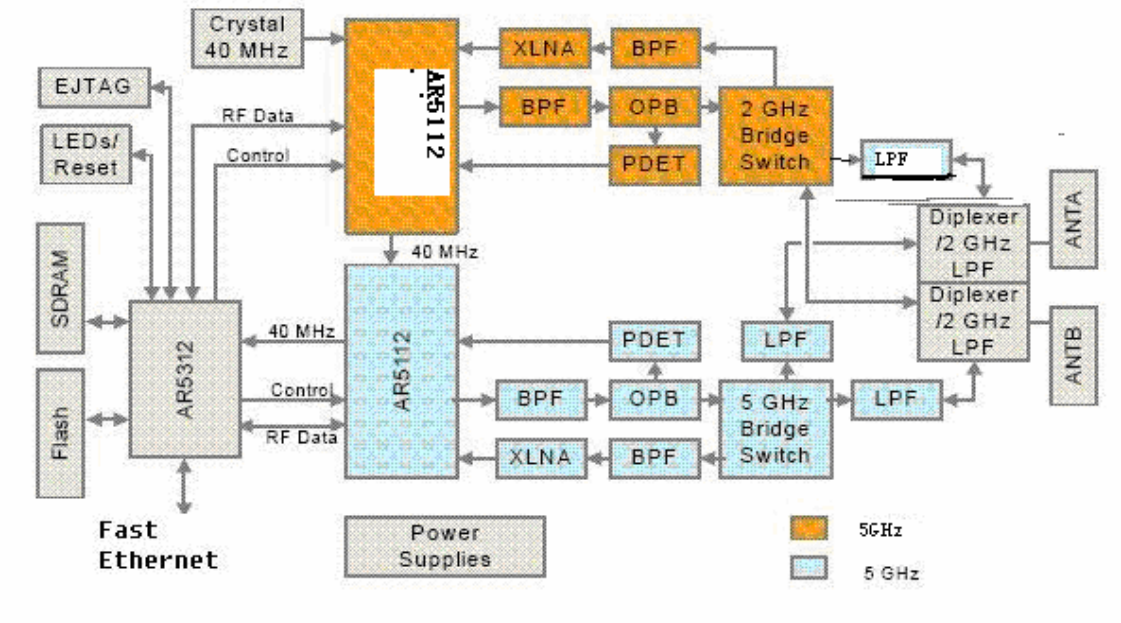
One major target of the design is to lower cost, compare to KD-921WS, need control whole bom within $150. We need design one board for 3 system.

3. ARCHITECTURE

3.1. SOFTWARE/HARDWARE PARTITIONS

Hardware is based on Atheros reference design AP30 which use SOC chipset AR5312, two AR5112. Software is Linux OS plus application ported from KD-921WS

System block diagram



4. HARDWARE DESIGN

4.1. DIGITAL HW SUBSYSTEMS

4.1.1. AR5312

By using Atheros SOC chipset, we could save nearly 20$, but we lost some cpu performance. Cpu not as good as Intel Xscale processors

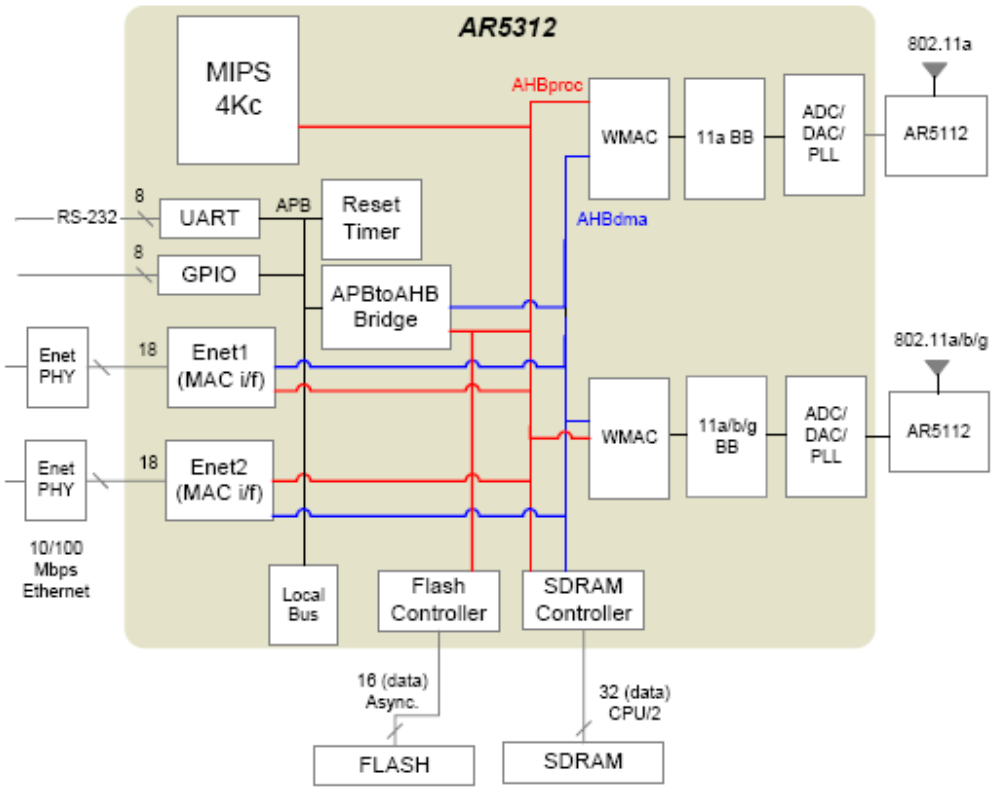
The Atheros AR5312 is part of the three-chip AR5002AP solution for dual, concurrent IEEE 802.11a/b/g 2.4/5 GHz wireless local area network (WLANs) access point applications. The AR5312 supports 802.11a/b/g MAC/baseband processing; two 802.3 MAC and MII interfaces to external Ethernet PHY; SDRAM controller; external memory interface for Flash, ROM or RAM; GPIO; LED controls; a high-speed UART with DMA supporting data rates up to 1 Mbps for serial port applications; and a flexible local bus. When combined with the AR5112s Radioon- a-Chip (RoC), the AR5002AP chipset enables a cost effective silicon solution for dual WLAN access point applications.

Features

- Integrated KD-921WS processor
- 220 MHz processor frequency
- Supports OFDM modulation

- Data rates of 1, 2, 5.5, 6, 9, 12, 18, 24, 36, 48, 54 Mbps and Atheros Turbo Mode offering up to 108 Mbps
- Two IEEE 802.3 Ethernet MAC supporting 10/100 Mbps, full and half duplex, and MIIinterface to external Ethernet PHY
- UART with DMA supports data rates up to 1 Mbps
- Flexible, programmable local bus
- IEEE 1149.1 standard test access port and boundary scan architecture supported
- EJTAG based debugging of the processor core supported
- With the AR5112/AR2112—Complete all-CMOS solution for 802.11a 5 GHz WLANs frequency band operation; and for 802.11b/g 2.4 GHz WLANs

AR5312 block diagram



4.1.2. FLASH

Boot flash memory

The boot flash Memory is Spansionl's strataflash memory S29GL128P90TFIR10,

.it offers a fast page access time of 25 ns with a corresponding random access time as fast as 90 ns.

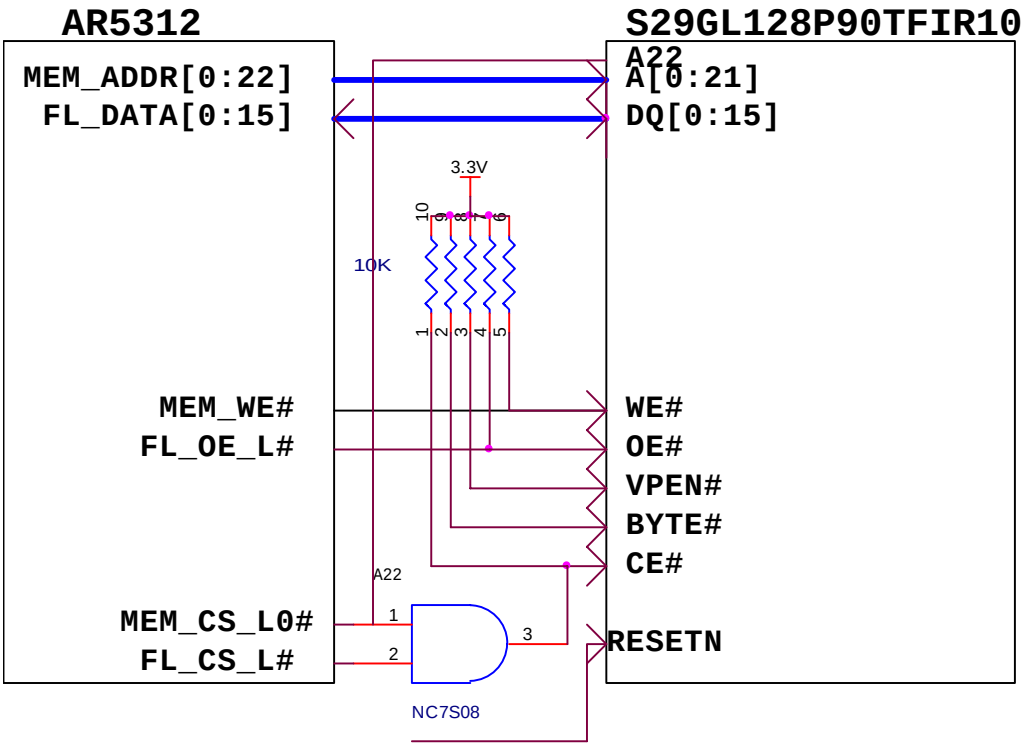
Performance

- Random access time is 90ns, page access time is 25ns, CE# access time is 90ns, OE# access time is 25ns;
- Single word programming typical time is 60us, effective write buffer programming per word 15us typical, effective write buffer programming per word 15us typical,;
- Suspend and Resume commands for Program and Erase operations;
- Write operation status bits indicate program and erase operation completion;
- Support for CFI (Common Flash Interface)
- Persistent and Password methods of Advanced Sector Protection
- highest address sector protected

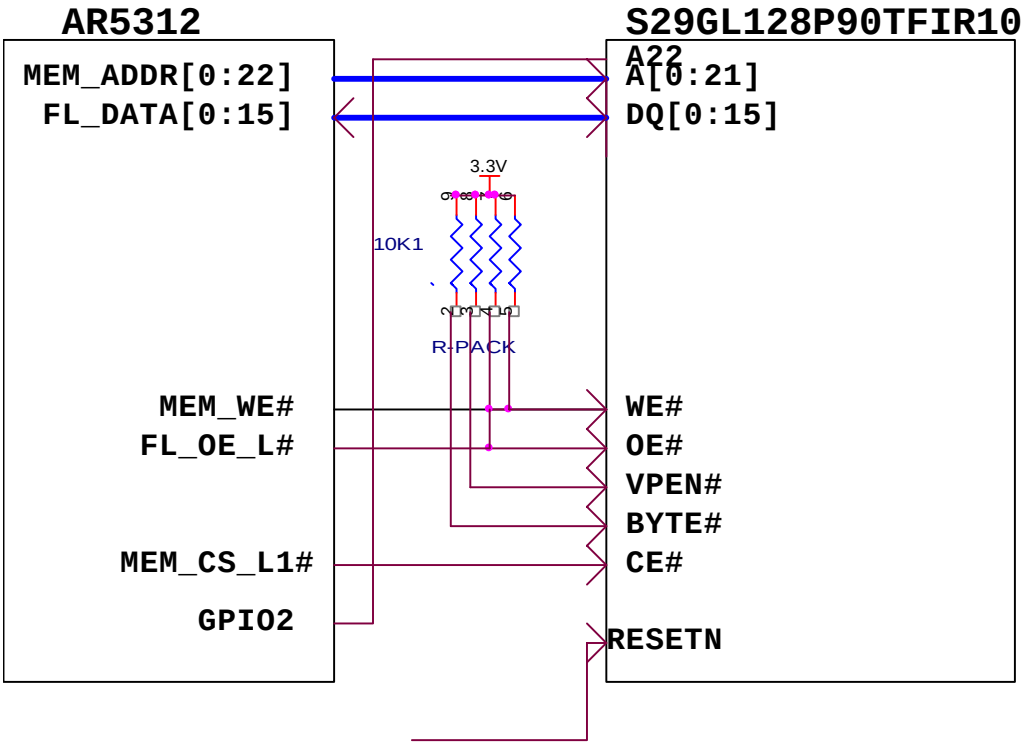
boot falsh interface

The following diagram illustrates how the boot ROM is connected to processor. The design can use up to two 16 Mbyte, 16 bit flash in the 56 TSOP package, totally have 24Mbyte boot flash usable.

The below is the AR5312 and the U81 block diagram



The below is the block diagram between AR5312 and U83

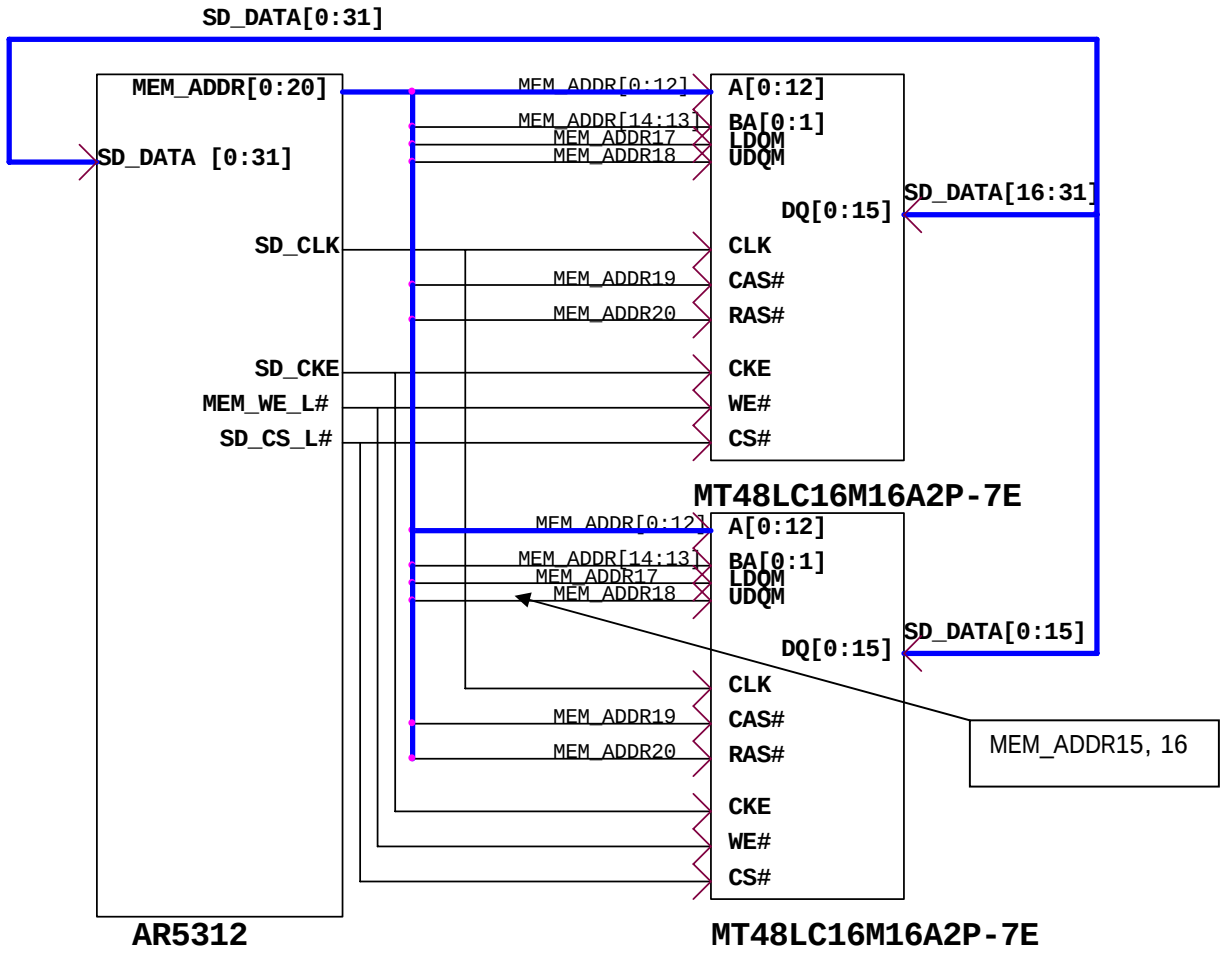


One thing we should indicate that

4.1.3.SDRAM

We now use two 4 Meg x 16 x 4 banks SDRAM, its clock frequency is 133MHz, and access time is 5.4ns, 1.5ns setup time, 0.8ns hold time.

System SDRAM block diagram



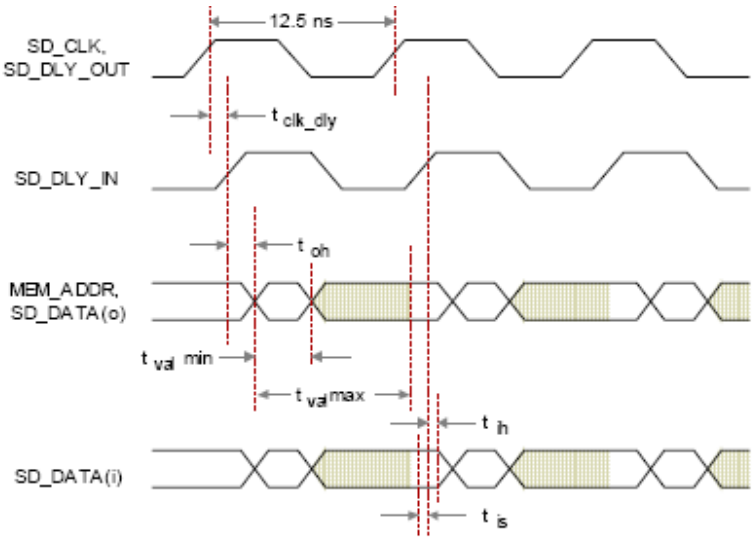


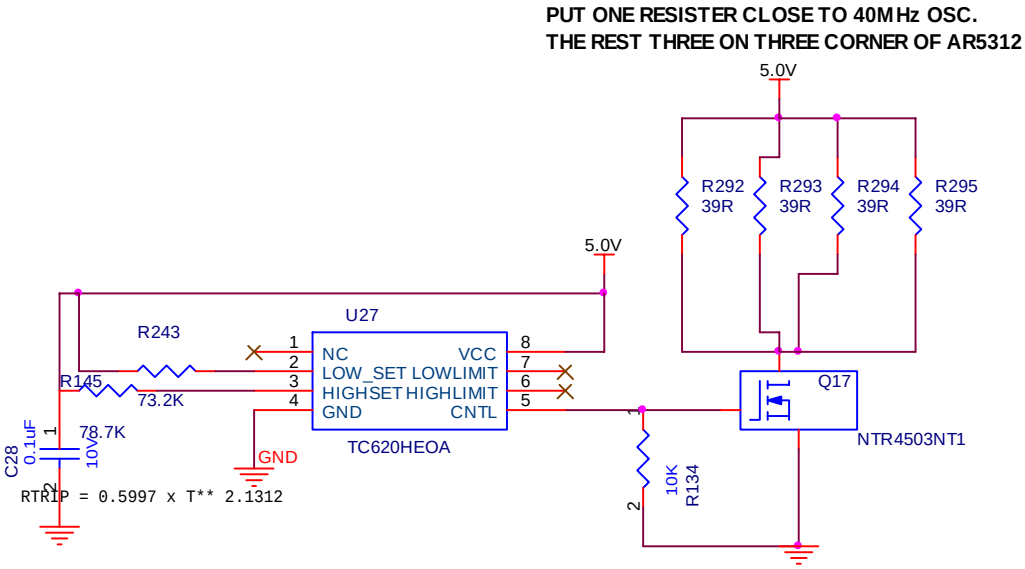
Figure 14-1. **AR5312 SDRAM Interface Timing**

4.1.4. TEMPERATURE CONTROL CIRCUIT

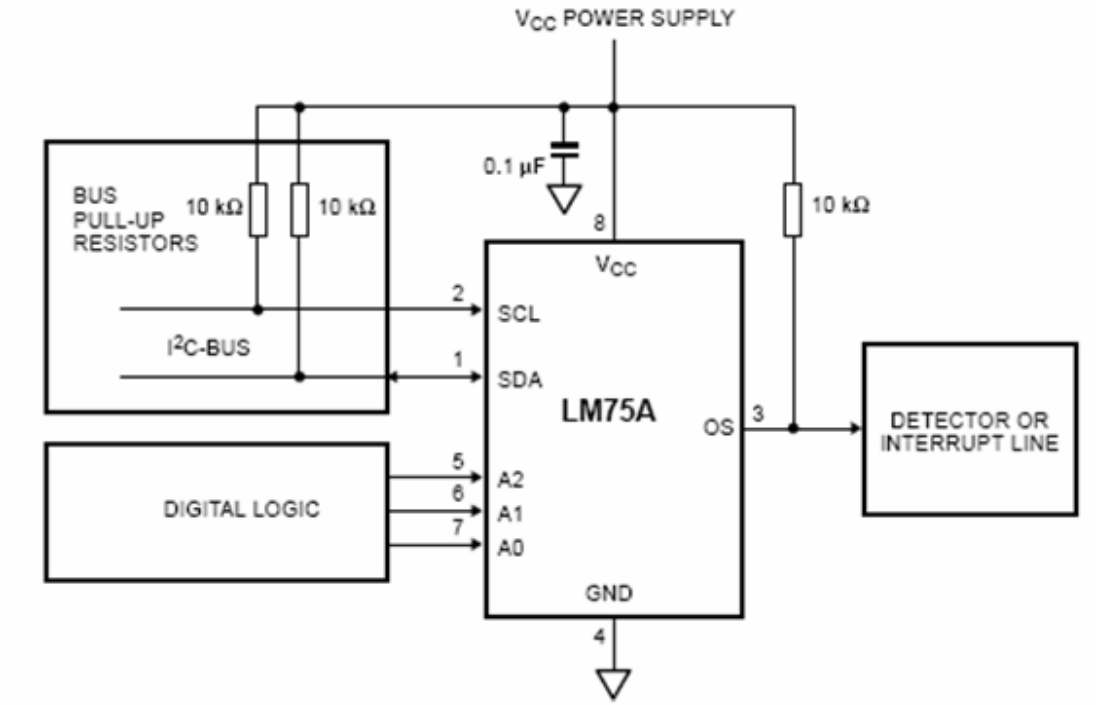
We now have two temperature control circuits,

Because we want to use the MST at -40 degrees, and the AR5312 can only works from 0 to 85 degrees. So we have to heat the AR5312 to make it work. we now use three 1 watts surface mount resistor s around the AR5312, and one 1 watt surface mount resistor besides the 40MHz crystal.

Circuit for hardware control

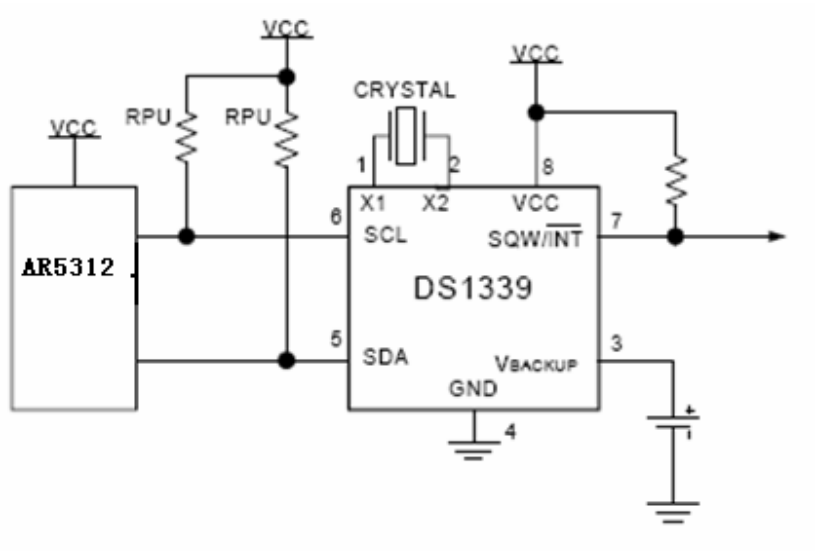


Software temperature control circuit, slave address is 1001000B



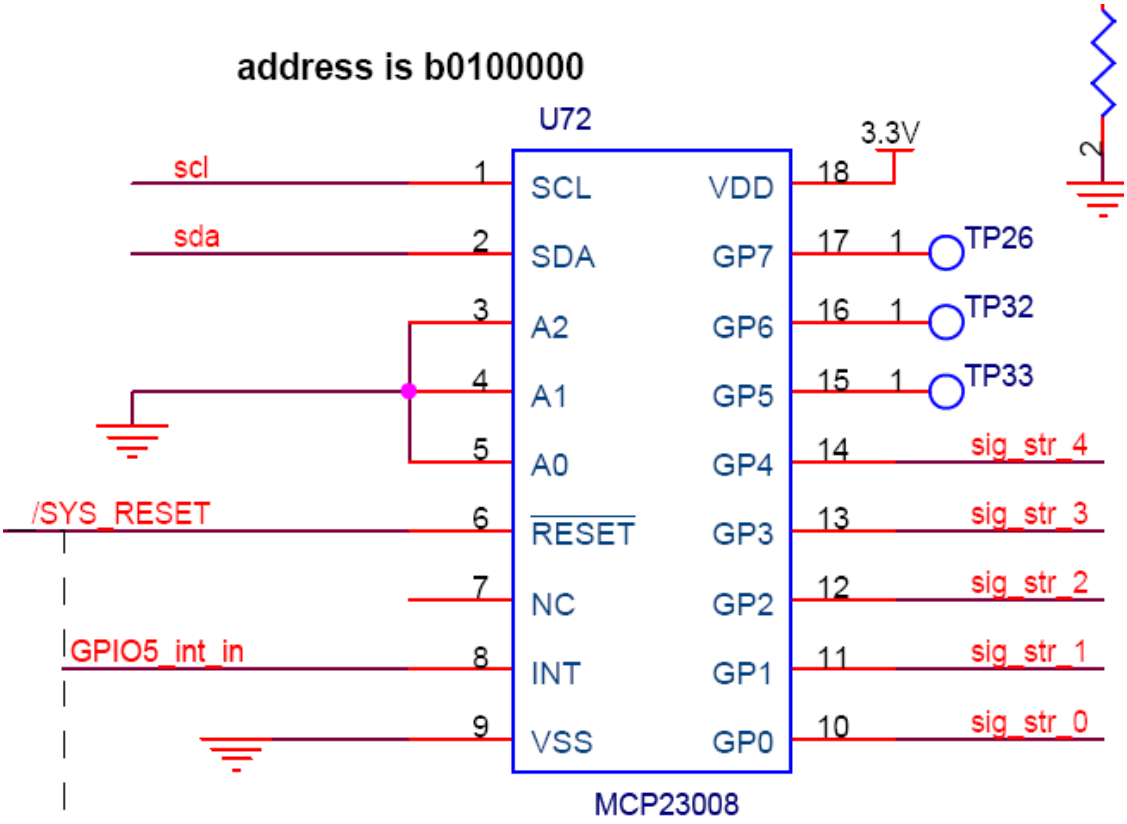
4.1.5. REAL-TIME CLOCK

The DS1339 serial real-time clock (RTC) is a low power clock/date device with two programmable time of day alarms and a programmable square-wave output. Address and data are transferred serially through an I2C bus. The clock/date provides seconds, minutes, hours, day, date, month, and year, information, slave address of this chip is 1101000B*



4.1.6. RADIO STRENGTH LED

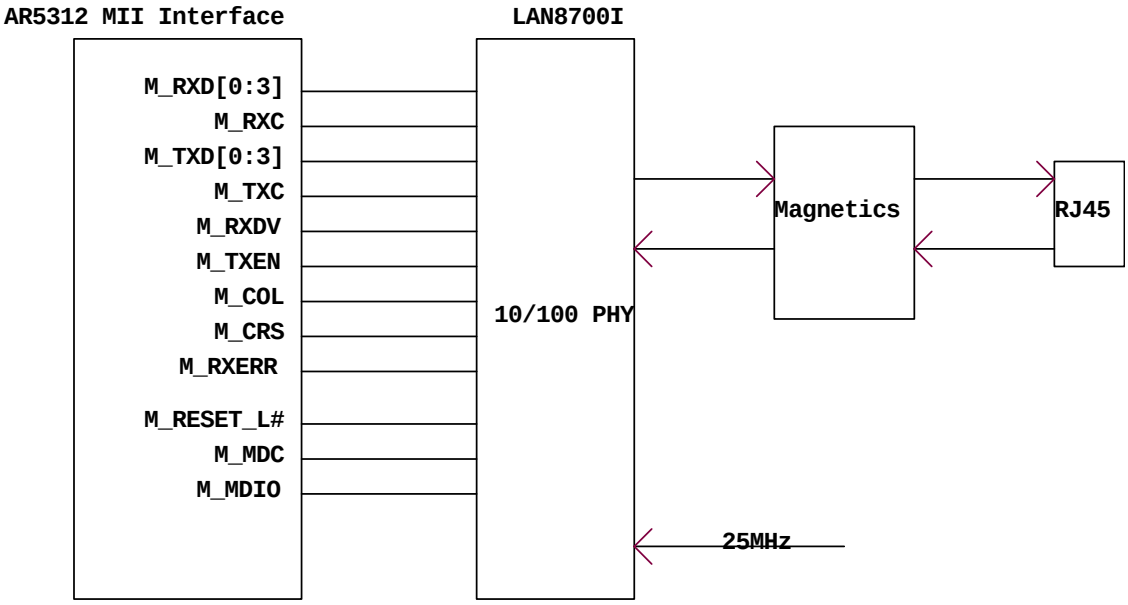
We define signal strength is from sig_str0 to sig_str4, one led is weak, and 5 led is strongest.



4.1.7.100 BASE T PHY

The Chip we use is SMSC Lan8700I, it support HP Auto-MDIX, and has ESD protection levels of IEC61000-4-2, +- 8KV contact mode, +- 15KV for air discharge mode per NTS test Facility

MII block diagram



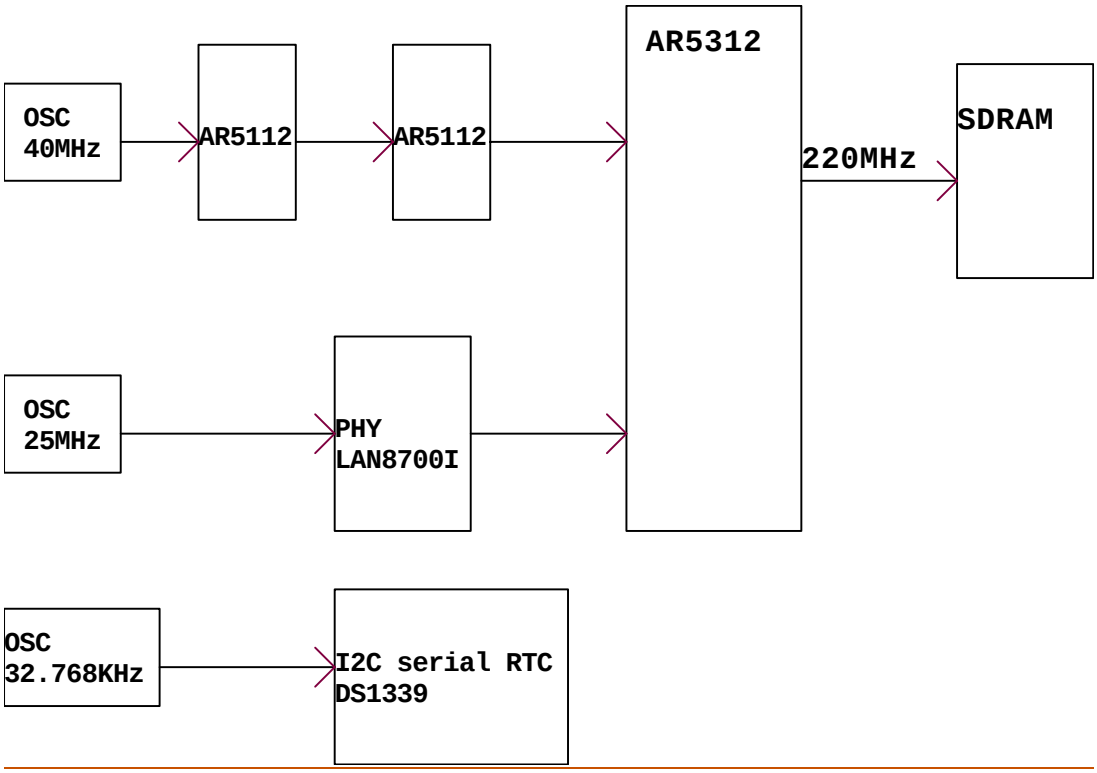
4.1.8. CLOCK

AR5312 needs a 40MHz reference clock, and Sourced by one of the twoAR5112 chips. Must be 40 MHz ± 20 ppm for correct radiooperation.

This clock is multiplied internally by the processors to 220 MHz and driven to the SDRAM interface.

The system needs the clock as following:

- *AR5112 and AR5312 are all need 40MHz reference clock, and we use one crystal for AR5112, and then the 40MHz clock pass to the other AR5112, and then to AR5312;*
- *Each Ethernet PHY needs one 25MHz reference clock;*
- *The DS1339 serial clock needs 32.768KHz clock;*



4.1.9. GPIO DEFINITIONS

- *GPIO 0 and 1 are used as I2C bus,* GPIO 0 used as I2C clock, GPIO1 used as I2C data, Use IO expander, MCP23008 to add 8 GPIOs.
- *GPIO 2, 3 and 4 are reserved ;*
- *GPIO 5 used as the 8-bit I/O expander with serial interface MCP23008's interrupt input;*
- *GPIO 6 used to recover system configuration, short time pull high reset system, long time pull high will recover system configuration.*
- *GPIO 7 used to connect with the system status LED;*

4.1.10. DEBUG INTERFACE ON THE BOARD

1. console port, is used for the serial RS232 port, and use the same port as Ethernet port, not provide for customer;
2. JTAG port, J9 is the JTAG port. Not install for final product.

4.1.11. LED INDICATE

1. RF signal strength5 segment led ,

2. Up to two Ethernet link status. D20 and D25 indicate the speed that we select, when the LED on, select 10Mbps, else off; D21 and D26 indicate the state of link, LED on is link on, else off; D24 and D27 indicate the state of carrier sense,

3. Up to two radio link status.

4. Power

System status	Eth link0	Eth link1	RADIO 0	RADIO1
STRENGTH 0	STRENGTH 1	Strength2	Strength 3	Strength 4

4.2. RF SUBSYSTEMS

Though we only use one radio in KD-921WS, we will keep the second radio as option.

For my understanding we need one a/b/g radio software configurable which use AR5112. The reference design in AP30 is only for A band, but in AP48, we can find reference design for a/b/g. we can combine the design to AP30.

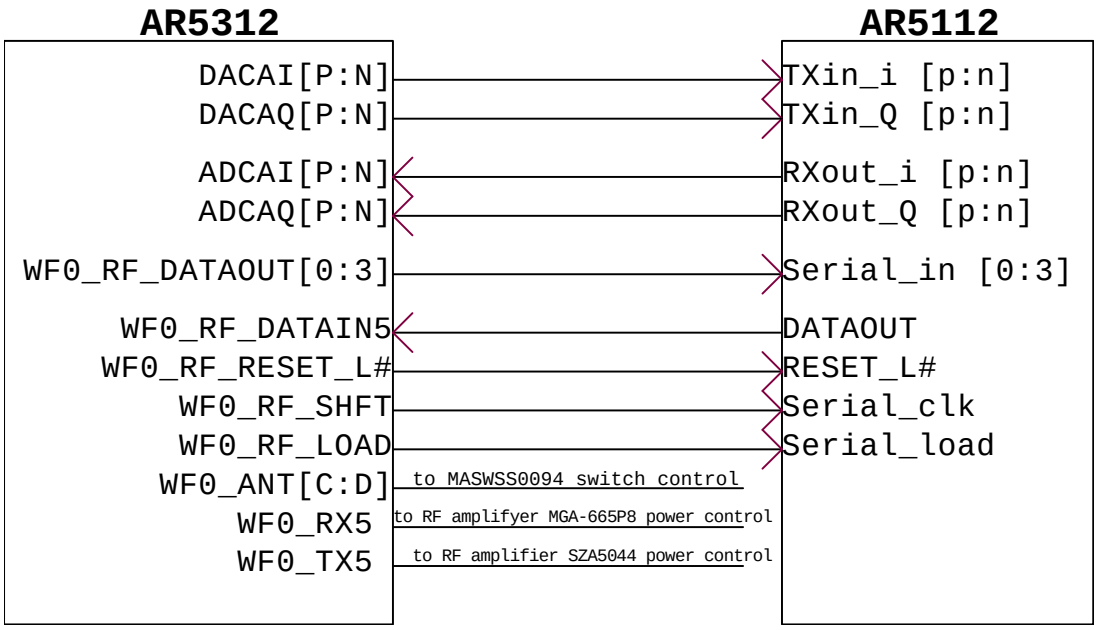
And one A radio as option.(note here AR5312 only support one 802.11 a/b/g and one 802.11a,).

For sensitivity we reference to AR5002AP_Access_Point_reference_Guide

Radio interface

AR5312 has two radio interfaces, radio interface 0 and radio interface 1, radio interface 0 is for the 802.11a; and radio interface 1 is for the 802.11a/b/g. they connect with two AR5112 respectively.

Radio interface0 to AR5112 block diagram

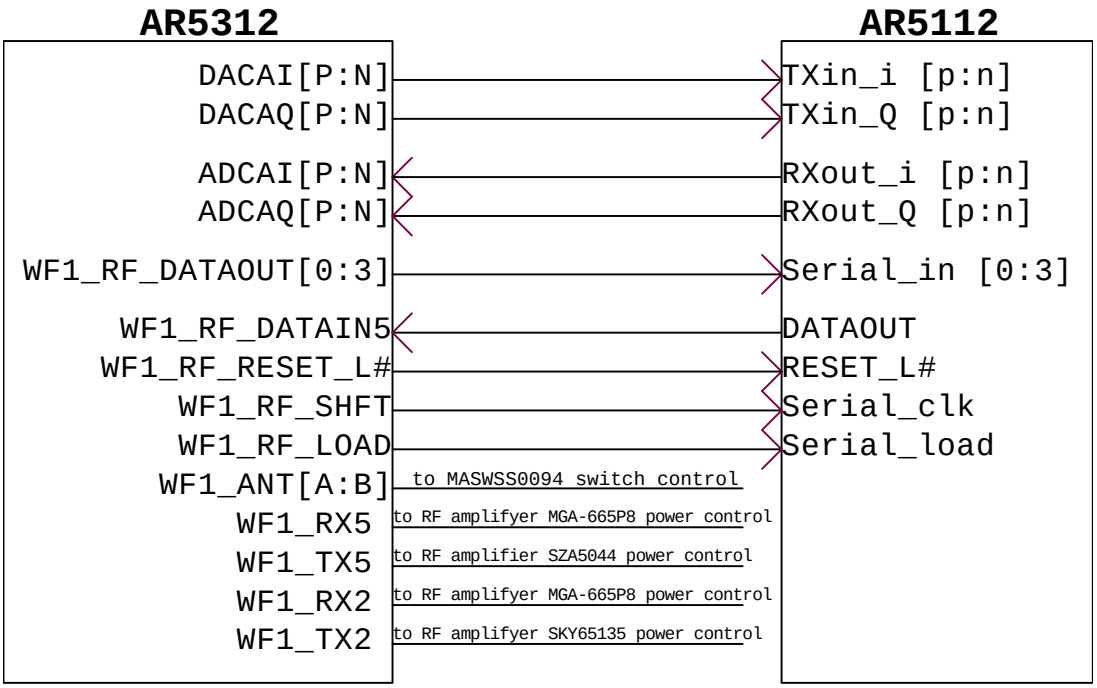


The WF0_RX5 is used to control the power down of the low noise amplifier MGA-665P8 (U77), but it is first pass through an inverter, so when WF0_RX5 is high the MGA-665P8 power down.

WF0_TX5 is used to control the power on of the 5 GHz 5V Power Amplifier SZA5044 (U75 and U76), when it is high the SZA5044 with power supply on.
WF0_ANTC and WF0_ANTD control the broadband DPDT diversity switch MASWSS0094 (S2), the function table as bellows:

Control V_C1	Control V_C2	ANT 1 - Rx	ANT 1 - Tx	ANT 2 - Tx	ANT 2 - Rx
1	0	On	Off	On	Off
0	1	Off	On	Off	On
1	1	Off	Off	Off	Off
0	0	Off	Off	Off	Off

Radio interface 1 to AR5112 block diagram



The WF1_ANTA and WF1_ANTB they are both used to control the broadband DPDT diversity switch MASWSS0094 (S3).

WF1_RX5 is used to control the power down of low noise amplifier MGA-665P8 (U80), it is first pass through an inverter and then to the MGA-665P8, so when WF1_RX5 is high the MGA-665P8 power down. So it is with WF1_RX2 (which control the U79).

WF1_TX5 is used to control the power on and power off of the SZA5044 (U74), when it is high, the power on.

WF1_TX2 is used to control the power on and off of the SKY65135 (U8), when it is high, the power on.

4.3. MECHANICAL AND ENVIRONMENTAL

We now use Plastic enclosure To save money.

within 40cm wide, 25 deep, and 15cm high, with less than 20lbs, mountain brackets should be included as well

Operating temperature range: -40° to 60°
Storage temperature range: -40° to 80°
Weather rating: IP66 weathertight

Wind survivability: > 165mph

Wind loading (165mph): < 1024 Newtons

MIL-STD-810F 509.4 Salt Fog rust resistance compliant

Shock & vibration: ETSI 300-19-2-4 spec T41.E class 4M3, this ensures us to be used in a moving train)

Transportation: ISTA 2A

5. SOFTWARE CONSIDERATION

Table 2-2. **AR5312 Address Map**

Usage	Start Address	End Address
SDRAM (Data Bank 0)	0x0000_0000	0x07FF_FFFF
SDRAM/Flash (Data Bank 1)	0x0800_0000	0x0FFF_FFFF
Flash (Data Bank 2)	0x1000_0000	0x17FF_FFFF
WLAN0 (802.11a only)	0x1800_0000	0x180F_FFFF
Ethernet 0	0x1810_0000	0x181F_FFFF
Ethernet 1	0x1820_0000	0x182F_FFFF
SDRAM Controller	0x1830_0000	0x183F_FFFF
Flash Controller	0x1840_0000	0x184F_FFFF
WLAN1 (802.11a/802.11b/802.11g)	0x1850_0000	0x185F_FFFF
Reserved	0x1860_0000	0x1BFF_FFFF
UART	0x1C00_0000	0x1C00_0FFF
Reserved	0x1C00_1000	0x1C00_1FFF
GPIO	0x1C00_2000	0x1C00_2FFF
System Control	0x1C00_3000	0x1C00_3FFF
UART/Local DMA	0x1C00_4000	0x1C00_4FFF
Local Bus	0x1C00_5000	0x1C00_5FFF
Reserved	0x1C00_6000	0x1DFF_FFFF
Flash (Data Bank 0)	0x1E00_0000	0x1EFF_FFFF
Reserved	0x1F00_0000	0x1FBF_FFFF
Flash (Data Bank 0)	0x1FC0_0000	0x1FFF_FFFF