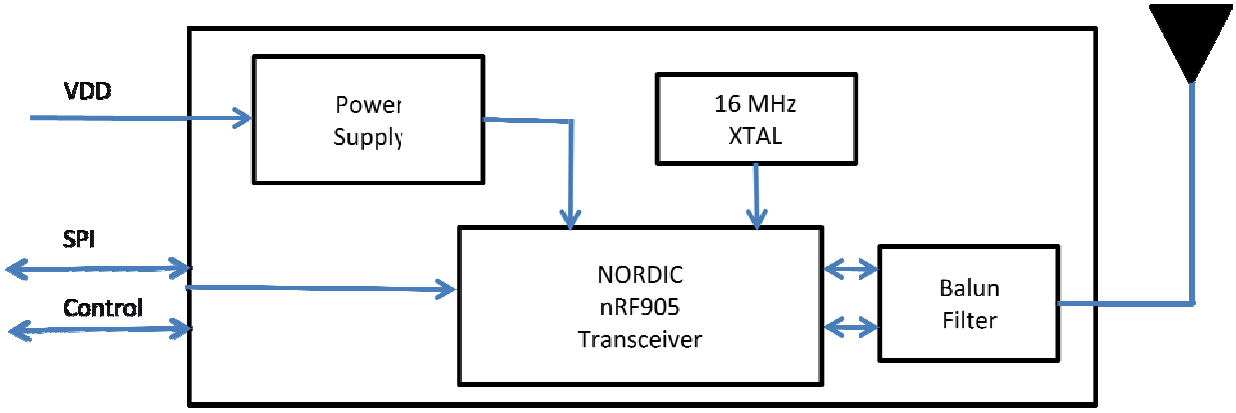
Introduction

The 300-0045 is a wireless transceiver module based on the Nordic's nRF905. The module contains all parts necessary to create a wireless link. The module contains the radio IC, power regulation and conditioning, on board oscillator, matched network, and integrated antenna. Data and control is passed to the module through a Serial Peripheral Interface (SPI). The module takes care of the 10 bit preamble, address checking, and CRC for error checking. It also Manchester encodes/decodes the data and uses Gaussian Frequency Shift Keying (GFSK) modulation. Maximum data rate is 50 kbps and maximum line of sight transmission distance is 1000'.

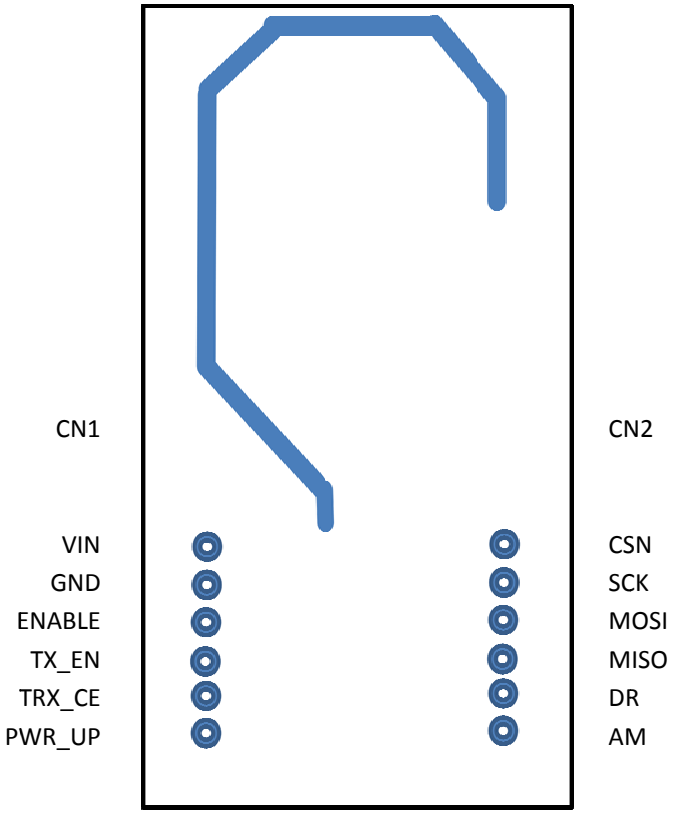
Block Diagram



Pin Function

Pin #	Name	Direction	Pin Descriptions
CN1			
1	PWR_UP	Digital input	Transceiver Power Up
2	TRX_CE	Digital input	Transmit/Receive Enable
3	TX_EN	Digital input	Transmit Enable
4	ENABLE	Digital input	Power Supply Enable
5	GND	Power	Ground
6	VIN	Power	Input Power Supply
CN2			
1	AM	Digital output	Address Match
2	DR	Digital output	Receive and transmit Data Ready
3	MISO	SPI - interface	SPI Master In Slave Out from Module to Host
4	MOSI	SPI - interface	SPI Master Out Slave In from Host to Module
5	SCK	SPI - Clock	SPI clock
6	CSN	SPI - enable	SPI enable, active low

Pin Assignment



Operation

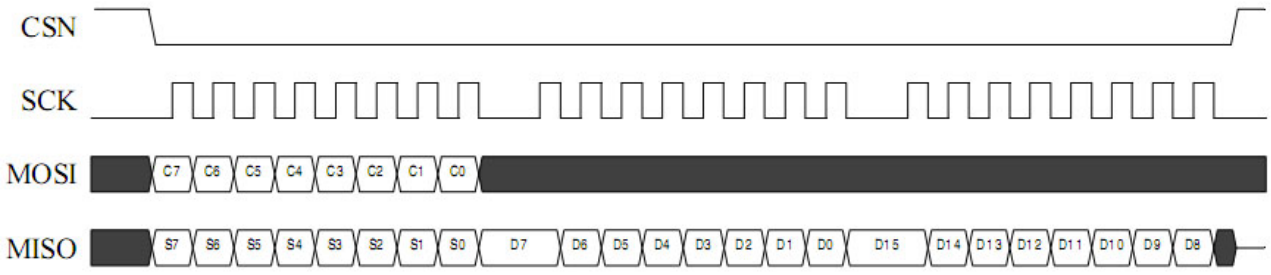
Power input

The pins VIN, GND, and ENABLE are the power supply pins of the module. The module has on board power regulation to allow a wide range of operating voltages. The module also provides and enable pin to control the power to the entire module.

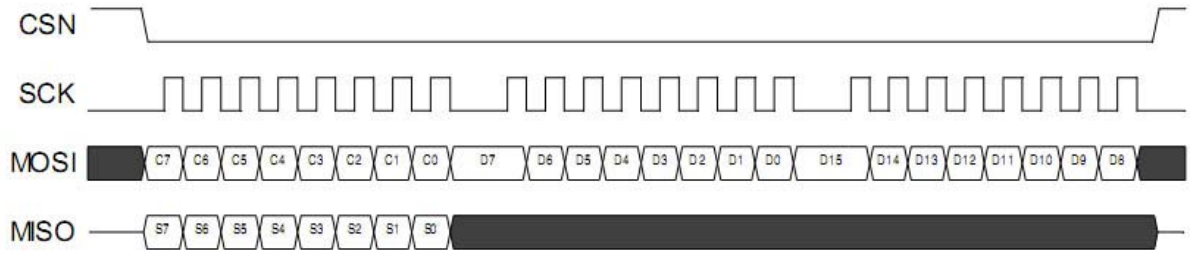
Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage	Vin	3.8	-	8	V
CE Input Voltage "H" (ON Mode)	Vih	1.5	-	Vin	V
CE Input Voltage "L" (OFF Mode)	Vil	0	-	0.25	V

Serial Peripheral Interface

Communication with the module is done through a standard serial peripheral interface (SPI). The four pins provided for this interface are MISO (Master In Slave Out), MOSI (Master Out Slave In), SCK (SPI clock), and CSN (SPI enable, active low). The module acts as a slave in the communication interface. The interface supports SPI mode 0. SPI operation and timing is given below. The device must be in one of the power saving modes for the configuration registers to be read or written to. The module provides access to the five internal registers of the nRF905 radio ic, the instruction set is used to determine what operation is performed.



SPI read operation.



SPI write operation.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Data to SCK Setup	Tdc	5		ns
SCK to Data Hold	Tdh	5		ns
CSN to Data Valid	Tcsd		45	ns
SCK to Data Valid	Tcd		45	ns
SCK Low Time	Tcl	40		ns
SCK High Time	Tch	40		ns
SCK Frequency	Tsck	DC	10	MHz
SCK Rise and Fall	Tr,Tf		100	ns
CSN to SCK Setup	Tcc	5		ns
SCK to CSN Hold	Tcch	5		ns
CSN Inactive time	Tcwh	500		ns
CSN to Output High Z	Tcdz		45	ns

SPI timing parameters (C_{load} = 10pF).

Instruction Set

The available commands to be used on the SPI interface are shown below. Whenever CSN is set low the interface expects an instruction. Every new instruction must be started by a high to low transition on CSN.

Instruction Name	Instruction Format	Operation
W_CONFIG (WC)	0000 AAAA	Write Configuration register. AAAA indicates which byte the write operation is to be started from. Number of bytes depends on the start address AAAA.
R_CONFIG (RC)	0001 AAAA	Read Configuration register. AAAA indicates which byte the read operation is to be started from. Number of bytes depends on the start address AAAA.
W_TX_PAYLOAD (WTP)	0010 0000	Write TX payload – 9 bytes
R_TX_PAYLOAD (RTP)	0010 0001	Read TX payload – 9 bytes
W_TX_ADDRESS(WTA)	0010 0010	Write TX address – 4 bytes
R_TX_ADDRESS(RTA)	0010 0011	Read TX address – 4 bytes
R_RX_PAYLOAD(RRP)	0010 0100	Read RX payload – 9 bytes
CHANNEL_CONFIG (CC)	1000 pphc cccc cccc	Special command for fast setting of CH_NO, HFREQ_PLL, and PA_PWR in the Configuration register. CH_NO=ccccccccc, HFREQ_PLL = h, PA_PWR = pp

Internal Registers

The five internal registers that the module provides access to are as follows:

Status Register (Read-only)

Contains status of data ready (DR) and address match (AM)

Byte #	Content bit [7:0], MSB = bit[7]	Init value
0	AM, bit [6] not used, DR, bit [0:4] not used	X

RF Configuration Register (Read/Write)

Contains transceiver setup information such as frequency and output power.

Byte #	Content bit [7:0], MSB = bit[7]	Init value
0	CH_NO[7:0]	0110_1100
1	bit[7:6] not used, AUTO_RETRAN, RX_RED_PWR, PA_PWR[1:0], HFREQ_PLL, CH_NO[8]	0000_0000
2	bit[7] not used, TX_AFW[2:0] , bit[3] not used, RX_AFW[2:0]	0100_0100
3	bit[7:6] not used, RX_PW[5:0]	0010_0000
4	bit[7:6] not used, TX_PW[5:0]	0010_0000
5	RX_ADDRESS (device identity) byte 0	1110_0111
6	RX_ADDRESS (device identity) byte 1	1110_0111
7	RX_ADDRESS (device identity) byte 2	1110_0111
8	RX_ADDRESS (device identity) byte 3	1110_0111
9	CRC_MODE,CRC_EN, XOF[2:0], UP_CLK_EN, UP_CLK_FREQ[1:0]	1110_0111

TX Address (Read/Write)

Contains address of target device. This module uses a 32 bit address.

Byte #	Content bit [7:0], MSB = bit[7]	Init value
0	TX_ADDRESS[7:0]	1110_0111
1	TX_ADDRESS[15:8]	1110_0111
2	TX_ADDRESS[23:16]	1110_0111
3	TX_ADDRESS[31:24]	1110_0111

TX Payload (Read/Write)

Register containing the payload information to sent in a data packet. This module uses 9 byte long data packets.

Byte #	Content bit [7:0], MSB = bit[7]	Init value
0	TX_PAYLOAD[7:0]	-
1	TX_PAYLOAD[15:8]	-
2	TX_PAYLOAD[23:16]	-
3	TX_PAYLOAD[31:24]	-
4	TX_PAYLOAD[39:32]	-
5	TX_PAYLOAD[47:40]	-
6	TX_PAYLOAD[55:48]	-
7	TX_PAYLOAD[63:56]	-
8	TX_PAYLOAD[71:64]	-

RX Payload (Read-only)

Contains the payload information derived from a received valid data packet. This module uses 9 byte long data packets. Valid received data is indicated with a high data ready (DR) and address match (AM) signal.

Byte #	Content bit [7:0], MSB = bit[7]	Init value
0	RX_PAYLOAD[7:0]	-
1	RX_PAYLOAD[15:8]	-
2	RX_PAYLOAD[23:16]	-
3	RX_PAYLOAD[31:24]	-
4	RX_PAYLOAD[39:32]	-
5	RX_PAYLOAD[47:40]	-
6	RX_PAYLOAD[55:48]	-
7	RX_PAYLOAD[63:56]	-
8	RX_PAYLOAD[71:64]	-

Power up

The power up pin is used to enable/disable the nRF905 chip and is active high. The chip consumes a minimal amount of current in power down mode (PWR_UP = 0) but still retains the configuration word content. SPI programming is still active in power down mode.

TRX_CE

This pin enables the radio portion of the module and is active high. The module will only transmit or receive data if TRX_CE is high. The device enters standby mode if TRX_CE is pulled low. This is a low current consumption mode and retains the data in the configuration registers. While the current consumption is greater than in power down mode, the startup time for transmission is less. It is recommended to do SPI communications in either power down or standby mode.

TX_EN

The TX_EN pin is used to switch the module between transmit and receive mode. When TX_EN is high the module is placed in transmit mode. If TX_EN is pulled low, the module is in receive mode. Note that the status of the power up and TRX_CE pins over ride the functionality of the TX_EN pin. The radio must be active before and radio communications will take place.

NOTE: The minimum voltage required for a high reading on the power up, TRX_CE, and TX_EN pins is 2.4 volts and the maximum allowed voltage on the pins is 3.3 volts.

PWR_UP	TRX_CE	TX_EN	Operating Mode
0	X	X	Power down and SPI programming
1	0	X	Standby and SPI programming
1	X	0	Read data from RX register
1	1	0	Radio enabled – Receive mode
1	1	1	Radio enabled – Transmit mode

Address Match (AM)

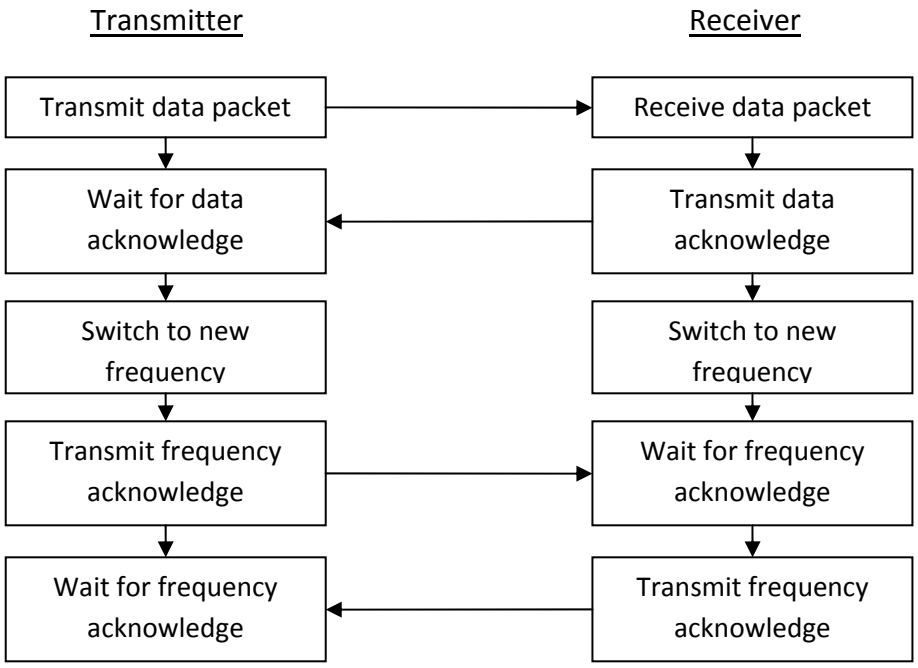
When the module is in receive mode, the Address Match (AM) pin is set high as soon as an incoming packet with an address that is identical with the device's own identity is received. With the Address Match pin the controller is alerted that the module is receiving data actually before the Data Ready (DR) signal is set high. If the Data Ready (DR) pin is not set high i.e. the CRC is incorrect then the Address Match (AM) pin is reset to low at the end of the received data packet. This function can be very useful for an MCU. If Address Match (AM) is high then the MCU can make a decision to wait and see if Data Ready (DR) will be set high indicating a valid data packet has been received or ignore that a possible packet is being received and switch modes.

Data Ready (DR)

The Data Ready (DR) signal makes it possible to largely reduce the complexity of the MCU software program. In transmit mode, the Data Ready (DR) signal is set high when a complete packet is transmitted, telling the MCU that the module is ready for new actions. It is reset to low at the start of a new packet transmission or when switched to a different mode i.e. receive mode or standby mode. In receive mode, the signal is set high when module has received a valid packet, i.e. a valid address, packet length and correct CRC. The MCU can then retrieve the payload via the SPI interface. The Data Ready (DR) pin is reset to low once the data has been clocked out of the data buffer or the device is switched to transmit mode.

Protocol

A frequency hopping protocol is used with this module. It uses 50 frequencies that are pseudo-randomly selected on the master side. On air time for one data packet is approximately 3 milliseconds. The data packet consists of a preamble, destination address, transmitted data, next frequency in the hopping sequence, and the CRC. The protocol incorporates a one to many "star" network. This means that there is one master that can communicate with many slaves. The master can communicate with each slave individually. The master always initiates a data transmission and controls the hopping sequence. When a data packet is sent, the master sends the data along with the next frequency in the hopping frequency (generated through a random number function) and error checking information. When the slave receives the packet, it sends back an acknowledge packet to the master and then hops to the next frequency in the sequence. When the master receives the acknowledge packet from the slave it hops to the next frequency in the sequence and sends out a new acknowledge packet. Once the slave receives the packet on the new frequency, it sends an acknowledge packet back to the master and the data transmission is considered complete. The master will resend the packet on the same frequency if the acknowledge is not received in 12 milliseconds. If an acknowledge packet is not received on the second try, the master will send out the data packet on the other 50 frequencies used until an acknowledge packet is returned. The master randomly selects a frequency to try until all 50 frequencies have been tried. This is an error recovery mode in case the master and slave become unsynchronized. If there is still no response after all frequencies have been tried, the master ends communication attempts with slave until the next request is made. The following illustration shows the communication sequence.


Transmitter
Receiver
Transmit data packet
Receive data packet
Wait for data acknowledge
Transmit data acknowledge
Switch to new frequency
Switch to new frequency
Transmit frequency acknowledge
Wait for frequency acknowledge
Wait for frequency acknowledge
Transmit frequency acknowledge

FCC Requirements

As this is a module that will be included inside an end product, the end product must have an external label that states "Contains Transmitter Module FCC ID: XNJ-01."

This module is only designed to be used with the integrated copper trace antenna. Changes or modifications to this antenna will void the user's authority to operate this device.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.