SC680A&SC682A&SC686A Series

Hardware Design

Smart Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal

powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-09-09	Rorschach GUO/ Xiong XIAO	Creation of the document
1.0	2023-02-24	Rorschach GUO/ Xiong XIAO/ Alyssa WU	First official release
1.1	2023-09-25	Lucian HUANG/ Cary YANG/ Alyssa WU	1. Added the variant SC680A-JP (Table 2, Table 3, Table 38, Table 41, Table 44, Table 59). 2. Added the 33 pF capacitors on HPH_L and HPH_R (Figure 23). 3. Updated the resistance of R2 from 20K to 0R (Figure 23). 4. Updated the content of analog audio interfaces design considerations (Chapter 4.9.5). 5. Updated the memory configuration (Chapter 2.2).
1.2	2024-03-04	Lucian HUANG/ Today JIN	1. Updated the memory of SC680A and SC686A series (Table 4). 2. Updated ELDO1_1V8 to ELDO3_1V8 (Figure 9). 3. Deleted GNSS L5 and NavIC, and added SBAS (Table 3, Table 4 and Chapter 5.2). 4. Updated Wi-Fi output power and sensitivity (Table 50 and Table 51). 5. Added the note about the prohibition of mercury-containing materials (Chapter 8.2).
1.3.0	2025-01-13	Ryan LIU/ Alvin JIANG/ Eren FAN/ Eric MO/ Alyssa WU/ Robinson SHEN	Preliminary 1. Added applicable module series SC682A series. 2. Added data update rate (Table 4). 3. Updated reference circuit for RF antenna interface and added relevant notes (Chapter

	5.1.4, Chapter 5.2.3, Chapter 5.3.3). 4. Updated GLONASS frequency to 1601.7 ±4.2 (Table 53). 5. Updated the module's coplanarity standard (Chapter 7.1). 6. Added a note on IMEI code (Chapter 7.3). 7. Updated the pre-baking time to 24 h (Chapter 8.1). 8. Added a note prohibiting storage or use of unprotected modules in environments containing corrosive gases (Chapter 8.2).

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1 Introduction

This document defines SC680A, SC682A and SC686A series modules and describes their air and hardware interfaces which are connected with your applications.

With this document, you can quickly understand the interface specifications, electrical and mechanical details, as well as other related information of the modules. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the modules.

NOTE

For conciseness purposes, SC680A, SC682A and SC686A series modules will hereinafter be referred to collectively as “the module/modules” in parts hereof applicable to both three module series, and individually as “SC680A series”, “SC682A series” and “SC686A series” in parts hereof referring to the differences between the three of them.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

SC680A, SC682A and SC686A series are smart LTE modules providing industrial-grade performance. SC680A and SC682A series are based on Android while SC686A series is based on Linux. The module supports multiple audio and video codecs, built-in high performance Adreno™ 610 GPU and multiple audio and video input/output interfaces as well as abundant GPIO interfaces. With these, the module is engineered to meet the demanding requirements in M2M applications. Its general features are listed below:

Table 2: Brief Introduction

SC680A & SC682A & SC686A Series	
Packaging types and pin counts	152 LCC pins + 171 LGA pins
Dimensions (mm)	(43.0 ±0.15) × (44.0 ±0.15) × (2.85 ±0.2)
Weight	**SC680A&SC686A Series:** Approx. 11.8 g **SC682A Series:** TBD
Models	**SC680A Series:** SC680A-NA, SC680A-EM, SC680A-JP and SC680A-WF **SC686A Series:** SC686A-NA, SC686A-EM and SC686A-WF **SC682A Series:** SC682A-NA, SC682A-EM, SC682A-JP and SC682A-WF

2.1. Frequency Bands and Functions

Table 3: Wireless Network Type

Wireless Network Type	SC680A-NA& SC682A-NA& SC686A-NA	SC680A-EM& SC682A-EM& SC686A-EM	SC680A-JP& SC682A-JP	SC680A-WF& SC682A-WF& SC686A-WF
LTE-FDD	B2/B4/B5/B7/B12/ B13/B14/B17/B25/ B26/B66/B71	B1/B2/B3/B4/B5/B7/ B8/B20/B28	B1/B3/B5/B8/B11/ B18/B19/B21/B26/ B28	-
LTE-TDD	B41	B38/B40/B41	B41	-
Intra-band 2 x CA (DL)	**SC680A-NA& SC686A-NA:** 2A-2A, 2C, 4A-4A, 5A-5A, 5B, 7A-7A, 7C, 25A-25A, 66A-66A, 66B, 66C, 41A-41A, 41C	**SC680A-EM& SC686A-EM:** 1A-1A, 1C, 2A-2A, 2C, 3A-3A, 3C, 4A-4A, 5A-5A, 5B, 7A-7A, 7B, 7C, 38C, 40A-40A, 40C, 41A-41A, 41C	**SC680A-JP:** 1A-1A, 1C, 3A-3A, 3C, 5A-5A, 5B, 41A-41A, 41C	-
WCDMA	-	B1/B2/B4/B5/B8	**SC680A-JP:** B1/B6/B8/B19	-
GSM	-	GSM850/EGSM900 /DCS1800/PCS190 0	-	-
GNSS (Optional)	GPS/GLONASS/ BDS/Galileo/ SBAS/QZSS	GPS/GLONASS/ BDS/Galileo/ SBAS/QZSS	GPS/GLONASS/ BDS/Galileo/ SBAS/QZSS	-
Wi-Fi 802.11 a/b/g/n/ac	2400-2483.5 MHz 5150-5850 MHz	2400-2483.5MHz 5150-5850 MHz	2400-2483.5MHz 5150-5850 MHz	2400-2483.5 MHz 5150-5850 MHz
Bluetooth 5.0/5.1	2402–2480 MHz	2402–2480 MHz	2402–2480 MHz	2402–2480 MHz

2.2. Key Features

Table 4: Key Features

Features	Details
Application Processor	● 64-bit ARM v8.0 compliant application processor ● Kryo Gold: quad high-performance cores 2.0 GHz with 1 MB L2 cache ● Kryo Silver: quad low-power cores 1.8 GHz with 512 KB L2 cache
Modem DSP	**SC680A&SC686A Series:** Hexagon DSP, dual-HVX at 1.0 GHz **SC682A Series:** Hexagon DSP, dual-HVX 512
GPU	Adreno™ GPU 610 at 950 MHz with 64-bit addressing
Memory	**SC680A Series:** ● 4 GB + 64 GB (LPDDR4X uMCP, Default) ● 3 GB + 32 GB (LPDDR4X eMCP, Optional) **SC686A Series:** ● 2 GB + 16 GB (LPDDR4X eMCP, Default) ● 3 GB + 32 GB LPDDR4X eMCP, Optional) **SC682A Series:** ● 3 GB + 32 GB (Discrete LPDDR4X EMMC, Default)
Operating System	**SC680A Series:** Android 12/13/14 **SC686A Series:** Linux **SC682A Series:** Android 13/14*/15*
Power Supply	● Supply voltage: 3.55–4.4 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
USB Interface	● Compliant with USB 3.1 Gen 1 and USB 2.0 specifications, with transmission rates up to 5 Gbps on USB 3.1 Gen 1 and 480 Mbps on USB 2.0 ● Supports USB OTG ● Used for AT command communication, data transmission, software debugging, firmware upgrade.
(U)SIM Interfaces	● Two (U)SIM interfaces ● Support USIM/SIM card: 1.8/2.95 V ● Support Dual SIM Dual Standby (supported by default)
SPI	Support up to three SPIs. One of them is default configuration and two of them are multiplexed from other interfaces

	● The default SPI supports master mode only ● For details about two SPIs that can be multiplexed from other interfaces, see ***Table 19*** ● 1.8 V operation voltage with clock rates up to 50 MHz
UART Interfaces [1]	Support up to four UART interfaces. Two of them are default configurations and two of them are multiplexed from other interfaces ● Default UART interfaces: UART5 and Debug UART – UART5: 4-wire UART interface, supports RTS and CTS hardware flow control, up to 115200 bps – Debug UART: 2-wire UART interface, dedicated for debugging, including Linux console and log output, up to 115200 bps ● For details about two UART interfaces that can be multiplexed from other interfaces, see ***Table 19***
I2C Interfaces	Support up to seven I2C interfaces ● Four of them are dedicated I2C interfaces, used for camera, TP and sensor peripherals ● One of them is generic I2C interface ● For details about two I2C interfaces that can be multiplexed from other interfaces, see ***Table 19*** ● Comply with *I2C-bus specification version 3.0* ● Multi-master mode is not supported
I2S Interfaces	Support up to two I2S interfaces that can be multiplexed from other interfaces, see ***Table 20***
Analog Audio Interfaces	**Audio Inputs:** 3 analog microphone inputs, MIC1 and MIC2 integrated with internal bias voltage **Audio Outputs:** ● Class AB stereo headphone output ● Class AB earpiece differential output ● Class K speaker differential amplifier output
Audio Codec	● EVS, EVRC, EVRC-B, EVRC-WB ● G.711 and G.729A/AB ● GSM-FR, GSM-EFR, and GSM-HR ● AMR-NB, AMR-WB
ADC Interfaces	2 generic ADC interfaces
SD Card Interface	● Supports SD 3.0 protocol ● Supports SD card hot-plug ● Supports 1.8/2.95 V SD card
LCM Interface	● Supports one 4-lane MIPI DSI, up to 1.5 Gbps/lane ● Supports FHD + (2520 × 1080) @ 60 fps
Video Codec	● Video encoding: 1080p @ 60 fps 8-bit HEVC (H.265); 1080p @ 60 fps 8-bit H.264

[1] For details about the multiplexing and conflict relationships of UART, I2C and SPI interfaces, see ***Table 19.***

	● Video decoding: 1080p @ 60 fps 8-bit H.264; 1080p @ 60 fps 8-bit HEVC (H.265), VP9 ● Encoding + decoding: 1080p @ 30 fps + 1080p @ 30 fps
Camera Interfaces	● Support three 4-lane MIPI CSI, up to 2.5 Gbps/lane ● Support 3 cameras (4-lane + 4-lane + 4-lane) or 4 cameras (4-lane + 4-lane + 2-lane + 1-lane) ● Triple-ISP: (13 MP + 13 MP) @ 30 fps, (25 MP + 5 MP) @ 30 fps or (16 MP + 16 MP) @ 24 fps ● Support up to 3 concurrently working cameras
Real Time Clock	Supported
WLAN Features	● 2.4 GHz and 5 GHz, supports 802.11 a/b/g/n/ac, up to 433 Mbps ● Supports AP and STA modes
Bluetooth Features	**SC680A&SC682A Series:** ● *Bluetooth Core Specification Version 5.1* **SC686A Series:** ● *Bluetooth Core Specification Version 5.0* ● Bluetooth Classic & Bluetooth Low Energy (BLE)
GNSS Features [2] (Optional)	● GPS/GLONASS/BDS/Galileo/SBAS/QZSS ● L1 ● Data update rate:1 Hz ● Support AGNSS.
Antenna Interfaces	● Main antenna interface ● Diversity antenna interface ● Wi-Fi & Bluetooth antenna interface[3] ● GNSS antenna interface (optional)
LTE Features	● Supports Rel-10 Cat 6 [4] for FDD and TDD ● Supports 1.4 MHz, 3 MHz, 5 MHz, 10 MHz, 15 MHz, 20 MHz, RF bandwidth ● Supports Multi-user MIMO in DL direction ● Uplink modulations: QPSK, 16QAM ● Downlink modulations: QPSK, 16QAM and 64QAM ● LTE-FDD max. data rates: **SC680A&SC686A Series:** 300 Mbps (DL)/50 Mbps (UL) **SC682A Series:** 150 Mbps (DL)/50 Mbps (UL) ● LTE-TDD max. data rates: **SC680A&SC686A Series:** 265 Mbps (DL)/30 Mbps (UL) **SC682A Series:** 130 Mbps (DL)/30 Mbps (UL)

[2] SC680A-WF, SC682A-WF and SC686A-WF do not support GNSS.
[3] SC680A-WF, SC682A-WF and SC686A-WF only support Wi-Fi & Bluetooth antenna interface.
[4] SC682A series supports Rel-10 Cat 4 for FDD and TDD.

UMTS Features	● Supports 3GPP Rel-9 DC-HSDPA/HSPA+/HSDPA/HSUPA/WCDMA ● Uplink modulation: 16QAM ● Downlink modulations: QPSK, 16QAM and 64QAM ● DC-HSDPA max. data rate: 42 Mbps (DL) ● HSUPA max. data rate: 5.76 Mbps (UL) ● WCDMA max. data rates: 384 kbps (DL)/384 kbps (UL)
GSM Features	**R99:** ● CSD transmit speed rate: 9.6 kbps, 14.4 kbps **GPRS:** ● Supports GPRS multi-slot class 33 (33 by default) ● Coding scheme: CS 1–4 ● Max. data rates 107 kbps (DL)/85.6 kbps (UL) **EDGE:** ● Supports EDGE multi-slot class 33 (33 by default) ● Supports GMSK and 8-PSK for different MCS ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. data rates: 296 kbps (DL)/236.8 kbps (UL)
Temperature Range	● Operating temperature range [5]: -35 to +75 °C ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	● USB interface ● OTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Pin Description

The following table shows the DC characteristics and pin descriptions.

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input

[5] Within the operating temperature range, the module meets 3GPP specifications.

DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PIO	Power Input/Output
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	36, 37, 38	PIO	Power supply for the module	Vmax = 4.4 V Vmin = 3.55 V Vnom = 3.8 V	It must be provided with sufficient current up to 3.0 A. It is suggested to use a TVS to increase voltage surge withstand capability.
LDO9A_1V8	9	PO	1.8 V output power for external GPIO's pull up circuits and level-shifting circuits.	Vnom = 1.8 V $I_O$max = 20 mA	Cannot be used for peripheral power supply. No external capacitor is required.
ELDO3_1V8	10	PO	1.8 V output power for I/O VDD of cameras, LCDs, TP and sensors.	Vnom = 1.8 V $I_O$max = 300 mA	Add a 1.0–2.2 µF bypass capacitor if used. If unused, keep this pin unconnected. Maximum external capacitance must not exceed 9 µF. Internally controlled by GPIO_56.
ELDO1_2V8	11	PO	2.8 V output power for	Vnom = 2.8 V $I_O$max = 300 mA	Add a 1.0–4.7 µF bypass capacitor if

			VDD of sensors and TPs.		used. If unused, keep this pin unconnected. Maximum external capacitance must not exceed 9 μF. Internally controlled by GPIO_54 and GPIO_55.
ELDO2_2V85 or ELDO2_2V8 [6]	12	PO	Output power for cameras and LCDs.	**SC680A&SC686A Series:** Vnom = 2.85 V $I_O$max = 300 mA **SC682A Series:** Vnom = 2.8 V $I_O$max = 300 mA	Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin unconnected. Maximum external capacitance must not exceed 9 μF. Internally controlled by GPIO_31.
LDO2C_1V1	13	PO	1.1 V output power for DVDD of rear camera.	Vnom = 1.1 V $I_O$max = 800 mA	Add a 1.0–2.2 μF bypass capacitor if used. If unused, keep this pin unconnected. Maximum external capacitance must not exceed 15.3 μF.
LDO3C_2V8	14	PO	2.8 V output power for AVDD of camera.	Vnom = 2.8 V $I_O$max = 300 mA	Add a 1.0–2.2 μF bypass capacitor if used. If unused, keep this pin unconnected. Maximum external capacitance must not exceed 47.8 μF.
LDO1C_1V2	15	PO	1.2 V output power for DVDD of front camera.	Vnom = 1.2 V $I_O$max = 800 mA	Add a 1.0–2.2 μF bypass capacitor if used. If unused, keep this pin unconnected. Maximum external capacitance must not exceed 15.3 μF.

[6] Pin 12 is defined as ELDO2_2V85 for SC680A&SC686A series, while as ELDO2_2V8 for SC682A series.

VPH_PWR	220, 221	PO	Power supply for peripherals	Vnom = VBAT $I_O$max = 1000 mA	It can provide a maximum continuous current of 1 A.
VRTC	16	PIO	Power supply for RTC	Vmin = 2.0 V Vnom = 3.0 V Vmax = 3.25 V	
GND	3, 4, 18, 20, 31, 34, 35, 40, 43, 47, 56, 62, 87, 98, 101, 112, 125, 128, 130, 133, 135, 148, 150, 154, 157, 159, 160, 163, 166, 170, 173, 176, 182, 193, 195, 219, 225, 243, 257–323				
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_BIAS	167	AO	Bias voltage output for microphone	Vmin = 1.0 V Vmax = 2.85 V	
MIC1_P	44	AI	Microphone input for channel 1 (+)		Integrated with internal bias voltage.
MIC1_M	45	AI	Microphone input for channel 1 (-)		
MIC_GND	168		Microphone reference ground		If unused, connect this pin to ground.
MIC2_P	46	AI	Microphone input for headset (+)		Integrated with internal bias voltage.
MIC3_P	169	AI	Microphone input for channel 2 (+)		No internal bias voltage is integrated.
EAR_P	53	AO	Earpiece output (+)		
EAR_M	52	AO	Earpiece output (-)		
SPK_P	55	AO	Speaker output (+)		
SPK_M	54	AO	Speaker output (-)		
HPH_R	51	AO	Headphone right channel output		
HPH_L	49	AO	Headphone left channel		

			output		
HPH_GND	50		Headphone reference ground		It should be connected to main ground.
HS_DET	48	AI	Headset hot-plug detect		Pulled up internally.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	41, 42	PIO	Charging power input. Power supply for OTG device. USB/adapter insertion detection.	Vmax = 10.0 V Vmin = 4.0 V	Test points must be reserved.
USB_DM	33	AIO	USB 2.0 differential data (-)		Test points must be reserved. 90 Ω differential impedance.
USB_DP	32	AIO	USB 2.0 differential data (+)		
USB_SS1_RX_P	171	AI	USB 3.1 Channel 1 super-speed receive (+)		90 Ω differential impedance. USB 3.1 Gen 1 standard compliant.
USB_SS1_RX_M	172	AI	USB 3.1 Channel 1 super-speed receive (-)		
USB_SS1_TX_P	174	AO	USB 3.1 Channel 1 super-speed transmit (+)		
USB_SS1_TX_M	175	AO	USB 3.1 Channel 1 super-speed transmit (-)		
USB_SS2_RX_P	156	AI	USB 3.1		

			Channel 2 super-speed receive (+)		
USB_SS2_RX_M	155	AI	USB 3.1 Channel 2 super-speed receive (-)		
USB_SS2_TX_P	165	AO	USB 3.1 Channel 2 super-speed transmit (+)		
USB_SS2_TX_M	164	AO	USB 3.1 Channel 2 super-speed transmit (-)		
UUSB_TYPEC	217	AI	uUSB & USB Type-C configuration		If Micro USB is intended to be used, this pin should be connected to ground via a 1 kΩ resistor. If USB Type-C is intended to be used, this pin should be left unconnected.
USB_CC1	224	AI	USB Type-C configuration channel 1		
USB_CC2	223	AI	USB Type-C configuration channel 2		
USB_SS_SEL	226	DO	USB Type-C switch control		
SS_DIR_IN	212	DI	Configuration channel status detect	1.8 V	When using Micro USB, connect it to ground with a 7.32 kΩ resistor. When using USB Type-C, connect the pin to SS_DIR_OUT.
SS_DIR_OUT	213	AO	Configuration channel		When using Micro USB, keep this pin

			status output		unconnected. When using USB Type-C, connect the pin to SS_DIR_IN.
USB_ID	30	AI	USB ID detect		High level by default.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	141	PO	(U)SIM1 card power supply	1.8/2.95 V	Either 1.8 V or 2.95 V (U)SIM card is supported. The total capacity of the external capacitor(s) cannot exceed 2.2 μF.
USIM1_DATA	142	DIO	(U)SIM1 card data		Externally pulled up to USIM1_VDD with a 10 kΩ resistor.
USIM1_CLK	143	DO	(U)SIM1 card clock		
USIM1_RST	144	DO	(U)SIM1 card reset		
USIM1_DET	145	DI	(U)SIM1 card hot-plug detect	1.8 V	Active low. Require external pull-up to 1.8 V. If unused, keep this pin unconnected. Disabled by default and can be enabled through software configuration.
USIM2_VDD	210	PO	(U)SIM2 card power supply	1.8/2.95 V	Either 1.8 V or 2.95 V (U)SIM card is supported. The total capacity of external capacitor cannot exceed 2.2 μF.
USIM2_DATA	209	DIO	(U)SIM2 card data		Externally pulled up to USIM2_VDD with a 10 kΩ resistor.
USIM2_CLK	208	DO	(U)SIM2 card		

			clock		
USIM2_RST	207	DO	(U)SIM2 card reset		
USIM2_DET	256	DI	(U)SIM2 card hot-plug detect	1.8 V	Active low. Require external pull-up to 1.8 V. If unused, keep this pin unconnected. Disabled by default and can be enabled through software configuration.
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	70	DO	SD card clock	1.8/2.95 V	50 Ω impedance.
SD_CMD	69	DIO	SD card command		
SD_DATA0	68	DIO	SDIO data bit 0		
SD_DATA1	67	DIO	SDIO data bit 1		
SD_DATA2	66	DIO	SDIO data bit 2		
SD_DATA3	65	DIO	SDIO data bit 3		
SD_DET	64	DI	SD card hot-plug detect		Active low.
SD_VDD	63	PO	SD card power supply	Vnom =1.8/2.95 V $I_O$max = 800 mA	The maximum external capacitance must not exceed 18.8 μF.
SD_PU_VDD	179	PO	1.8/2.95 V output power for SD card pull-up circuits	Vnom = 1.8/2.95 V $I_O$max = 50 mA	The maximum external capacitance must not exceed 2.2 μF.
Touch Panel Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_RST	138	DO	TP reset	1.8 V	
TP_INT	139	DI	TP interrupt		

TP_I2C_SCL	140	OD	TP I2C clock		TP I2C requires external pull-up circuit. Can only be used for TP interface.
TP_I2C_SDA	206	OD	TP I2C data		
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_BL_A	21	PO	Current output for LCD backlight	Vmax = 29.5 V I_{LED}max = 100 mA	
LCD_BL_K1	22	AI	Current sink for LCD backlight	I_{LED}max = 25 mA	
LCD_BL_K2	23	AI	Current sink for LCD backlight		
LCD_BL_K3	24	AI	Current sink for LCD backlight		
LCD_BL_K4	25	AI	Current sink for LCD backlight		
PWM	152	DO	PWM output	Vnom = VBAT	
LCD_RST	127	DO	LCD reset	1.8 V	
LCD_TE	126	DI	LCD tearing effect		
DSI_CLK_P	115	AO	LCD MIPI clock (+)		100 Ω differential impedance.
DSI_CLK_N	116	AO	LCD MIPI clock (-)		
DSI_LN0_P	117	AO	LCD MIPI lane 0 data (+)		
DSI_LN0_N	118	AO	LCD MIPI lane 0 data (-)		
DSI_LN1_P	119	AO	LCD MIPI lane 1 data (+)		
DSI_LN1_N	120	AO	LCD MIPI lane 1 data (-)		
DSI_LN2_P	121	AO	LCD MIPI lane 2 data		

			(+)		
DSI_LN2_N	122	AO	LCD MIPI lane 2 data (-)		
DSI_LN3_P	123	AO	LCD MIPI lane 3 data (+)		
DSI_LN3_N	124	AO	LCD MIPI lane 3 data (-)		
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI0_CLK_P	77	AI	MIPI CSI0 clock (+)		
CSI0_CLK_N	78	AI	MIPI CSI0 clock (-)		
CSI0_LN0_P	79	AI	MIPI CSI0 lane 0 data (+)		
CSI0_LN0_N	80	AI	MIPI CSI0 lane 0 data (-)		
CSI0_LN1_P	81	AI	MIPI CSI0 lane 1 data (+)		100 Ω differential impedance. Used for front camera by default.
CSI0_LN1_N	82	AI	MIPI CSI0 lane 1 data (-)		
CSI0_LN2_P	83	AI	MIPI CSI0 lane 2 data (+)		
CSI0_LN2_N	84	AI	MIPI CSI0 lane 2 data (-)		
CSI0_LN3_P	85	AI	MIPI CSI0 lane 3 data (+)		
CSI0_LN3_N	86	AI	MIPI CSI0 lane 3 data (-)		
CSI1_CLK_P	88	AI	MIPI CSI1 clock (+)		100 Ω differential impedance. Used for rear camera by default.
CSI1_CLK_N	89	AI	MIPI CSI1 clock (-)		
CSI1_LN0_P	90	AI	MIPI CSI1 lane 0 data (+)		

CSI1_LN0_N	91	AI	MIPI CSI1 lane 0 data (-)		
CSI1_LN1_P	92	AI	MIPI CSI1 lane 1 data (+)		
CSI1_LN1_N	93	AI	MIPI CSI1 lane 1 data (-)		
CSI1_LN2_P	94	AI	MIPI CSI1 lane 2 data (+)		
CSI1_LN2_N	95	AI	MIPI CSI1 lane 2 data (-)		
CSI1_LN3_P	96	AI	MIPI CSI1 lane 3 data (+)		
CSI1_LN3_N	97	AI	MIPI CSI1 lane 3 data (-)		
CSI2_CLK_P	183	AI	MIPI CSI2 clock (+)		
CSI2_CLK_N	184	AI	MIPI CSI2 clock (-)		
CSI2_LN0_P	185	AI	MIPI CSI2 lane 0 data (+)		
CSI2_LN0_N	186	AI	MIPI CSI2 lane 0 data (-)		
CSI2_LN1_P	187	AI	MIPI CSI2 lane 1 data (+)		100 Ω differential impedance. Used for depth camera by default.
CSI2_LN1_N	188	AI	MIPI CSI2 lane 1 data (-)		
CSI2_LN2_P	189	AI	MIPI CSI2 lane 2 data (+)		
CSI2_LN2_N	190	AI	MIPI CSI2 lane 2 data (-)		
CSI2_LN3_P	191	AI	MIPI CSI2 lane 3 data (+)		
CSI2_LN3_N	192	AI	MIPI CSI2 lane 3 data (-)		
SCAM_MCLK	100	DO	Master clock of front camera	1.8 V	

SCAM_RST	72	DO	Reset of front camera		
SCAM_PWDN	71	DO	Power down of front camera		
MCAM_MCLK	99	DO	Master clock of rear camera		
MCAM_RST	74	DO	Reset of rear camera		
MCAM_PWDN	73	DO	Power down of rear camera		If unused, keep this pin unconnected.
DCAM_MCLK	194	DO	Master clock of depth camera		
DCAM_RST	180	DO	Reset of depth camera		
DCAM_PWDN	181	DO	Power down of depth camera		
CAM4_MCLK	236	DO	Master clock of fourth camera		
CAM_I2C_SCL	75	OD	I2C clock of front and rear cameras	1.8 V	Dedicated for camera interfaces.
CAM_I2C_SDA	76	OD	I2C data of front and rear cameras		
DCAM_I2C_SDA	197	OD	I2C data of depth camera		
DCAM_I2C_SCL	196	OD	I2C clock of depth camera		
Flash & Torch Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
FLASH1_LED	26	AO	Flash/torch driver output		Support flash and torch modes.
FLASH2_LED	162	AO	Flash/torch driver output		

Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	39	DI	Turn on/off the module	1.8 V	Pulled up to 1.8 V internally. Active low.
VOL_UP	146	DI	Volume up		If unused, keep these pins unconnected.
VOL_DOWN	147	DI	Volume down		
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	5	DO	Debug UART transmit	1.8 V	If unused, keep this pin unconnected. Test points must be reserved.
DBG_RXD	6	DI	Debug UART receive		
UART5_TXD	199	DO	UART5 transmit	1.8 V	
UART5_RXD	198	DI	UART5 receive		
UART5_RTS	245	DO	Request to send signal from the module		
UART5_CTS	246	DI	Clear to send signal to the module		
Sensor I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SENSOR_I2C_SCL	131	OD	I2C clock for external sensor	1.8 V	External pull-up is required for external sensors.

SENSOR_I2C_SDA	132	OD	I2C data for external sensor		SENSOR_I2C interface only supports sensors of the ADSP architecture. Cannot be used for touch panel, NFC, I2C keyboard, etc.
Sensor Interrupt Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ACCEL_INT	252	DI	Acceleration sensor interrupt	1.8 V	
ALPS_INT	253	DI	Ambient light/proximity sensor interrupt		
MAG_INT	254	DI	Geomagnetic sensor interrupt		
GYRO_INT	255	DI	Gyroscopic sensor interrupt		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C1_SDA	204	OD	I2C1 serial data	1.8 V	The module's internal power chip has occupied the addresses 0x47, 0x02 and 0x36 of the I2C bus. A 2.2 kΩ pull-up resistor has been integrated inside the module. Can only be used as I2C instead of GPIO.
I2C1_SCL	205	OD	I2C1 serial clock		

RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_GNSS	134	AI	GNSS antenna interface		50 Ω impedance.
ANT_MAIN	19	AIO	Main antenna interface		
ANT_DRX	149	AI	Diversity antenna interface		
ANT_WIFI/BT	129	AIO	Wi-Fi/ Bluetooth antenna interface		
Antenna Tuner Control Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC_8	241	DIO	Generic RF controller	1.8 V	Only used for RF tuner control.
GRFC_9	242	DIO			
SPI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI0_CS	58	DO	SPI0 chip select	1.8 V	The module supports SPI as a master only.
SPI0_CLK	59	DO	SPI0 clock		
SPI0_MOSI	60	DO	SPI0 master-out slave-in		
SPI0_MISO	61	DI	SPI0 master-in slave-out		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	151	AI	General-purpose ADC interface		Maximum input voltage: 1.8 V

ADC1	153	AI	General-purpose ADC interface		
Charging Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BAT_P	27	AI	Battery voltage detect (+)		Must be connected to the battery anode.
BAT_M	28	AI	Battery voltage detect (-)		Must be connected to the battery ground.
BAT_THERM	29	AI	Battery temperature detect		If used, connect it to an external 47 kΩ NTC thermistor. If unused, connect it to ground with a 47 kΩ resistor.
BAT_ID	17	AI	Battery type detect		If unused, keep this pin unconnected.
RGB Interfaces					
RGB_R [7] or RESERVED	214	AO	Current output for red LED		
RGB_G [8] or RESERVED	218	AO	Current output for green LED		
RGB_B [9] or RESERVED	222	AO	Current output for blue LED		
Vibration Motor Driver Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VIB_DRV_P	161	PO	Vibration motor driver output control	Vmin = 1.5 V Vmax= 3.54 V	
Other Interfaces					

[7] Pin 214 is defined as RGB_R for SC682A series, while as RESERVED for SC680A & SC6868A series.
[8] Pin 218 is defined as RGB_G for SC682A series, while as RESERVED for SC680A & SC6868A series.
[9] Pin 222 is defined as RGB_B for SC682A series, while as RESERVED for SC680A & SC6868A series.

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_BOOT	57	DI	Force the module into download mode	1.8 V	Pulled up to 1.8 V internally. Active low. A test point is recommended to be reserved.
CBL_PWR_N	240	DI	Cable power on; initiates power on when grounded	1.8 V	If unused, keep this pin unconnected.
GNSS_LNA_EN	202	DO	GNSS LNA enable control	1.8 V	For internal testing only. Keep this pin unconnected.
S1A	215		S1A and S1B are connected inside the module		
S1B	216				
S2A	211		S2A and S2B are connected inside the module		
S2B	233				
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_65	247	DIO	General-purpose input/output	1.8 V	
GPIO_66	248	DIO			
GPIO_67	136	DIO			
GPIO_68	137	DIO			
GPIO_71	7	DIO			
GPIO_80	8	DIO			
GPIO_83	200	DIO			
GPIO_84	201	DIO			

GPIO_86	237	DIO		
GPIO_96	113	DIO		
GPIO_97	114	DIO		
GPIO_98	232	DIO		
GPIO_99	231	DIO		
GPIO_100	178	DIO		
GPIO_101	177	DIO		
GPIO_102	250	DIO		
GPIO_103	203	DIO		
GPIO_104	249	DIO		
GPIO_105	251	DIO		
GPIO_107	238	DIO		
GPIO_108	234	DIO		
GPIO_111	230	DIO		
GPIO_112	229	DIO		

Reserved Pins	
Pin Name	**Pin No.**
RESERVED	1, 2, 102–111, 158, 227, 228, 235, 239, 244

NOTE

1. Keep all RESERVED pins unconnected.
2. All GND pins should be connected to the ground unless otherwise specified.

2.4. EVB Kit

Quectel supplies an evaluation board (Smart EVB G5) with accessories to develop and test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Power Supply

3.1.1. Power Supply Pins

The module provides three VBAT pins, two VPH_PWR pins. VBAT pins must be connected to an external power supply to supply power for the module. VPH_PWR pins are used to power peripherals.

Table 7: Pins Description of Power Supply Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT	36, 37, 38	PIO	Power supply for the module	Vmax = 4.4 V Vmin = 3.55 V Vnom = 3.8 V	It must be provided with sufficient current up to 3.0 A. It is suggested to use a TVS to increase voltage surge withstand capability.
VPH_PWR	220, 221	PO	Power supply for peripherals	Vnom = VBAT $I_O$max = 1000 mA	It can provide a maximum continuous current of 1 A.

3.1.2. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current up to 3 A at least. If the voltage drop between the input and output is not too high, it is suggested to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure shows a reference design for +5 V input power source.

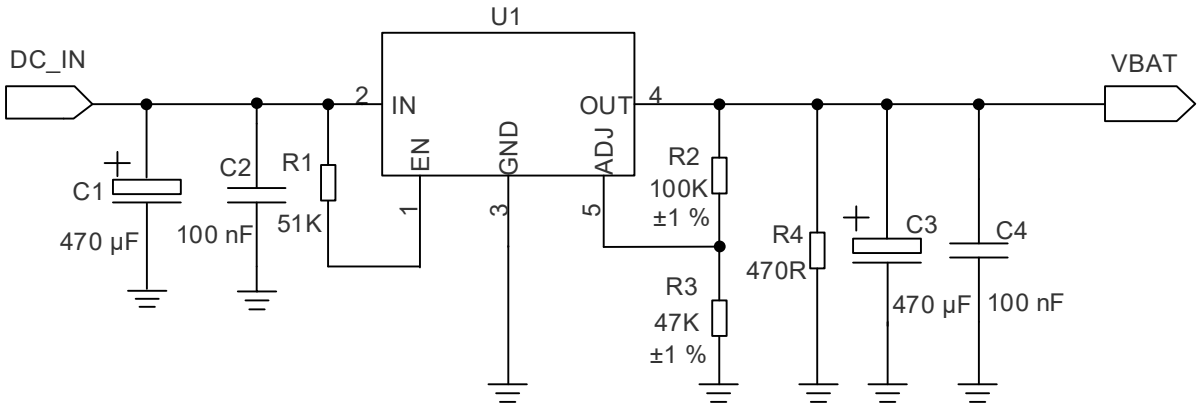


Figure 1: Reference Design for Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not turn off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY, then you can cut off the power supply.

3.1.3. Voltage Stability Requirements

The power supply range of the module is from 3.55 V to 4.4 V, and the recommended value is 3.8 V. The power supply performance, such as load capacity and voltage ripple, directly influences the module's performance and stability. Under ultimate conditions, the module may have a transient peak current of up to 3 A. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 3.1 V, the module will power off automatically. Therefore, make sure the input voltage never drops below 3.1 V.

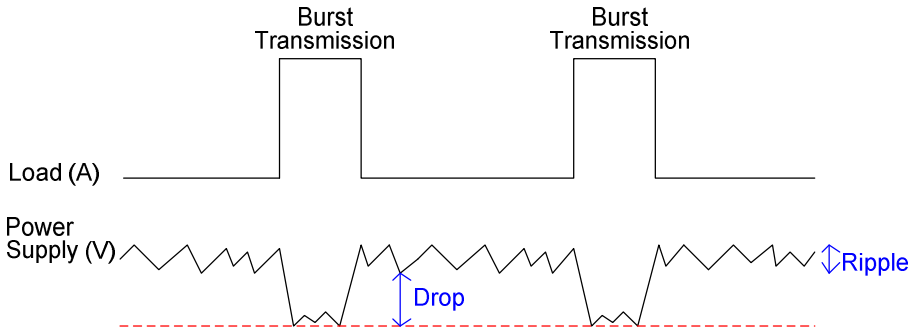


Figure 2: Power Supply Limits during Burst Transmission

To prevent the voltage from dropping below 3.1 V, use a bypass capacitor of about 100 μF with low ESR (ESR = 0.7 Ω), and reserve a multi-layer ceramic chip capacitor (MLCC) array due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) to compose the MLCC array, and place these capacitors close to VBAT pins. Additionally, add a 4.7 μF capacitor in parallel. The width of VBAT trace should be not less than 3 mm. In principle, the longer the VBAT trace is, the wider it should be. Additionally, the ground plane of the power supply part should be as complete as possible.

To suppress the impact of power fluctuations and ensure the stability of the output power supply, it is suggested to add a TVS of at least 2000 W and place it as close to the VBAT pin as possible to enhance surge protection.

The following figure shows the structure of the power supply.

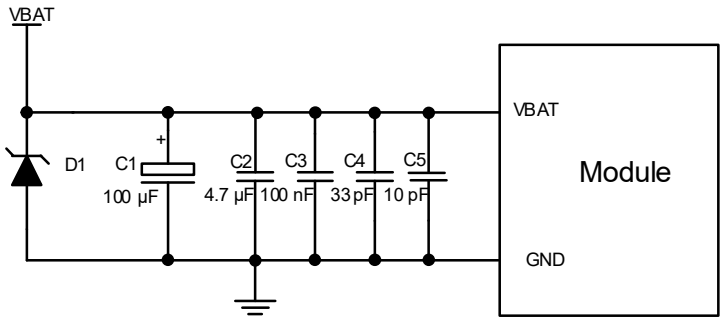


Figure 3: Structure of Power Supply

3.1.4. Battery Charge and Management

The module supports battery charging. The battery charging function of the module supports trickle charging, pre-charge, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion batteries.

- **Trickle charging:** When the battery voltage is below 2.1 V, a 75-mA trickle charging current is applied to the battery.
- **Pre-charge mode:** When the battery voltage is between 2.1 V and the pre-charge cut-off voltage (software programmable range: 2.4–3.0 V, 3.0 V by default), the system will switch to pre-charge mode. The charging current software programmable range is from 100 mA to 450 mA (450 mA by default).
- **Constant current mode (CC mode):** When the battery voltage exceeds the pre-charge cut-off voltage, the system will switch to CC mode. The maximum charging current is 3000 mA when an adapter is used for battery charging, and the maximum charging current is 500 mA for USB charging.
- **Constant voltage mode (CV mode):** When the battery voltage reaches the final value 4.35 V, the system will switch to CV mode and the charging current will decrease gradually. When the charging current reduces to about 100 mA, charging is completed.

Table 8: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
BAT_P	27	AI	Battery voltage detect (+)	Must be connected to the battery anode.
BAT_M	28	AI	Battery voltage detect (-)	Must be connected to the battery ground.
BAT_THERM	29	AI	Battery temperature detect	If used, connect it to an external 47 kΩ NTC thermistor. If unused, connect it to ground with a 47 kΩ resistor.
BAT_ID	17	AI	Battery type detect	If unused, keep this pin unconnected.

The module supports battery temperature detection in the condition that the battery integrates a thermistor (47 kΩ ±1 % NTC thermistor with a B-constant of 4050 kΩ ±1 % by default) and the thermistor is connected to BAT_THERM pin, or there will be malfunctions such as boot error, battery charging failure, and battery level display error.

A reference design for the battery charging circuit is shown below.

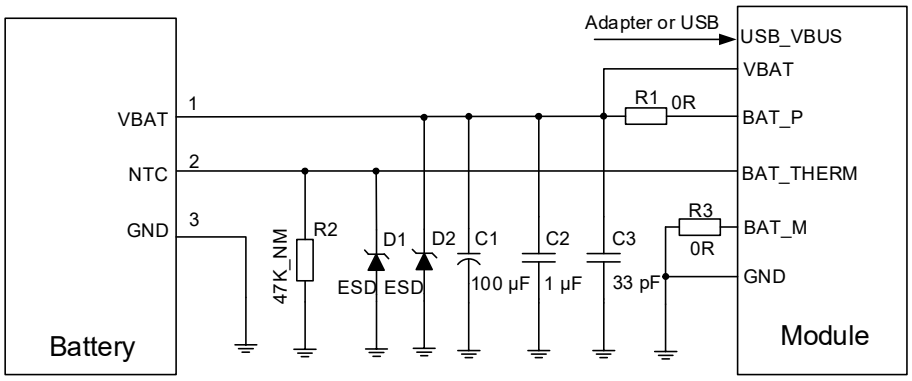


Figure 4: Reference Design for Battery Charging Circuit

Mobile devices such as mobile phones and handheld POS systems are powered by batteries. When different batteries are utilized, the charging and discharging curve must be modified correspondingly to achieve the best effect.

If the thermistor is not available in the battery, or an adapter is utilized for powering the module, only VBAT and GND need to be connected. Otherwise, the system may misjudge that the battery temperature is abnormal, which will cause battery charging failure. To avoid this, BAT_THERM should be connected to GND via a 47 kΩ resistor. If BAT_THERM is unconnected, the system will be unable to detect the battery, resulting in unsuccessful battery charging.

BAT_P and BAT_M must be connected. Otherwise, the module will have abnormalities in voltage detection, as well as an associated turn on/off issues and battery charging/discharging issues.

3.2. Turn On with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	39	DI	Turn on/off the module	Pulled up to 1.8 V internally. Active low.

The module can be turned on by driving the PWRKEY pin low for at least 1.6 s.

It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference design is illustrated in the following figure.

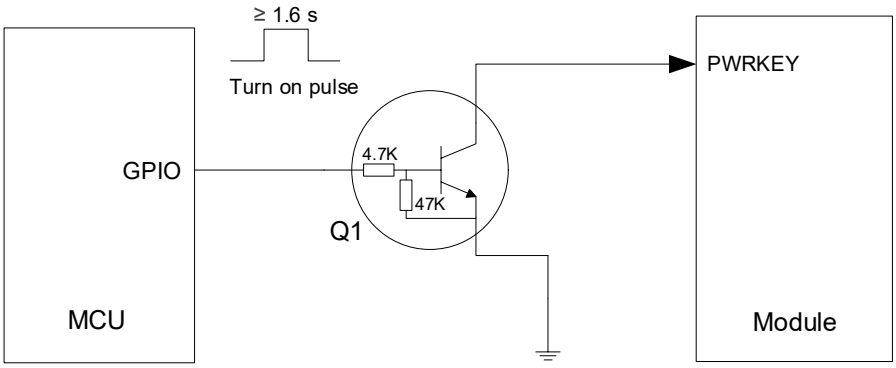


Figure 5: Reference Design for Turn-on with Driver Circuit

The other way to control the PWRKEY is by using a push button. When pressing the push button, an electrostatic strike may be generated from finger. Therefore, you should place a TVS near the push button for ESD protection. Additionally, a 1 kΩ resistor is connected in series to PWRKEY for ESD protection.

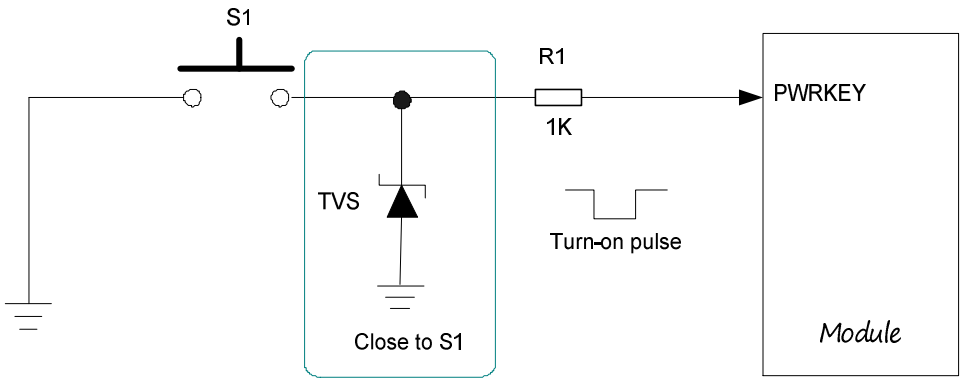


Figure 6: Reference Design for Turn-on with Push Button

The turn-on timing is illustrated in the following figure.

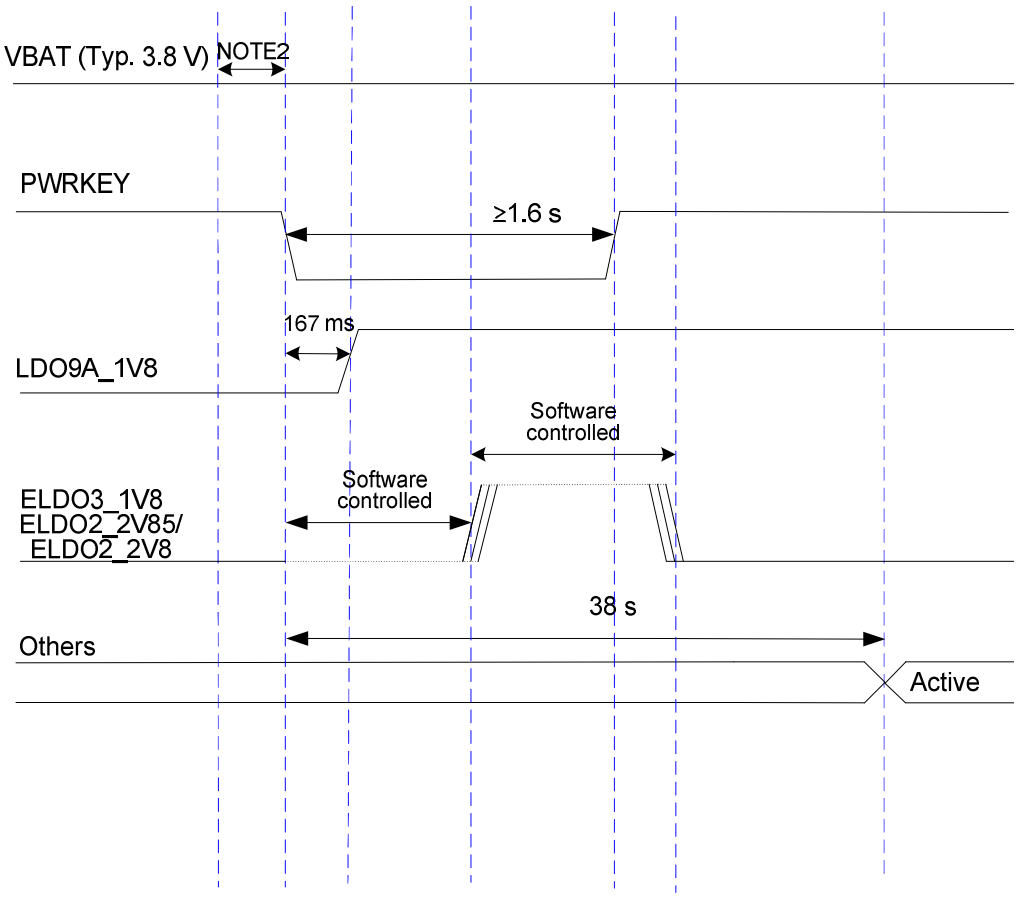


Figure 7: Timing of Turn-on with PWRKEY

NOTE

1. When the module is turned on for the first time, its turn-on timing may be different from that shown above.
2. Ensure that the voltage of VBAT is stable before driving PWRKEY pin low, and it is recommended to drive PWRKEY low after VBAT reaches 3.8 V and remains stable for 30 ms. PWRKEY pin cannot be driven low all the time.

3.3. Turn Off

Drive the PWRKEY pin low for at least 1 s, and then choose to turn off the module when the prompt window comes up.

The other way to turn off the module is to drive PWRKEY pin low for at least 8 s. The module will execute the forced shutdown. The forced turn-off timing is illustrated in the following figure.

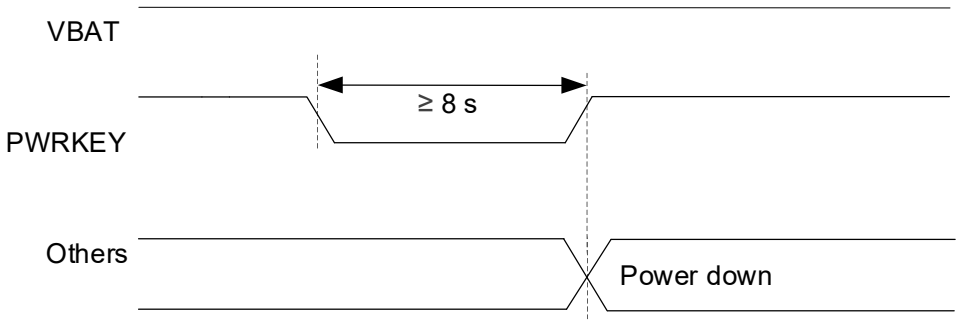


Figure 8: Timing of Forced Turn-off with PWRKEY

3.4. VRTC

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supply for the VBAT. The power source can be an external battery or capacitor according to application demands.

The following are some reference circuit designs when an external battery or capacitor is utilized for powering RTC.

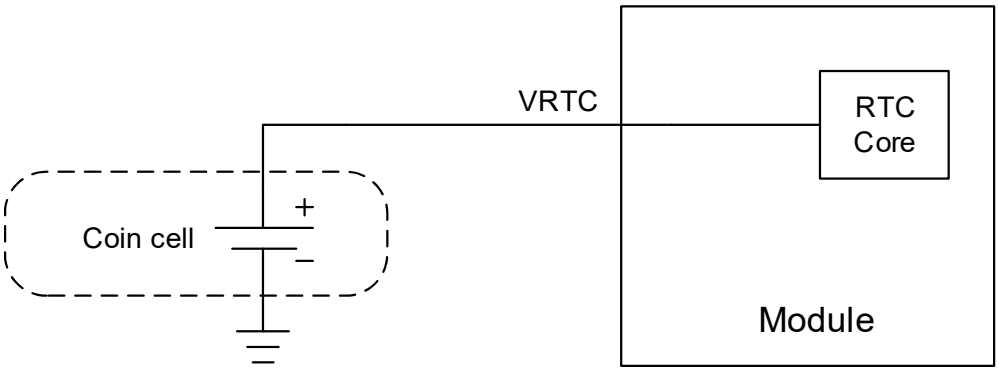


Figure 9: RTC Powered by Rechargeable Coin Cell Battery

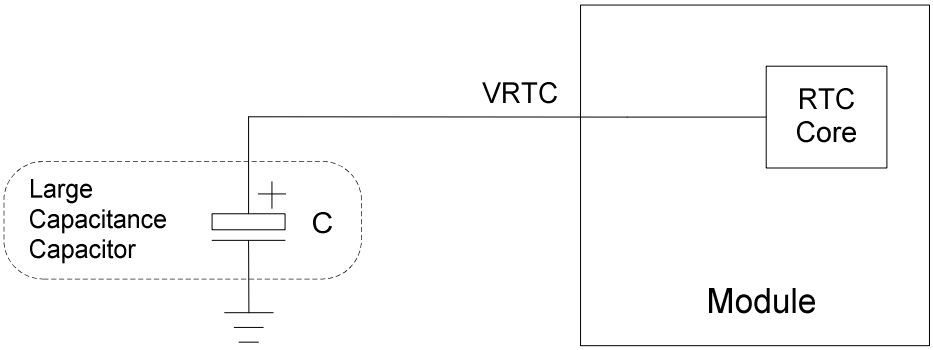


Figure 10: RTC Powered by Large Capacitance Capacitor

- When VBAT is disconnected, the recommended input voltage range for VRTC is 2.0–3.25 V and the recommended typical value is 3.0 V.
- When powered by VBAT, the RTC deviation is 50 ppm. When powered by VRTC, the RTC deviation is about 200 ppm.
- If a rechargeable battery is used, ESR of the battery should be less than 2 kΩ.

3.5. Power Output

The module supports multiple output of regulated voltage for peripherals. It is recommended to connect a 33 pF and a 10 pF capacitor in parallel to suppress high-frequency noise.

Table 10: Power Information

Pin Name	Default Voltage (V)	Drive Current (mA)	Power Supply Status @ Standby
LDO9A_1V8	1.8	20	Keeps ON
ELDO3_1V8	1.8	300	-
ELDO1_2V8	2.8	300	-
ELDO2_2V85 or ELDO2_2V8 [10]	**SC680A&SC686A series**：2.85 **SC682A series**：2.8	300	-
LDO2C_1V1	1.1	800	-
LDO3C_2V8	2.8	300	-
LDO1C_1V2	1.2	800	-

[10] Pin 12 is defined as ELDO2_2V85 for SC680A&SC686A series, while as ELDO2_2V8 for SC682A series.

4 Application Interfaces

4.1. USB Interface

The module provides one USB interface. The USB interface complies with the USB 3.1 Gen 1 and USB 2.0 specifications, and supports SuperSpeed (5 Gbps) for USB 3.1 Gen 1, high-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps) for USB 2.0. The USB interface supports USB OTG function, and is used for AT command communication, data transmission, software debugging and firmware upgrade.

The following table shows the pin definition of USB interface.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	41, 42	PIO	Charging power input. Power supply for OTG device. USB/adapter insertion detection.	Test points must be reserved.
USB_DM	33	AIO	USB 2.0 differential data (-)	Test points must be reserved. 90 Ω differential impedance.
USB_DP	32	AIO	USB 2.0 differential data (+)	
USB_SS1_RX_P	171	AI	USB 3.1 Channel 1 super-speed receive (+)	90 Ω differential impedance. USB 3.1 Gen 1 standard compliant.
USB_SS1_RX_M	172	AI	USB 3.1 Channel 1 super-speed receive (-)	
USB_SS1_TX_P	174	AO	USB 3.1 Channel 1 super-speed transmit (+)	
USB_SS1_TX_M	175	AO	USB 3.1 Channel 1 super-speed transmit (-)	
USB_SS2_RX_P	156	AI	USB 3.1 Channel 2 super-speed receive (+)	90 Ω differential impedance. USB 3.1 Gen 1 standard compliant.
USB_SS2_RX_M	155	AI	USB 3.1 Channel 2 super-speed receive (-)	
USB_SS2_TX_P	165	AO	USB 3.1 Channel 2 super-speed transmit (+)	

USB_SS2_TX_M	164	AO	USB 3.1 Channel 2 super-speed transmit (-)	
UUSB_TYPEC	217	AI	uUSB & USB Type-C configuration	If Micro USB is intended to be used, this pin should be connected to ground via a 1 kΩ resistor. If USB Type-C is intended to be used, this pin should be left unconnected.
USB_CC1	224	AI	USB Type-C configuration channel 1	
USB_CC2	223	AI	USB Type-C configuration channel 2	
USB_SS_SEL	226	DO	USB Type-C switch control	
SS_DIR_IN	212	DI	Configuration channel status detect	When using Micro USB, connect it to ground with a 7.32 kΩ resistor. When using USB Type-C, connect the pin to SS_DIR_OUT.
SS_DIR_OUT	213	AO	Configuration channel status output	When using Micro USB, keep this pin unconnected. When using USB Type-C, connect the pin to SS_DIR_IN.
USB_ID	30	AI	USB ID detect	High level by default.

4.1.1. Micro USB Mode

A reference design for Micro USB mode is shown below.

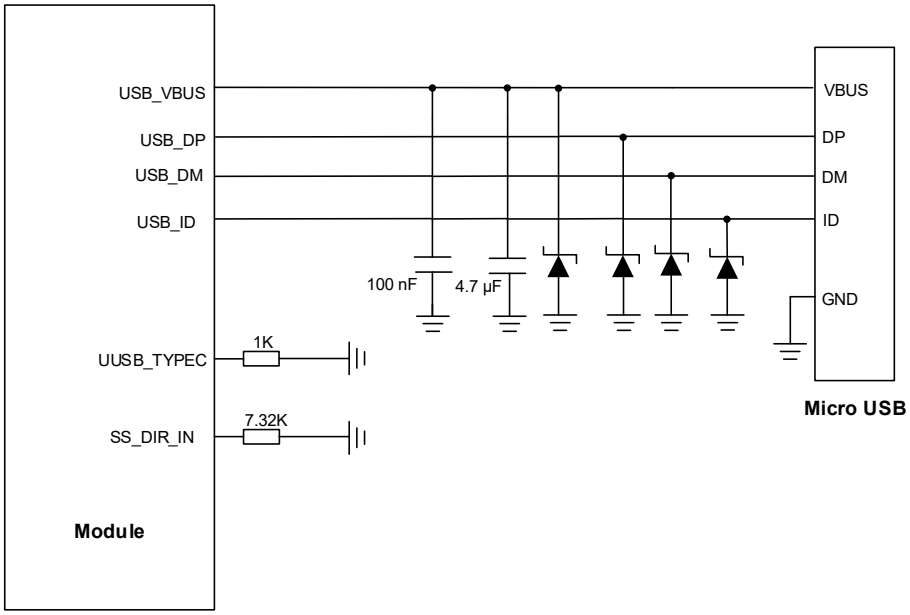


Figure 11: Reference Design for Micro USB Mode

4.1.2. USB Type-C Mode

A reference design for USB Type-C mode shown below.

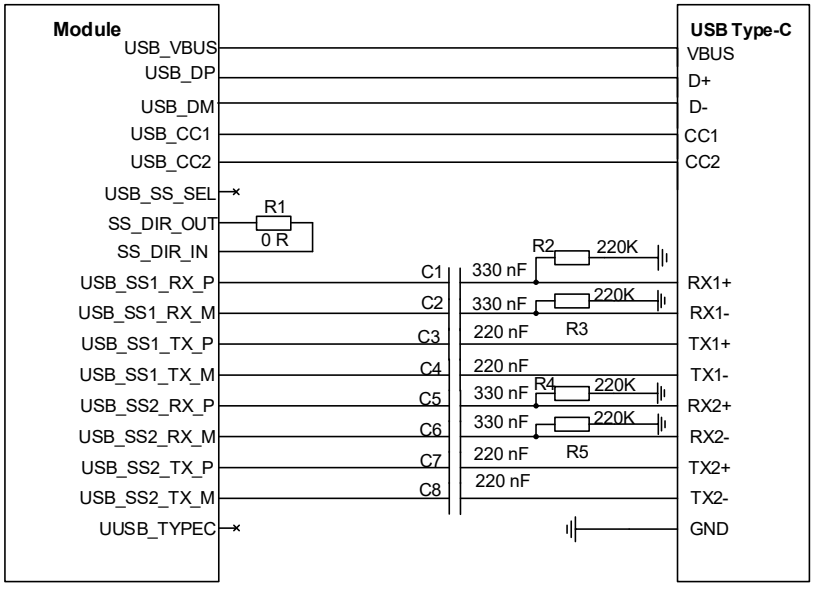


Figure 12: Reference Design for USB Type-C Mode

To ensure USB performance, you should follow the following principles while designing USB interface.

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB differential trace is 90 Ω.
- The ground reference plane under the USB signals must be continuous without any cuts or any holes to ensure impedance continuity.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be not more than 2 pF for USB 2.0 and not more than 0.5 pF for USB 3.1. Keep the ESD protection components as close as possible to the USB connector.
- For USB 2.0, the total trace length of each signal should be not more than 200 mm, and the length matching (P/M) of each differential pair should be not more than 2 mm.
- For USB 3.1, intra-pair length matching (P/M) should be not more than 0.7 mm, while the inter-pair length matching (Tx/Rx) should be not more than 10 mm.
- For signal traces, provide spacing from power supply traces, crystal-oscillators, magnetic devices, sensitive signals such as RF signals, analog signals, and noise signals generated by clock, and DC-DC. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.

Table 12: SC680A&SC686A Series USB Trace Length Inside the Module (Unit: mm)

Signal	Pin No.	Length	Length Difference (P – M)
USB_DP	32	37.12	-0.54
USB_DM	33	37.66	
USB_SS1_RX_P	171	22.08	0
USB_SS1_RX_M	172	22.08	
USB_SS1_TX_P	174	19.87	-0.31
USB_SS1_TX_M	175	20.18	
USB_SS2_RX_P	156	38.27	0.04
USB_SS2_RX_M	155	38.23	
USB_SS2_TX_P	165	33.68	-0.02
USB_SS2_TX_M	164	33.70	

Table 13: SC682A Series USB Trace Length Inside the Module (Unit: mm)

Signal	Pin No.	Length	Length Difference (P – M)
USB_DP	32	70.82	0.63
USB_DM	33	70.19	
USB_SS1_RX_P	171	28.58	-0.13
USB_SS1_RX_M	172	28.45	
USB_SS1_TX_P	174	25.74	-0.28
USB_SS1_TX_M	175	25.46	
USB_SS2_RX_P	156	73.79	-0.24
USB_SS2_RX_M	155	73.55	
USB_SS2_TX_P	165	69.17	-0.31
USB_SS2_TX_M	164	68.86	

4.2. USB_BOOT Interface

The module provides a USB_BOOT pin. You can pull up USB_BOOT to LDO9A_1V8 before turning on the module, thus the module will enter forced download mode when turned on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 14: Pins Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	57	DI	Force the module into download mode	Pulled up to 1.8 V internally. Active low. A test point is recommended to be reserved.

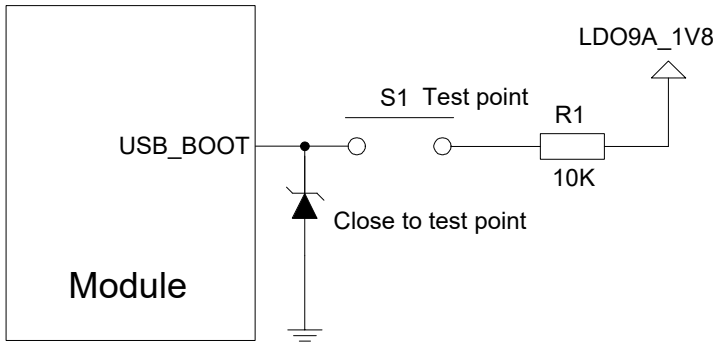


Figure 13: Reference Design for USB_BOOT

4.3. (U)SIM Interfaces

The module provides two (U)SIM interfaces which meet ETSI and IMT-2000 requirements. Dual SIM Dual Standby is supported by default. Either 1.8 V or 2.95 V (U)SIM card is supported, and the (U)SIM interfaces are powered by the dedicated low dropout regulators in the module.

Table 15: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	141	PO	(U)SIM1 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported. The total capacity of the external capacitor(s) cannot exceed 2.2 μF.
USIM1_DATA	142	DIO	(U)SIM1 card data	Externally pulled up to USIM1_VDD with a 10 kΩ resistor.
USIM1_CLK	143	DO	(U)SIM1 card clock	
USIM1_RST	144	DO	(U)SIM1 card reset	
USIM1_DET	145	DI	(U)SIM1 card hot-plug detect	Active low. Require external pull-up to 1.8 V. If unused, keep this pin unconnected. Disabled by default and can be enabled through software configuration.
USIM2_VDD	210	PO	(U)SIM2 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported. The total capacity of external

				capacitor cannot exceed 2.2 μF.
USIM2_DATA	209	DIO	(U)SIM2 card data	Externally pulled up to USIM2_VDD with a 10 kΩ resistor.
USIM2_CLK	208	DO	(U)SIM2 card clock	
USIM2_RST	207	DO	(U)SIM2 card reset	
USIM2_DET	256	DI	(U)SIM2 card detect	Active low. Require external pull-up to 1.8 V. If unused, keep this pin unconnected. Disabled by default and can be enabled through software configuration.

The module supports (U)SIM card hot-plug via the USIM_DET pin, which is disabled by default and can be enabled through software configuration.

A reference design for (U)SIM interface with an 8-pin (U)SIM card connector is shown below.

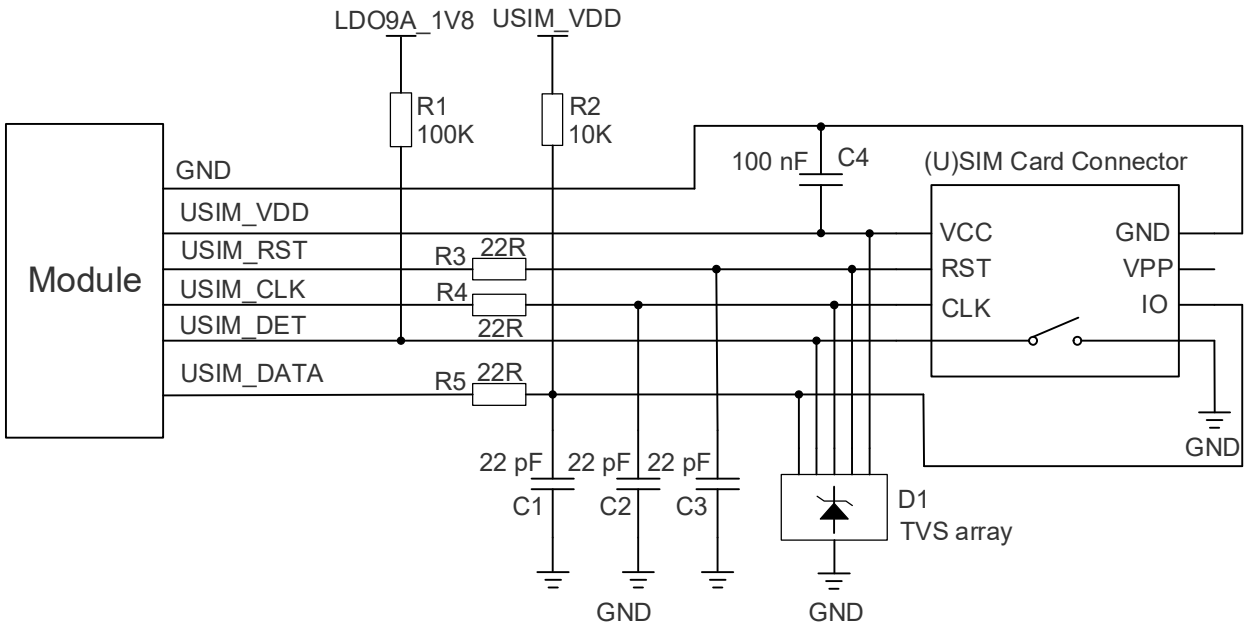


Figure 14: Reference Design for (U)SIM Interface with an 8-Pin (U)SIM Card Connector

A reference design for (U)SIM card interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

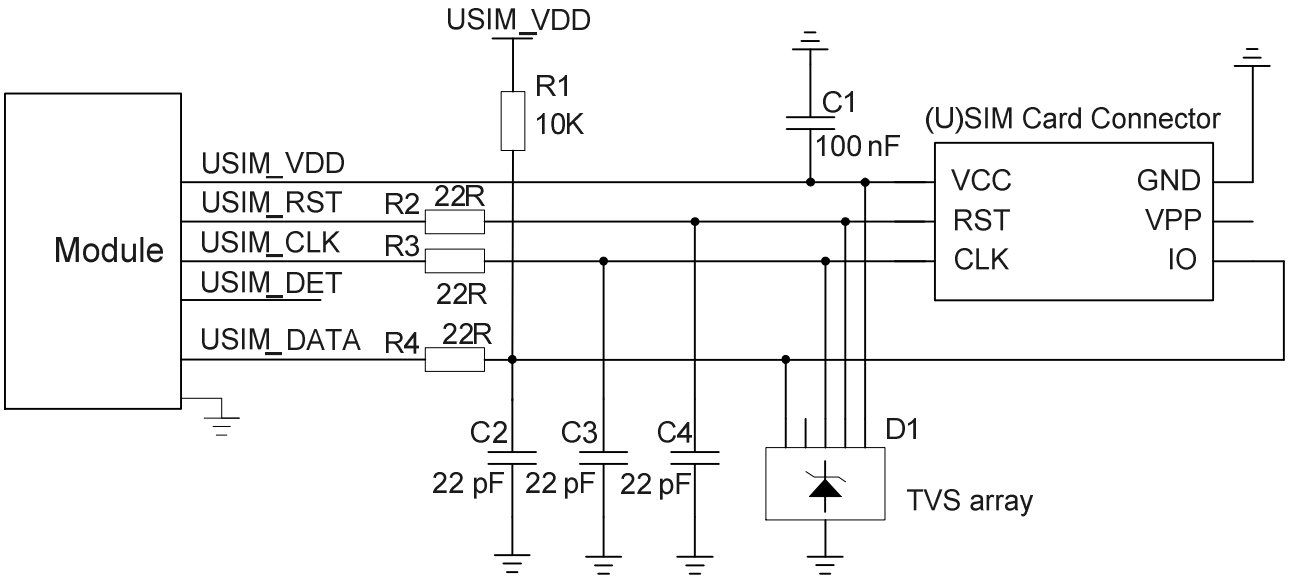


Figure 15: Reference Design for (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, you should follow the criteria below in (U)SIM circuit design.

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- (U)SIM card signal traces should provide spacing from power supply traces, crystal-oscillators, magnetic devices, sensitive signals such as RF signals, analog signals, and noise signals generated by clock and DC-DC.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, it is recommended to add a TVS array of which the parasitic capacitance should be less than 30 pF. The 22 Ω resistors should be added in series between the module and the (U)SIM card connector to suppress EMI and filter out RF interference.
- Add 22 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter out RF interference, and place them as close to the (U)SIM card connector as possible.
- The pull-up resistor 10 kΩ on USIM_DATA trace improves anti-jamming capability and should be placed close to the (U)SIM card connector.

4.4. SPI

The module supports up to three SPIs. One of them is default configuration, and supports master mode only. Two of them can be multiplexed from other interfaces, see ***Table 19*** for details.

Table 16: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI0_CS	58	DO	SPI0 chip select	The module supports SPI as a master only.
SPI0_CLK	59	DO	SPI0 clock	
SPI0_MOSI	60	DO	SPI0 master-out slave-in	
SPI0_MISO	61	DI	SPI0 master-in slave-out	

4.5. UART Interfaces

The module supports up to four UART interfaces. Two of them are default configurations and two of them can be multiplexed from other interfaces, see ***Table 19*** for details.

Two default UART interfaces are:

- **UART5:** 4-wire UART interface, supports hardware flow control.
- **Debug UART:** 2-wire UART interface, dedicated for debugging, including Linux console and log output.

Pin definition of the UART interfaces is here as follows:

Table 17: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	5	DO	Debug UART transmit	If unused, keep this pin connected. Test points must be reserved.
DBG_RXD	6	DI	Debug UART receive	
UART5_TXD	199	DO	UART5 transmit	
UART5_RXD	198	DI	UART5 receive	
UART5_RTS	245	DO	Request to send signal from the module	
UART5_CTS	246	DI	Clear to send signal to the module	

UART5 is a 4-wire UART interface with 1.8 V power domain. A level-shifting chip should be used if your application is equipped with a 3.3 V UART interface. The following figure shows a reference design.

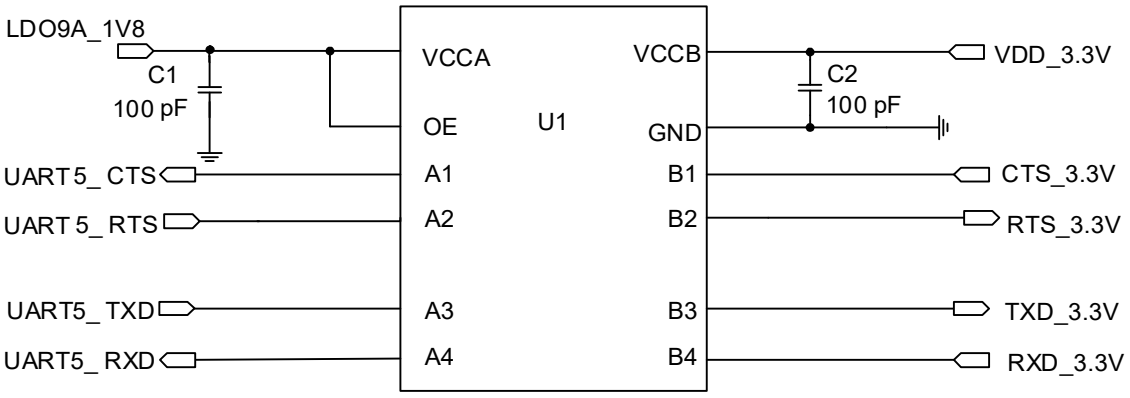


Figure 16: Reference Design for UART with Level-shifting Chip (for UART5)

The following figure is a reference design for the connection between the module and a PC. A level-shifting chip and an RS-232 level-shifting chip are recommended to be added between the module and PC, as shown below:

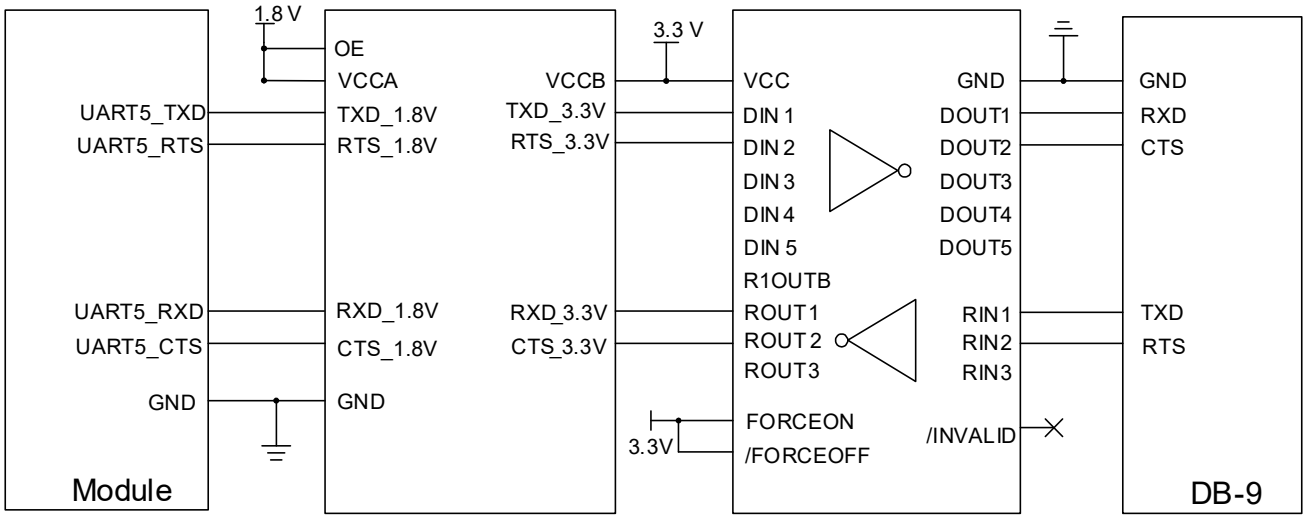


Figure 17: Reference Design for UART with RS-232 Level-shifting Chip (for UART5)

NOTE

Debug UART is similar to UART5. For the reference design, refer to that of UART5.

4.6. I2C Interfaces

The module provides up to seven I2C interfaces. Four of them are used for camera, TP and sensor peripherals. One of them is general I2C interface. Two of them can be multiplexed from other interfaces, see ***Table 19*** for details.

All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8 V. The SENSOR_I2C interface only supports sensors of the ADSP architecture. CAM_I2C/DCAM_I2C signals are controlled by Linux Kernel code and support connection with video output related devices.

Table 18: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SDA	204	OD	I2C1 serial data	The module's internal power chip has occupied the addresses 0x47, 0x02 and 0x36 of the I2C bus. A 2.2 kΩ pull-up resistor has been integrated inside the module. Can only be used as I2C instead of GPIO.
I2C1_SCL	205	OD	I2C1 serial clock	

4.7. I2S Interfaces

The module does not support I2S interface by default, but it can be multiplexed from GPIO interfaces. The module supports up to two I2S interfaces, one of which is a low-power I2S interface. Data signals of both interfaces can be configured as input or output, and the reference power domain of the interfaces is 1.8 V.

4.8. UART/SPI/I2C/I2S Multiplexing Relationship

UART/SPI/I2C/I2S multiplexing relationship is shown in the following tables.

Table 19: UART/SPI/I2C Multiplexing Relationship

Channel	Pin No.	Pin Name	GPIO No.	Multiplexing Functions		
				UART	SPI	I2C
QUP0 SE0	58	SPI0_CS	GPIO_3	UART0_RX	SPI0_CS	

	59	SPI0_CLK	GPIO_2	UART0_TX	SPI0_CLK	
	60	SPI0_MOSI	GPIO_1	UART0_RTS	SPI0_MOSI	I2C0_SCL
	61	SPI0_MISO	GPIO_0	UART0_CTS	SPI0_MISO	I2C0_SDA
QUP0 SE2	7	GPIO_71	GPIO_71	UART2_TX	SPI2_CLK	
	8	GPIO_80	GPIO_80	UART2_RX	SPI2_CS	
	140	TP_I2C_SCL	GPIO_7	UART2_RTS	SPI2_MOSI	I2C2_SCL
	206	TP_I2C_SDA	GPIO_6	UART2_CTS	SPI2_MISO	I2C2_SDA
QUP0 SE5	198	UART5_RXD	GPIO_17	UART5_RX	SPI5_CS	
	199	UART5_TXD	GPIO_16	UART5_TX	SPI5_CLK	
	245	UART5_RTS	GPIO_15	UART5_RTS	SPI5_MOSI	I2C5_SCL
	246	UART5_CTS	GPIO_14	UART5_CTS	SPI5_MISO	I2C5_SDA

NOTE

1. QUP-SE is flexible and supports three types of interfaces: UART, SPI and I2C.
2. The same set of QUP-SE cannot support two protocols at the same time. For example, the same set of QUP cannot support UART and I2C at the same time. If a protocol only occupies part of the pins of this group of QUP, other pins can only be used for GPIO.

Table 20: I2S Multiplexing Relationship Table

Channel	Pin No.	Pin Name	GPIO No.	I2S Multiplexing Function
1	234	GPIO_108	GPIO_108	MI2S_MCLK1_A
2	231	GPIO_99	GPIO_99	LPI_MI2S0_WS
	232	GPIO_98	GPIO_98	LPI_MI2S0_CLK
	177	GPIO_101	GPIO_101	LPI_MI2S0_DATA1/ MI2S_MCLK1_B
	178	GPIO_100	GPIO_100	LPI_MI2S0_DATA0
3	203	GPIO_103	GPIO_103	LPI_MI2S1_WS
	250	GPIO_102	GPIO_102	LPI_MI2S1_CLK
	249	GPIO_104	GPIO_104	LPI_MI2S1_DATA0

	251	GPIO_105	GPIO_105	LPI_MI2S1_DATA1/ MI2S_MCLK0_A

4.9. Analog Audio Interfaces

The module provides 3 analog input channels and 3 analog output channels. The following table shows the pin definition.

Table 21: Pin Definition of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC_BIAS	167	AO	Bias voltage output for microphone	
MIC1_P	44	AI	Microphone input for channel 1 (+)	Integrated with internal bias voltage.
MIC1_M	45	AI	Microphone input for channel 1 (-)	
MIC_GND	168		Microphone reference ground	If unused, connect this pin to ground.
MIC2_P	46	AI	Microphone input for headset (+)	Integrated with internal bias voltage.
MIC3_P	169	AI	Microphone input for channel 2 (+)	No internal bias voltage is integrated.
EAR_P	53	AO	Earpiece output (+)	
EAR_M	52	AO	Earpiece output (-)	
SPK_P	55	AO	Speaker output (+)	
SPK_M	54	AO	Speaker output (-)	
HPH_R	51	AO	Headphone right channel output	
HPH_L	49	AO	Headphone left channel output	
HPH_GND	50		Headphone reference ground	It should be connected to main ground.
HS_DET	48	AI	Headset hot-plug detect	Pulled up internally.

- The module offers 3 analog input channels, including 1 differential input pair and 2 single-ended channels.
- The output voltage range of MIC_BIAS is programmable between 1.0 V and 2.85 V, and the maximum output current is 3 mA.

- The earpiece interface uses differential output.
- The loudspeaker interface uses the differential output as well. The output channel is available with a Class K amplifier whose output power is 1.2 W when the load is 8 Ω.
- The headphone interface features stereo left and right channel output, and headset insert detection function is supported.

4.9.1. Reference Design for Microphone Interfaces

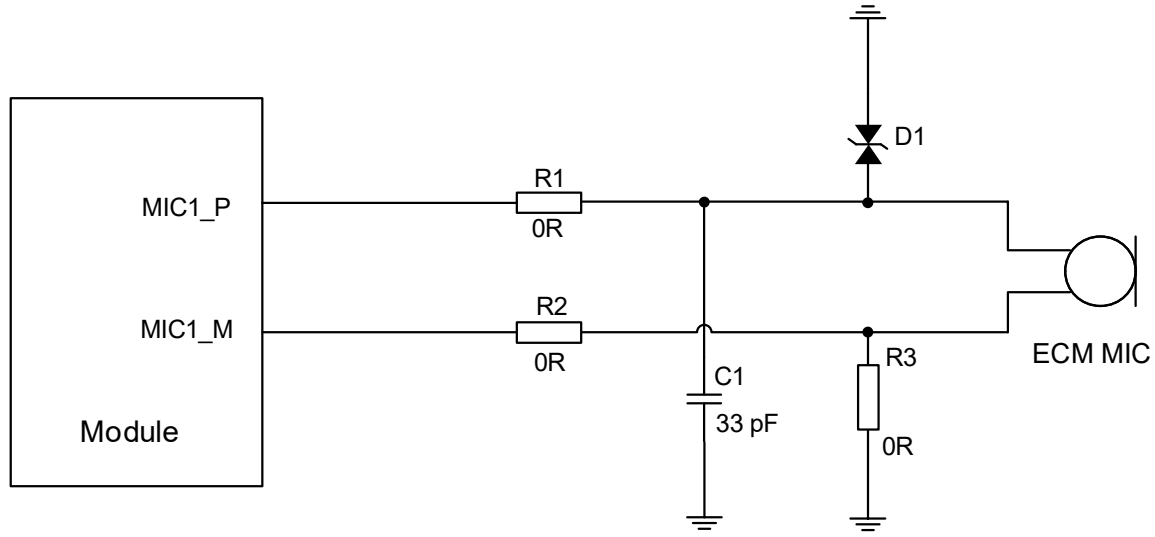


Figure 18: Reference Design for ECM Microphone Interface

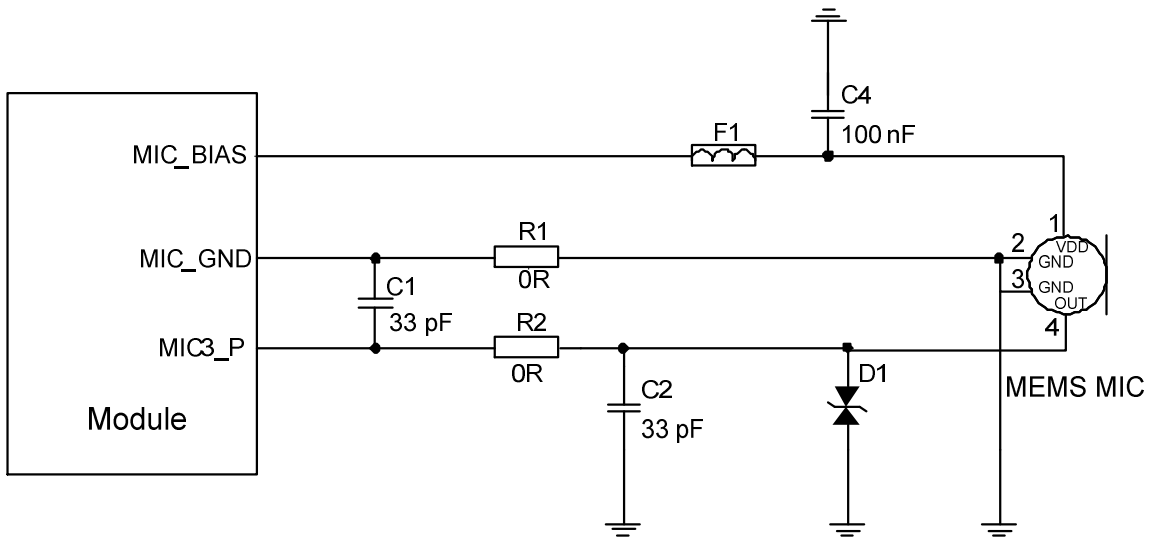


Figure 19: Reference Design for MEMS Microphone Interface

4.9.2. Reference Design for Earpiece Interface

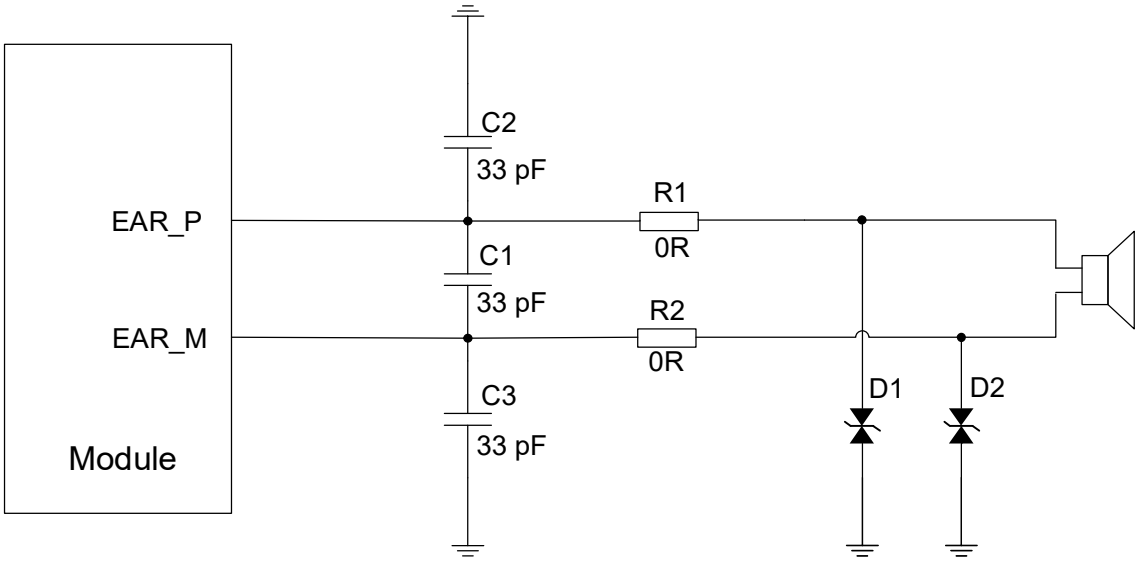


Figure 20: Reference Design for Earpiece Interface

4.9.3. Reference Design for Headset Interface

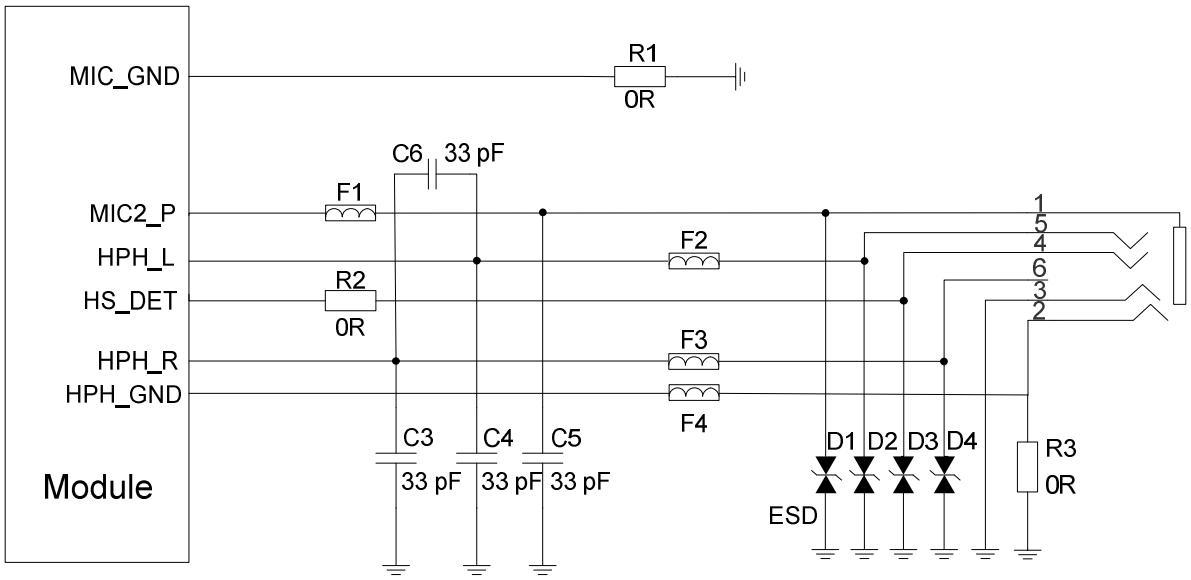


Figure 21: Reference Design for Headset Interface

4.9.4. Reference Design for Loudspeaker Interface

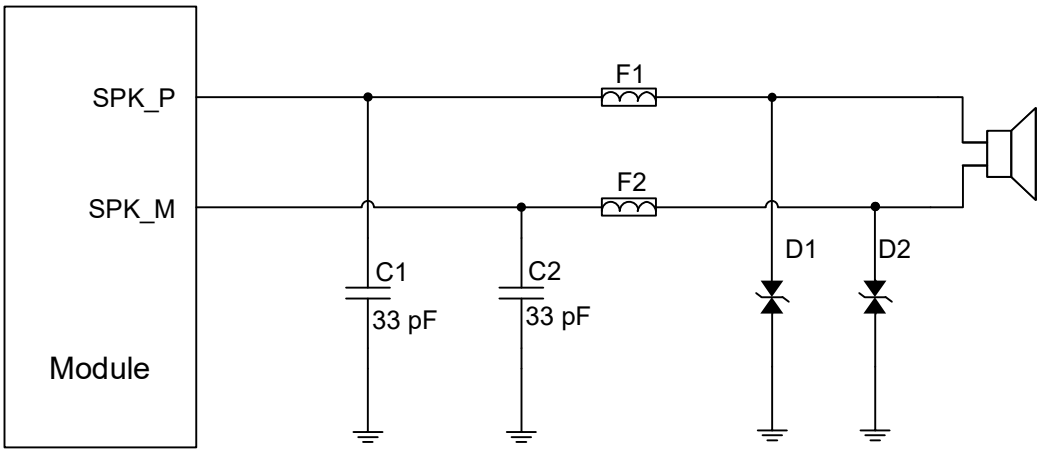


Figure 22: Reference Design for Loudspeaker Interface

4.9.5. Analog Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. Without this capacitor, TDD noise could be heard during the call. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you would have to discuss with your capacitor vendors to choose the most suitable capacitor to filter out high-frequency noises.

For models that support GSM, the severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required. The filter capacitors on the PCB should be placed near the audio device or audio interface as close as possible, and the trace should be as short as possible. They should be passed before reaching other connection points.

To decrease signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

4.10. ADC Interfaces

The module provides 2 Analog-to-Digital Converter (ADC) interfaces which support up to 15-bit resolution, and the pin definition is shown below.

Table 22: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	151	AI	General-purpose ADC interface	Maximum input voltage: 1.8 V
ADC1	153	AI		

4.11. SD Card Interface

The module supports SD 3.0 specifications. The pin definition of the SD card interface is shown below.

Table 23: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	70	DO	SD card clock	50 Ω impedance.
SD_CMD	69	DIO	SD card command	
SD_DATA0	68	DIO	SDIO data bit 0	
SD_DATA1	67	DIO	SDIO data bit 1	
SD_DATA2	66	DIO	SDIO data bit 2	
SD_DATA3	65	DIO	SDIO data bit 3	
SD_DET	64	DI	SD card hot-plug detect	Active low.
SD_VDD	63	PO	SD card power supply	The maximum external capacitance must not exceed 18.8 μF.
SD_PU_VDD	179	PO	1.8/2.95 V output power for SD card pull-up circuits	The maximum external capacitance must not exceed 2.2 μF.

A reference design for SD card interface is shown below.

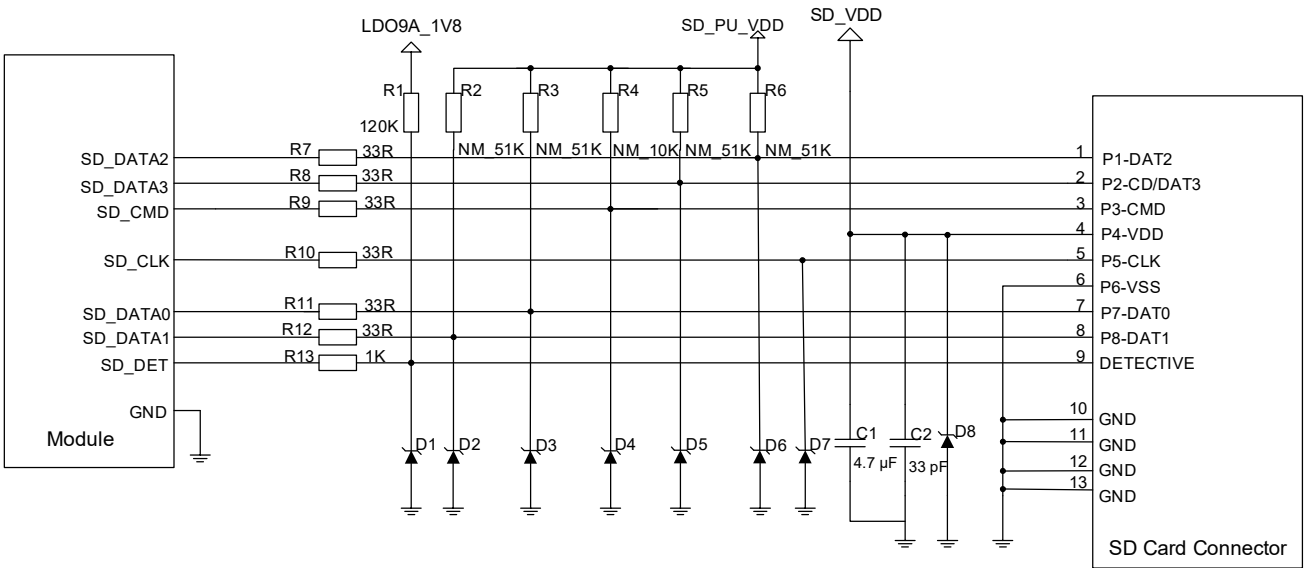


Figure 23: Reference Design for SD Card Interface

SD_VDD is a peripheral driver power supply for SD card. The maximum drive current is 800 mA. Because of the high drive current, it is recommended to keep the trace width as 0.5 mm at least. To ensure the stability of drive power, add a 4.7 µF and a 33 pF capacitor in parallel near the SD card connector.

SD_CMD, SD_CLK, SD_DATA[0:3] are all high-speed signal traces. In PCB design, control the characteristic impedance of them as 50 Ω, and do not cross them with other traces. It is recommended to route these traces on the inner layer of PCB, and keep their lengths the same. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control impedance to 50 Ω ±10 %, and add ground shielding.
- The total trace length of each signal (except for SD_DET) should be less than 150 mm for 50 MHz DDR/100 MHz SDR clock frequency modes.
- The trace length difference between SD_CLK and SD_CMD/SD_DATA[0:3] should not exceed 6 mm for 50 MHz DDR/100 MHz SDR clock frequency modes.
- spacing between signal traces should be 1.5 times the trace width.
- The load capacitance of SD_DATA[0:3], SD_CLK and SD_CMD traces should be less than 5 pF.

Table 24: SC680A&SC686A series SD Card Interface Trace Length Inside the Module (Unit: mm)

Signal	Pin No.	Length
SD_CLK	70	50.15

SD_CMD	69	50.69
SD_DATA0	68	51.05
SD_DATA1	67	51.21
SD_DATA2	66	50.53
SD_DATA3	65	50.88

Table 25: SC682A series SD Card Interface Trace Length Inside the Module (Unit: mm)

Signal	Pin No.	Length
SD_CLK	70	56.26
SD_CMD	69	56.36
SD_DATA0	68	56.34
SD_DATA1	67	56.43
SD_DATA2	66	57.04
SD_DATA3	65	57.25

4.12. LCM Interface

The module provides an LCM interface, which is MIPI DSI standard compliant. The interface supports high-speed differential data transmission and supports FHD + (1080 × 2520 @ 60 fps). The maximum rate can reach up to 1.5 Gbps/lane. The pin definition of the LCM interface is shown below.

Table 26: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_BL_A	21	PO	Current output for LCD backlight	
LCD_BL_K1	22	AI	Current sink for LCD backlight	
LCD_BL_K2	23	AI	Current sink for LCD backlight	
LCD_BL_K3	24	AI	Current sink for LCD backlight	

LCD_BL_K4	25	AI	Current sink for LCD backlight	
PWM	152	DO	PWM output	
LCD_RST	127	DO	LCD reset	
LCD_TE	126	DI	LCD tearing effect	
DSI_CLK_P	115	AO	LCD MIPI clock (+)	100 Ω differential impedance.
DSI_CLK_N	116	AO	LCD MIPI clock (-)	
DSI_LN0_P	117	AO	LCD MIPI lane 0 data (+)	
DSI_LN0_N	118	AO	LCD MIPI lane 0 data (-)	
DSI_LN1_P	119	AO	LCD MIPI lane 1 data (+)	
DSI_LN1_N	120	AO	LCD MIPI lane 1 data (-)	
DSI_LN2_P	121	AO	LCD MIPI lane 2 data (+)	
DSI_LN2_N	122	AO	LCD MIPI lane 2 data (-)	
DSI_LN3_P	123	AO	LCD MIPI lane 3 data (+)	
DSI_LN3_N	124	AO	LCD MIPI lane 3 data (-)	

The following figures show the reference design for LCM interface.

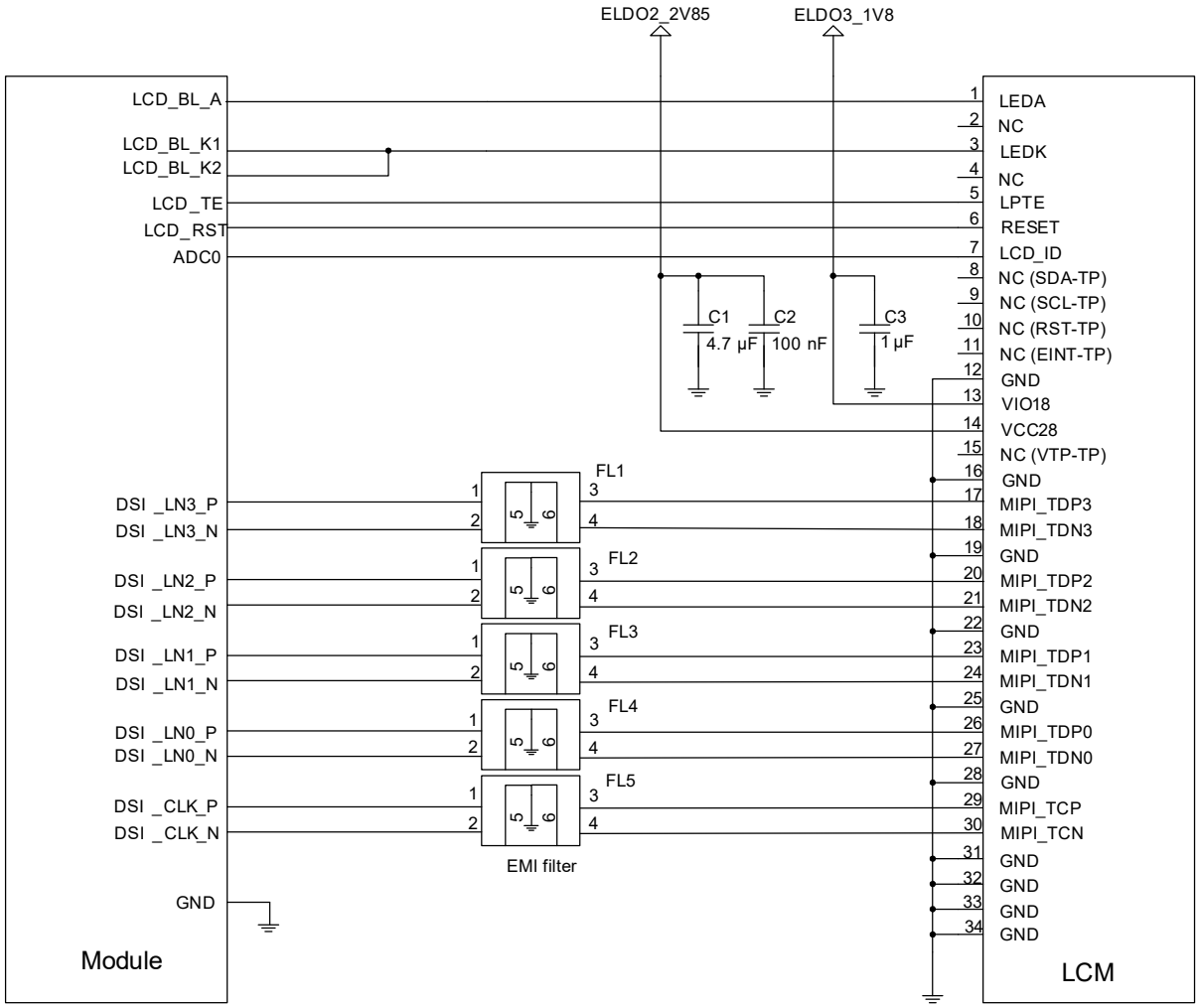


Figure 24: Reference Design for LCM Interface

MIPI are high-speed signal lines. It is recommended to add common-mode chokes in series near the LCM connector to reduce electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If different LCMs use the same model of IC, it is recommended that LCM factory burn an OTP register to distinguish different screens. You can also connect the LCD_ID pin of LCM to the ADC0 pin of the module, but the output voltage of LCD_ID should not exceed the voltage range of the ADC0 pin.

NOTE

The principles for designing LCM interface are similar to those for designing camera interface in ***Chapter 4.13.1***.

4.13. Camera Interfaces

Based on MIPI CSI standard, the module supports 3 cameras (4-lane + 4-lane + 4-lane) or 4 cameras (4-lane + 4-lane + 2-lane + 1-lane), and supports up to 3 concurrently working cameras. The maximum pixel of the camera can reach up to 25 MP. The video and photo quality are determined by various factors such as the camera sensor and camera lens quality.

Table 27: Pin Definition of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
CSI0_CLK_P	77	AI	MIPI CSI0 clock (+)	100 Ω differential impedance. Used for front camera by default.
CSI0_CLK_N	78	AI	MIPI CSI0 clock (-)	
CSI0_LN0_P	79	AI	MIPI CSI0 lane 0 data (+)	
CSI0_LN0_N	80	AI	MIPI CSI0 lane 0 data (-)	
CSI0_LN1_P	81	AI	MIPI CSI0 lane 1 data (+)	
CSI0_LN1_N	82	AI	MIPI CSI0 lane 1 data (-)	
CSI0_LN2_P	83	AI	MIPI CSI0 lane 2 data (+)	
CSI0_LN2_N	84	AI	MIPI CSI0 lane 2 data (-)	
CSI0_LN3_P	85	AI	MIPI CSI0 lane 3 data (+)	
CSI0_LN3_N	86	AI	MIPI CSI0 lane 3 data (-)	
CSI1_CLK_P	88	AI	MIPI CSI1 clock (+)	100 Ω differential impedance. Used for rear camera by default.
CSI1_CLK_N	89	AI	MIPI CSI1 clock (-)	
CSI1_LN0_P	90	AI	MIPI CSI1 lane 0 data (+)	
CSI1_LN0_N	91	AI	MIPI CSI1 lane 0 data (-)	
CSI1_LN1_P	92	AI	MIPI CSI1 lane 1 data (+)	
CSI1_LN1_N	93	AI	MIPI CSI1 lane 1 data (-)	
CSI1_LN2_P	94	AI	MIPI CSI1 lane 2 data (+)	
CSI1_LN2_N	95	AI	MIPI CSI1 lane 2 data (-)	
CSI1_LN3_P	96	AI	MIPI CSI1 lane 3 data (+)	
CSI1_LN3_N	97	AI	MIPI CSI1 lane 3 data (-)	
CSI2_CLK_P	183	AI	MIPI CSI2 clock (+)	100 Ω differential

CSI2_CLK_N	184	AI	MIPI CSI2 clock (-)	impedance. Used for depth camera by default.
CSI2_LN0_P	185	AI	MIPI CSI2 lane 0 data (+)	
CSI2_LN0_N	186	AI	MIPI CSI2 lane 0 data (-)	
CSI2_LN1_P	187	AI	MIPI CSI2 lane 1 data (+)	
CSI2_LN1_N	188	AI	MIPI CSI2 lane 1 data (-)	
CSI2_LN2_P	189	AI	MIPI CSI2 lane 2 data (+)	
CSI2_LN2_N	190	AI	MIPI CSI2 lane 2 data (-)	
CSI2_LN3_P	191	AI	MIPI CSI2 lane 3 data (+)	
CSI2_LN3_N	192	AI	MIPI CSI2 lane 3 data (-)	
SCAM_MCLK	100	DO	Master clock of front camera	
SCAM_RST	72	DO	Reset of front camera	
SCAM_PWDN	71	DO	Power down of front camera	
MCAM_MCLK	99	DO	Master clock of rear camera	
MCAM_RST	74	DO	Reset of rear camera	
MCAM_PWDN	73	DO	Power down of rear camera	If unused, keep this pin unconnected.
DCAM_MCLK	194	DO	Master clock of depth camera	
DCAM_RST	180	DO	Reset of depth camera	
DCAM_PWDN	181	DO	Power down of depth camera	
CAM4_MCLK	236	DO	Master clock of fourth camera	
CAM_I2C_SCL	75	OD	I2C clock of front and rear cameras	Dedicated for camera interfaces.
CAM_I2C_SDA	76	OD	I2C data of front and rear cameras	
DCAM_I2C_SDA	197	OD	I2C data of depth camera	
DCAM_I2C_SCL	196	OD	I2C clock of depth camera	

The following is a reference design for triple-camera applications.

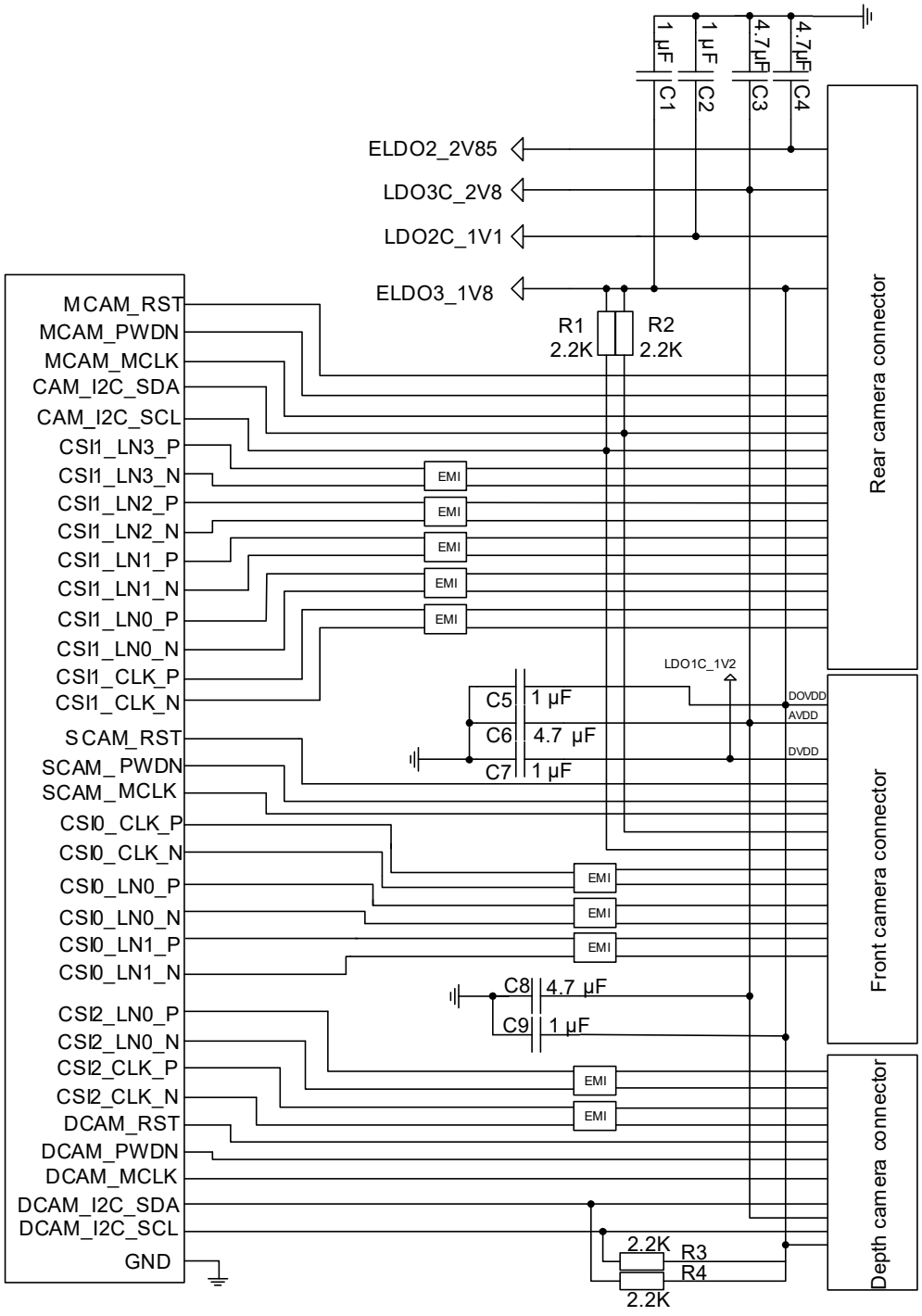


Figure 25: Reference Design of Triple-Camera Applications

4.13.1. MIPI Design Considerations

To ensure performance, the following principles should be complied with when designing LCM and camera interfaces:

- Special attention should be paid to the pin description of LCM and camera interfaces. Different video devices will have varied definitions for their corresponding connectors. Ensure that the devices and the connectors are correctly connected.
- MIPI are high-speed signal traces, supporting maximum data rate up to 2.5 Gbps. The differential impedance should be controlled to 100 Ω. Additionally, it is recommended to route the traces on the inner layer of PCB, and do not cross it with other traces. For the same group of DSI or CSI signals, keep all the MIPI traces be of the same length. To avoid crosstalk, a distance of 1.5 times the trace width among MIPI signal traces is recommended. During impedance matching, do not connect MPI signal traces to GND on different planes to ensure impedance consistency.
- It is recommended to select a TVS of low capacitance for ESD protection and the recommended parasitic capacitance should be lower than 1 pF.
- Route MIPI traces according to the following rules:
  a) The total trace length should not exceed 150 mm;
  b) Control the differential impedance to 100 Ω ±10 %;
  c) Control intra-lane length difference within 0.7 mm;
  d) Control inter-lane length difference within 1.4 mm.

Table 28: SC680A&SC686A series MIPI Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length	Length Difference (P – N)
DSI_CLK_P	115	64.61	-0.27
DSI_CLK_N	116	64.88	
DSI_LN0_P	117	64.77	0.11
DSI_LN0_N	118	64.66	
DSI_LN1_P	119	64.84	0.17
DSI_LN1_N	120	64.67	
DSI_LN2_P	121	64.73	-0.25
DSI_LN2_N	122	64.98	
DSI_LN3_P	123	64.92	-0.31
DSI_LN3_N	124	65.23	
CSI0_CLK_P	77	21.23	-0.06
CSI0_CLK_N	78	21.29	
CSI0_LN0_P	79	21.08	0.07
CSI0_LN0_N	80	21.01	

CSI0_LN1_P	81	20.79	-0.26
CSI0_LN1_N	82	21.05	
CSI0_LN2_P	83	21.15	-0.21
CSI0_LN2_N	84	21.36	
CSI0_LN3_P	85	21.12	-0.31
CSI0_LN3_N	86	21.43	
CSI1_CLK_P	88	13.48	-0.24
CSI1_CLK_N	89	13.72	
CSI1_LN0_P	90	13.49	-0.32
CSI1_LN0_N	91	13.81	
CSI1_LN1_P	92	13.37	-0.30
CSI1_LN1_N	93	13.67	
CSI1_LN2_P	94	13.43	-0.12
CSI1_LN2_N	95	13.55	
CSI1_LN3_P	96	13.35	-0.29
CSI1_LN3_N	97	13.64	
CSI2_CLK_P	183	21.10	0.12
CSI2_CLK_N	184	20.98	
CSI2_LN0_P	185	13.64	0.16
CSI2_LN0_N	186	13.48	
CSI2_LN1_P	187	13.37	0.43
CSI2_LN1_N	188	12.94	
CSI2_LN2_P	189	6.38	0.53
CSI2_LN2_N	190	5.85	
CSI2_LN3_P	191	9.66	0.08
CSI2_LN3_N	192	9.58	

Table 29: SC682A series MIPI Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length	Length Difference (P – N)
DSI_CLK_P	115	69.82	-0.01
DSI_CLK_N	116	69.83	
DSI_LN0_P	117	69.61	-0.07
DSI_LN0_N	118	69.68	
DSI_LN1_P	119	70.29	0.3
DSI_LN1_N	120	69.99	
DSI_LN2_P	121	69.94	0.15
DSI_LN2_N	122	69.79	
DSI_LN3_P	123	69.73	0.03
DSI_LN3_N	124	69.70	
CSI0_CLK_P	77	48.46	-0.3
CSI0_CLK_N	78	48.76	
CSI0_LN0_P	79	49.08	0.02
CSI0_LN0_N	80	49.06	
CSI0_LN1_P	81	48.69	-0.28
CSI0_LN1_N	82	48.97	
CSI0_LN2_P	83	49.04	0.16
CSI0_LN2_N	84	48.88	
CSI0_LN3_P	85	49.04	0.05
CSI0_LN3_N	86	48.99	
CSI1_CLK_P	88	44.51	-0.02
CSI1_CLK_N	89	44.53	
CSI1_LN0_P	90	45.16	0.07

CSI1_LN0_N	91	45.09	
CSI1_LN1_P	92	44.89	0.12
CSI1_LN1_N	93	44.77	
CSI1_LN2_P	94	45.09	0.14
CSI1_LN2_N	95	44.95	
CSI1_LN3_P	96	45.05	0.09
CSI1_LN3_N	97	44.96	
CSI2_CLK_P	183	70.45	0.02
CSI2_CLK_N	184	70.43	
CSI2_LN0_P	185	62.86	0.03
CSI2_LN0_N	186	62.83	
CSI2_LN1_P	187	62.29	-0.01
CSI2_LN1_N	188	62.30	
CSI2_LN2_P	189	55.20	-0.01
CSI2_LN2_N	190	55.21	
CSI2_LN3_P	191	58.93	-0.02
CSI2_LN3_N	192	58.95	

Table 30: Mapping of CSI Data Rates and Trace Length (D-PHY)

Data Rate	Flex Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
500 Mbps/lane	76.2	-0.5	< 260
	152.4	-1	< 190
750 Mbps/lane	76.2	-0.7	< 210
	152.4	-1.15	< 155
1.0 Gbps/lane	76.2	-0.75	< 200
	152.4	-1.4	< 125

1.5 Gbps/lane	76.2	-0.9	< 145
	152.4	-1.8	< 60
2.1 Gbps/lane	76.2	-1.3	< 170
	152.4	-2.3	< 90
2.5 Gbps/lane	76.2	-2.1	< 210
	152.4	-3.5	< 150

Table 31: Mapping of DSI Data Rates and Trace Length (D-PHY)

Data Rate	Flex Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
500 Mbps/lane	76.2	-0.5	< 280
	152.4	-1.0	< 210
750 Mbps/lane	76.2	-0.7	< 210
	152.4	-1.15	< 150
1.0 Gbps/lane	76.2	-0.75	< 200
	152.4	-1.4	< 100
1.5 Gbps/lane	76.2	-0.9	< 135
	152.4	-1.8	< 40
2.1 Gbps/lane	76.2	-1.3	< 110
	152.4	-2.3	< 80
2.5 Gbps/lane	76.2	-2.1	< 70
	152.4	-3.5	< 0

4.14. Touch Panel Interface

The module provides one I2C interface for connection with Touch Panel (TP), and provides the corresponding power supply and interrupt pins. The pin definition of touch panel interface is illustrated below.

Table 32: Pin Definition of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
TP_RST	138	DO	TP reset	
TP_INT	139	DI	TP interrupt	
TP_I2C_SCL	140	OD	TP I2C clock	TP I2C requires external pull-up circuit. Can only be used for TP interface.
TP_I2C_SDA	206	OD	TP I2C data	

A reference design for TP interface is shown below.

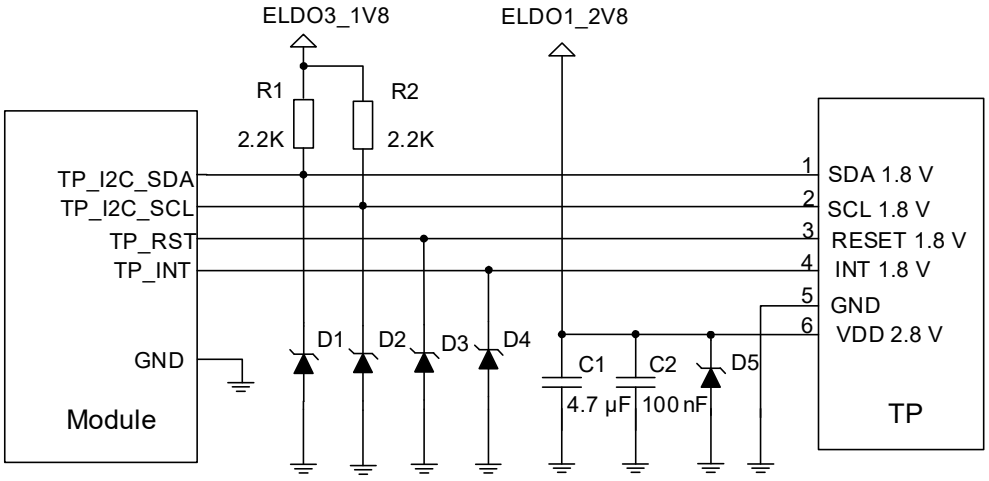


Figure 26: Reference Design for Touch Panel Interface

4.15. Sensor Interfaces

The module supports communication with sensors via I2C interface, and it supports various sensors such as acceleration sensor, gyroscopic sensor, compass, ambient light/proximity sensor, and temperature sensor.

Table 33: Pin Definition of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ACCEL_INT	252	DI	Acceleration sensor interrupt	

ALPS_INT	253	DI	Ambient light/proximity sensor interrupt	
MAG_INT	254	DI	Geomagnetic sensor interrupt	
GYRO_INT	255	DI	Gyroscopic sensor interrupt	
SENSOR_I2C_SCL	131	OD	I2C clock for external sensor	External pull-up is required for external sensors. SENSOR_I2C interface only supports sensors of the ADSP architecture. Cannot be used for touch panel, NFC, I2C keyboard, etc.
SENSOR_I2C_SDA	132	OD	I2C data for external sensor	

4.16. Flash & Torch Interfaces

The module supports 2 flash LED drivers, with maximum output current up to 1.5 A per channel. The default output current is 1000 mA in flash mode and 300 mA in torch mode.

Table 34: Pin Definition of Flash & Torch Interfaces

Pin Name	Pin No.	I/O	Description	Comment
FLASH1_LED	26	AO	Flash/torch driver output	Support flash and torch modes.
FLASH2_LED	162	AO	Flash/torch driver output	

A reference design is shown below.

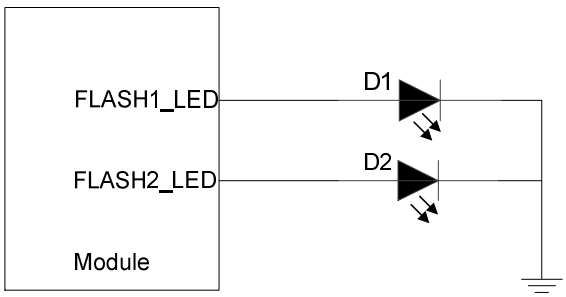


Figure 26: Reference Design for Flash & Torch Interfaces

4.17. Keypad Interfaces

The module supports three keypads: PWRKEY to turn on/off the module and VOL_UP and VOL_DOWN to adjust the volume.

Table 35: Pin Definition of Keypad Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	39	DI	Turn on/off the module	Pulled up to 1.8 V internally. Active low.
VOL_UP	146	DI	Volume up	If unused, keep these pins unconnected.
VOL_DOWN	147	DI	Volume down	

4.18. Vibration Motor Driver Interface

The module supports eccentric rotating machines (ERM). The pin definition of vibration motor driver interface is listed below.

Table 36: Pin Definition of Vibration Motor Driver Interface

Pin Name	Pin No.	I/O	Description	Comment
VIB_DRV_P	161	PO	Vibration motor driver output control	

The vibration motor is driven by an exclusive circuit, and the reference design is shown below.

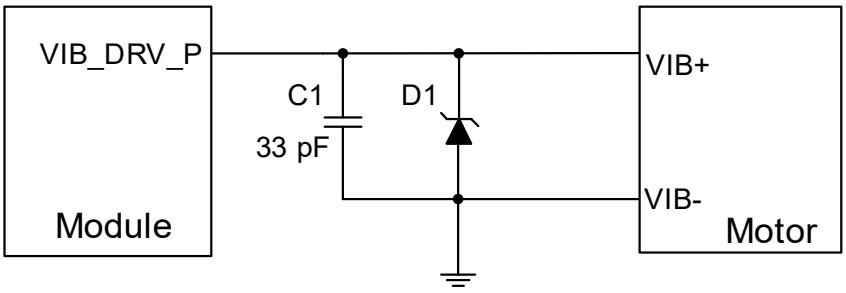


Figure 27: Reference Design for Vibration Motor Connection

4.19. RGB Interfaces [11]

SC682A series provides 3 RGB interfaces with maximum output current up to 12 mA.

Table 37: Pin Definition of RGB Interfaces

Pin Name	Pin No.	I/O	Description
RGB_R	214	AO	Current output for red LED
RGB_G	218	AO	Current output for green LED
RGB_B	222	AO	Current output for blue LED

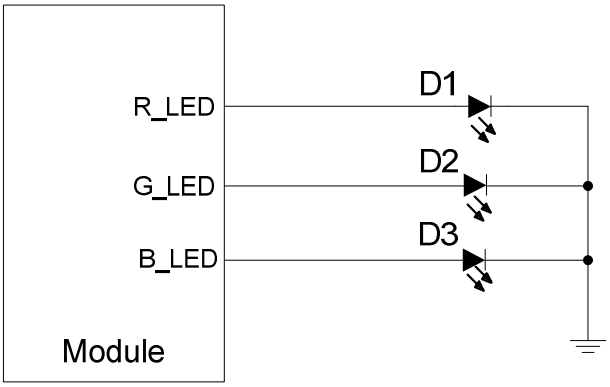


Figure 28: Reference Design for RGB Interfaces

4.20. GPIO Interfaces

The module has abundant GPIO interfaces with power domain of 1.8 V. The pin definition is listed below.

Table 38: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	I/O	Description
GPIO_65	247	DIO	General-purpose input/output

[11] RGB interfaces are supported by SC682A series only.

GPIO_66	248	DIO
GPIO_67	136	DIO
GPIO_68	137	DIO
GPIO_71	7	DIO
GPIO_80	8	DIO
GPIO_83	200	DIO
GPIO_84	201	DIO
GPIO_86	237	DIO
GPIO_96	113	DIO
GPIO_97	114	DIO
GPIO_98	232	DIO
GPIO_99	231	DIO
GPIO_100	178	DIO
GPIO_101	177	DIO
GPIO_102	250	DIO
GPIO_103	203	DIO
GPIO_104	249	DIO
GPIO_105	251	DIO
GPIO_107	238	DIO
GPIO_108	234	DIO
GPIO_111	230	DIO
GPIO_112	229	DIO

NOTE

For more details about GPIO configuration, see ***document [2]***.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to conduct a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interfaces & Frequency Bands

The pin definition is shown below:

Table 39: Pin Definition of Cellular Network Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	19	AIO	Main antenna interface	50 Ω impedance.
ANT_DRX	149	AI	Diversity antenna interface	

NOTE

Only passive antennas are supported.

Table 40: Operating Frequency of SC680A-NA&SC682A-NA&SC686A-NA

Operating Frequency	Transmit (MHz)	Receive (MHz)
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894

LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B12	699–716	729–746
LTE-FDD B13	777–787	746–756
LTE-FDD B14	788–798	758–768
LTE-FDD B17	704–716	734–746
LTE-FDD B25	1850–1915	1930–1995
LTE-FDD B26	814–849	859–894
LTE-FDD B66	1710–1780	2110–2200 [12] or 2110–2180 [13]
LTE-FDD B71	663–698	617–652
LTE-TDD B41	2496–2690	2496–2690

Table 41: Operating Frequency of SC680A-EM&SC682A-EM&SC686A-EM

Operating Frequency	Transmit (MHz)	Receive (MHz)
LTE-FDD B1	1920–1980	2110–2180
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803
LTE-TDD B38	2570–2620	2570–2620

[12] SC680A-NA&SC686A-NA B66 operating frequency supports 2110–2200 MHz.
[13] SC682A-NA B66 operating frequency supports 2110–2180 MHz.

LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2496–2690	2496–2690
WCDMA B1	1920–1980	2110–2170
WCDMA B2	1850–1910	1930–1990
WCDMA B4	1710–1755	2110–2155
WCDMA B5	824–849	869–894
WCDMA B8	880–915	925–960
GSM850	824–849	869–894
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
PCS1900	1850–1910	1930–1990

Table 42: Operating Frequency of SC680A-JP&SC682A-JP

Operating Frequency	Transmit (MHz)	Receive (MHz)
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B8	880–915	925–960
LTE-FDD B11	1427.9–1447.9	1475.9–1495.9
LTE-FDD B18	815–830	860–875
LTE-FDD B19	830–845	875–890
LTE-FDD B21	1447.9–1462.9	1495.9–1510.9
LTE-FDD B26	814–849	859–894
LTE-FDD B28	703–748	758–803
LTE-TDD B41	2496–2690	2496–2690

WCDMA B1	1920–1980	2110–2170
WCDMA B6	830–840	875–885
WCDMA B8	880–915	925–960
WCDMA B19	830–845	875–890

NOTE

SC682A-JP does not support WCDMA bands (B1/B6/B8/B19).

5.1.2. Tx Power

The following tables show the RF output power of the module.

Table 43: SC680A-NA&SC682A-NA&SC682A-JP&SC686A-NA Tx Power

Frequency Bands	Max. Tx Power	Min. Tx Power
LTE	23 dBm ±2 dB	< -39 dBm

Table 44: SC680A-EM&SC682A-EM&SC686A-EM Tx Power

Frequency Bands	Max. Tx Power	Min. Tx Power
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE	23 dBm ±2 dB	< -39 dBm
WCDMA	23 dBm ±2 dB	< -49 dBm

Table 45: SC680A-JP Tx Power

Frequency Bands	Max. Tx Power	Min. Tx Power

LTE	23 dBm ±2 dB	< -39 dBm
WCDMA	23 dBm ±2 dB	< -49 dBm

NOTE

For GPRS transmission on 4 uplink timeslots, the maximum output power reduction is 4.0 dB. The design conforms to *3GPP TS 51.010-1* ***subclause 13.16***.

5.1.3. Rx Sensitivity

The following tables show conducted RF receiver sensitivity of the module.

Table 46: Conducted RF Receiver Sensitivity of SC680A-NA&SC686A-NA (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
LTE-FDD B2 (10 MHz)	-98.4	-98	-101.2	-94.3
LTE-FDD B4 (10 MHz)	-97.1	-98.4	-100.8	-96.3
LTE-FDD B5 (10 MHz)	-99	-99.4	-102.2	-94.3
LTE-FDD B7 (10 MHz)	-95.9	-97.9	-100.1	-94.3
LTE-FDD B12 (10 MHz)	-98.6	-97.2	-101.1	-93.3
LTE-FDD B13 (10 MHz)	-98.6	-97.9	-101.4	-93.3
LTE-FDD B14 (10 MHz)	-98.2	-96.9	-100.7	-93.3
LTE-FDD B17 (10 MHz)	-97.3	-97.2	-100.4	-93.3
LTE-FDD B25 (10 MHz)	-98.2	-98	-101.1	-92.8
LTE-FDD B26 (10 MHz)	-98.8	-99.7	-102	-93.8
LTE-FDD B66 (10 MHz)	-96.8	-98.4	-100.7	-95.8
LTE-FDD B71 (10 MHz)	-97	-97.1	-100.2	-93.5
LTE-TDD B41 (10 MHz)	-96.2	-96.8	-99.5	-94.3

Table 47: Conducted RF Receiver Sensitivity of SC682A-NA (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
LTE-FDD B2 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B4 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B12 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B13 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B14 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B17 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B25 (10 MHz)	TBD	TBD	TBD	-92.8
LTE-FDD B26 (10 MHz)	TBD	TBD	TBD	-93.8
LTE-FDD B66 (10 MHz)	TBD	TBD	TBD	-95.8
LTE-FDD B71 (10 MHz)	TBD	TBD	TBD	-93.5
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3

Table 48: Conducted RF Receiver Sensitivity of SC680A-EM&SC686A-EM(Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	-109.5	-	-	-102.4
EGSM900	-110	-	-	-102.4
DCS1800	-109.5	-	-	-102.4
PCS1900	-108	-	-	-102.4
WCDMA B1	-109.2	-109.8	-	-106.7

WCDMA B2	-108.5	-108.5	-	-104.7
WCDMA B4	-109.2	-110	-	-106.7
WCDMA B5	-109.5	-112.5	-	-104.7
WCDMA B8	-109.3	-112	-	-103.7
LTE-FDD B1 (10 MHz)	-97.5	-98	-101	-96.3
LTE-FDD B2 (10 MHz)	-97.3	-96.8	-100.2	-94.3
LTE-FDD B3 (10 MHz)	-97.5	-97.5	-101	-93.3
LTE-FDD B4 (10 MHz)	-97.3	-98	-101	-96.3
LTE-FDD B5 (10 MHz)	-98.5	-100	-102.5	-94.3
LTE-FDD B7 (10 MHz)	-95.1	-97.2	-99.5	-94.3
LTE-FDD B8 (10 MHz)	-99.3	-99.5	-102.5	-93.3
LTE-FDD B20 (10 MHz)	-99	-99	-102	-93.3
LTE-FDD B28 (10 MHz)	-99.3	-99	-102.2	-94.8
LTE-TDD B38 (10 MHz)	-96.5	-97.5	-99.3	-96.3
LTE-TDD B40 (10 MHz)	-96.5	-97.5	-100.5	-96.3
LTE-TDD B41 (10 MHz)	-95.3	-96.3	-99	-94.3

Table 49: Conducted RF Receiver Sensitivity of SC682A-EM (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	TBD	-	-	-102.4
EGSM900	TBD	-	-	-102.4
DCS1800	TBD	-	-	-102.4
PCS1900	TBD	-	-	-102.4
WCDMA B1	TBD	TBD	-	-106.7
WCDMA B2	TBD	TBD	-	-104.7

WCDMA B4	TBD	TBD	-	-106.7
WCDMA B5	TBD	TBD	-	-104.7
WCDMA B8	TBD	TBD	-	-103.7
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B2 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B4 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B20 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B28 (10 MHz)	TBD	TBD	TBD	-94.8
LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B40 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3

Table 50: Conducted RF Receiver Sensitivity of SC680A-JP (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
LTE-FDD B1 (10 MHz)	-98	-98.8	-101.5	-96.3
LTE-FDD B3 (10 MHz)	-98	-98.8	-101.6	-93.3
LTE-FDD B5 (10 MHz)	-99.1	-99.7	-102.4	-94.3
LTE-FDD B8 (10 MHz)	-99.2	-99.7	-102.5	-93.3
LTE-FDD B11 (10 MHz)	-98.2	-99.7	-101.8	-96.3
LTE-FDD B18 (10 MHz)	-98.9	-99.8	-102.4	-96.3
LTE-FDD B19 (10 MHz)	-98.9	-99.7	-102.4	-96.3

LTE-FDD B21 (10 MHz)	-98.1	-98.5	-101.3	-96.3
LTE-FDD B26 (10 MHz)	-99	-99.7	-102.4	-93.8
LTE-FDD B28 (10 MHz)	-98.9	-99.7	-102.4	-94.8
LTE-TDD B41 (10 MHz)	-96	-96.9	-99.7	-94.3
WCDMA B1	-110.2	-111.2	-	-106.7
WCDMA B6	-111.2	-112.3	-	-106.7
WCDMA B8	-111.4	-111.9	-	-104.7
WCDMA B19	-111.2	-112.3	-	-106.7

Table 51: Conducted RF Receiver Sensitivity of SC682A-JP (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B11 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B18 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B19 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B21 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B26 (10 MHz)	TBD	TBD	TBD	-93.8
LTE-FDD B28 (10 MHz)	TBD	TBD	TBD	-94.8
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3

5.1.4. Reference Design

The module provides main and diversity RF antenna interfaces for antenna connection.

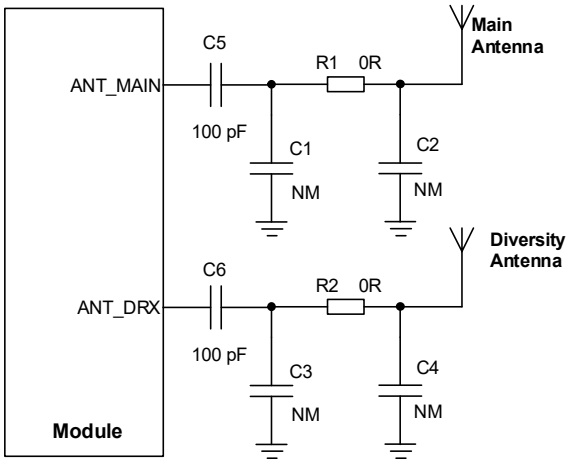


Figure 29: Reference Design for Main and Diversity Antenna Interfaces

NOTE

1. To improve receiver sensitivity, ensure that the clearance among antennas is appropriate.
2. Use a dual L-type circuit for all the antenna interfaces for better cellular performance and easy debugging.
3. Capacitors(C1/C2/C3/C4) are not mounted by default.
4. Place the dual L-type matching components (C5 & C1 & R1 & C2, C6 & C3 & R2 & C4) to antennas as close as possible.
5. If there is DC power at the antenna ports, C5 and C6 must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, C5 and C6 should not be reserved.

5.2. GNSS [14] (Optional)

The module integrates the IZat™ GNSS engine (Gen 8C) which supports multiple positioning and navigation systems including GPS, GLONASS, BDS, Galileo, SBAS and QZSS. With an embedded LNA, the module provides greatly improved positioning accuracy.

5.2.1. Antenna Interface & Frequency Bands

The following tables show the pin definition and frequency of GNSS antenna interface.

[14] SC680A-WF, SC682A-WF and SC686A-WF do not support GNSS.

Table 52: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	134	AI	GNSS antenna interface	50 Ω impedance.

Table 53: GNSS Frequency

GNSS Constellation Types	Frequency	Unit
GPS	1575.42 ±1.023 (L1)	MHz
GLONASS	1601.7 ±4.2	
Galileo	1575.42 ±2.046	
BDS	1561.098 ±2.046	
QZSS	1575.42 ±1.023 (L1)	
SBAS	1575.42 ±1.023 (L1)	

5.2.2. GNSS Performance

Table 54: GNSS Performance of SC680A&SC686A series

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-146	dBm
	Reacquisition	Autonomous	-158	
	Tracking	Autonomous	-158	
TTFF	Cold start @ open sky	Autonomous	34.5	s
		AGNSS start	9.3	
	Warm start @ open sky	Autonomous	25.4	
		AGNSS start	1.3	
	Hot start @ open sky	Autonomous	2.2	
		AGNSS start	1.4	

Accuracy	CEP-50	Autonomous @ open sky	2.5	m

Table 55: GNSS Performance of SC682A series

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	TBD	dBm
	Reacquisition	Autonomous	TBD	
	Tracking	Autonomous	TBD	
TTFF	Cold start @ open sky	Autonomous	TBD	s
		AGNSS start	TBD	
	Warm start @ open sky	Autonomous	TBD	
		AGNSS start	TBD	
	Hot start @ open sky	Autonomous	TBD	
		AGNSS start	TBD	
Accuracy	CEP-50	Autonomous @ open sky	TBD	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

5.2.3.1. Recommended Design of Passive Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A

reference design is given below.

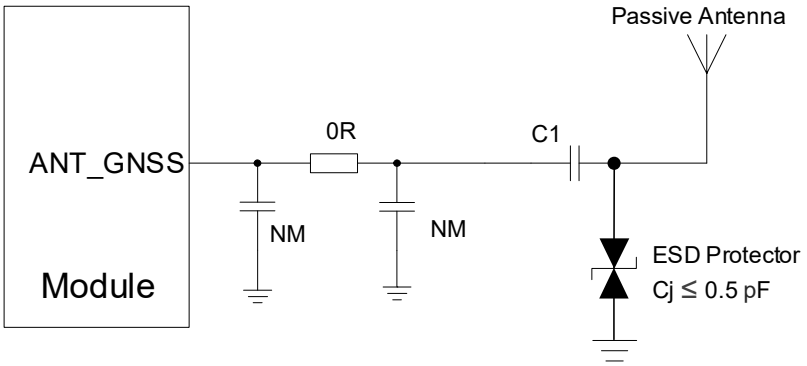


Figure 30: Reference Design for Passive Antenna

NOTE

1. It is not recommended to add an external LNA when using a passive GNSS antenna.
2. If there is DC power at the antenna ports, C1 must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, C1 should not be reserved.

5.2.3.2. Recommended Design of Active Antenna

In any case, it is recommended to use a passive antenna. If an active antenna is indeed needed in your application, it is recommended to reserve a π-type attenuation circuit and use a high-performance LDO in the power system design. The active antenna is powered by a 56 nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3 V to 5.0 V. Although featuring low power consumption, the active antenna still requires stable and clean power supplies. It is recommended to use high-performance LDO as the power supply. A reference design for the active GNSS antenna is shown below.

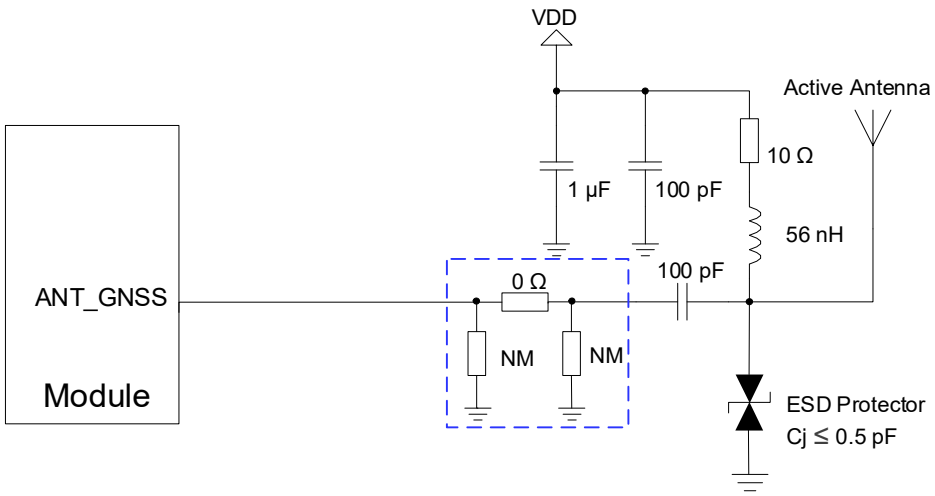


Figure 31: Reference Design for Active Antenna

NOTE

It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.2.3.3. GNSS RF Design Guidelines

Improper design of antenna and layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, or reduced positioning accuracy. In order to avoid this, follow the reference design rules as below:

- Maximize the distance between the GNSS part and the other RF part (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, GNSS RF signal traces and RF components should be placed far away from high-speed circuits, switch-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with a harsh electromagnetic environment or with high requirement on ESD protection, it is recommended to add ESD protection components for the antenna interface. Only components with ultra-low junction capacitance such as 0.5 pF can be selected. Otherwise, there will be effects on the impedance characteristic of the RF circuit loop or attenuation of the bypass RF signal may be caused.
- Keep the impedance of either feeder line or PCB trace as 50 Ω, and keep the trace length as short as possible.

5.3. Wi-Fi/Bluetooth

The module provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth functions. The interface impedance is 50 Ω. You can connect external antennas such as PCB antenna, sucker antenna and ceramic antenna to the module via these interfaces to achieve Wi-Fi and Bluetooth functions.

Table 56: Pin Definition of Wi-Fi/Bluetooth Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	129	AIO	Wi-Fi/Bluetooth antenna interface	50 Ω impedance.

Table 57: Wi-Fi/Bluetooth Frequency

Type	Frequency	Unit
Wi-Fi 802.11a/b/g/n/ac	2400–2483.5MHz 5150–5850 MHz	MHz
Bluetooth 5.0/5.1	2402–2480	MHz

5.3.1. Wi-Fi

The module supports 2.4 GHz and 5 GHz dual-band WLAN wireless communication based on IEEE 802.11a/b/g/n/ac standard protocols. The maximum data rate is up to 433 Mbps. The features are as below:

- Wake-on-WLAN (WoWLAN)
- AP and STA modes
- Wi-Fi Direct
- MCS 0–7 for HT20 and HT40
- MCS 0–8 for VHT20
- MCS 0–9 for VHT40 and VHT80

The following tables list the Wi-Fi transmitting and receiving performance of the module.

Table 58: Wi-Fi Transmitting Performance

Bands	Standard	Data Rates	Output Power
2.4 GHz	802.11b	1 Mbps	16 dBm ±2.5 dB

	802.11b	11 Mbps	16 dBm ±2.5 dB
	802.11g	6 Mbps	16 dBm ±2.5 dB
	802.11g	54 Mbps	14 dBm ±2.5 dB
	802.11n HT20	MCS 0	15 dBm ±2.5 dB
	802.11n HT20	MCS 7	13 dBm ±2.5 dB
	802.11n HT40	MCS 0	14 dBm ±2.5 dB
	802.11n HT40	MCS 7	13 dBm ±2.5 dB
5 GHz	802.11a	6 Mbps	15 dBm ±2.5 dB
	802.11a	54 Mbps	13 dBm ±2.5 dB
	802.11n HT20	MCS 0	15 dBm ±2.5 dB
	802.11n HT20	MCS 7	13 dBm ±2.5 dB
	802.11n HT40	MCS 0	15 dBm ±2.5 dB
	802.11n HT40	MCS 7	13 dBm ±2.5 dB
	802.11ac VHT20	MCS 0	15 dBm ±2.5 dB
	802.11ac VHT20	MCS 8	13 dBm ±2.5 dB
	802.11ac VHT40	MCS 0	14 dBm ±2.5 dB
	802.11ac VHT40	MCS 9	12 dBm ±2.5 dB
	802.11ac VHT80	MCS 0	14 dBm ±2.5 dB
	802.11ac VHT80	MCS 9	12 dBm ±2.5 dB

Table 59: Wi-Fi Receiving Performance of SC680A&SC686A Series

Bands	Standard	Data Rates	Sensitivity (dBm)
2.4 GHz	802.11b	1 Mbps	-96
	802.11b	11 Mbps	-88
	802.11g	6 Mbps	-90
	802.11g	54 Mbps	-74

	802.11n HT20	MCS 0	-89
	802.11n HT20	MCS 7	-70
	802.11n HT40	MCS 0	-87
	802.11n HT40	MCS 7	-67
5 GHz	802.11a	6 Mbps	-89
	802.11a	54 Mbps	-74
	802.11n HT20	MCS 0	-88
	802.11n HT20	MCS 7	-69
	802.11n HT40	MCS 0	-85
	802.11n HT40	MCS 7	-66
	802.11ac VHT20	MCS 0	-89
	802.11ac VHT20	MCS 8	-66
	802.11ac VHT40	MCS 0	-86
	802.11ac VHT40	MCS 9	-62
	802.11ac VHT80	MCS 0	-82
	802.11ac VHT80	MCS 9	-58

Table 60: Wi-Fi Receiving Performance of SC682A Series

Bands	Standard	Data Rates	Sensitivity (dBm)
2.4 GHz	802.11b	1 Mbps	TBD
	802.11b	11 Mbps	TBD
	802.11g	6 Mbps	TBD
	802.11g	54 Mbps	TBD
	802.11n HT20	MCS 0	TBD
	802.11n HT20	MCS 7	TBD
	802.11n HT40	MCS 0	TBD
	802.11n HT40	MCS 7	TBD

5 GHz	802.11a	6 Mbps	TBD
	802.11a	54 Mbps	TBD
	802.11n HT20	MCS 0	TBD
	802.11n HT20	MCS 7	TBD
	802.11n HT40	MCS 0	TBD
	802.11n HT40	MCS 7	TBD
	802.11ac VHT20	MCS 0	TBD
	802.11ac VHT20	MCS 8	TBD
	802.11ac VHT40	MCS 0	TBD
	802.11ac VHT40	MCS 9	TBD
	802.11ac VHT80	MCS 0	TBD
	802.11ac VHT80	MCS 9	TBD

NOTE

The module conforms to the IEEE 802.11a/b/g/n/ac specifications.

5.3.2. Bluetooth

SC680A&SC682A series support Bluetooth 5.1 (BR/EDR+BLE) specification as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes, while SC686A series supports Bluetooth 5.0 (BR/EDR+BLE) specification as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally support up to 7 wireless connections.
- Maximally support up to 3.5 Piconets simultaneously.
- Support one SCO (Synchronous Connection Oriented) or eSCO connection.

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 61: Bluetooth Data Rates and Versions

Version	Data rate	Maximum Application Throughput

1.2	1 Mbit/s	> 80 Kbit/s
2.0 + EDR	3 Mbit/s	> 80 Kbit/s
3.0 + HS	24 Mbit/s	Refer to 3.0 + HS
4.0	24 Mbit/s	Refer to 4.0 LE
5.0	48 Mbit/s	Refer to 5.0 LE
5.1	TBD	TBD

Referenced specifications are listed below:

- *Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009*
- *Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009*
- *Bluetooth 5.0 RF-PHY Cover Standard: RF-PHY.TS.5.0.0, December 06, 2016*

The following table lists the Bluetooth transmitting and receiving performance of the module.

Table 62: Bluetooth Tx and Rx Performance of SC680A&SC686A Series (Unit: dBm)

Transmitting Performance			
Packet Types	DH5	2-DH5	3-DH5
Transmitting Power	8 ±2.5	6 ±2.5	6 ±2.5
Receiving Performance			
Packet Types	DH5	2-DH5	3-DH5
Receiving Sensitivity	-92	-92	-86

Table 63: Bluetooth Tx and Rx Performance of SC682A Series (Unit: dBm)

Transmitting Performance			
Packet Types	DH5	2-DH5	3-DH5
Transmitting Power	8 ±2.5	6 ±2.5	6 ±2.5

Receiving Performance			
Packet Types	DH5	2-DH5	3-DH5
Receiving Sensitivity	TBD	TBD	TBD

5.3.3. Reference Design

A reference design for Wi-Fi/Bluetooth antenna interface is shown as below. C1 and C2 are not mounted and a 0 Ω resistor (R1) is mounted by default.

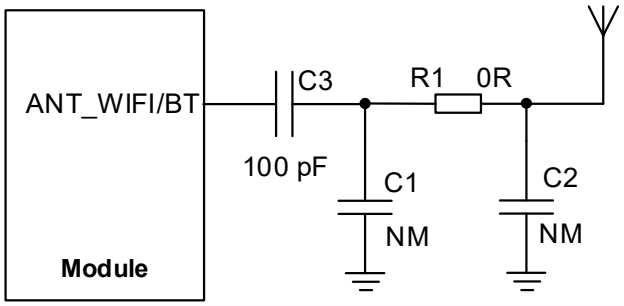


Figure 32: Reference Design for Wi-Fi/Bluetooth Antenna

NOTE

If there is DC power at the antenna ports, C3 must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, C3 should not be reserved.

5.4. RF Routing Guidelines

For your PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

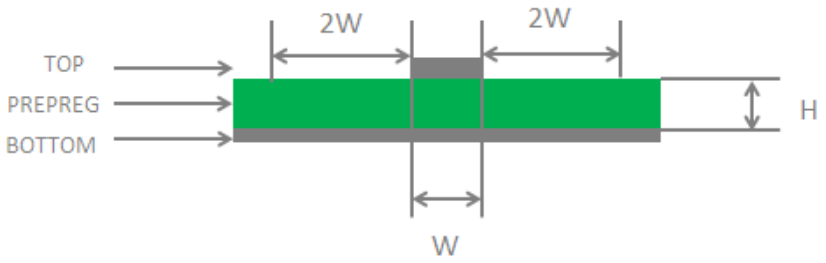


Figure 33: Microstrip Design on a 2-layer PCB

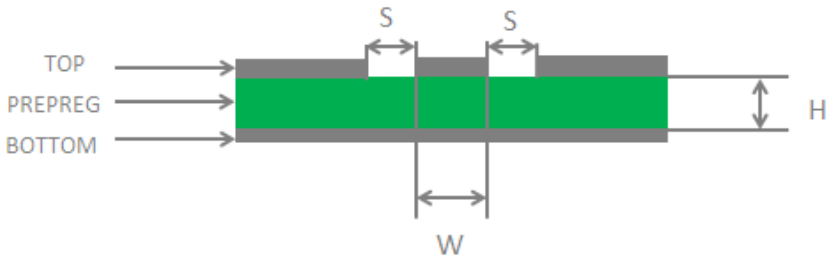


Figure 34: Coplanar Waveguide Design on a 2-layer PCB

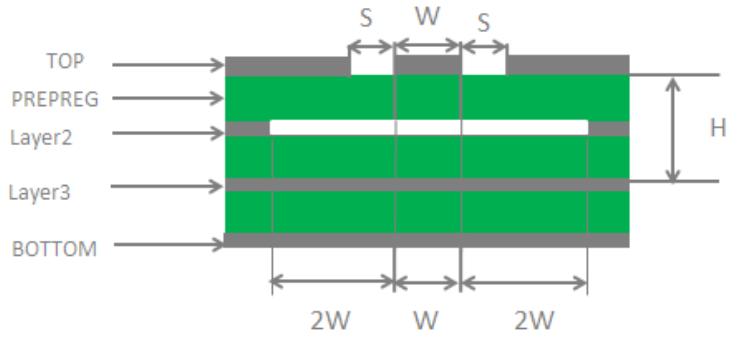


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

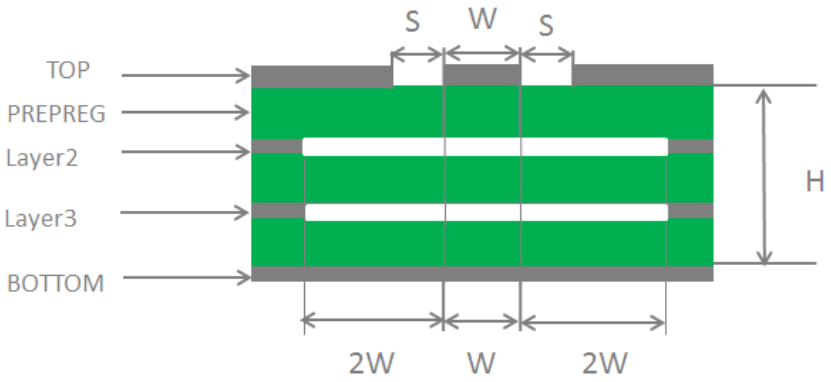


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

5.5. Antenna Design Requirements

Table 64: Antenna Design Requirements

Antenna Type	Requirements
GNSS (Optional)	Frequency range :1559–1609 MHz Polarization: RHCP or linear VSWR: ≤ 2 (Typ.)
	For passive antenna usage: Passive antenna gain: > 0 dBi
	For active antenna usage: Active antenna noise figure: < 1.5 dB (Typ.) Active antenna embedded LNA gain: < 17 dB (Typ.)
Cellular	VSWR: ≤ 2 Efficiency: > 30 % Gain: 1 dBi Max input power: 50 W Input impedance: 50 Ω Polarization: Vertical Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz)

	< 2 dB: HB (> 2.3 GHz)
Wi-Fi/Bluetooth	VSWR: ≤ 2 Gain: 1 dBi Max Input Power: 50 W Input Impedance: 50 Ω Polarization Type: Vertical Cable Insertion Loss: < 1 dB

5.6. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connectors provided by Hirose.

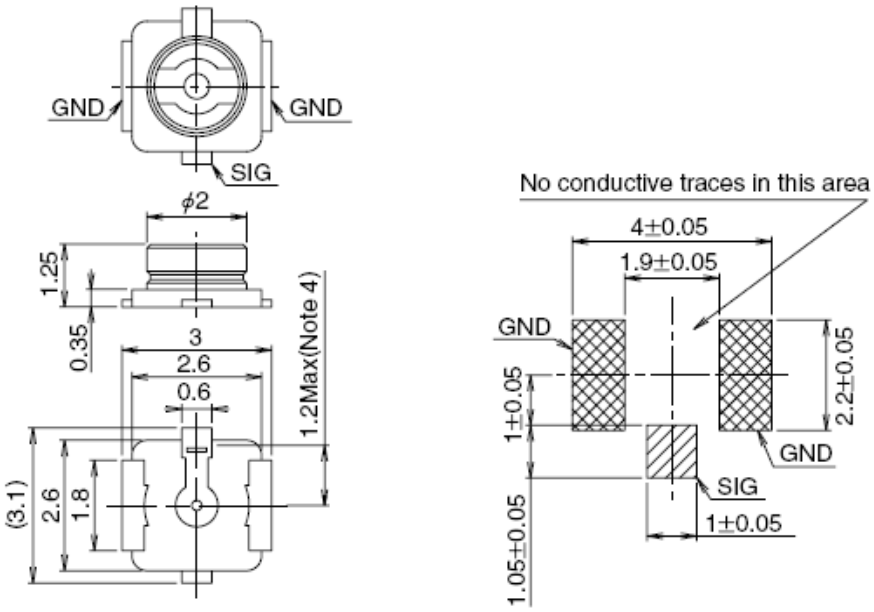


Figure 37: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

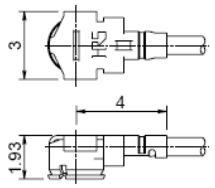
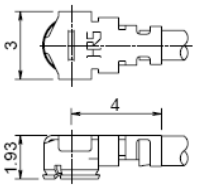
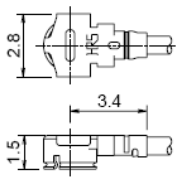
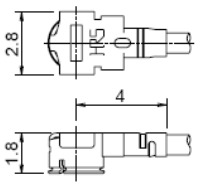
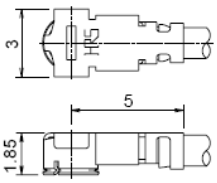
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 38: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connector.

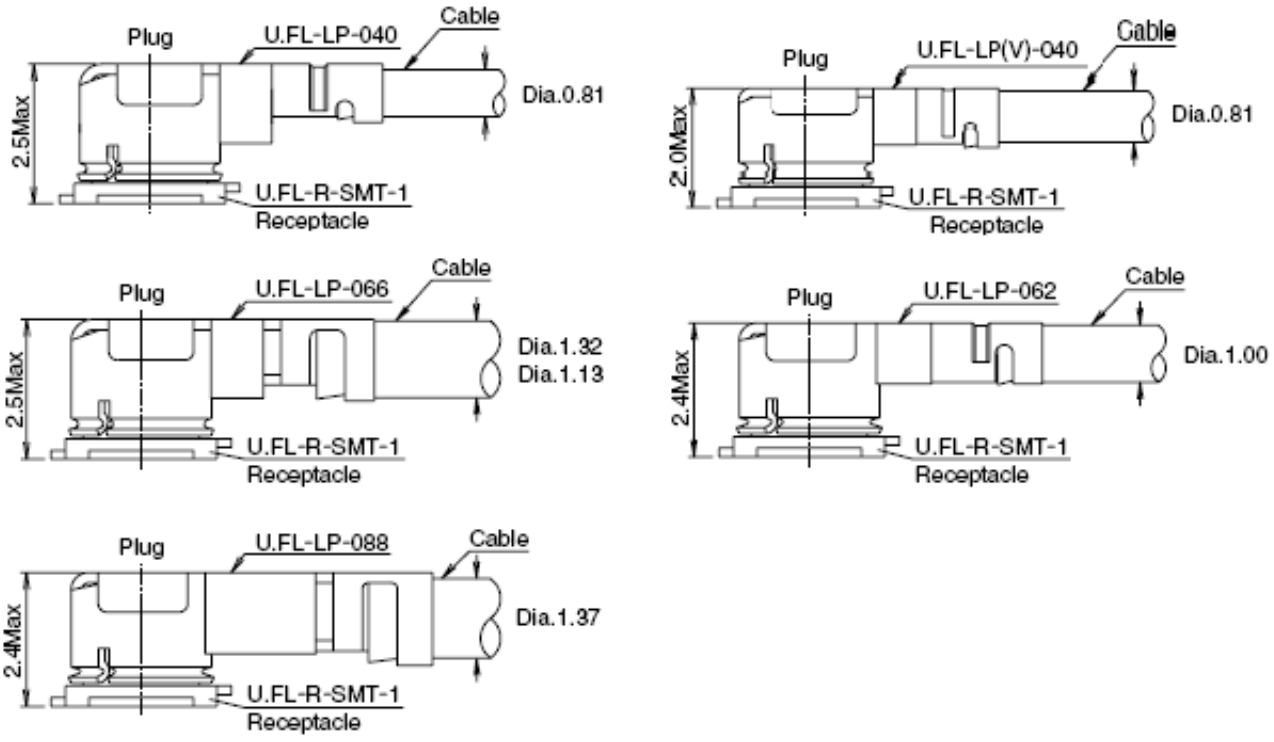


Figure 39: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 65: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.3	4.75	V
USB_VBUS	-0.3	16	V
Peak current of VBAT	-	3	A
Voltage on digital pins	-0.3	2.09	V

6.2. Power Supply Ratings

Table 66: Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltages must be kept between the minimum and maximum values.	3.55	3.8	4.4	V
	Voltage drop during transmitting burst	At maximum power control level	0	0	400	mV
I_{VBAT}	Peak supply current	At maximum power control level	-	1.8	3.0	A

USB_VBUS	USB connection detection	-	4	-	10	V

6.3. Power Consumption

Table 67: SC680A-NA&SC686A-NA Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power off	100	μA
Sleep state	Screen out	4.1	mA
LTE-FDD supply current Sleep state (USB disconnected)	LTE-FDD PF = 32	6.08	mA
	LTE-FDD PF = 64	4.93	mA
	LTE-FDD PF = 128	4.40	mA
	LTE-FDD PF = 256	4.09	mA
LTE-TDD supply current Sleep state (USB disconnected)	LTE-TDD PF = 32	6.24	mA
	LTE-TDD PF = 64	5.10	mA
	LTE-TDD PF = 128	4.45	mA
	LTE-TDD PF = 256	4.10	mA
LTE data transfer	LTE-FDD B2 @ max. power	657	mA
	LTE-FDD B4 @ max. power	608	mA
	LTE-FDD B5 @ max. power	595	mA
	LTE-FDD B7 @ max. power	901	mA
	LTE-FDD B12 @ max. power	749	mA
	LTE-FDD B13 @ max. power	617	mA
	LTE-FDD B14 @ max. power	593	mA
	LTE-FDD B17 @ max. power	771	mA
	LTE-FDD B25 @ max. power	736	mA
	LTE-FDD B26 @ max. power	633	mA

	LTE-FDD B66 @ max. power	583	mA
	LTE-FDD B71 @ max. power	582	mA
	LTE-TDD B41 @ max. power	402	mA

Table 68: SC682A-NA Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power off	TBD	μA
Sleep state	Screen out	TBD	mA
LTE-FDD supply current Sleep state (USB disconnected)	LTE-FDD PF = 32	TBD	mA
	LTE-FDD PF = 64	TBD	mA
	LTE-FDD PF = 128	TBD	mA
	LTE-FDD PF = 256	TBD	mA
LTE-TDD supply current Sleep state (USB disconnected)	LTE-TDD PF = 32	TBD	mA
	LTE-TDD PF = 64	TBD	mA
	LTE-TDD PF = 128	TBD	mA
	LTE-TDD PF = 256	TBD	mA
LTE data transfer	LTE-FDD B2 @ max. power	TBD	mA
	LTE-FDD B4 @ max. power	TBD	mA
	LTE-FDD B5 @ max. power	TBD	mA
	LTE-FDD B7 @ max. power	TBD	mA
	LTE-FDD B12 @ max. power	TBD	mA
	LTE-FDD B13 @ max. power	TBD	mA
	LTE-FDD B14 @ max. power	TBD	mA
	LTE-FDD B17 @ max. power	TBD	mA
	LTE-FDD B25 @ max. power	TBD	mA
	LTE-FDD B26 @ max. power	TBD	mA

	LTE-FDD B66 @ max. power	TBD	mA
	LTE-FDD B71 @ max. power	TBD	mA
	LTE-TDD B41 @ max. power	TBD	mA

Table 69: SC680A-EM&SC686A-EM Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power off	100	μA
Sleep state	Screen out	4.1	mA
GSM supply current Sleep state (USB disconnected)	Sleep state (USB disconnected) @ DRX=2	5.63	mA
	Sleep state (USB disconnected) @ DRX=5	4.66	mA
	Sleep state (USB disconnected) @ DRX=9	4.44	mA
WCDMA supply current Sleep state (USB disconnected)	WCDMA PF = 64	4.94	mA
	WCDMA PF = 128	4.43	mA
	WCDMA PF = 256	4.23	mA
	WCDMA PF = 512	4.14	mA
LTE-FDD supply current Sleep state (USB disconnected)	LTE-FDD PF = 32	6.42	mA
	LTE-FDD PF = 64	5.15	mA
	LTE-FDD PF = 128	4.57	mA
	LTE-FDD PF = 256	4.26	mA
LTE-TDD supply current Sleep state (USB disconnected)	LTE-TDD PF = 32	6.53	mA
	LTE-TDD PF = 64	5.31	mA
	LTE-TDD PF = 128	4.67	mA
	LTE-TDD PF = 256	4.22	mA
WCDMA voice call	B1 @ max. power	582	mA
	B2 @ max. power	566	mA
	B4 @ max. power	547	mA

	B5 @ max. power	508	mA
	B8 @ max. power	510	mA
GPRS data transfer	GSM850 @ 1DL 4UL	602	mA
	GSM900 @ 1DL 4UL	568	mA
	DCS1800 @ 1DL 4UL	430	mA
	PCS1900 @ 1DL 4UL	435	mA
EDGE data transfer	GSM850 @ 1DL 4UL	598	mA
	GSM900 @ 1DL 4UL	554	mA
	DCS1800 @ 1DL 4UL	477	mA
	PCS1900 @ 1DL 4UL	473	mA
LTE data transfer	LTE-FDD B1 @ max. power	630	mA
	LTE-FDD B2 @ max. power	578	mA
	LTE-FDD B3 @ max. power	601	mA
	LTE-FDD B4 @ max. power	576	mA
	LTE-FDD B5 @ max. power	551	mA
	LTE-FDD B7 @ max. power	809	mA
	LTE-FDD B8 @ max. power	581	mA
	LTE-FDD B20 @ max. power	599	mA
	LTE-FDD B28 @ max. power	567	mA
	LTE-TDD B38 @ max. power	417	mA
	LTE-TDD B40 @ max. power	432	mA
	LTE-TDD B41 @ max. power	417	mA
GSM voice call	GSM850 @ PCL 5	318	mA
	GSM900 @ PCL 5	303	mA
	DCS1800 @ PCL 0	249	mA
	PCS1900 @ PCL 0	222	mA

WCDMA data transfer	B1 (HSDPA) @ max. power	542	mA
	B2 (HSDPA) @ max. power	514	mA
	B4 (HSDPA) @ max. power	531	mA
	B5 (HSUPA) @ max. power	472	mA
	B8 (HSDPA) @ max. power	470	mA
	B1 (HSUPA) @ max. power	547	mA
	B2 (HSUPA) @ max. power	518	mA
	B4 (HSUPA) @ max. power	537	mA
	B5 (HSUPA) @ max. power	492	mA
	B8 (HSUPA) @ max. power	490	mA

Table 70: SC682A-EM Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power off	TBD	μA
Sleep state	Screen out	TBD	mA
GSM supply current Sleep state (USB disconnected)	Sleep state (USB disconnected) @ DRX=2	TBD	mA
	Sleep state (USB disconnected) @ DRX=5	TBD	mA
	Sleep state (USB disconnected) @ DRX=9	TBD	mA
WCDMA supply current Sleep state (USB disconnected)	WCDMA PF = 64	TBD	mA
	WCDMA PF = 128	TBD	mA
	WCDMA PF = 256	TBD	mA
	WCDMA PF = 512	TBD	mA
LTE-FDD supply current Sleep state (USB disconnected)	LTE-FDD PF = 32	TBD	mA
	LTE-FDD PF = 64	TBD	mA
	LTE-FDD PF = 128	TBD	mA
	LTE-FDD PF = 256	TBD	mA

LTE-TDD supply current Sleep state (USB disconnected)	LTE-TDD PF = 32	TBD	mA
	LTE-TDD PF = 64	TBD	mA
	LTE-TDD PF = 128	TBD	mA
	LTE-TDD PF = 256	TBD	mA
WCDMA voice call	B1 @ max. power	TBD	mA
	B2 @ max. power	TBD	mA
	B4 @ max. power	TBD	mA
	B5 @ max. power	TBD	mA
	B8 @ max. power	TBD	mA
GPRS data transfer	GSM850 @ 1DL 4UL	TBD	mA
	GSM900 @ 1DL 4UL	TBD	mA
	DCS1800 @ 1DL 4UL	TBD	mA
	PCS1900 @ 1DL 4UL	TBD	mA
EDGE data transfer	GSM850 @ 1DL 4UL	TBD	mA
	GSM900 @ 1DL 4UL	TBD	mA
	DCS1800 @ 1DL 4UL	TBD	mA
	PCS1900 @ 1DL 4UL	TBD	mA
LTE data transfer	LTE-FDD B1 @ max. power	TBD	mA
	LTE-FDD B2 @ max. power	TBD	mA
	LTE-FDD B3 @ max. power	TBD	mA
	LTE-FDD B4 @ max. power	TBD	mA
	LTE-FDD B5 @ max. power	TBD	mA
	LTE-FDD B7 @ max. power	TBD	mA
	LTE-FDD B8 @ max. power	TBD	mA
	LTE-FDD B20 @ max. power	TBD	mA
	LTE-FDD B28 @ max. power	TBD	mA

	LTE-TDD B38 @ max. power	TBD	mA
	LTE-TDD B40 @ max. power	TBD	mA
	LTE-TDD B41 @ max. power	TBD	mA
GSM voice call	GSM850 @ PCL 5	TBD	mA
	GSM900 @ PCL 5	TBD	mA
	DCS1800 @ PCL 0	TBD	mA
	PCS1900 @ PCL 0	TBD	mA
WCDMA data transfer	B1 (HSDPA) @ max. power	TBD	mA
	B2 (HSDPA) @ max. power	TBD	mA
	B4 (HSDPA) @ max. power	TBD	mA
	B5 (HSUPA) @ max. power	TBD	mA
	B8 (HSDPA) @ max. power	TBD	mA
	B1 (HSUPA) @ max. power	TBD	mA
	B2 (HSUPA) @ max. power	TBD	mA
	B4 (HSUPA) @ max. power	TBD	mA
	B5 (HSUPA) @ max. power	TBD	mA
	B8 (HSUPA) @ max. power	TBD	mA

Table 71: SC680A-JP Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power off	101	μA
Sleep state	Screen out	4.32	mA
WCDMA supply current Sleep state (USB disconnected)	WCDMA PF = 64	4.68	mA
	WCDMA PF = 128	4.11	mA
	WCDMA PF = 256	3.89	mA
	WCDMA PF = 512	3.79	mA
LTE-FDD supply current	LTE-FDD PF = 32	5.88	mA

Sleep state (USB disconnected)	LTE-FDD PF = 64	4.79	mA
	LTE-FDD PF = 128	4.21	mA
	LTE-FDD PF = 256	3.93	mA
LTE-TDD supply current Sleep state (USB disconnected)	LTE-TDD PF = 32	6.14	mA
	LTE-TDD PF = 64	4.87	mA
	LTE-TDD PF = 128	4.25	mA
	LTE-TDD PF = 256	3.95	mA
WCDMA voice call	B1 @ max. power	624	mA
	B6 @ max. power	524	mA
	B8 @ max. power	620	mA
	B19 @ max. power	530	mA
LTE data transfer	LTE-FDD B1 @ max. power	666	mA
	LTE-FDD B3 @ max. power	616	mA
	LTE-FDD B5 @ max. power	567	mA
	LTE-FDD B8 @ max. power	648	mA
	LTE-FDD B11 @ max. power	526	mA
	LTE-FDD B18 @ max. power	575	mA
	LTE-FDD B19 @ max. power	564	mA
	LTE-FDD B21 @ max. power	547	mA
	LTE-FDD B26 @ max. power	599	mA
	LTE-FDD B28 @ max. power	687	mA
	LTE-TDD B41 @ max. power	335	mA
WCDMA data transfer	B1 (HSDPA) @ max. power	570	mA
	B6 (HSDPA) @ max. power	487	mA
	B8 (HSDPA) @ max. power	660	mA
	B19 (HSDPA) @ max. power	516	mA
	B1 (HSUPA) @ max. power	611	mA

	B6 (HSUPA) @ max. power	486	mA
	B8 (HSUPA) @ max. power	659	mA
	B19 (HSUPA) @ max. power	536	mA

Table 72: SC682A-JP Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power off	TBD	μA
Sleep state	Screen out	TBD	mA
LTE-FDD supply current Sleep state (USB disconnected)	LTE-FDD PF = 32	TBD	mA
	LTE-FDD PF = 64	TBD	mA
	LTE-FDD PF = 128	TBD	mA
	LTE-FDD PF = 256	TBD	mA
LTE-TDD supply current Sleep state (USB disconnected)	LTE-TDD PF = 32	TBD	mA
	LTE-TDD PF = 64	TBD	mA
	LTE-TDD PF = 128	TBD	mA
	LTE-TDD PF = 256	TBD	mA
LTE data transfer	LTE-FDD B1 @ max. power	TBD	mA
	LTE-FDD B3 @ max. power	TBD	mA
	LTE-FDD B5 @ max. power	TBD	mA
	LTE-FDD B8 @ max. power	TBD	Ma
LTE data transfer	LTE-FDD B11 @ max. power	TBD	mA
	LTE-FDD B18 @ max. power	TBD	mA
	LTE-FDD B19 @ max. power	TBD	mA
	LTE-FDD B21 @ max. power	TBD	mA
LTE data transfer	LTE-FDD B26 @ max. power	TBD	mA
	LTE-FDD B28 @ max. power	TBD	mA

	LTE-TDD B41 @ max. power	TBD	mA

NOTE

The power consumption data above is for reference only, which may vary among different modules. For detailed information, contact Quectel Technical Support for the power consumption test report of the specific module.

6.4. Digital I/O Characteristics

Table 73: 2.95 V Digital I/O Characteristics – (U)SIM

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.1	V
V_{IH}	High-level input voltage	2.06	3.25	V
V_{IL}	Low-level input voltage	-0.3	0.59	V
V_{OH}	High-level output voltage	2.36	-	V
V_{OL}	Low-level output voltage	-	0.4	V

Table 74: 1.8 V Digital I/O Characteristics - (U)SIM

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.7	1.9	V
V_{IH}	High-level input voltage	1.26	2.1	V
V_{IL}	Low-level input voltage	-0.3	0.36	V
V_{OH}	High-level output voltage	1.44	-	V
V_{OL}	Low-level output voltage	-	0.4	V

Table 75: 2.95 V Digital I/O Characteristics – SD Card

Parameter	Description	Min.	Max.	Unit

SD_VDD	Power supply	2.7	3.1	V
V_{IH}	High-level input voltage	1.84	3.25	V
V_{IL}	Low-level input voltage	-0.3	0.74	V
V_{OH}	High-level output voltage	2.21	-	V
V_{OL}	Low-level output voltage	-	0.37	V

Table 76: 1.8 V Digital I/O Characteristics – SD Card

Parameter	Description	Min.	Max.	Unit
SD_VDD	Power supply	1.7	1.9	V
V_{IH}	High-level input voltage	1.27	2	V
V_{IL}	Low-level input voltage	-0.3	0.58	V
V_{OH}	High-level output voltage	1.4	-	V
V_{OL}	Low-level output voltage	-	0.45	V

Table 77: 1.8 V I/O Characteristics - Others

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	1.17	2.09	V
V_{IL}	Low-level input voltage	-0.3	0.63	V
V_{OH}	High-level output voltage	1.35	-	V
V_{OL}	Low-level output voltage	-	0.45	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 78: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±5	±10	kV
Other Interfaces	±0.5	±0.1	kV

6.6. Operating and Storage Temperatures

Table 79: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [15]	-35	+25	+75	°C
Storage temperature range	-40	-	+90	°C

[15] Within the operating temperature range, the module meets 3GPP specifications.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

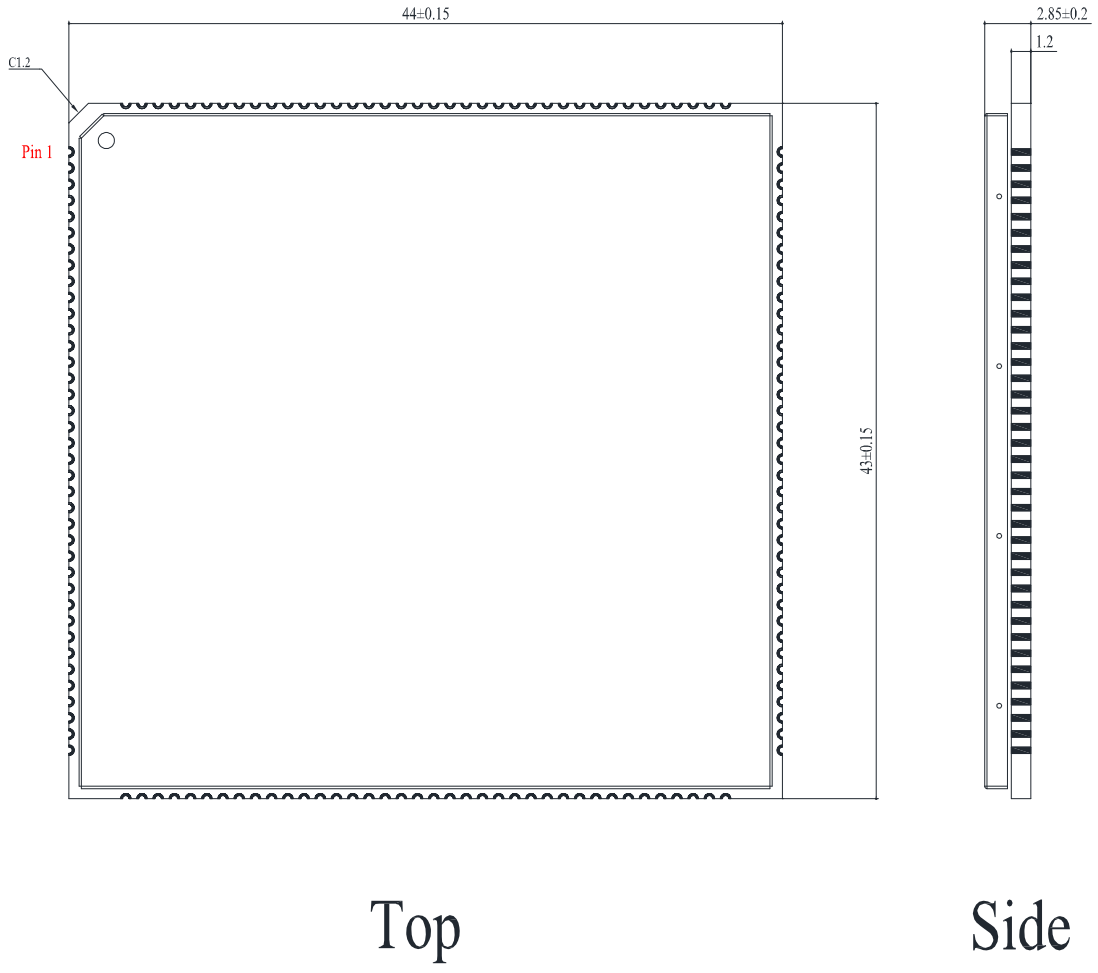


Figure 40: Module Top and Side Dimensions (Unit: mm)

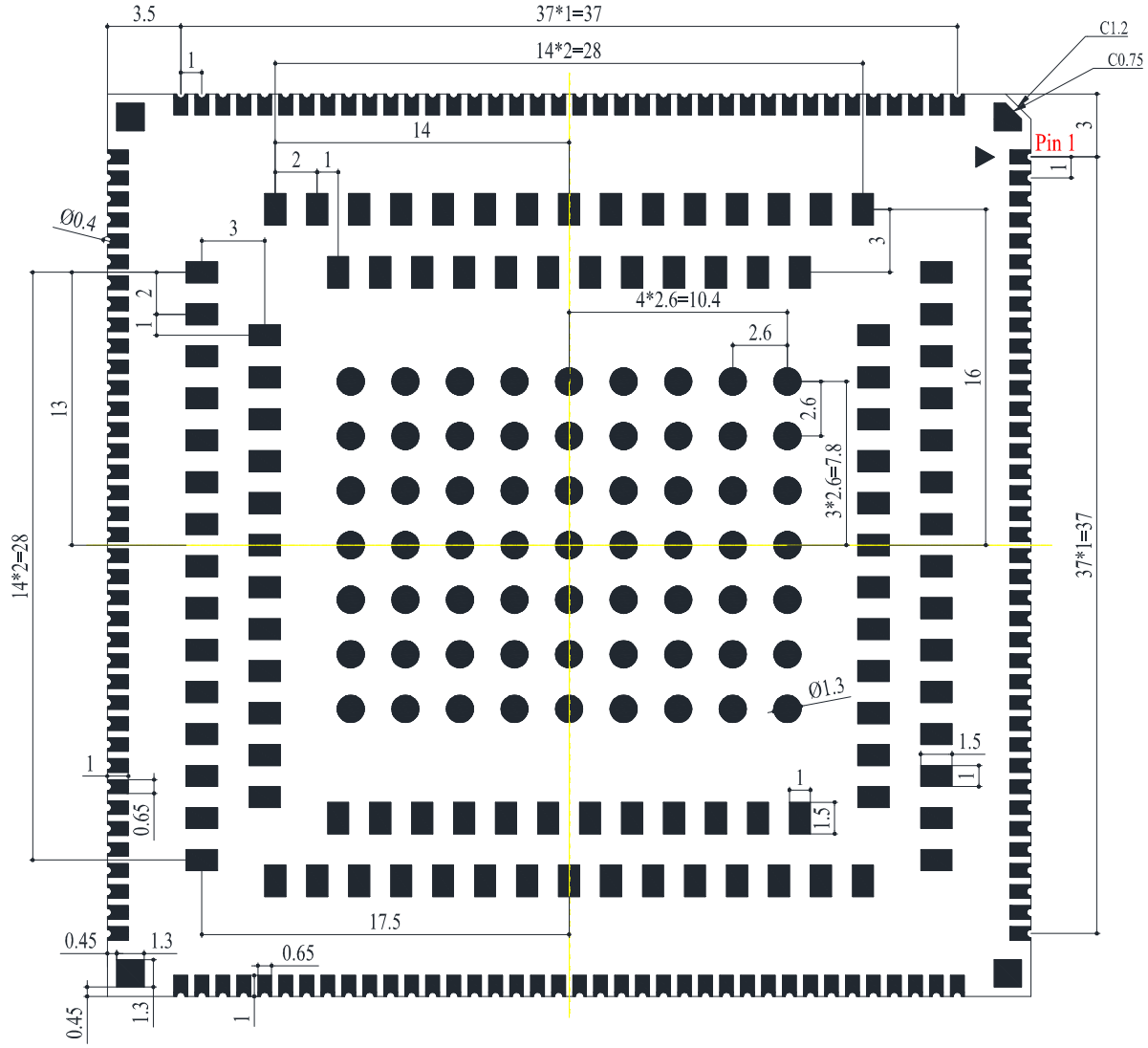


Figure 41: Module Bottom Dimensions (Unit: mm)

NOTE

1. Copper leakage is prohibited at the triangle mark at the bottom of the module.
2. The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

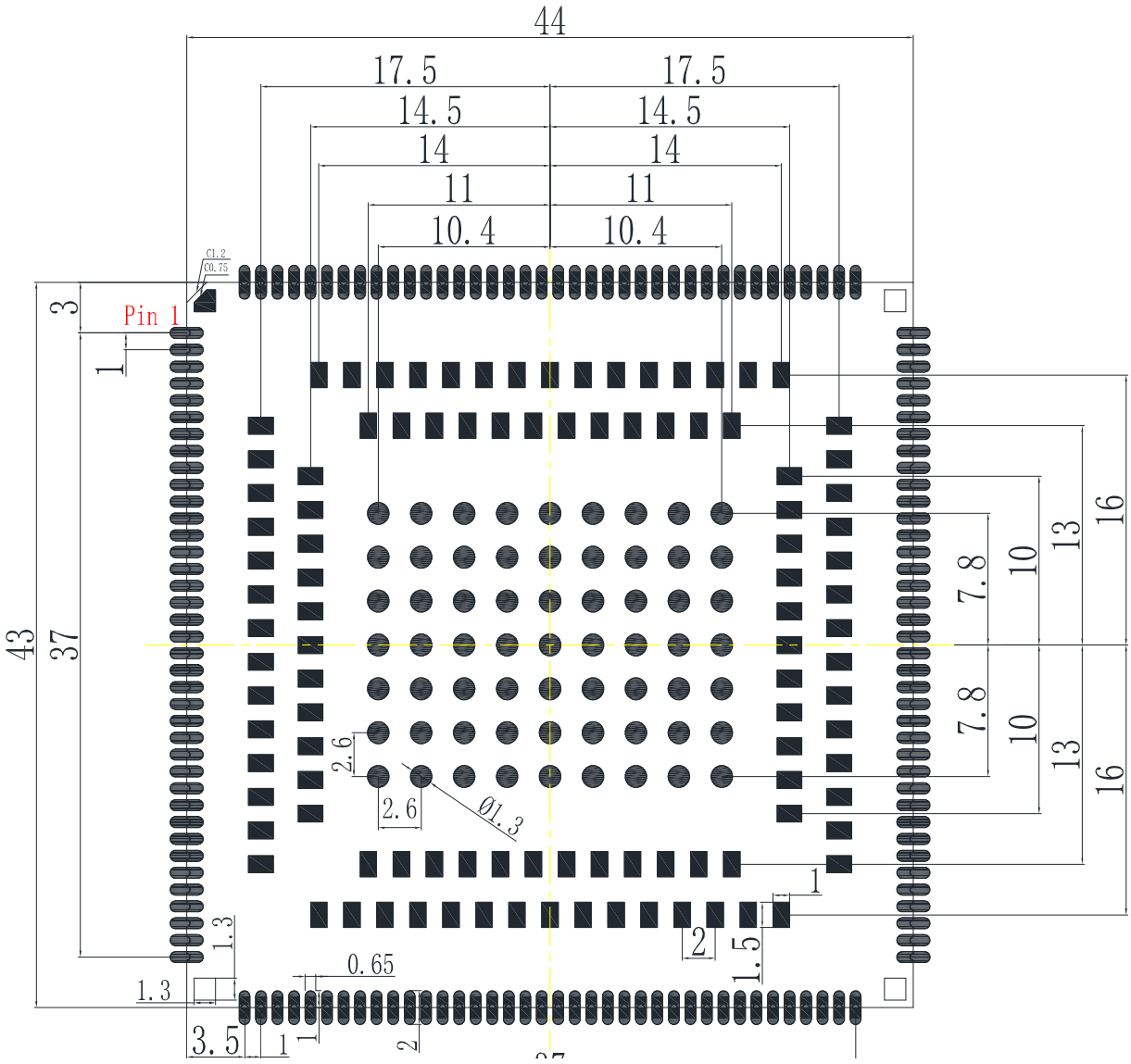


Figure 42: Recommended Footprint (Unit: mm)

NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. To keep the reliability of the mounting and soldering, keep the motherboard thickness as at least 1.2 mm.

7.3. Top and Bottom Views

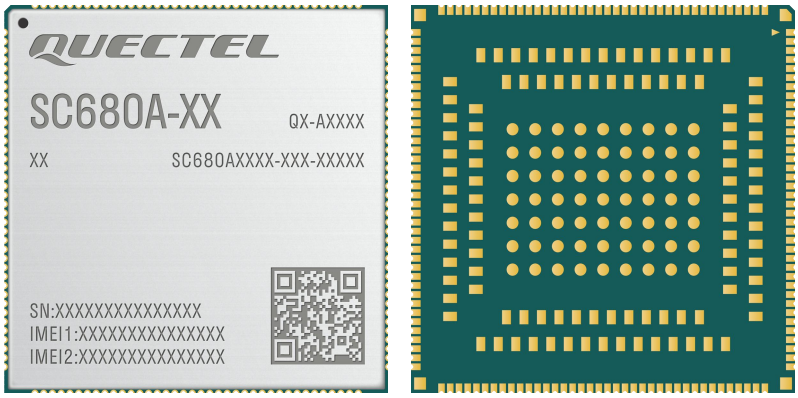


Figure 43: Top and Bottom Views of SC680A Series

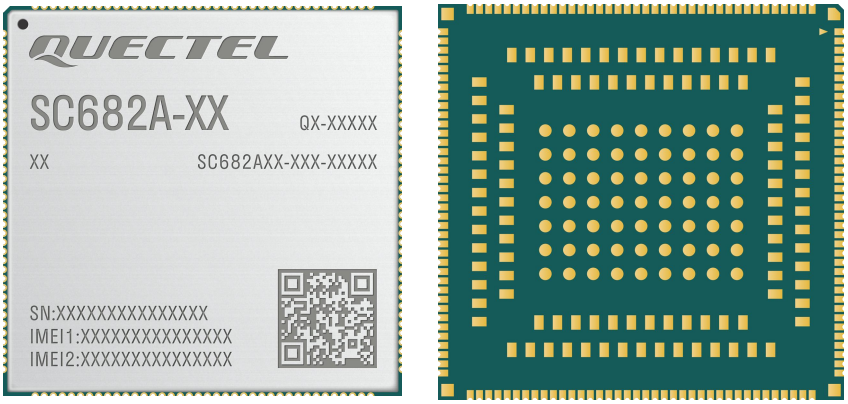


Figure 44: Top and Bottom Views of SC682A Series

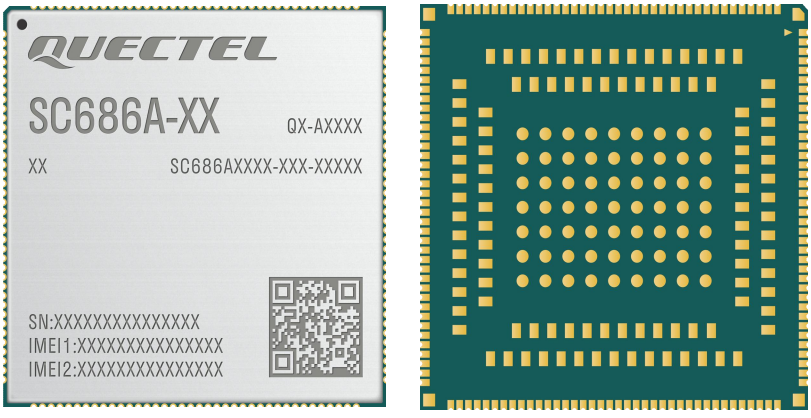


Figure 45: Top and Bottom Views of SC686A Series

NOTE

1. Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.
2. Cellular modules supporting (U)SIM have an IMEI code, which is printed on their shielding cover. Non-cellular modules have no IMEI code, therefore, there is no IMEI code on their shielding cover.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [16] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 24 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[16] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18 mm–0.20 mm. For more details, please refer to ***document [4]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

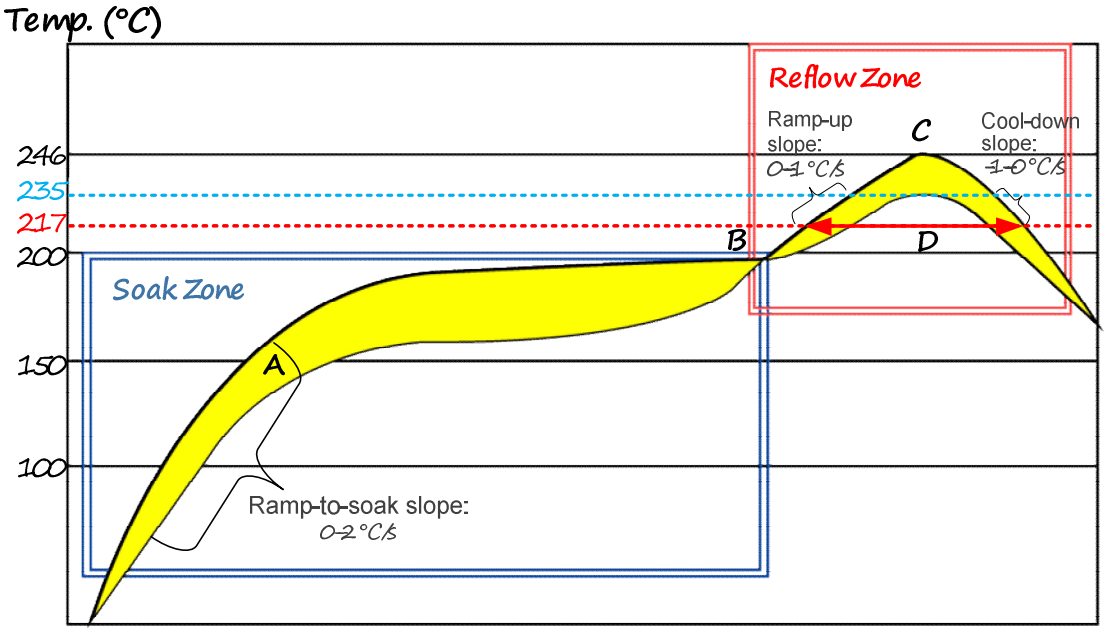


Figure 46: Recommended Reflow Soldering Thermal Profile

Table 80: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–2 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
217–235 °C Ramp-up Slope	0–1 °C/s
Reflow Time (D: over 217°C)	40–65 s
Max Temperature	235–246 °C
235–217 °C Cool-down Slope	-1–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. Due to the large-size form factor, an excessive temperature change may cause excessive thermal deformation of the metal shielding frame and cover. Thus, it is recommended to reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste to avoid excessive temperature change. If possible, choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
6. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
7. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [5]***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

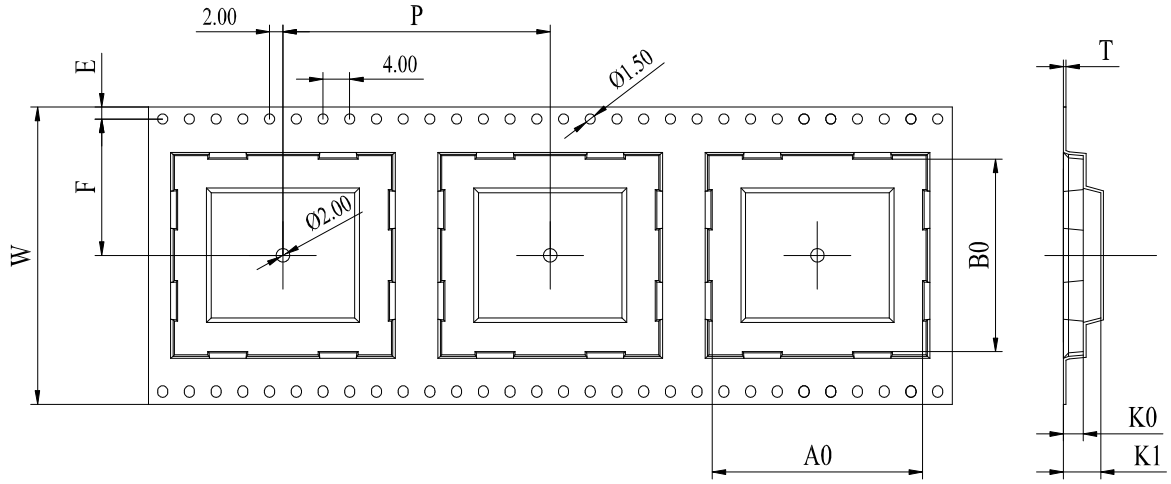


Figure 47: Carrier Tape Dimension Drawing (Unit: mm)

Table 81: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	56	0.35	44.5	43.5	4.1	5.4	34.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

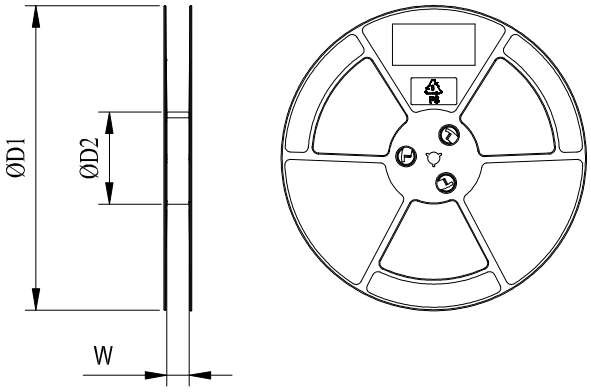


Figure 48: Plastic Reel Dimension Drawing

Table 82: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	180	72.5

8.3.3. Mounting Direction

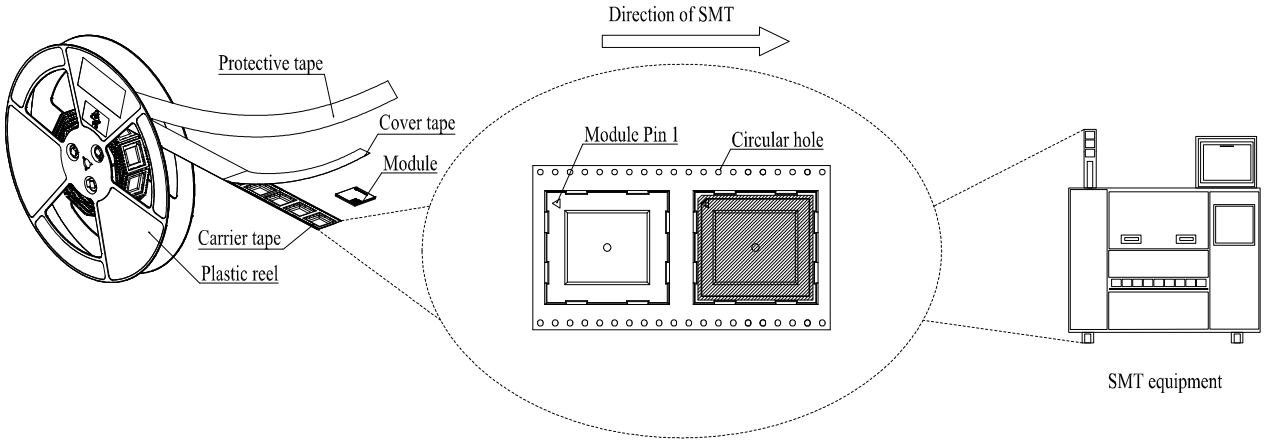
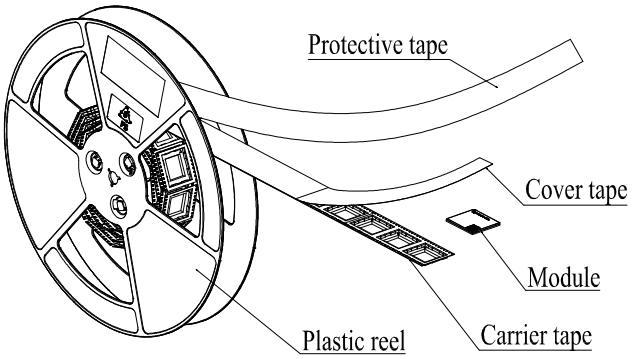


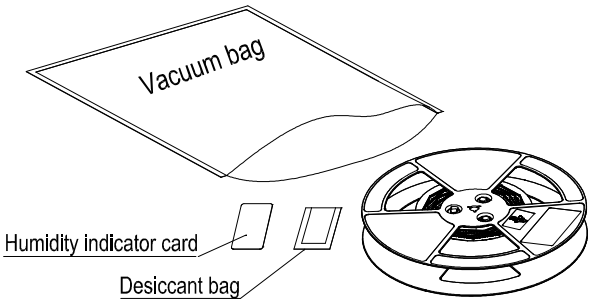
Figure 49: Mounting Direction

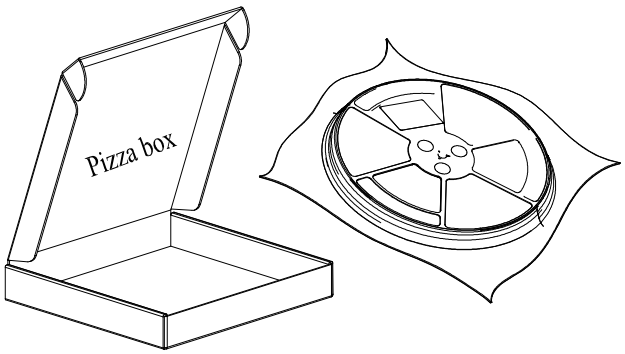
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 200 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 800 modules.

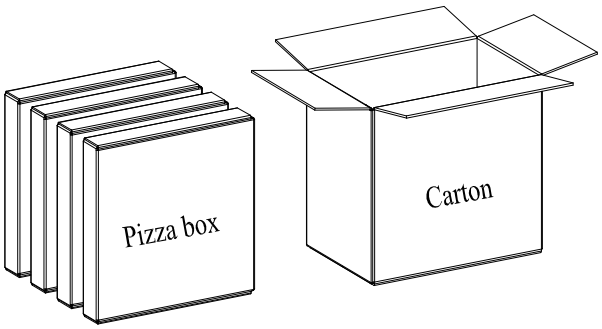


Figure 50: Packaging Process

9 Appendix References

Table 83: Related Documents

Document Name
[1] Quectel_Smart_EVB_G5_User_Guide
[2] Quectel_SC680A&SC682A&SC686A_Series_GPIO_Configuration
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_Stencil_Design_Requirements
[5] Quectel_Module_SMT_Application_Note
[6] Quectel_SC680A&SC682A&SC686A_Series_Reference_Design

Table 84: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR-NB	Adaptive Multi Rate-Narrow Band Speech Codec
AMR-WB	Adaptive Multi-Rate Wideband
AP	Application Processor
ARM	Advanced RISC Machine
BDS	BeiDou Navigation Satellite System
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
CA	Carrier Aggregation
Cj	Junction Capacitance

CS	Coding Scheme
CSD	Circuit Switched Data
CSI	Camera Serial Interface
CTS	Clear To Send
DCE	Data Communications Equipment
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DCS	Data Coding Scheme
DDR	Double Data Rate
DL	Downlink
DRX	Diversity Reception
DSI	Display Serial Interface
DSP	Digital Signal Processor
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
eLDO	External Low-dropout Regulator
EMI	Electromagnetic Interference
eMMC	Embedded Multimedia Card
ESD	Electrostatic Discharge
EVRC	Enhanced Variable Rate Coder
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)

GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPIO	General-Purpose Input/Output
GPS	Global Positioning System
GPU	Graphics Processing Unit
GSM	Global System for Mobile Communications
GRFC	Generic Radio Frequency Controller
HB	High Band
HEVC	High Efficiency Video Coding
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IC	Integrated Circuit
$I_{LED}max$	Maximum LED Current (per string)
IoT	Internet of Things
ISP	Image Signal Processor
LB	Low Band
LCC	Leadless Chip Carrier (package)
LCM	Liquid Crystal Monitor
LED	Light Emitting Diode
LGA	Land Grid Array

LNA	Low Noise Amplifier
LTE	Long Term Evolution
M2M	Machine to Machine
MAC	Media Access Control
MB	Middle Band
MCS	Modulation and Coding Scheme
MCU	Microcontroller Unit
ME	Mobile Equipment
MIMO	Multiple Input Multiple Output
MIPI	Mobile Industry Processor Interface
MO	Mobile Originated
MP	Main Profile
MS	Mobile Station
MT	Mobile Terminated
NavIC	Indian Regional Navigation Satellite System (IRNSS)
NSA	Non-Stand Alone
OTA	Over-the-air programming
OTG	On-The-Go
OTP	One Time Programmable
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PHY	Physical Layer
PMU	Power Management Unit

POS	Point of Sale
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RI	Ring Indicator
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SA	Stand Alone
SD	Secure Digital
SDR	Software-Defined Radio
SIMO	Single Input Multiple Output
SMS	Short Message Service
SoC	System on a Chip
SPI	Serial Peripheral Interface
STA	Station
TBD	To Be Determined
TDD	Time Division Duplexing
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code

USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{I}max	Absolute Maximum Input Voltage
V_{I}min	Absolute Minimum Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

FCC ID: XMR2025SC682ANA

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel. that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:
“Contains FCC ID: XMR2025SC682ANA”
“Contains IC: 10224A-025SC682ANA”
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC

ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Band	Antenna Type	Max Gain Allowed (dBi)
LTE B2	Dipole	8.00
LTE B4		5.00
LTE B5		11.47
LTE B7		8.00
LTE B12		10.76
LTE B13		11.23
LTE B14		11.29
LTE B17		10.80
LTE B25		8.00
LTE B26		11.42
LTE B41		8.00
LTE B66		5.00
LTE B71		10.54
Bluetooth		0.47
WiFi 2.4G		0.47
WiFi 5G		1.28

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.

- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, and part 15 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

IC: 10224A-025SC682ANA

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.
Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront

pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 10224A-025SC682ANA”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 10224A-025SC682ANA ".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.