RG255C-GL

Hardware Design

5G Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-09-15	Jared WANG/ Ethan FANG/ Sherlock ZHAO	Creation of the document
1.0.0	2023-11-13	Jared WANG/ Ethan FANG/ Sherlock ZHAO	Preliminary
1.0.1	2023-12-15	Jada LIN	Preliminary: Added a note on avoiding abnormal RF functions caused by current sink on the module's pins (Chapter 2.4).
1.0.2	2024-03-20	Jared WANG/ Ethan FANG/ Sherlock ZHAO	Preliminary: 1. Updated the weight of the module (Table 2). 2. Added a footnote for eSIM; updated the max. transmission data rates of 5G NR and LTE; updated the supported 3GPP information and uplink modulations of LTE; updated the information of USB serial driver (Table 4). 3. Added two footnotes illustrating the transmitting power of B30 and n30 (Table 4 and Table 28). 4. Updated the DC characteristics of pin 8 and pin 9, and added a comment for them (Table 6). 5. Updated the figure of turning-on timing (Figure 12). 6. Updated the figure of reference circuit of RESET_N by using button (Figure 15). 7. Added the information of ADC resolution (Chapter 4.8).

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1 Introduction

This document defines RG255C-GL module, and describes its air interfaces and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details as well as other related information of RG255C-GL module. To facilitate its application in different fields, relevant reference design is also provided for your reference. Associated with application note and user guide, you can use RG255C-GL module to design and set up mobile applications easily.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.

2 Product Overview

The module is an SMD module with compact packaging, which can meet most of the demands of M2M applications.

Table 2: Basic Information

RG255C-GL	
Packaging type	LGA
Pin counts	204 pins
Dimensions	(29.0 ±0.2) mm × (32.0 ±0.2) mm × (2.4 ±0.2) mm
Weight	Approx. 5.2 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

	RG255C-GL
5G NR SA	n1/n2/n3/n5/n7/n8/n12/n13/n14/n18/n20/n25/n26/n28/n30/n38/n40/n41/n48/n66/n70/n71/n77/n78/n79
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B25/B26/B28/B30/B66/B70/B71
LTE-TDD	B34/B38/B39/B40/B41/B42/B43/B48
GNSS (optional)	GPS/GLONASS/BDS/Galileo

2.2. Key Features

The following table describes the detailed features of RG255C-GL module.

Table 4: Key Features

Category	Description
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
SMS	● Only supports SGS, IMS and NAS SMS ● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
eSIM [1]	Optional
Transmitting Power	● 5G NR bands: Class 3 (23 dBm ±2 dB) [2] ● 5G NR n38/n40/n41/n77/n78/n79 HPUE [3]: Class 2 (26 dBm +2/-3 dB) ● LTE bands: Class 3 (23 dBm ±2 dB) [4] ● LTE B38/B40/B41/B42/B43 HPUE [3]: Class 2 (26 dBm ±2 dB)
5G NR Features	● Supports 3GPP Rel-17 Redcap. 5G NR sub-6 ● Supported modulations: - Uplink: QPSK, 16QAM, 64QAM and 256QAM - Downlink: QPSK, 16QAM, 64QAM and 256QAM ● Supports SCS 15 kHz [5] and 30 kHz [5] ● Supports SA on operation mode ● Supports Option 2 ● Max. transmission data rates [6]: - SA: 223 Mbps (DL), 123 Mbps (UL) ● SRS: - SA: 1T2R (n38/n40/n41/n48/n77/n78/n79)
LTE Features	● Supports 3GPP Rel-16 ● Supported modulations: - Uplink: QPSK, 16QAM, 64QAM and 256QAM - Downlink: QPSK, 16QAM, 64QAM and 256QAM ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Max. transmission data rates [6]:

[1] If you need this function, contact Quectel Technical Support.
[2] The transmitting power of n30 is Class 3 (22 dBm ±2 dB).
[3] HPUE is only for single carrier.
[4] The transmitting power of B30 is Class 3 (22 dBm ±2 dB).
[5] 5G NR FDD bands only support 15 kHz SCS, and NR TDD bands only support 30 kHz SCS.
[6] The maximum rates are theoretical and the actual values depend on the network configuration.

	- 195 Mbps (DL), 105 Mbps (UL)
Internet Protocol Features	Supports TCP/UDP/SSL/TLS/FTP(S)/HTTP(S)/MQTT(S)/SMTP(S)/NTP/PING/NITZ/LwM2M* protocols
(U)SIM Interfaces	● Supports (U)SIM card: 1.8/3.0 V ● Supports Dual SIM Single Standby
USB Tethering	Supports RmNet, RNDIS, ECM, DUN, MBIM
USB Interface	● Compliant with USB 2.0 specification; the data transmission rate can reach up to 480 Mbps ● Used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB* ● Supports USB serial driver for: Windows 8/8.1/10/11, Linux 2.6–6.7, Android 4.x–13.x
UART	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate reaches up to 4 Mbps, 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● 115200 bps baud rate
Audio Features	● Supports one digital audio interface: PCM interface ● LTE: AMR/AMR-WB ● Supports echo cancellation and noise suppression
PCM Interface	● Used for audio function with external codec ● Supports 16-bit linear data format ● Supports long frame synchronization and short frame synchronization ● Supports master and slave modes, but must be the master in long frame synchronization
SPI	● Provides a full-duplex, synchronous and serial communication link with the peripheral devices ● One SPI, only supports master mode ● 1.8 V operation voltage with clock rates up to 50 MHz
PCIe Interface	● Complaint with PCIe Gen 2, 1 lane ● Supports RC (Root Complex) mode and EP (End Point) mode ● Could be used to connect Wi-Fi and ethernet PHY
SGMII Interface	Supports 10 Mbps/100 Mbps/1000 Mbps Ethernet work mode
Network Indication	● NET_MODE: used for network registration status indication ● NET_STATUS: used for network connectivity status indication
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Diversity antenna interface (ANT_DRX) ● GNSS antenna interface (ANT_GNSS) (optional)

	• 50 Ω characteristic impedance
Rx-diversity	Supports 5G NR/LTE Rx-diversity
GNSS Features [7]	• Supports L1/L2/L5 • Supports GPS, GLONASS, BDS, Galileo • Protocol: NMEA 0183 • Data update rate: 1 Hz by default
AT Commands	• Compliant with *3GPP TS 27.007*, *3GPP TS 27.005* • Quectel enhanced AT commands
Firmware Upgrade	USB interface or DFOTA
Temperature Range	• Operating temperature range: -30 to +75 °C [8] • Extended temperature range: -40 to +85 °C [9] • Storage temperature range: -40 to +90 °C
RoHS	All hardware components are fully complying with EU RoHS directive

[7] If you need the function of L2, contact Quectel Technical Support.

[8] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[9] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

2.3. Functional Diagram

The following figure shows the block diagram of the module.

- Power management
- Baseband
- DDR + NAND flash
- Radio frequency part
- Peripheral interfaces

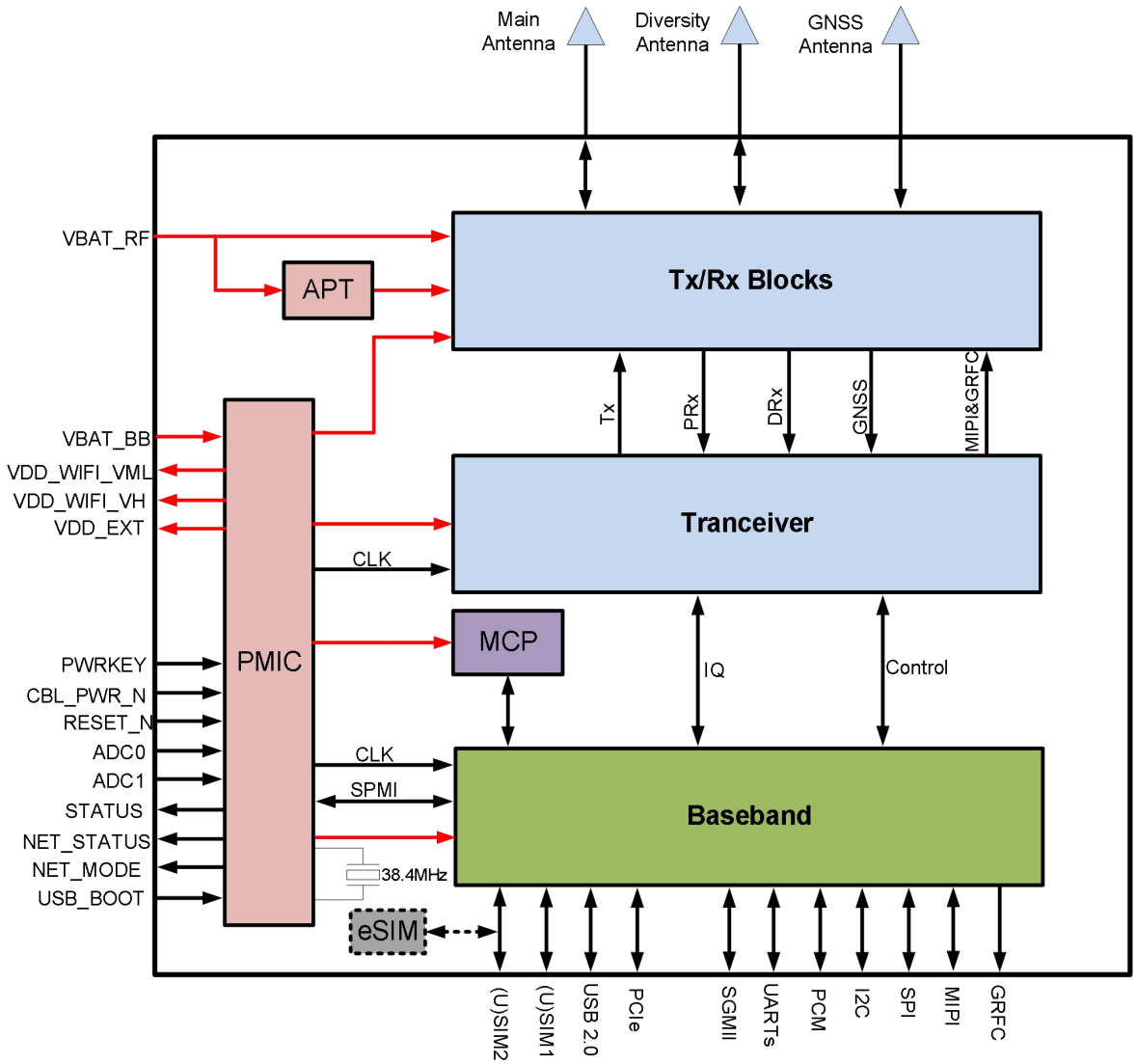


Figure 1: Functional Diagram

2.4. Pin Assignment

The following figure shows the pin assignment of the module.

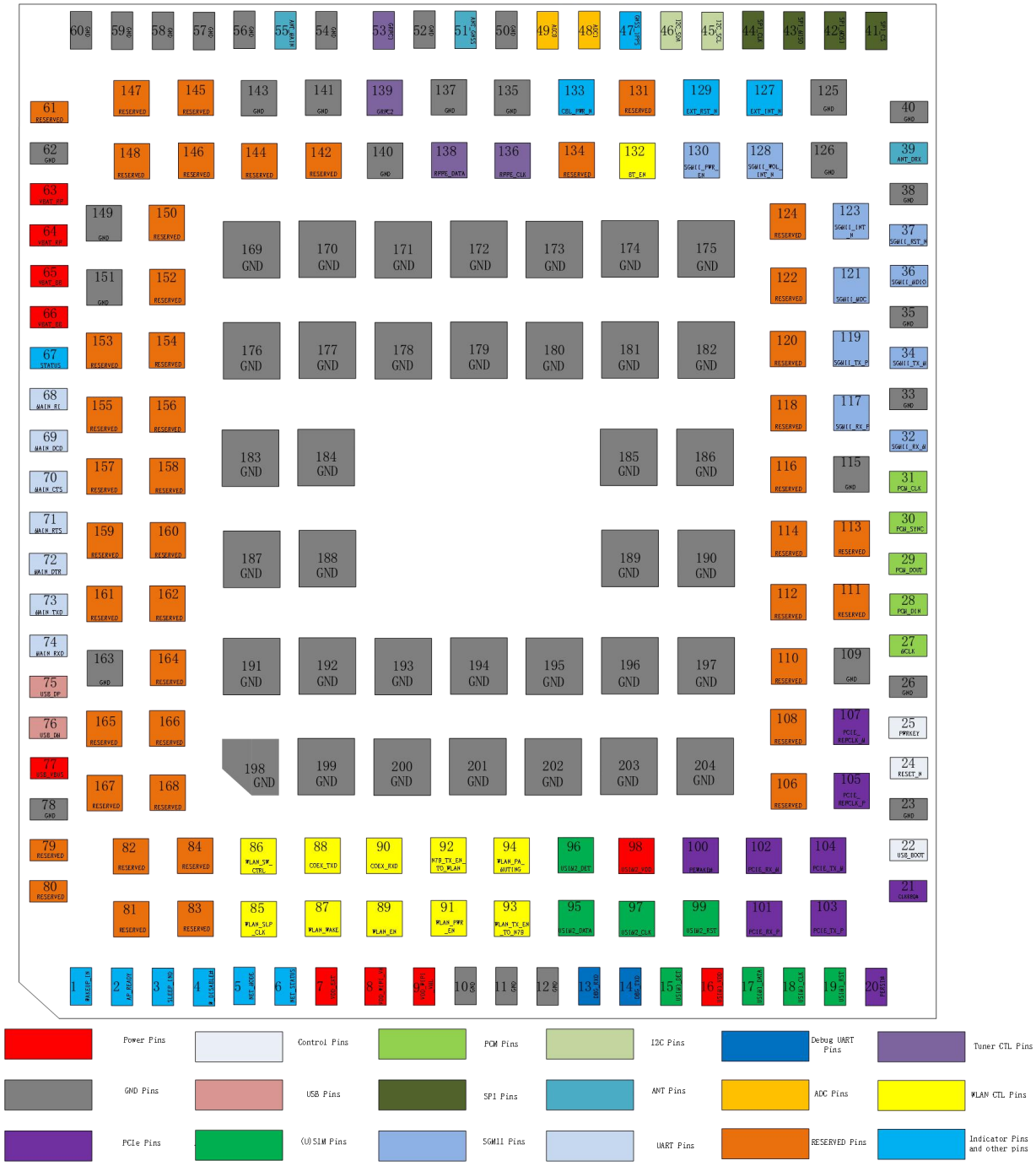


Figure 2: Pin Assignment (Top View)

NOTE

Ensure that the pull-up power supply of the module's pins is VDD_EXT or controlled by VDD_EXT, and there is no current sink on the module's pins before the module turns on. For more details, contact Quectel Technical Support.

2.5. Pin Definitions

The following table shows the DC characteristics and pin descriptions.

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	65, 66	PI	Power supply for module's BB part	Vmax = 4.3 V Vmin = 3.3 V	

VBAT_RF	63, 64	PI	Power supply for module's RF part	Vnom = 3.8 V	
VDD_EXT	7	PO	Provide 1.8 V for external circuits	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.
VDD_WIFI_VH	8	PO	Power supply for Wi-Fi	Vnom = 1.824 V $I_O$max = 200 mA	Internal power supply for Wi-Fi.
VDD_WIFI_VML	9	PO	Power supply for Wi-Fi	Vnom = 1.244 V $I_O$max = 800 mA	
GND					
Pin Name	**Pin No.**				
GND	10–12, 23, 26, 33, 35, 38, 40, 50, 52, 54, 56–60, 62, 78, 109, 115, 125, 126, 135, 137, 140, 141, 143, 149, 151, 163, 169–204				
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	25	DI	Turn on/off the module		Pulled up internally to 1.5 V power domain.
CBL_PWR_N	133	DI	Initiate power on when grounded		Alternate input pin which can be used to initiate the power-up sequence when grounded; pulled up internally.
RESET_N	24	DI	Reset the module		Pulled up internally to 1.5 V power domain. Active low. A test point is recommended to be reserved if unused.
Indication Signals					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	67	OD	Indicate the module's operation status		An external pull-up resistor is required.

					If unused, keep it open.
NET_MODE	5	DO	Indicate the module's network registration mode	VDD_EXT	If unused, keep them open.
NET_STATUS	6	DO	Indicate the module's network activity status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	77	PI	USB connection detect	Vmax = 5.25 V Vmin = 3.3 V Vnom = 5.0 V	A test point must be reserved.
USB_DP	75	AIO	USB 2.0 differential data (+)		Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	76	AIO	USB 2.0 differential data (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	16	PO	(U)SIM1 card power supply	**High-voltage:** Vmin = 2.06 V Vnom = 3.0 V Vmax = 3.25 V **Low-voltage:** Vmin = 1.26 V Vnom = 1.8 V Vmax = 2.1 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	17	DIO	(U)SIM1 card data	USIM1_VDD	Pulled up internally with a 20 kΩ resistor.
USIM1_CLK	18	DO	(U)SIM1 card clock		
USIM1_RST	19	DO	(U)SIM1 card reset		
USIM1_DET	15	DI	(U)SIM1 card hot-plug detect	VDD_EXT	If unused, keep it open.
USIM2_VDD	98	PO	(U)SIM2 card power supply	**High-voltage:** Vmin = 2.06 V Vnom = 3.0 V	Either 1.8 V or 3.0 V is supported by the module

				Vmax = 3.25 V **Low-voltage:** Vmin = 1.26 V Vnom = 1.8 V Vmax = 2.1 V	automatically.
USIM2_DATA	95	DIO	(U)SIM2 card data	USIM2_VDD	Pulled up internally with a 20 kΩ resistor.
USIM2_CLK	97	DO	(U)SIM2 card clock		
USIM2_RST	99	DO	(U)SIM2 card reset		
USIM2_DET	96	DI	(U)SIM2 card hot-plug detect	VDD_EXT	If unused, keep it open.
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RI	68	DO	Main UART ring indication	VDD_EXT	If unused, keep them open.
MAIN_DCD	69	DO	Main UART data carrier detect		
MAIN_CTS	70	DO	Clear to send signal from the module		Connect to the MCU's CTS. If unused, keep it open.
MAIN_RTS	71	DI	Request to send signal to the module		Connect to the MCU's RTS. If unused, keep it open.
MAIN_DTR	72	DI	Main UART data terminal ready		If unused, keep them open.
MAIN_TXD	73	DO	Main UART transmit		
MAIN_RXD	74	DI	Main UART receive		
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	14	DO	Debug UART transmit	VDD_EXT	Test points must be reserved. If unused, keep them open.
DBG_RXD	13	DI	Debug UART receive		

ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	49	AI	General-purpose ADC interface	0–VBAT_BB	If unused, keep them open.
ADC1	48	AI			
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
MCLK	27	DO	Master clock output for codec	VDD_EXT	If unused, keep them open.
PCM_DIN	28	DI	PCM data input		
PCM_DOUT	29	DO	PCM data output		
PCM_SYNC	30	DIO	PCM data frame sync		
PCM_CLK	31	DIO	PCM clock		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
I2C_SCL	45	OD	I2C serial clock	VDD_EXT	Pull each of them up to VDD_EXT with 4.7 kΩ resistors. If unused, keep them open.
I2C_SDA	46	OD	I2C serial data		
PCIe Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_REFCLK_P	105	AIO	PCIe reference clock (+)		Requires differential impedance of 85 Ω. If unused, keep them open.
PCIE_REFCLK_M	107		PCIe reference clock (-)		
PCIE_TX_P	103	AO	PCIe transmit (+)		
PCIE_TX_M	104		PCIe transmit (-)		
PCIE_RX_P	101	AI	PCIe receive (+)		

PCIE_RX_M	102		PCIe receive (-)		
PERST#	20	DIO	PCIe reset	VDD_EXT	
CLKREQ#	21	OD/ DIO	PCIe clock request		
PEWAKE#	100	OD/ DIO	PCIe wake up		
WLAN Coexistence and Control Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK	85	DO	WLAN sleep clock		
WLAN_PWR_EN	91	DO	WLAN power supply enable control	VDD_EXT	Active high.
WLAN_WAKE	87	DI	Wake up module by an external Wi-Fi		
COEX_RXD	90	DI	5G/LTE and WLAN coexistence receive		
COEX_TXD	88	DO	5G/LTE and WLAN coexistence transmit		
N79_TX_EN_TO_ WLAN	92	DO	Notify n79 transmission from SDR transceiver to WLAN		
WLAN_TX_EN_ TO_N79	93	DI	Notify WLAN transmission from WLAN to SDR transceiver	1.8 V	
WLAN_PA_ MUTING	94	DO	GPIO from SDX to disable WLAN PA	VDD_EXT	
WLAN_SW_CTRL	86	DI	Wi-Fi power control		
WLAN_EN	89	DO	WLAN function enable control		
BT_EN	132	DO	Bluetooth enable control		Active high.
SPI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	41	DO	SPI chip select	VDD_EXT	Only master mode

SPI_MOSI	42	DO	SPI master-out slave-in		is supported.
SPI_MISO	43	DI	SPI master-in slave-out		
SPI_CLK	44	DO	SPI clock		
SGMII & CTL Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SGMII_RST_N	37	DO	SGMII reset external PHY	VDD_EXT	If unused, keep them open.
SGMII_INT_N	123	DI	SGMII interrupt		
SGMII_WOL_INT_N	128	DI	Wake-on-LAN interrupt input		
SGMII_PWR_EN	130	DO	Enable external power for SGMII PHY		
SGMII_MDIO	36	DIO	SGMII management data input/output		If unused, keep them open.
SGMII_MDC	121	DO	SGMII management data clock		
SGMII_TX_M	34	AO	SGMII transmit (-)		Connect with a 0.1 μF capacitor. Requires differential impedance of 90 Ω.
SGMII_TX_P	119		SGMII transmit (+)		
SGMII_RX_M	32	AI	SGMII receive (-)		Requires differential impedance of 90 Ω.
SGMII_RX_P	117		SGMII receive (+)		
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_DRX	39	AIO	Diversity antenna interface		50 Ω impedance. If unused, keep it open.
ANT_MAIN	55	AIO	Main antenna interface		50 Ω impedance.
ANT_GNSS	51	AI	GNSS antenna interface		50 Ω impedance. If unused, keep it open.
Antenna Tuner Control Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RFFE_DATA	138	DIO	Used for external MIPI IC Control	VDD_EXT	
RFFE_CLK	136	DO			
GRFC1	53	DO	Generic RF Controller		If unused, keep them open.
GRFC2	139	DO			
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	1	DI	Wake up the module	VDD_EXT	Wake up the module at low voltage level. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control		At low voltage level, the module can enter into airplane mode. If unused, keep it open. Pulled up by default.
AP_READY	2	DI	Application processor ready		If unused, keep them open.
SLEEP_IND	3	DO	Indicate the module's sleep mode		
EXT_INT_N	127	DI	External audio interrupt		
EXT_RST_N	129	DO	External audio reset		
GNSS_1PPS	47	DO	Support time service and repeater functions; support 1PPS pulse output and frame synchronization		
USB_BOOT					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

USB_BOOT	22	DI	Force the module to enter download mode	VDD_EXT	Cannot be pulled up before startup. A test point is recommended to be reserved.
RESERVED Pins					
Pin Name	**Pin No.**				
RESERVED	61, 79–84, 106, 108, 110–114, 116, 118, 120, 122, 124, 131, 134, 142, 144-148, 150, 152–162, 164–168				

2.6. EVB Kit

Quectel supplies an evaluation board (5G Red Cap EVB) with accessories to develop and test the module. For more details, see ***document [3]***.

3 Operating Characteristics

3.1. Operating Modes

The following table briefly outlines the operating modes to be mentioned in the following chapters.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Voice/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transmission rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to enter airplane mode. In this case, RF function will be invalid and all AT commands related to it will be inaccessible.	
Sleep Mode	The power consumption of the module will be reduced to an ultra-low level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	The power management unit shuts down the power supply. Software goes inactive. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

NOTE

For more details about **AT+CFUN**, see ***document [4]***.

3.2. Sleep Mode

With DRX technology, power consumption of the module will be reduced to an ultra-low level.

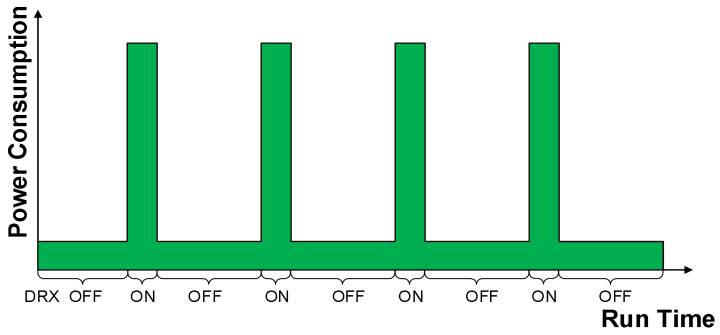


Figure 3: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1. UART Application Scenario

If the module communicates with the MCU via UART, both the following preconditions should be met to set the module to sleep mode:

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR to high level.

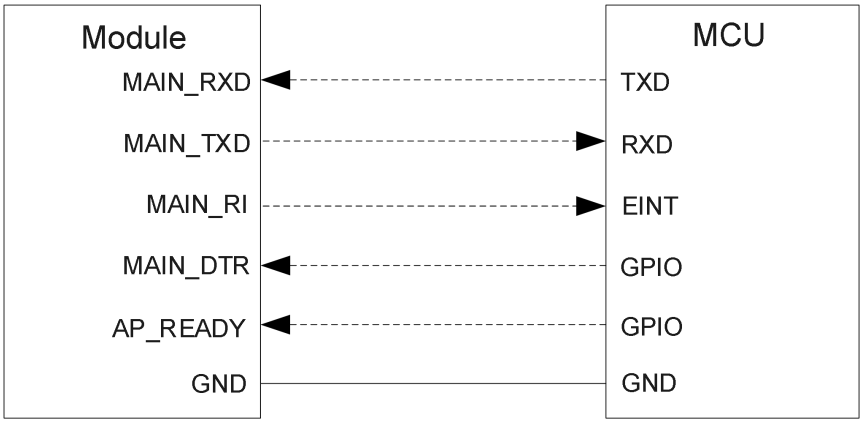


Figure 4: Sleep Mode Application via UART

- Driving MAIN_DTR to low level with MCU will wake up the module.
- When the module has a URC to report, MAIN_RI signal will wake up MCU. See ***Chapter 4.10.3*** for details about MAIN_RI behaviors.
- AP_READY will detect the sleep state of MCU (can be configured to high level or low level detection). See **AT+QCFG="apready"** for details.

3.2.2. USB Application Scenarios

For the two situations ('USB application with USB remote wakeup function' and 'USB application with USB Suspend/Resume and MAIN_RI function') below, three preconditions must be met to set the module to sleep mode:

- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held high or is kept unconnected.
- Ensure the host's USB bus, which is connected to the module's USB interface, enters Suspend state.

3.2.2.1. USB Application with USB Remote Wakeup Function

The following figure shows the connection between the module and the host.

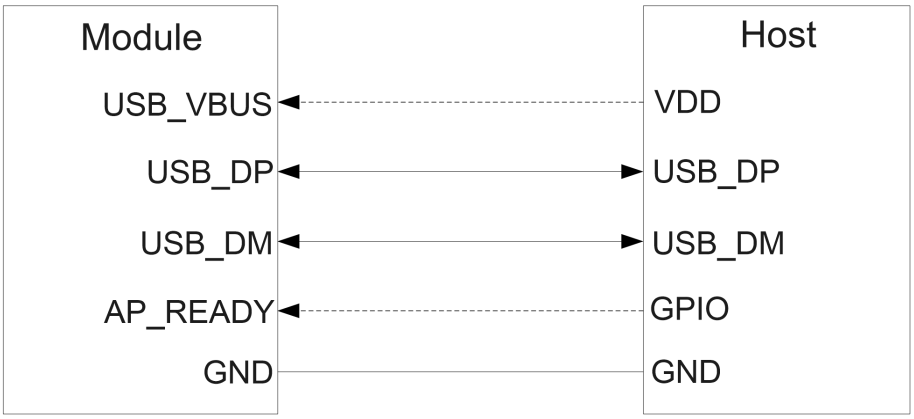


Figure 5: Sleep Mode Application with USB Remote Wakeup

- Sending data to the module via USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals through USB bus to wake up the host.

3.2.2.2. USB Application with USB Suspend/Resume and MAIN_RI Function

If the host supports USB Suspend and Resume, but does not support remote wake-up function, the MAIN_RI signal is needed to wake up the host.

The following figure shows the connection between the module and the host.

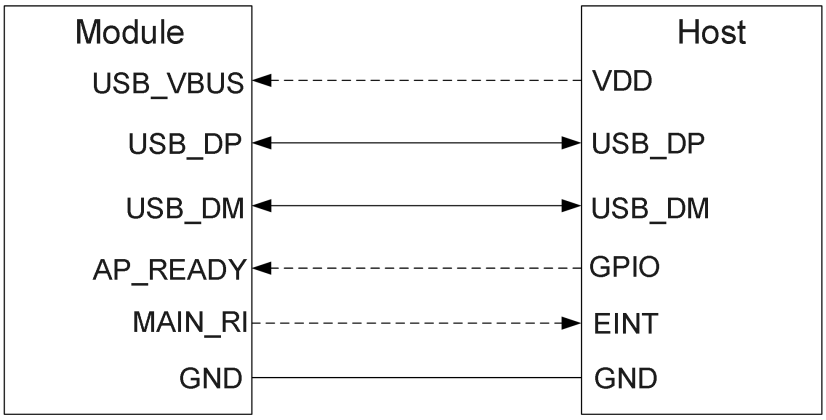


Figure 6: Sleep Mode Application with MAIN_RI

- Sending data to the module via USB will wake up the module.
- When the module has a URC to report, the module will wake up the host through MAIN_RI signal.

3.2.2.3. USB Application without USB Suspend Function

If the host does not support USB Suspend function, the following three preconditions must be met to set the module to sleep mode:

- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held high or is kept unconnected.
- Ensure USB_VBUS is disconnected via the external control circuit.

The following figure shows the connection between the module and the host.

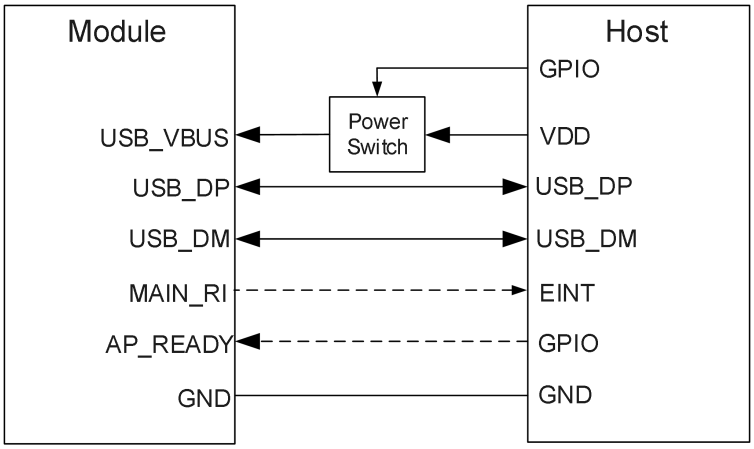


Figure 7: Sleep Mode Application without Suspend Function

Restore the power supply to USB_VBUS will wake up the module.

NOTE

Pay attention to the level match shown in dotted line between the module and the host.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Driving it to low level will let the module enter airplane mode.

Software:

AT+CFUN=<fun> provides choices of the functionality level by setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality. Both RF and (U)SIM functions are disabled.
- **AT+CFUN=1:** Full functionality mode (default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTE

1. The W_DISABLE# control function is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"**.
2. The execution of **AT+CFUN** will not affect GNSS function.

3.4. Power Supply

3.4.1. Power Supply Interface

The module provides four VBAT pins for connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's BB part

Table 8: Pin Definition of Power Supply

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	63, 64	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	65, 66	Power supply for module's BB part	3.3	3.8	4.3	V
GND	10–12, 23, 26, 33, 35, 38, 40, 50, 52, 54, 56–60, 62, 78, 109, 115, 125, 126, 135, 137, 140, 141, 143, 149, 151, 163, 169–204		-	-	-	V

3.4.2. Requirements for Voltage Stability

The power supply range of the module is from 3.3 V to 4.3 V. Make sure that the input voltage will never drop below 3.3 V.

To decrease voltage drop, two 100 µF capacitors with low ESR (ESR ≤ 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use five ceramic capacitors (22 µF, 100 nF, 6.8 nF, 220 pF, 68 pF) for VBAT_BB pins and seven ceramic capacitors (22 µF, 100 nF, 220 pF, 68 pF, 15 pF, 9.1 pF, 4.7 pF) for VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star configuration. The width of VBAT_BB trace should be not less than 1.5 mm; and the width of VBAT_RF trace should be not less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to avoid the damage caused by electric surge and electrostatics discharge (ESD), it is suggested that a TVS with suggested low reverse stand-off voltage V_{RWM} 4.5 V, low clamping voltage V_C and high reverse peak pulse current I_{PP} should be used. The following figure shows the star structure of the power supply.

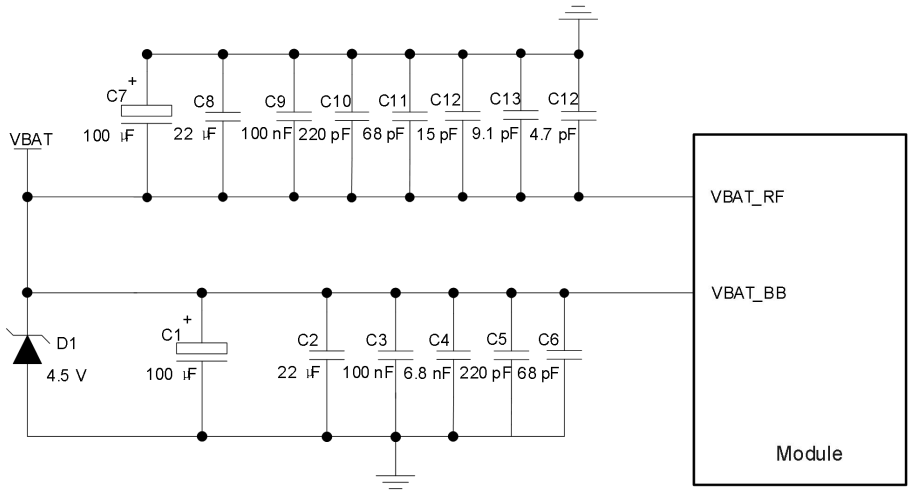


Figure 8: Star Configuration of Power Supply

3.4.3. Reference Design for Power Supply

The power source is critical to the module's performance. The power supply should be able to provide sufficient current of 3.0 A at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for 5.0 V input power source. The typical output of the power supply is about 3.8 V. The continuous current of the power supply should be 1.0 A at least and the peak current should be 3.0 A at least.

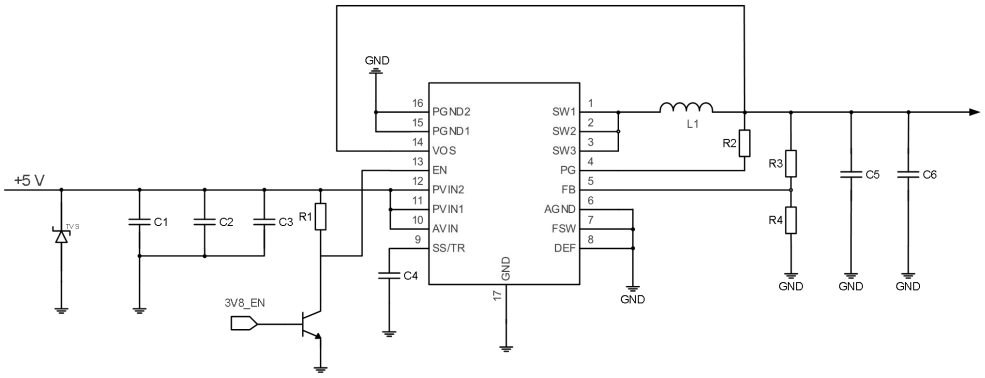


Figure 9: Reference Circuit of Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.

3.4.4. Power Supply Voltage Monitoring

AT+CBC can be used to monitor the VBAT_BB voltage value. For more details, see ***document [4]***.

3.5. Turn On

3.5.1. Turn On with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	25	DI	Turn on/off the module	Pulled up internally to 1.5 V power domain.

When the module is in turn-off mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

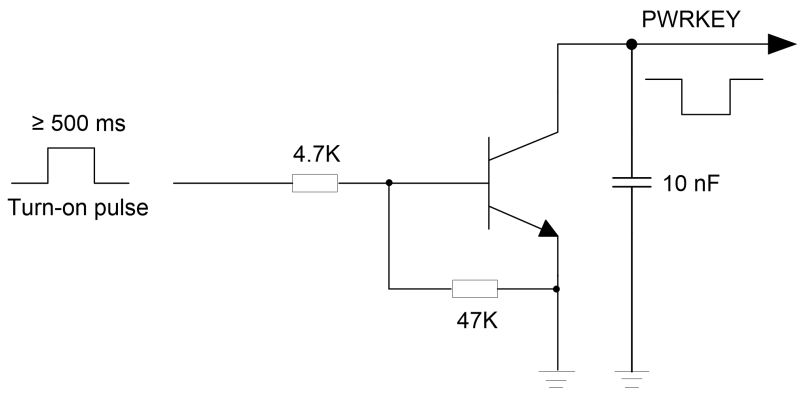


Figure 10: Turn on the Module by Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

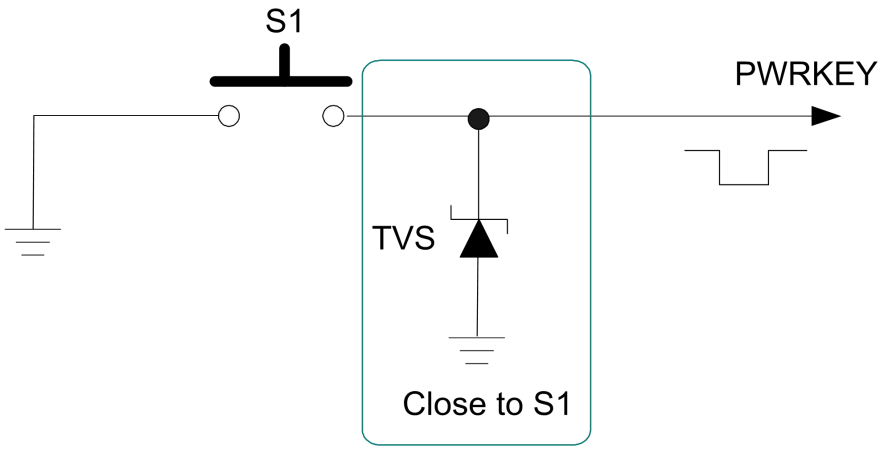


Figure 11: Reference Circuit of Turning on the Module with a Button

The turn-on scenario is illustrated in the following figure.

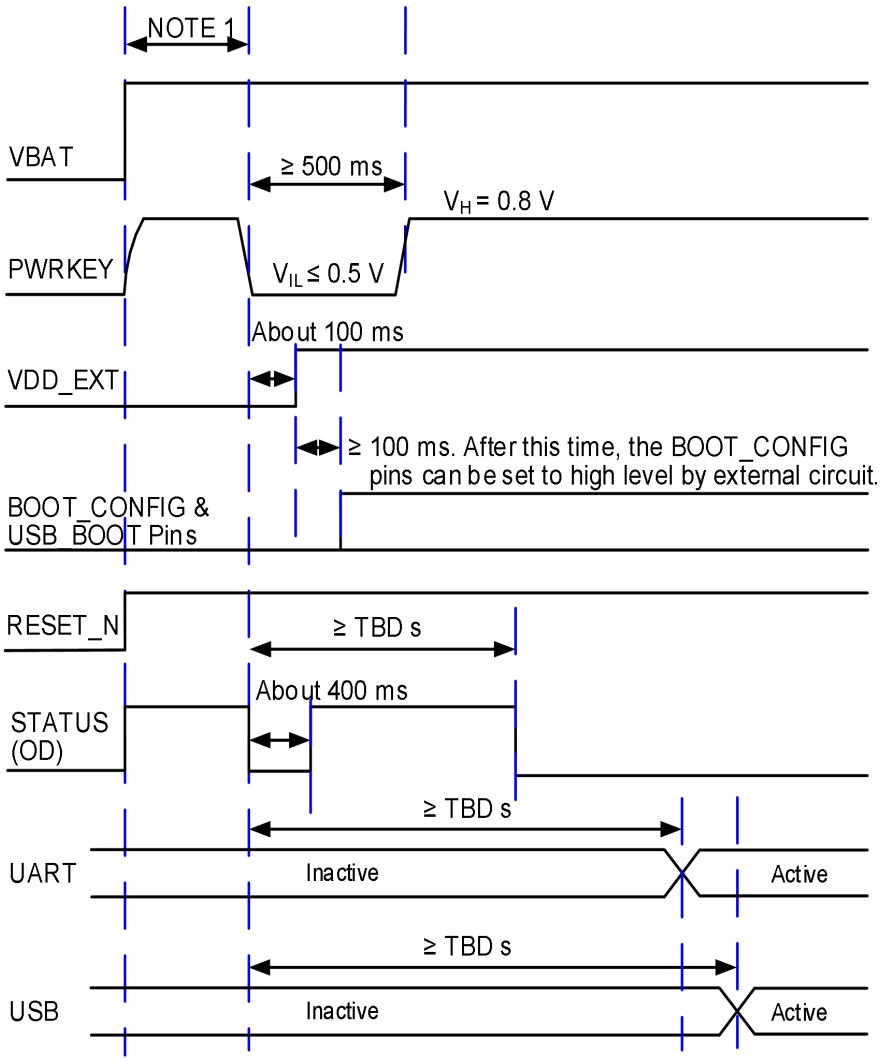


Figure 12:Turning-on Timing

NOTE

1. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. If the module needs to turn on automatically but does not need turn-off function, PWRKEY can be driven low directly to ground with a recommended 10 kΩ resistor.

3.6. Turn Off

3.6.1. Turn Off with PWRKEY

Driving the PWRKEY pin to a low level voltage for at least 650 ms, the module will execute turn-off procedure after the PWRKEY is released. The turn-off scenario is illustrated in the following figure.

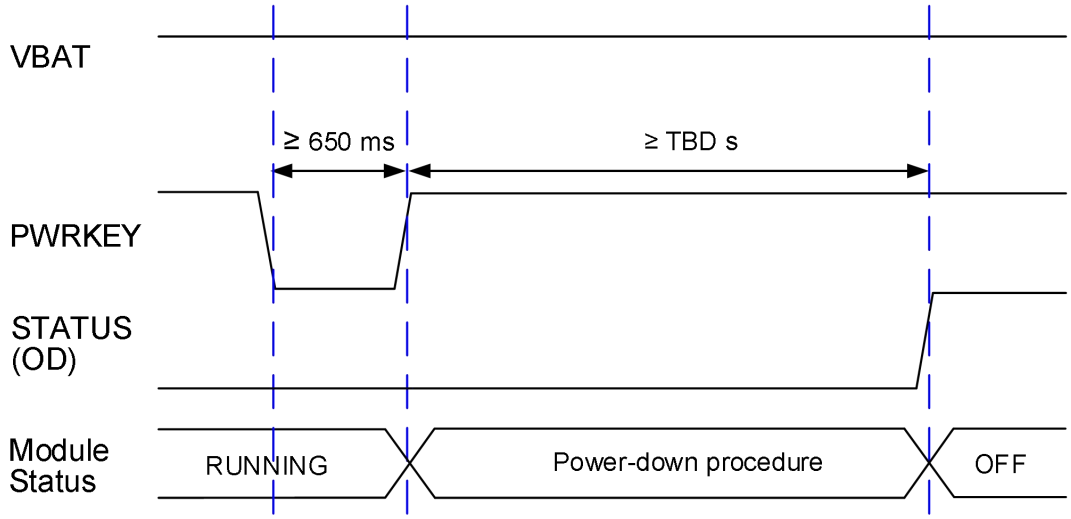


Figure 13: Turning-off Timing

3.6.2. Turn Off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turn off the module via PWRKEY pin.

See ***document [4]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.

2. When turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.

3.7. RESET_N

Drive RESET_N low for at least 150–460 ms and then releasing it can reset the module. RESET_N signal is sensitive to interference, consequently it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	24	DI	Reset the module	Pulled up internally to 1.5 V power domain. Active low. A test point is recommended to be reserved if unused.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

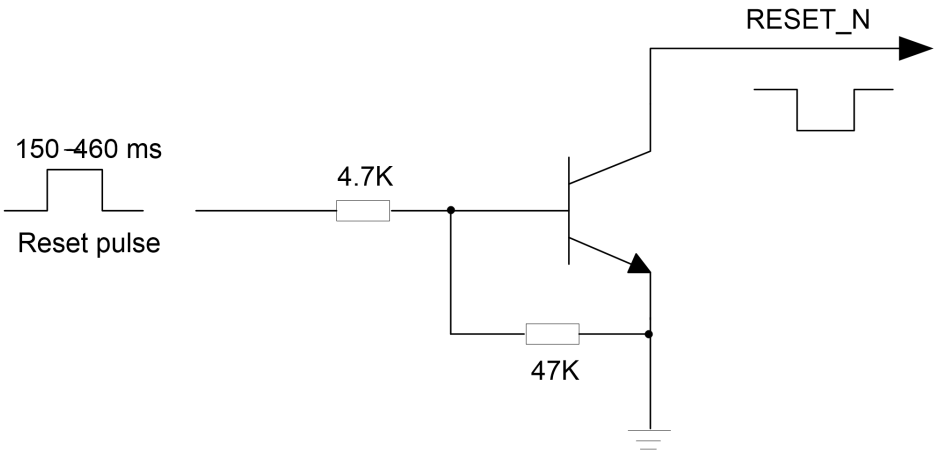


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

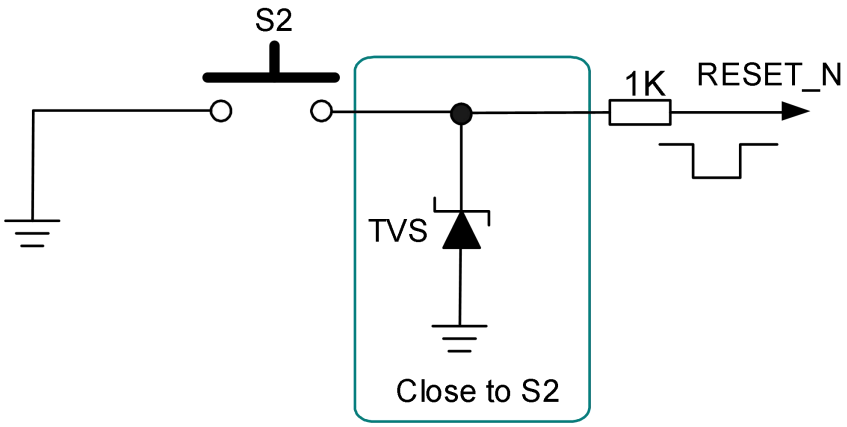


Figure 15: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

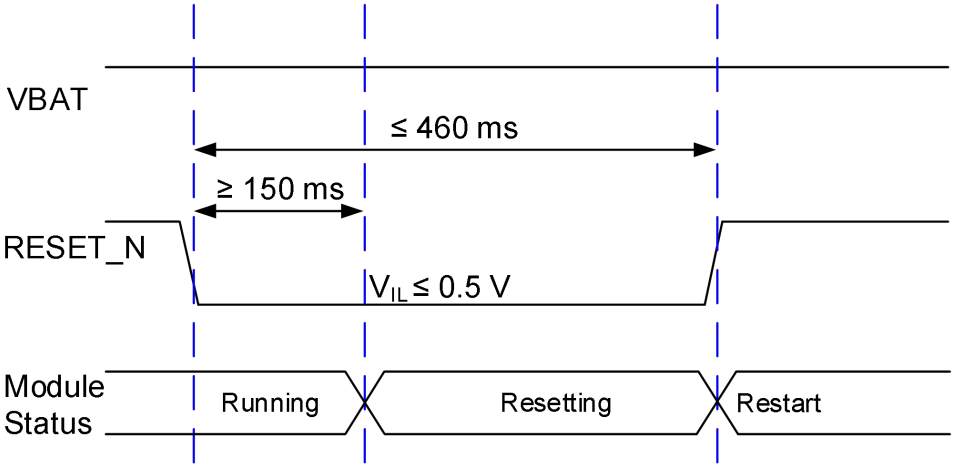


Figure 16: Reset Timing

NOTE

1. Use RESET_N only when you fail to turn off the module with the **AT+QPOWD** and PWRKEY.
2. Ensure there is no large capacitance on PWRKEY and RESET_N.

4 Application Interfaces

4.1. (U)SIM Interfaces

(U)SIM interfaces circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported, and Dual SIM Single Standby function is supported.

Table 11: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	16	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	17	DIO	(U)SIM1 card data	Pulled up internally with a 20 kΩ resistor.
USIM1_CLK	18	DO	(U)SIM1 card clock	
USIM1_RST	19	DO	(U)SIM1 card reset	
USIM1_DET	15	DI	(U)SIM1 card hot-plug detect	If unused, keep it open.
USIM2_VDD	98	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM2_DATA	95	DIO	(U)SIM2 card data	Pulled up internally with a 20 kΩ resistor.
USIM2_CLK	97	DO	(U)SIM2 card clock	
USIM2_RST	99	DO	(U)SIM2 card reset	
USIM2_DET	96	DI	(U)SIM2 card hot-plug detect	If unused, keep it open.

The module supports (U)SIM card hot-plug via the USIM_DET pins, and both high-level and low-level detections are supported. Hot-swap function is disabled by default and you can use **AT+QSIMDET** to configure this function. See ***document [4]*** for more details.

The following figure shows a reference design for (U)SIM card interface with an 8-pin (U)SIM card connector.

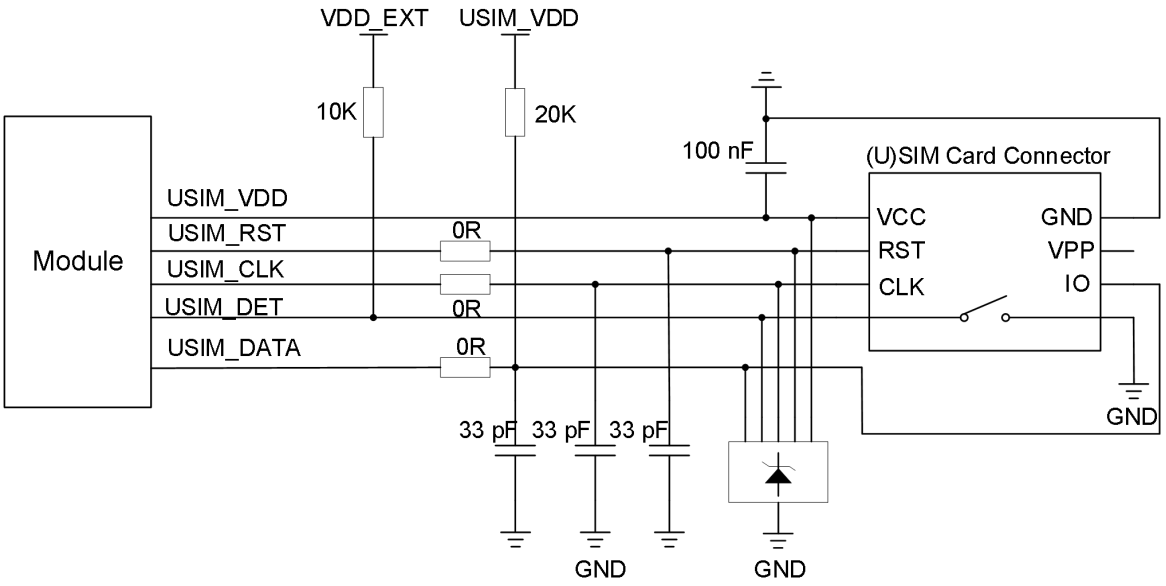


Figure 17: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET unconnected. A reference circuit of (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

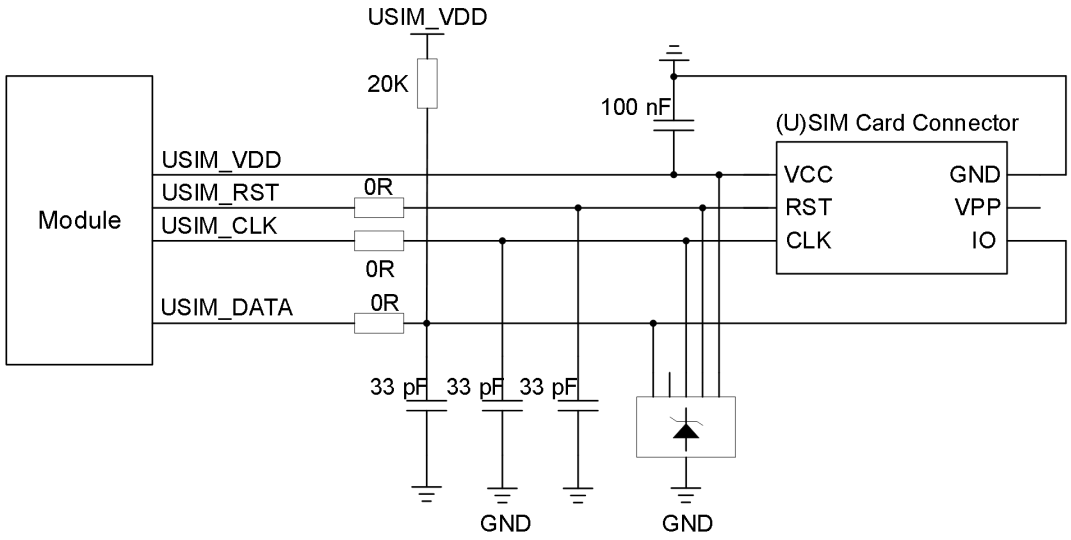


Figure 18: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, you should follow the principles below in the (U)SIM circuit design:

- Place the (U)SIM card connector close to the module. Keep the trace length as less than 200 mm if

possible.

- Keep (U)SIM card signals away from RF and power supply traces.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, you can add a TVS array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card connector to facilitate debugging. Additionally, add 33 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter out RF interference.
- For USIM_DATA, it is recommended to add a 20 kΩ pull-up resistor near the (U)SIM card connector to improve the anti-jamming capability of the (U)SIM card.

4.2. USB_BOOT

The module provides a USB_BOOT pin. You can pull up USB_BOOT to VDD_EXT before PWRKEY is enabled, and the module will enter forced download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Table 12: Pin Definition of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	22	DI	Force the module to enter download mode	Cannot be pulled up before startup. A test point is recommended to be reserved.

The following figures show the reference circuit of USB_BOOT and timing sequence of entering forced download mode.

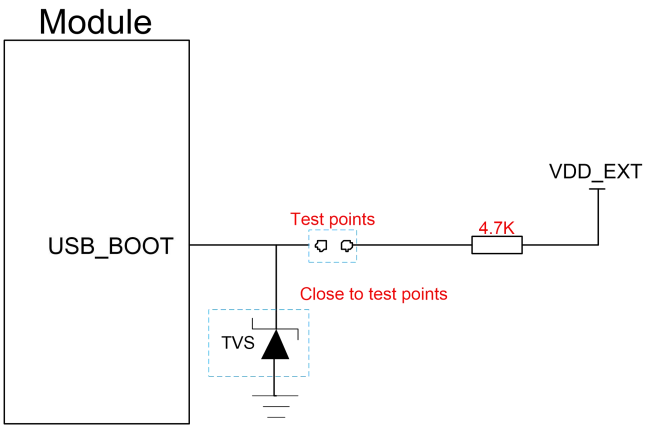


Figure 19: Reference Circuit of USB_BOOT

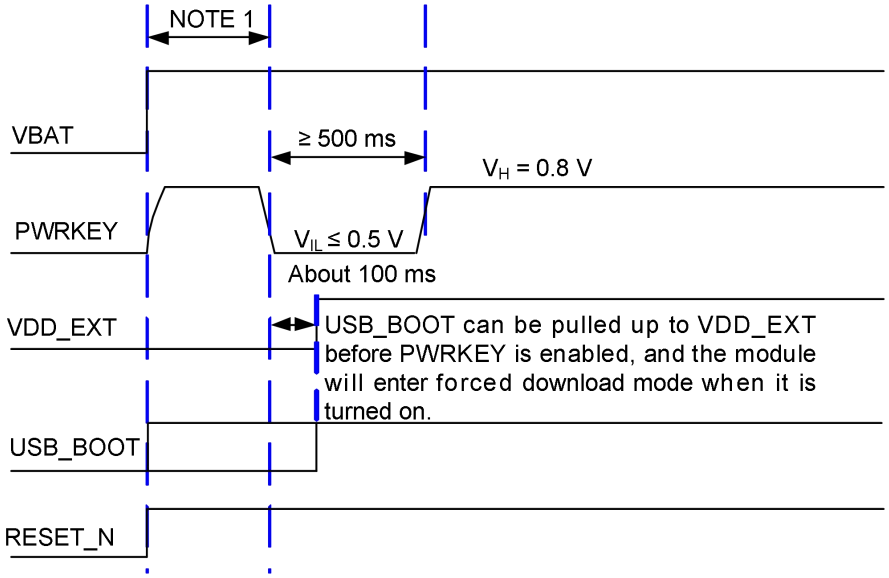


Figure 20: Timing Sequence for Entering Forced Download Mode

NOTE

1. Ensure VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low shall be at least 30 ms.
2. When using MCU to control the module to enter forced download mode, follow the above timing sequence. It is not recommended to pull up USB_BOOT to VDD_EXT before powering up VBAT.

4.3. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. The USB interface can only serve as a slave device and is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB*. The following table shows the pin definition of USB interface.

Table 13: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	75	AIO	USB 2.0 differential data (+)	Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	76	AIO	USB 2.0 differential data (-)	
USB_VBUS	77	PI	USB connection detection	Typical 5.0 V.

	A test point must be reserved.

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

It is recommended to use USB 2.0 interface for firmware upgrading, and reserve test points for debugging in your designs.

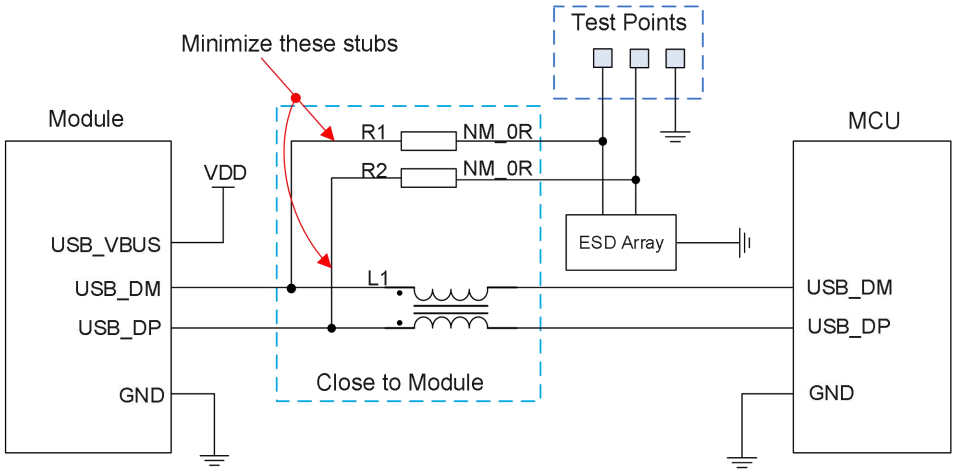


Figure 21: Reference Circuit of USB Interface

A common mode choke L1 is recommended to be added in series between the module and your MCU in order to suppress EMI. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data trace signal, L1/R1/R2 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

To ensure performance, you should follow the following principles when designing USB interface:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB 2.0 differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data traces. Typically, the stray capacitance should be less than 2 pF for USB 2.0.
- Keep the ESD protection components to the USB connector as close as possible.

4.4. UART

The module provides two UART.

Table 14: UART Information

UART Type	Supported Baud Rate	Default Baud Rate	Function
Main UART	300 bps, 600 bps, 1200 bps, 2400 bps, 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps, 1000000 bps, 2000000 bps and 3000000 bps	115200 bps	Data transmission and AT command communication
Debug UART	115200 bps	115200 bps	Linux console and log output

The following table shows the pin definition of UART.

Table 15: Pin Definition of UART

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	68	DO	Main UART ring indication	If unused, keep them open.
MAIN_DCD	69	DO	Main UART data carrier detect	
MAIN_CTS	70	DO	Clear to send signal from the module	Connect to the MCU's CTS. If unused, keep it open.
MAIN_RTS	71	DI	Request to send signal to the module	Connect to the MCU's RTS. If unused, keep it open.
MAIN_DTR	72	DI	Main UART data terminal ready	If unused, keep them open.
MAIN_TXD	73	DO	Main UART transmit	
MAIN_RXD	74	DI	Main UART receive	
DBG_TXD	14	DO	Debug UART transmit	Test points must be reserved. If unused, keep them open.
DBG_RXD	13	DI	Debug UART receive	

The module provides 1.8 V UART. A voltage-level translator should be used if your application is equipped with a 3.3 V UART. The following figure shows a reference design.

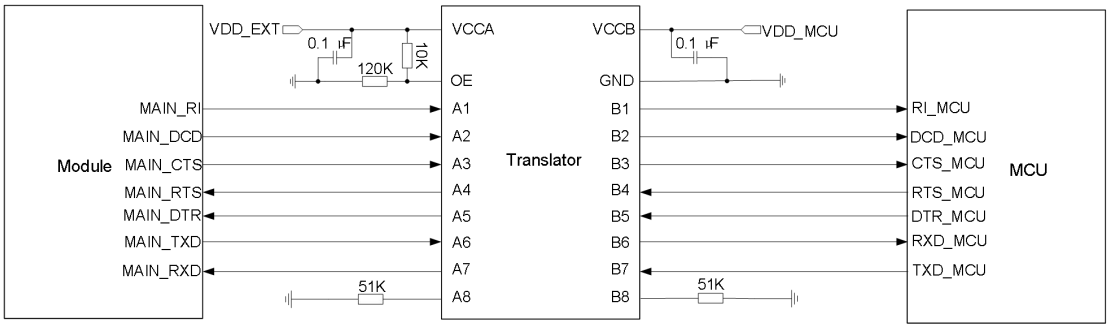


Figure 22: Reference Circuit with a Voltage-level Translator

Visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

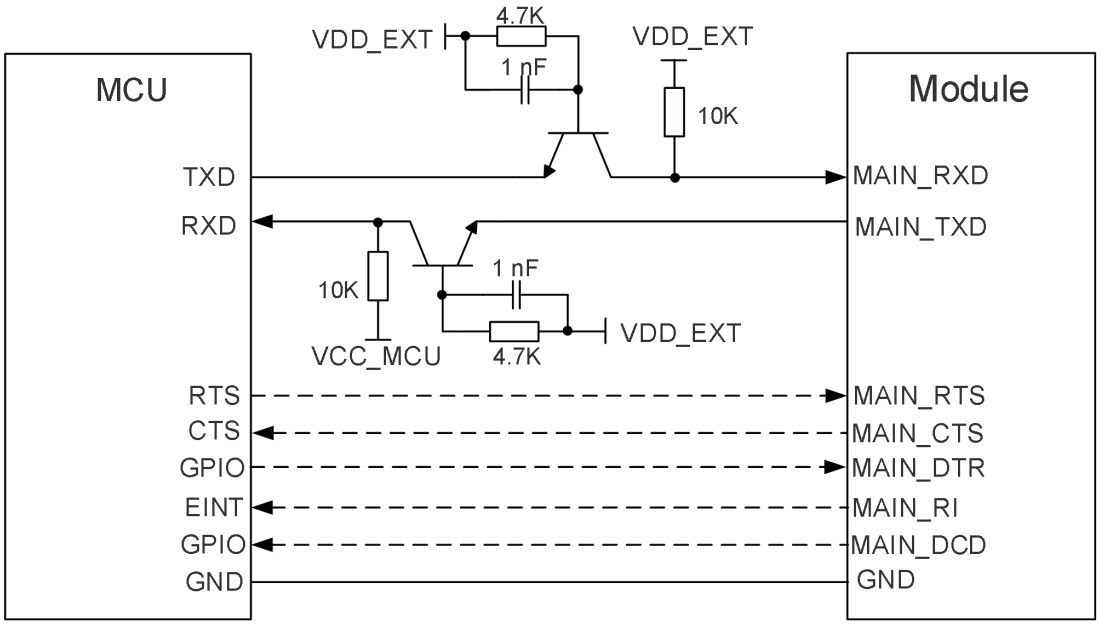


Figure 23: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is

connected to the MCU's RTS.

4.5. PCM and I2C Interfaces

The module provides one Pulse Code Modulation (PCM) digital interface for audio design, and one I2C interface:

Table 16: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	28	DI	PCM data input	If unused, keep them open.
PCM_DOUT	29	DO	PCM data output	
PCM_SYNC	30	DIO	PCM data frame sync	
PCM_CLK	31	DIO	PCM clock	
I2C_SCL	45	OD	I2C serial clock	Pull each of them up to VDD_EXT with 4.7 kΩ resistors. If unused, keep them open.
I2C_SDA	46	OD	I2C serial data	

The PCM interface supports the following modes.

- Short frame mode: the module works as both the master and slave devices.
- Long frame mode: the module works as the master mode only.

The module supports 16-bit linear encoding format. The following figures are the short frame mode timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 2048 kHz) and the long frame mode timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 256 kHz).

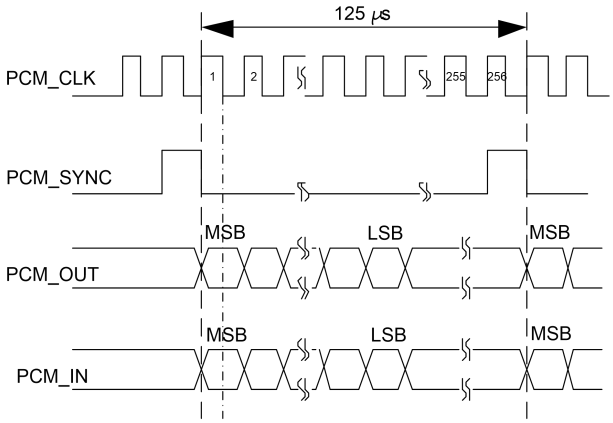


Figure 24: Timing of Short Frame Mode

In short frame mode, data is sampled on the falling edge of PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, PCM_CLK supports 256 kHz, 512 kHz, 1024 kHz and 2048 kHz when PCM_SYNC operates at 8 kHz, and also supports 4096 kHz when PCM_SYNC operates at 16 kHz.

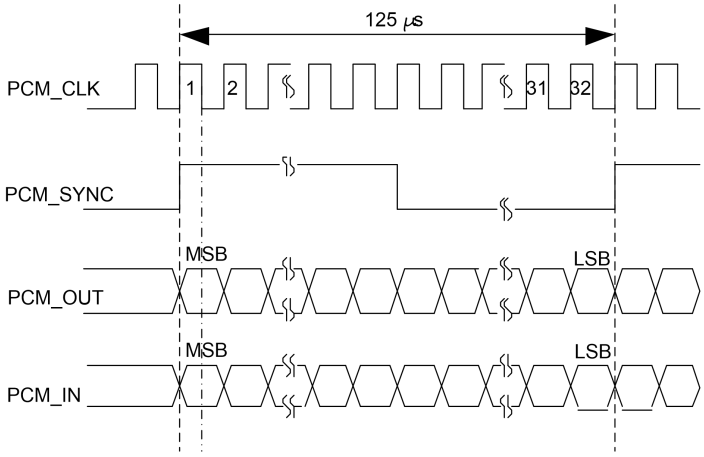


Figure 25: Timing of Long Frame Mode

In long frame mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK and an 8 kHz, 50% duty cycle PCM_SYNC.

The clock and mode of PCM can be configured by **AT+QDAI**, and the default configuration is short frame mode (PCM_CLK = 2048 kHz, PCM_SYNC = 8 kHz). See ***document [4]*** for more details.

The following figure shows a reference design of PCM and I2C interfaces with external codec IC.

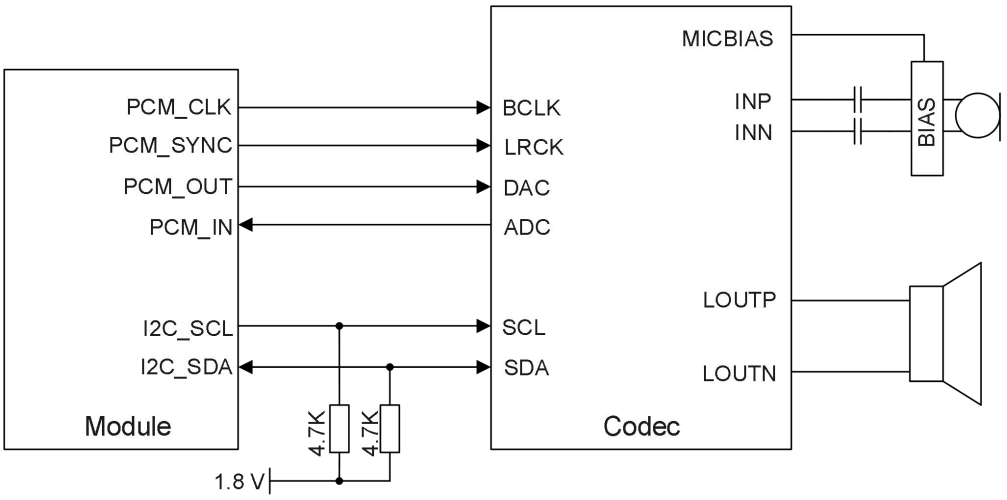


Figure 26: Reference Circuit of PCM and I2C Application with Audio Codec

NOTE

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuits on the PCM traces, especially for PCM_CLK.
2. The module works as a master device pertaining to I2C interface.

4.6. SPI

The module provides one SPI which only supports master mode with a maximum clock frequency of up to 50 MHz.

Table 17: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	44	DO	SPI clock	Only master mode is supported.
SPI_CS	41	DO	SPI chip select	
SPI_MISO	43	DI	SPI master-in slave-out	
SPI_MOSI	42	DO	SPI master-out slave-in	

The module provides a 1.8 V SPI. Use a voltage-level translator between the module and the peripheral device if the peripheral device is 3.3 V power domain. The following figure shows the reference design.

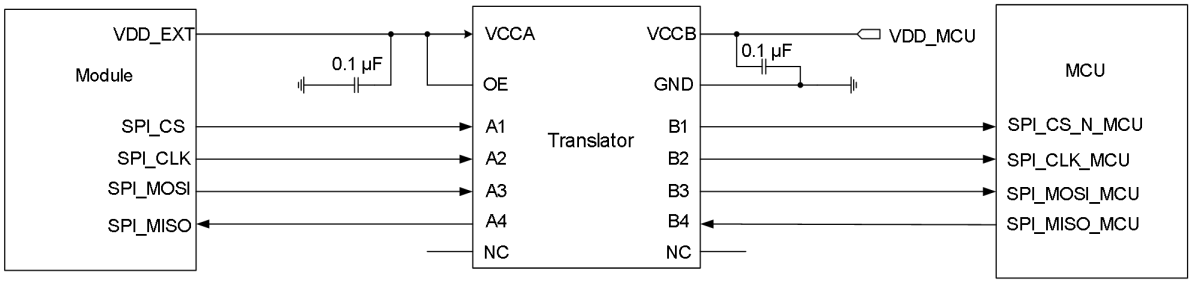


Figure 27: Reference Circuit of SPI with a Voltage-level Translator

4.7. Wireless Connectivity Interfaces

The following table shows the pin definition of wireless connectivity interfaces.

Table 18: Pin Definition of Wireless Connectivity Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCIe Part				
PCIE_REFCLK_P	105	AIO	PCIe reference clock (+)	Requires differential impedance of 85 Ω. If unused, keep them open.
PCIE_REFCLK_M	107		PCIe reference clock (-)	
PCIE_TX_P	103	AO	PCIe transmit (+)	
PCIE_TX_M	104		PCIe transmit (-)	
PCIE_RX_P	101	AI	PCIe receive (+)	
PCIE_RX_M	102		PCIe receive (-)	
PERST#	20	DIO	PCIe reset	
CLKREQ#	21	OD/ DIO	PCIe clock request	
PEWAKE#	100	OD/ DIO	PCIe wake up	
WLAN Coexistence and Control Part				
WLAN_SLP_CLK	85	DO	WLAN sleep clock	
WLAN_PWR_EN	91	DO	WLAN power control	Active high.

WLAN_WAKE	87	DI	Wake up module by an external Wi-Fi	
COEX_RXD	90	DI	5G/LTE and WLAN coexistence receive	
COEX_TXD	88	DO	5G/LTE and WLAN coexistence transmit	
WLAN_SW_CTRL	86	DI	Wi-Fi power control	
N79_TX_EN_TO_WLAN	92	DO	Notify n79 transmission from SDR transceiver to WLAN	
WLAN_PA_MUTING	94	DO	GPIO from SDX to disable WLAN PA	
WLAN_TX_EN_TO_N79	93	DI	Notify WLAN transmission from WLAN to SDR transceiver	
Bluetooth Part				
BT_EN	132	DO	Bluetooth enable control	Active high.

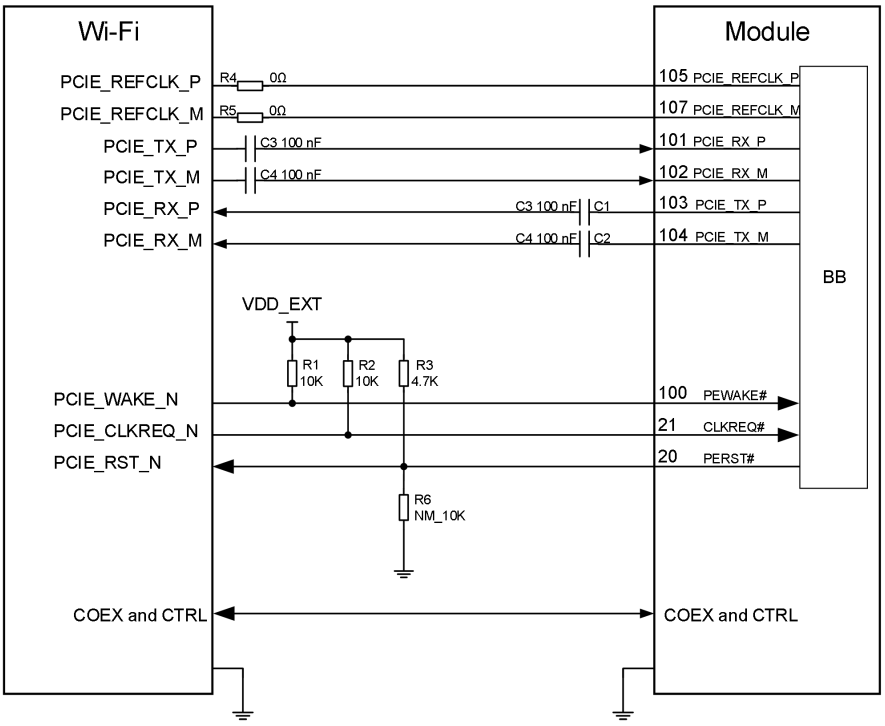


Figure 28: Reference Circuit of PCIe

4.8. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces.

Table 19: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	49	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	48	AI		

With **AT+QADC=<port>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0.
- **AT+QADC=1**: read the voltage value on ADC1.

For more details about these AT commands, see ***document [4]***.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground. The resolution of ADC is 15 bits.

The following table describes the characteristic of ADC function.

Table 20: Characteristics of ADC Interfaces

Parameter	Min.	Max.	Unit
ADC0 Input Voltage Range	0	VBAT_BB	V
ADC1 Input Voltage Range	0	VBAT_BB	V

NOTE

1. The input voltage of every ADC interface should not exceed its corresponding voltage range.
2. It is prohibited to directly supply any voltage to ADC interface when the module is not powered by the VBAT.
3. It is recommended to use a resistor divider circuit for ADC application.

4.9. SGMII Interface

The module provides an integrated Ethernet MAC with an SGMII interface and management interface. The key features of the SGMII interface are shown below:

- IEEE 802.3 compliant.
- Support 10 Mbps/100 Mbps/1000 Mbps Ethernet work mode.
- Support VLAN tagging.
- Support IEEE 1588 and Precision Time Protocol (PTP).

The following table shows the pin definition of SGMII interface.

Table 21: Pin Definition of SGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
Control Signal Part				
SGMII_RST_N	37	DO	SGMII reset external PHY	If unused, keep them open.
SGMII_INT_N	123	DI	SGMII interrupt	
SGMII_MDIO	36	DIO	SGMII management data input/output	
SGMII_MDC	121	DO	SGMII management data clock	
SGMII Signal Part				
SGMII_TX_M	34	AO	SGMII transmit (-)	Connect with a 0.1 μF capacitor. Requires differential impedance of 90 Ω.
SGMII_TX_P	119	AO	SGMII transmit (+)	
SGMII_RX_M	32	AI	SGMII receive (-)	Requires differential impedance of 90 Ω.
SGMII_RX_P	117	AI	SGMII receive (+)	

The following figure shows the simplified block diagram for Ethernet application.

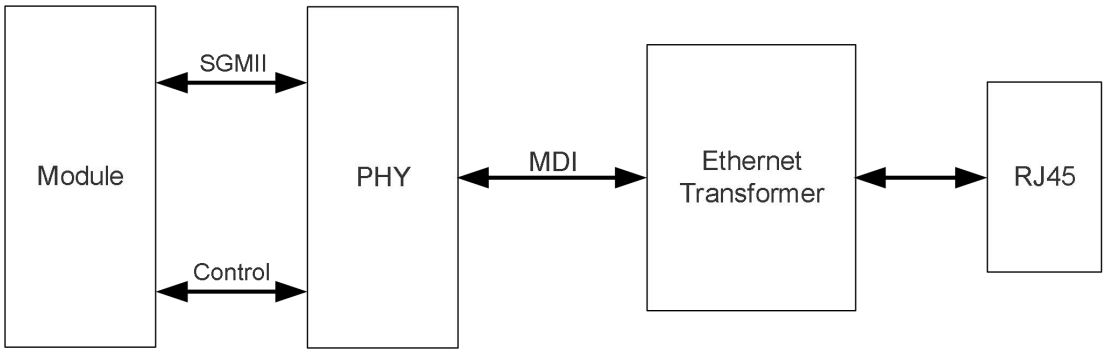


Figure 29: Simplified Block Diagram for Ethernet Application

To ensure the performance and reliability, follow the design notes below in the SGMII circuit design:

- Keep data traces and control signal traces of SGMII interface far away from power supply traces, crystal-oscillators, magnetic devices, sensitive signals and signals like RF signals, analog signals, and noise signals generated by clock, DC-DC.
- Keep the maximum trace length less than 10 inch and keep length matching on the differential pairs less than 20 mil.
- Keep the differential impedance of SGMII data traces within 90 Ω ±10 % and ensure the integrity of the reference ground.
- Make sure the trace spacing between SGMII_RX and SGMII_TX is at least 3 times of the trace width, and the same to the adjacent signal traces.

4.10. Indication Signals

Table 22: Pin Definition of Network Status Indication

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's network registration mode	If unused, keep them open.
NET_STATUS	6	DO	Indicate the module's network activity status	
STATUS	67	OD	Indicate the module's operation status	An external pull-up resistor is required. If unused, keep it open.
MAIN_RI	68	DO	Main UART ring indication	If unused, keep it

	open.

4.10.1. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two: NET_MODE and NET_STATUS. The following table describes the pin definition and logic level changes in different network status. The module provides two network status indication pins: the NET_MODE for the module's network registration status indication and the NET_STATUS for the module's network operation status indication. Both can drive corresponding LEDs.

Table 23: Network Status Indication Pin Level and Module Network Status

Pin Name	NET_MODE/NET_STATUS Level Status	Module Network Status
NET_MODE	Always High	Registered on LTE/5G NR network
	Always Low	Others
NET_STATUS	Blink slowly (200 ms High/1800 ms Low)	Network searching
	Blink slowly (1800 ms High/200 ms Low)	Idle
	Blink quickly (125 ms High/125 ms Low)	Data transmission is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

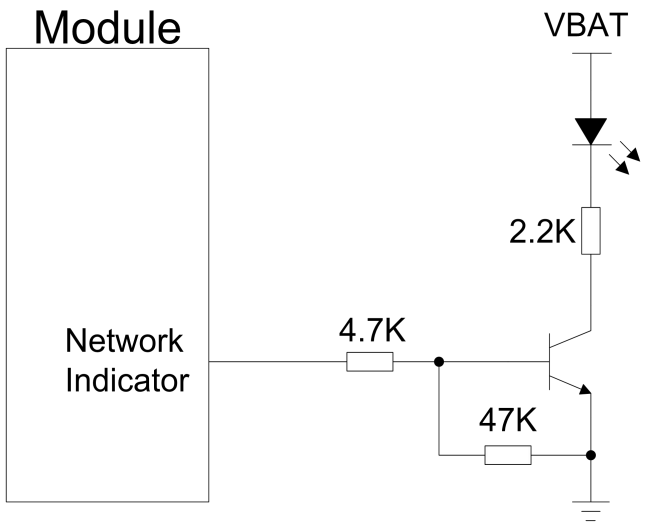


Figure 30: Reference Circuit of the Network Status Indication

4.10.2. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It can be connected to a GPIO of MCU with a pull-up resistor, or as LED indication circuit as below. When the module is turned on normally, the STATUS will present the low state. Otherwise, the STATUS will present high-impedance state.

The following figure shows different circuit designs of STATUS, and you can choose either one according to your application demands.

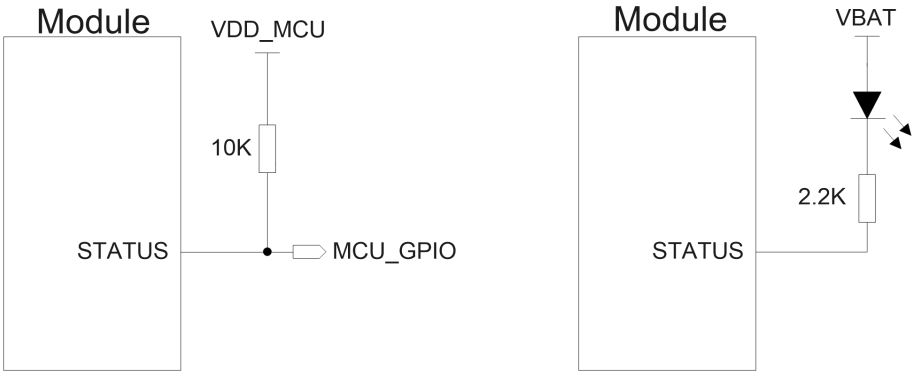


Figure 31: Reference Circuits of STATUS

NOTE

The status pin cannot be used as indication of module shutdown status when VBAT power supply is removed.

4.10.3. MAIN_RI

AT+QCFG="risignaltype","physical" can be used to configure MAIN_RI behavior. No matter on which port a URC is presented, the URC will trigger the behaviors of MAIN_RI pin.

NOTE

The **AT+QURCCFG** allows you to set the main UART or USB AT port as the URC information output port.

The default behaviors of MAIN_RI are shown as below, and can be changed by **AT+QCFG="urc/ri/ring"**. See ***document [4]*** for details.

Table 24: Behaviours of MAIN_RI

Module Status	MAIN_RI Level Status
Idle	MAIN_RI keeps at high level
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module's antenna interfaces include a main antenna interface, an Rx-diversity antenna interface which is used to resist the fall of signals caused by high-speed movement and multipath effect, and a GNSS antenna interface. The impedance of the antenna interfaces is 50 Ω.

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

Table 25: Pin Definition of Cellular Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Frequency Range (MHz)
ANT_MAIN	55	AIO	**Antenna 0 interface:** - **5G NR:** LB/MHB/5GLM_UHB/5GH TRX - **LTE:** LB/MHB/UHB TRX	**LB:** 617–960 MHz **MHB:** 1695–2690 MHz **5GLM_UHB:** 3300–3800 MHz **5GH:** 4400–5000 MHz
ANT_DRX	39	AIO	**Antenna 1 interface:** - **5G NR:** LB/MHB/5GLM_UHB/5GH DRX - **LTE:** LB/MHB/UHB DRX	**LB:** 617–960 MHz **MHB:** 1695–2690 MHz **5GLM_UHB:** 3300–3800 MHz **5GH:** 4400-5000 MHz

NOTE

The impedance of antenna interface is 50 Ω.

5.1.2. Antenna Tuner Control Interface

The module can use GRFC (generic RF control) interface to control external antenna tuner.

Table 26: Pin Description of GRFC Interface

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	53	DO	Generic RF Controller	If unused, keep them open.
GRFC2	139	DO		

Table 27: Truth Table of GRFC Interface (Unit: MHz)

GRFC1 Level	GRFC2 Level	Frequency Range	Band
Low	Low	TBD	TBD
Low	High	TBD	TBD
High	Low	TBD	TBD
High	High	TBD	TBD

5.1.3. Transmitting Power

The following table shows the RF output power of the module.

Table 28: RF Transmitting Power

Mode	Frequency Band	Max.	Min.
LTE	LTE bands	23 dBm ±2 dB (Class 3) [10]	< -40 dBm
	LTE HPUE bands (B38/B40/B41/B42/B43)	26 dBm ±2 dB (Class 2)	< -40 dBm
5G NR	5G NR bands	23 dBm ±2 dB (Class 3) [11]	< -40 dBm
	5G NR HPUE bands (n38/n40/n41/n77/n78/n79)	26 dBm +2/-3 dB (Class 2)	< -40 dBm

[10] The transmitting power of B30 is Class 3 (22 dBm ±2 dB).
[11] The transmitting power of n30 is Class 3 (22 dBm ±2 dB).

5.1.4. Receiving Sensitivity

The following table shows the conducted RF receiving sensitivity of the module.

Table 29: Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency	Receiving Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO [12]	
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B2 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B4 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B12 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B13 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B14 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B17 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B18 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B19 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B20 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B25 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B26 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B28 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B30 (10 MHz)	TBD	TBD	TBD	TBD
LTE-TDD B34 (10 MHz)	TBD	TBD	TBD	TBD
LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	TBD

[12] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which can improve RX performance.

LTE-TDD B39 (10 MHz)	TBD	TBD	TBD	TBD
LTE-TDD B40 (10 MHz)	TBD	TBD	TBD	TBD
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	TBD
LTE-TDD B42 (10 MHz)	TBD	TBD	TBD	TBD
LTE-TDD B43 (10 MHz)	TBD	TBD	TBD	TBD
LTE-TDD B48 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B66 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B70 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B71 (10 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n1 (20 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n2 (20 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n3 (20 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n5 (20 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n7 (20 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n8 (20 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n12 (10 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n13 (10 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n14(10 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n18 (10 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n20 (20 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n25 (20 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n26 (20 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n28 (20 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n30 (10 MHz)	TBD	TBD	TBD	TBD
5G NR TDD n38 (20 MHz)	TBD	TBD	TBD	TBD

5G NR TDD n40 (20 MHz)	TBD	TBD	TBD	TBD
5G NR TDD n41 (20 MHz)	TBD	TBD	TBD	TBD
5G NR TDD n48 (20 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n66 (20 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n70 (10 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n71 (20 MHz)	TBD	TBD	TBD	TBD
5G NR TDD n77 (20 MHz)	TBD	TBD	TBD	TBD
5G NR TDD n78 (20 MHz)	TBD	TBD	TBD	TBD
5G NR TDD n79 (20 MHz)	TBD	TBD	TBD	TBD

5.1.5. Reference Design

A reference design of cellular antenna interfaces is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

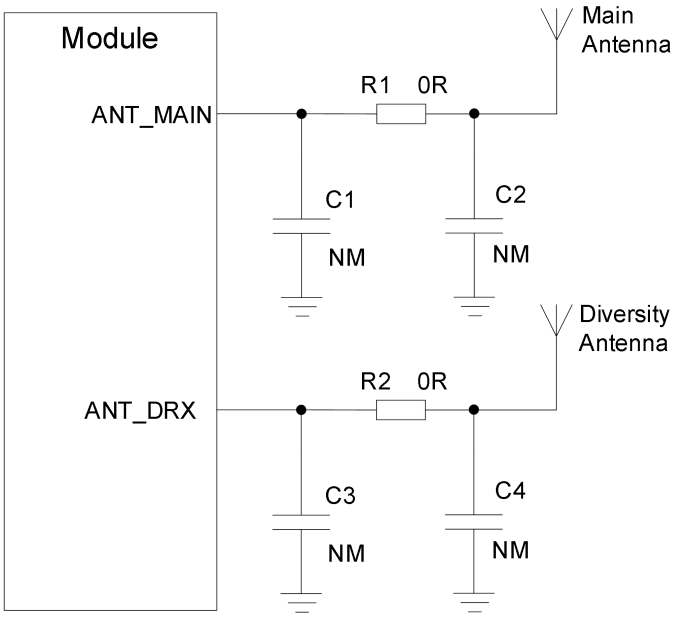


Figure 32: Reference Circuit of Cellular Antenna Interfaces

NOTE

1. Keep proper distance between the main antenna and the Rx-diversity antenna to improve the

receiving sensitivity.
2. For the operation of ANT_MAIN and ANT_DRX, see **AT+QCFG="divctl"** in ***document [4]*** for details.
3. Place the π-type matching components (R1, C1, C2 and R2, C3, C4) as close to the antenna as possible.
4. It is recommended that the straight-line distance between the antenna and the module be greater than 15 mm to achieve better wireless performance of the whole device.

5.2. GNSS (Optional)

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS and Galileo.

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, the module's GNSS engine is switched off. It has to be switched on via AT command.

5.2.1. Antenna Interface & Frequency Bands

Table 30: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	51	AI	GNSS antenna interface	50 Ω impedance. If unused, keep it open.

Table 31: GNSS Frequency (Unit: MHz)

GNSS Constellation Type	Frequency
GPS	1575.42 ±1.023 (L1) 1227.60 ±1.023 (L2) [13] 1176.45 ±10.23 (L5)
GLONASS	1597.5–1605.8
BDS	1561.098 ±2.046 (B1I)
Galileo	1575.42 ±2.046 (E1) 1176.45 ±10.23 (E5a)

[13] If you need this function, contact Quectel Technical Support.

5.2.2. GNSS Performance

The following table shows the GNSS performance of the module.

Table 32: GNSS Performance

Parameter	Mode	Condition	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	TBD	dBm
	Reacquisition	Autonomous	TBD	dBm
	Tracking	Autonomous	TBD	dBm
TTFF (GNSS)	Cold start @ open sky	Autonomous	TBD	s
		XTRA start	TBD	s
	Warm start @ open sky	Autonomous	TBD	s
		XTRA start	TBD	s
	Hot start @ open sky	Autonomous	TBD	s
		XTRA start	TBD	s
Accuracy (GNSS)	CEP-50	Autonomous @ open sky	TBD	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Cold start sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

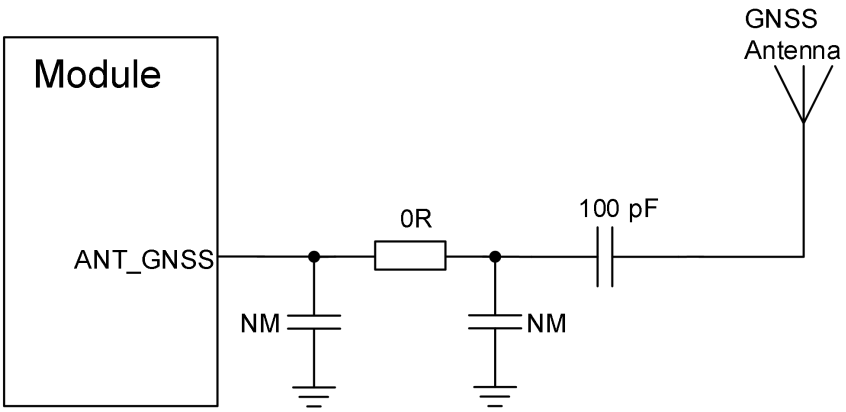


Figure 33: Reference Circuit of GNSS Antenna

NOTE

Only passive antenna is supported.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

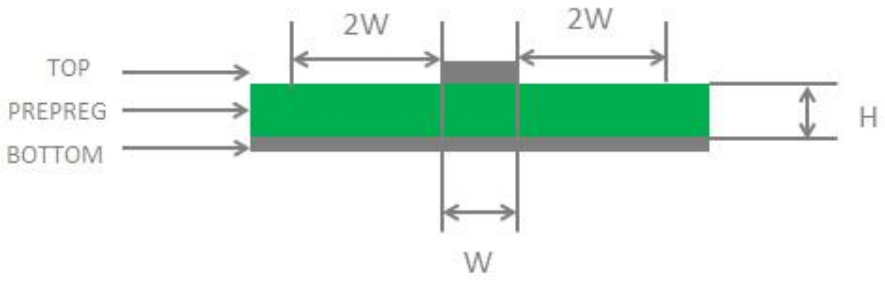


Figure 34: Microstrip Design on a 2-layer PCB

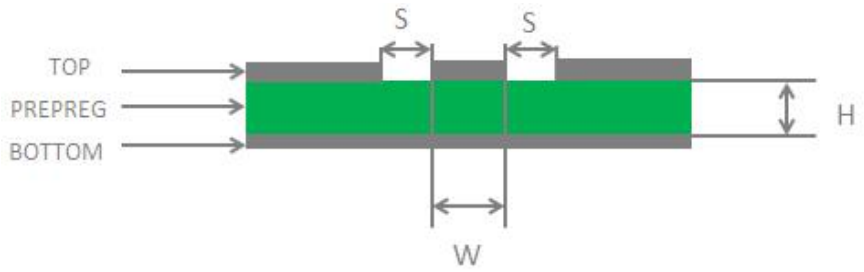


Figure 35: Coplanar Waveguide Design on a 2-layer PCB

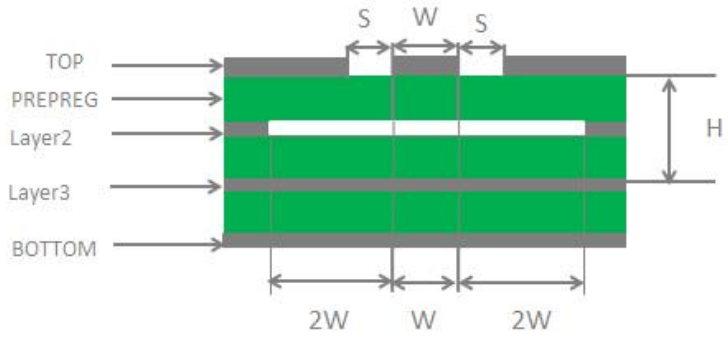


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

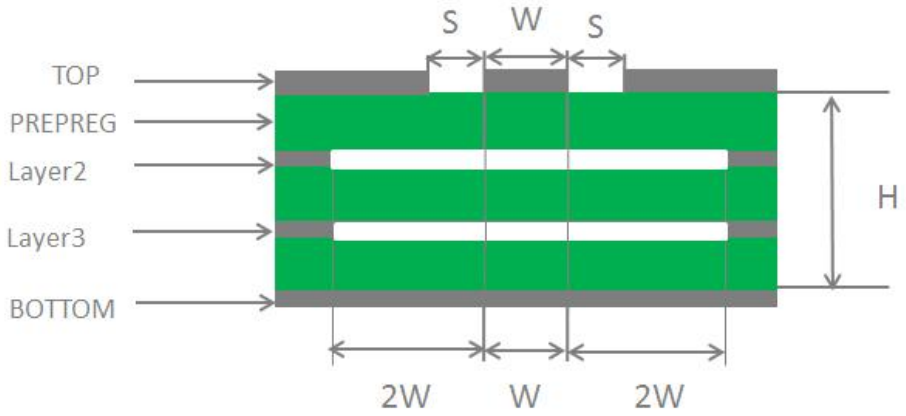


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully

connected to ground.

- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

5.4. Requirements for Antenna Design

Table 33: Requirements for Antenna Design

Antenna Type	Requirements
GNSS	• Frequency range: - L1: 1559–1609 MHz - L2: 1226–1229 MHz - L5: 1166–1187 MHz • Polarization: RHCP or linear • VSWR: ≤ 2 (Typ.)
	For passive antenna usage: - Passive antenna gain: > 0 dBi
Cellular	• VSWR: ≤ 2 • Efficiency: > 30 % • Max. input power: 50 W • Input impedance: 50 Ω • Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

NOTE

It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.5. RF Connector Recommendation

The receptacle dimensions are illustrated as below.

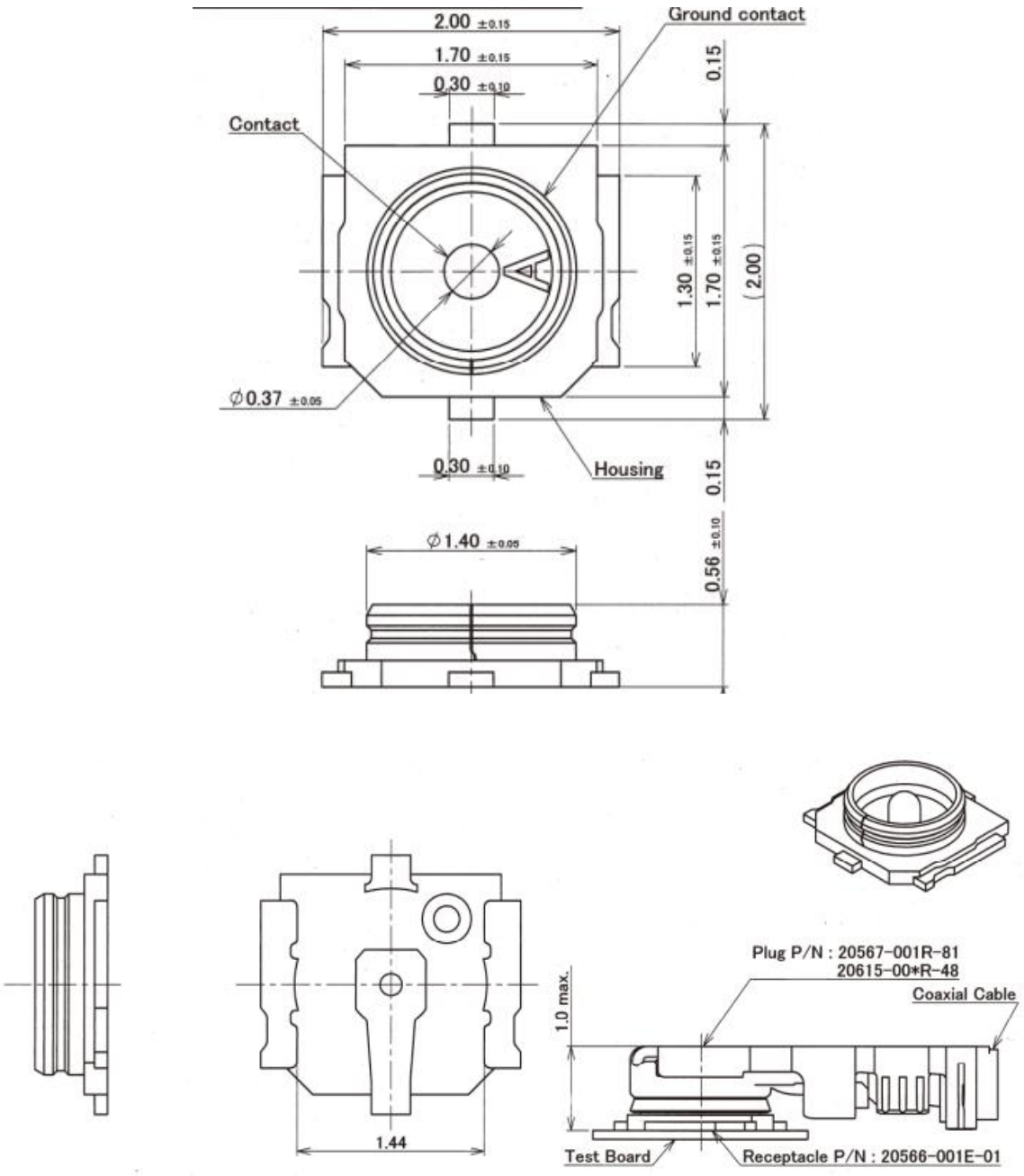


Figure 38: Dimensions of the Receptacles (Unit: mm)

The following figure shows the dimensions of mated plugs using Ø0.81 mm coaxial cables.

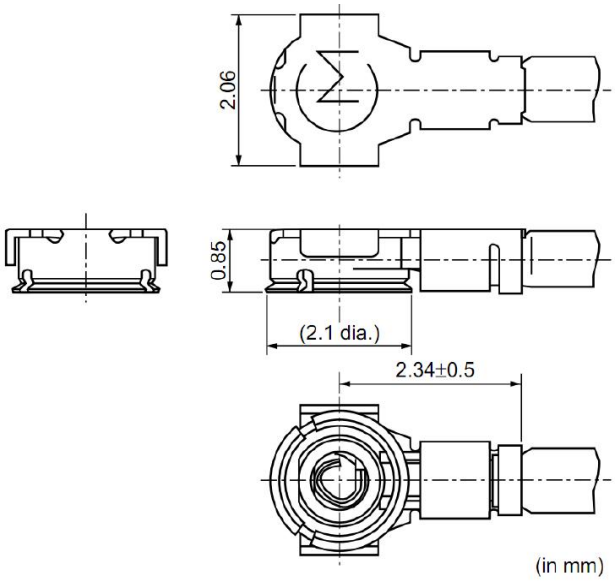


Figure 39: Dimensions of Mated Plugs Using Ø0.81 mm Coaxial Cables (Unit: mm)

5.5.1. Recommended RF Connector for Installation

5.5.1.1. Assemble Coaxial Cable Plug Manually

The illustration for plugging in a coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

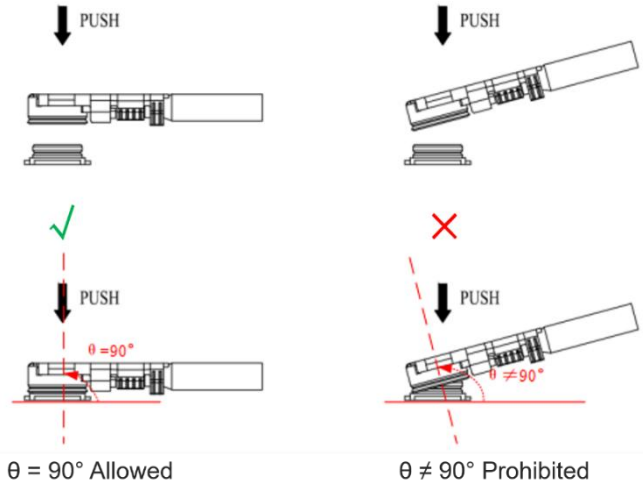


Figure 41: Plug in a Coaxial Cable Plug

The illustration of pulling out the coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

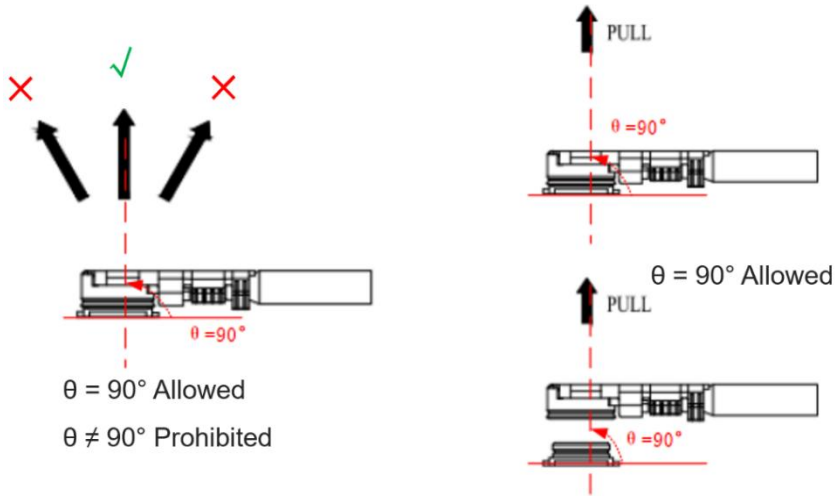


Figure 42: Pull out a Coaxial Cable Plug

5.5.1.2. Assemble Coaxial Cable Plug with Jig

The pictures of installing the coaxial cable plug with a jig is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

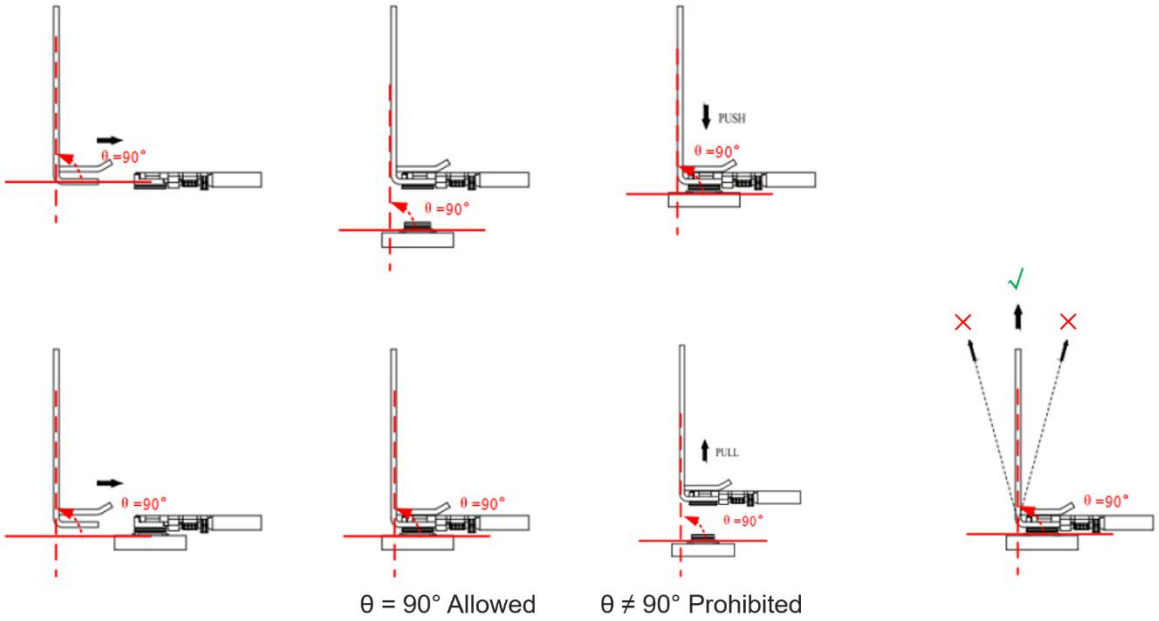


Figure 43: Install the Coaxial Cable Plug with Jig

5.5.2. Recommended Manufacturers of RF Connector and Cable

RF connectors and cables by I-PEX4 are recommended. For more details, visit https://www.i-pex.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 34: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.25	V
Peak Current of VBAT_BB	-	TBD	A
Peak Current of VBAT_RF	-	TBD	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

6.2. Power Supply Ratings

Table 35: Module's Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltage must be within this range	3.3	3.8	4.3	V
	Voltage drop during burst transmission	At maximum power control level	-	-	400	mV
I_{VBAT}	Peak power consumption	At Maximum power control level	-	TBD	TBD	A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

6.3. Power Consumption

Table 36: Power Consumption

Mode	Condition	Band/Combination	Typ.	Unit
Turn off	Power off	-	TBD	μA
Sleep Mode	**AT+CFUN=0** (USB 2.0 Suspend)	-	TBD	mA
	AT+CFUN=4 (USB 2.0 Suspend)	-	TBD	mA
	SA FDD PF = 64 (USB 2.0 active)	-	TBD	mA
	SA TDD PF = 64 (USB 2.0 active)	-	TBD	mA
Idle mode	SA PF = 64 (USB 2.0 active)	-	TBD	mA
	SA PF = 64 (USB 2.0 active)	-	TBD	mA
LTE data transmission (GNSS OFF)	LTE LB @ 24 dBm	B5	TBD	mA
	LTE MB @ 24 dBm	B1	TBD	mA
	LTE HB @ 24 dBm	B7	TBD	mA
	LTE HPUE @ 24 dBm	B41	TBD	mA

5G SA data transmission (GNSS OFF)	5G NR LB @ 23 dBm	n5	TBD	mA
	5G NR MB @ 23 dBm	n1	TBD	mA
	5G NR HB @ 23 dBm	n7	TBD	mA
	5G NR 5GLM_UHB @ 26 dBm	n78	TBD	mA
	5G NR 5GH @ 26 dBm	n79	TBD	mA

6.4. Digital I/O Characteristics

Table 37: VDD_EXT I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.65 × VDD_EXT	VDD_EXT + 0.3
V_{IL}	Low-level input voltage	-0.3	0.35 × VDD_EXT
V_{OH}	High-level output voltage	VDD_EXT - 0.45	-
V_{OL}	Low-level output voltage	-	0.45

Table 38: (U)SIM High/Low-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD + 0.3
V_{IL}	Low-level input voltage	-0.3	0.2 × USIM_VDD
V_{OH}	High-level output voltage	0.8 × USIM_VDD	-
V_{OL}	Low-level output voltage	-	0.4

6.5. ESD

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 39: Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 40: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [14]	-30	+25	+75	ºC
Extended Temperature Range [15]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

[14] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[15] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

6.7. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely;
  - Choose the heatsink with adequate fins to dissipate heat;
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;
  - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

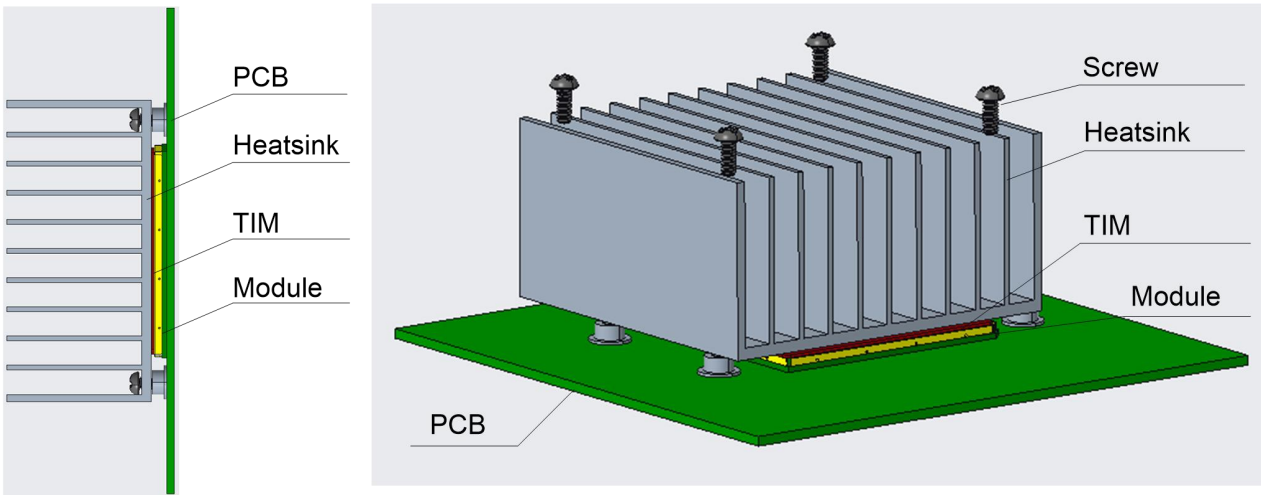


Figure 40: Placement and Fixing of the Heatsink

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm, and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

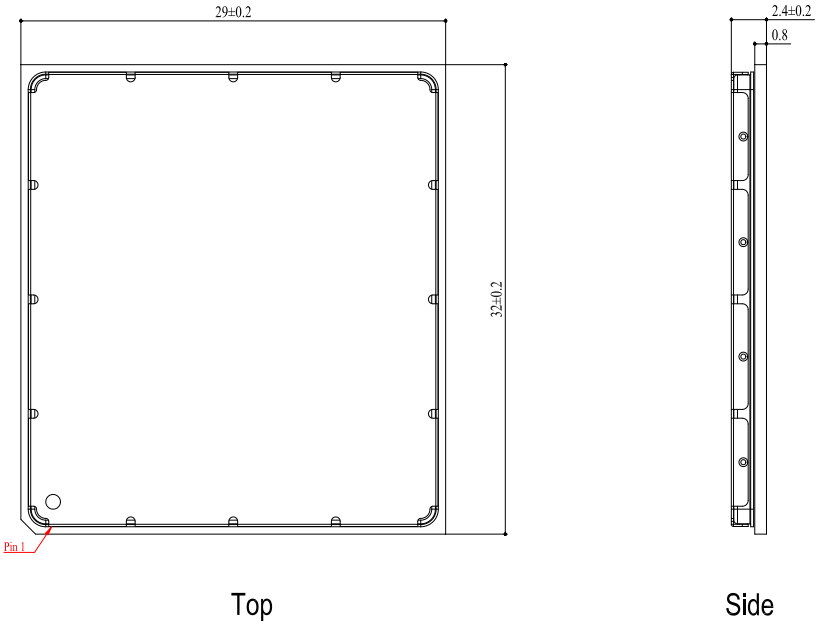


Figure 41: Top and Side Dimensions

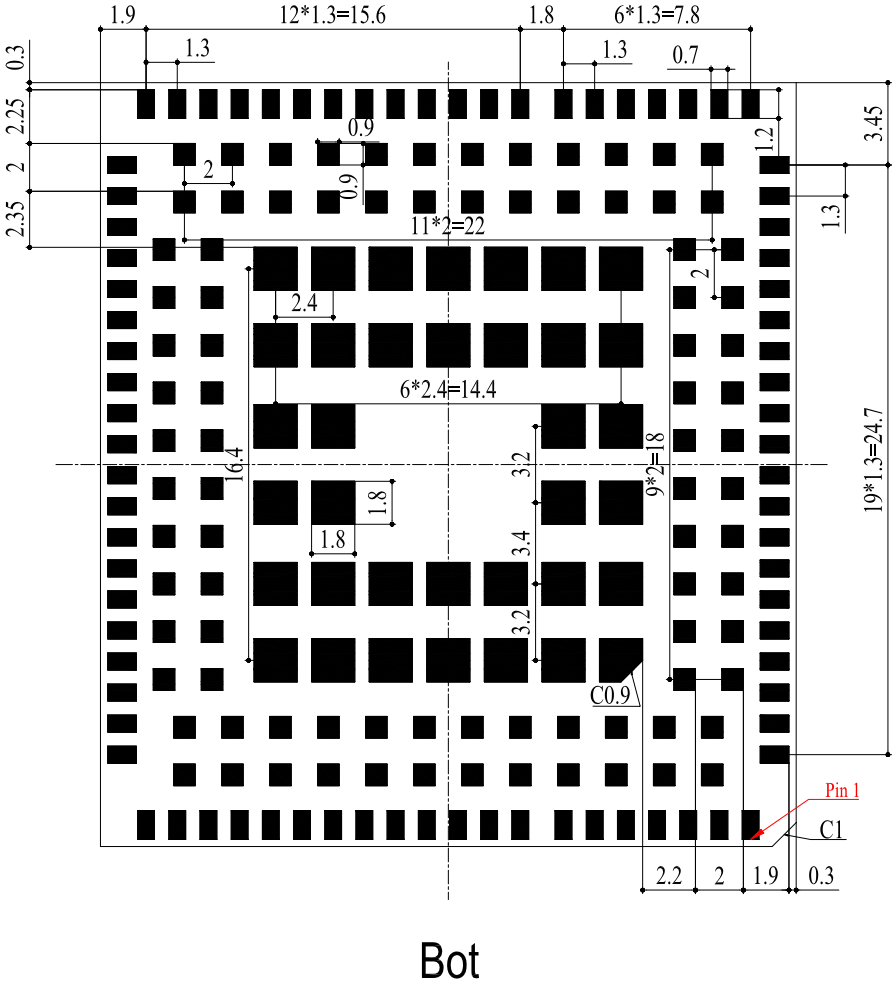


Figure 42: Bottom Dimension (Bottom View)

NOTE

The package warpage level of the module refers to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

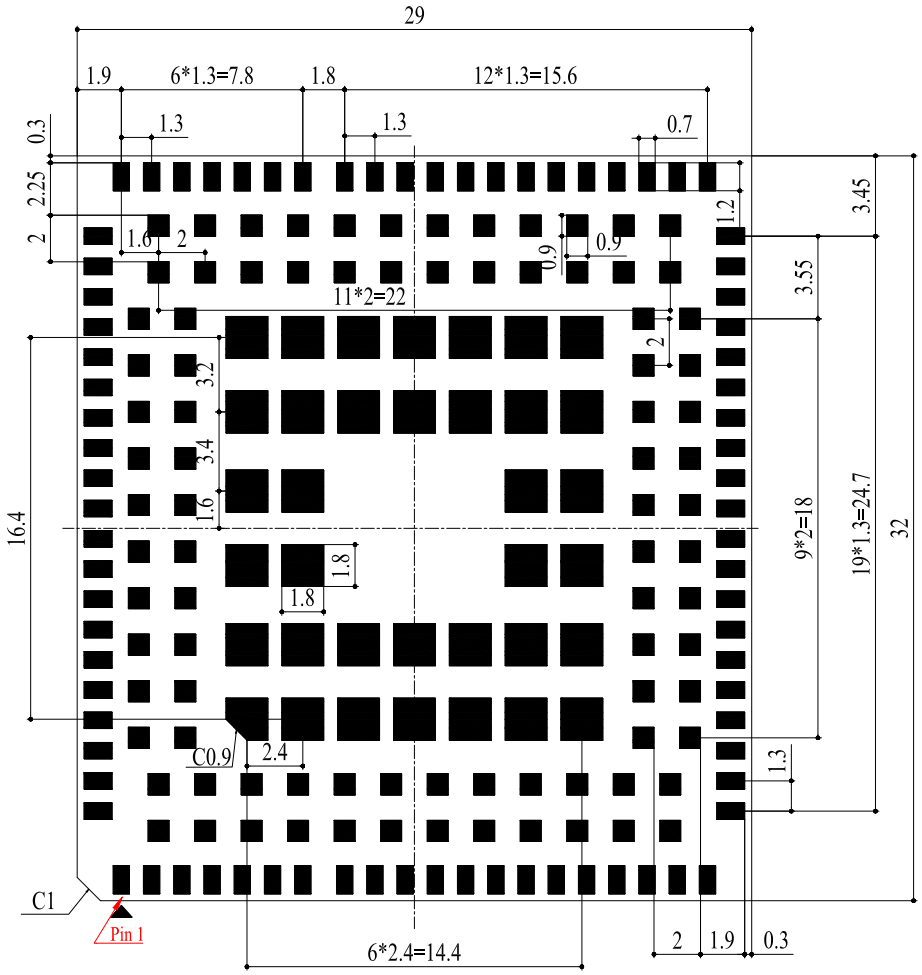


Figure 43: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom views

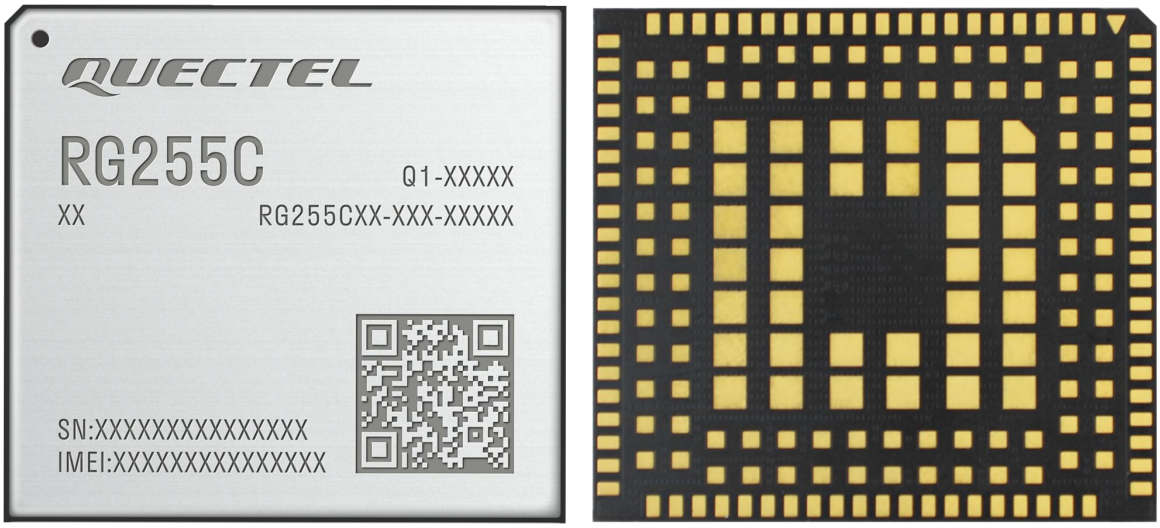


Figure 44: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [16] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[16] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [6]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

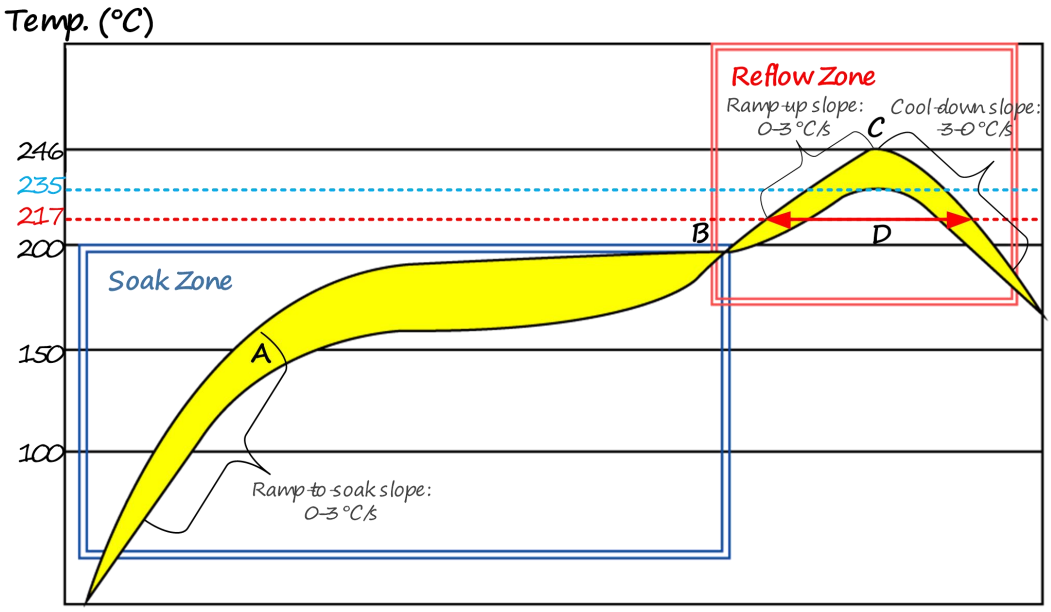


Figure 45: Recommended Reflow Soldering Thermal Profile

Table 41: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
5. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [7]***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

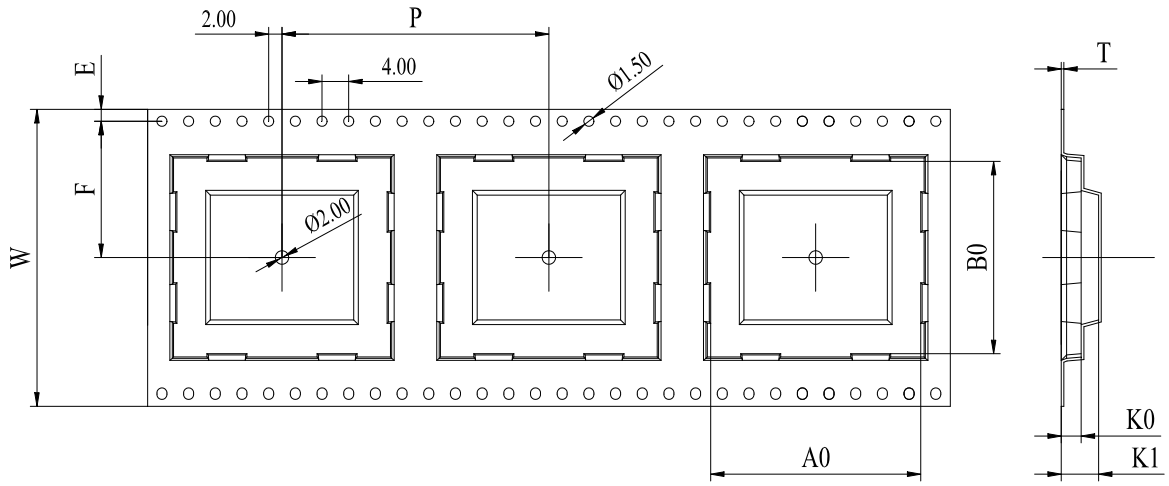


Figure 46: Carrier Tape Dimension Drawing (Unit: mm)

Table 42: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	44	0.35	32.5	29.5	3	3.8	20.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

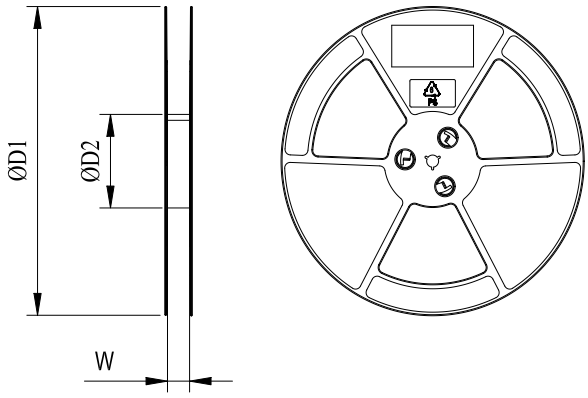


Figure 47: Plastic Reel Dimension Drawing

Table 43: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

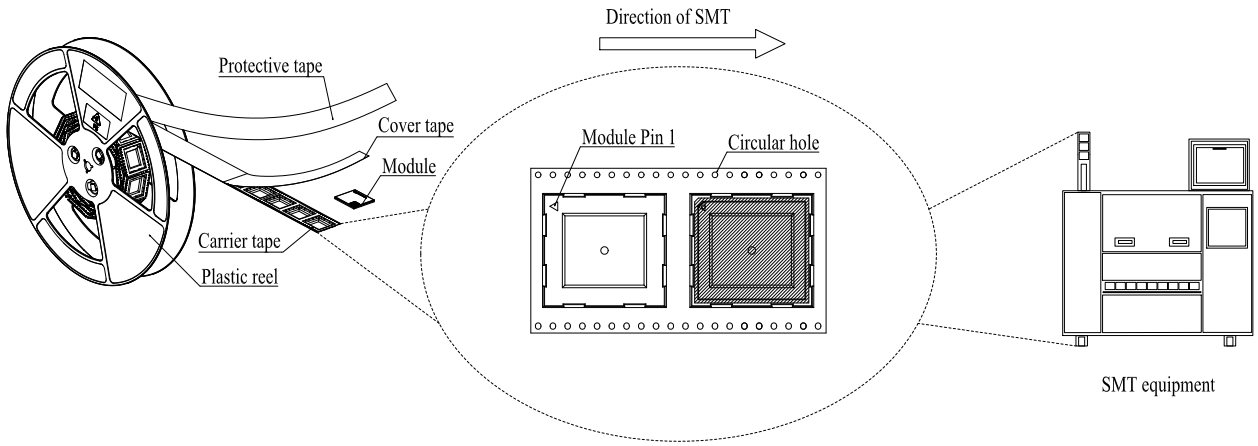
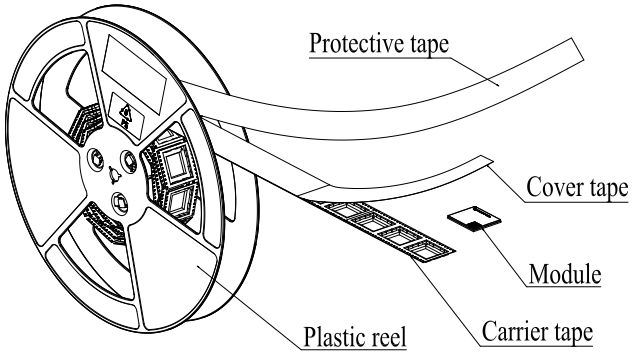


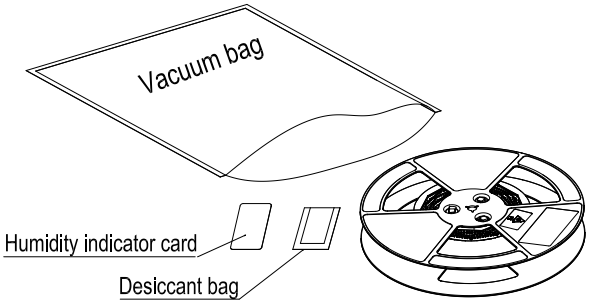
Figure 48: Mounting Direction

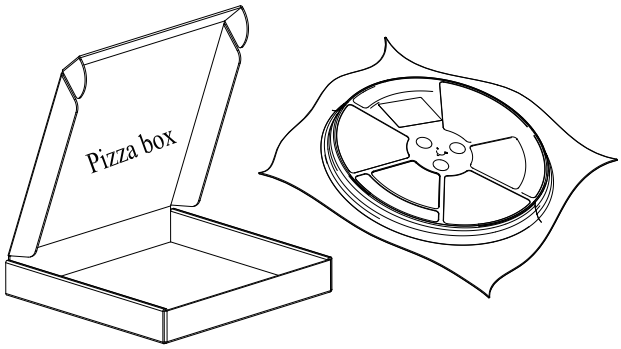
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 200 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 800 modules.

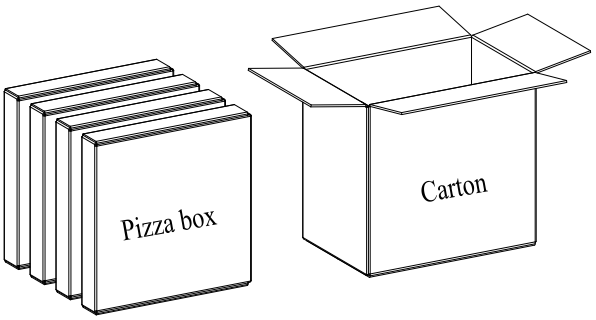


Figure 49: Packaging Process

9 Appendix A References

Table 44: Related Documents

Document Name
[1] Quectel_RG255C_Series_QuecOpen_GPIO_Configuration
[2] Quectel_RG255C_Series_Reference_Design
[3] Quectel_5G_RedCap_EVB_User_Guide
[4] Quectel_RG255C_Series&RM255C-GL_AT_Commands_Manual
[5] Quectel_RF_Layout_Application_Note
[6] Quectel_Module_Stencil_Design_Requirements
[7] Quectel_Module_SMT_Application_Note

Table 45: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
AMR-WB	Adaptive Multi-Rate Wideband
BDS	BeiDou Navigation Satellite System
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CTS	Clear To Send
DDR	Double Data Rate
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink

DTR	Data Terminal Ready
DUN	Dial-Up Networking
ECM	Ethernet Control Model
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP-SSL: FTP over SSL/FTP Secure
Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HPUE	High Power User Equipment
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
I/O	Input/Output
IMS	IP Multimedia Subsystem
LED	Light Emitting Diode
LTE	Long Term Evolution
LwM2M	Lightweight M2M
M2M	Machine to Machine
MBIM	Mobile Broadband Interface Model
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MQTT	Message Queuing Telemetry Transport

MS	Mobile Station (GSM engine)
MSL	Moisture Sensitivity Level
MT	Mobile Terminated
NAS	Non-Access Stratum.
NITZ	Network Identity and Time Zone / Network Informed Time Zone.
NTP	Network Time Protocol
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PING	Packet Internet Groper
POS	Point of Sale
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RMNet	Remote Network
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RNDIS	Remote Network Driver Interface Specification
Rx	Receive
SA	Standalone
SCS	Sub-Carrier Space
SGMII	Serial Gigabit Media Independent Interface
SIMO	Single Input Multiple Output

SMS	Short Message Service
SMD	Surface Mount Device
SMTP	Simple Mail Transfer Protocol
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TLS	Transport Layer Security
TX	Transmitting Direction
UDP	User Datagram Protocol
UL	Uplink
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
VLAN	Virtual Local Area Network
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
VSWR	Voltage Standing Wave Ratio
WLAN	Wireless Local Area Network

10 Appendix B Operating Frequencies

Table 46: Operating Frequencies (5G)

5G	Duplex Mode	Uplink Operating Band	Downlink Operating Band	Unit
n1	FDD	1920–1980	2110–2170	MHz
n2	FDD	1850–1910	1930–1990	MHz
n3	FDD	1710–1785	1805–1880	MHz
n5	FDD	824–849	869–894	MHz
n7	FDD	2500–2570	2620–2690	MHz
n8	FDD	880–915	925–960	MHz
n12	FDD	699–716	729–746	MHz
n13	FDD	777–787	746–756	MHz
n14	FDD	788–798	758–768	MHz
n18	FDD	815–830	860–875	MHz
n20	FDD	832–862	791–821	MHz
n24	FDD	1626.5–1660.5	1525–1559	MHz
n25	FDD	1850–1915	1930–1995	MHz
n26	FDD	814–849	859–894	MHz
n28	FDD	703–748	758–803	MHz
n29	SDL	-	717–728	MHz
n30	FDD	2305–2315	2350–2360	MHz
n34	TDD	2010–2025	2010–2025	MHz
n38	TDD	2570–2620	2570–2620	MHz
n39	TDD	1880–1920	1880–1920	MHz

n40	TDD	2300–2400	2300–2400	MHz
n41	TDD	2496–2690	2496–2690	MHz
n46	TDD	5150–5925	5150–5925	MHz
n47	TDD	5855–5925	5855–5925	MHz
n48	TDD	3550–3700	3550–3700	MHz
n50	TDD	1432–1517	1432–1517	MHz
n51	TDD	1427–1432	1427–1432	MHz
n53	TDD	2483.5–2495	2483.5–2495	MHz
n65	FDD	1920–2010	2110–2200	MHz
n66	FDD	1710–1780	2110–2200	MHz
n67	SDL	-	738–758	MHz
n70	FDD	1695–1710	1995–2020	MHz
n71	FDD	663–698	617–652	MHz
n74	FDD	1427–1470	1475–1518	MHz
n75	SDL	-	1432–1517	MHz
n76	SDL	-	1427–1432	MHz
n77	TDD	3300–4200	3300–4200	MHz
n78	TDD	3300–3800	3300–3800	MHz
n79	TDD	4400–5000	4400–5000	MHz
n80	SUL	1710–1785	-	MHz
n81	SUL	880–915	-	MHz
n82	SUL	832–862	-	MHz
n83	SUL	703–748	-	MHz
n84	SUL	1920–1980	-	MHz
n85	FDD	698–716	728–746	MHz
n86	SUL	1710–1780	-	MHz

n89	SUL	824–849	-	MHz
n90	TDD	2496–2690	2496–2690	MHz
n91	FDD	832–862	1427–1432	MHz
n92	FDD	832–862	1432–1517	MHz
n93	FDD	880–915	1427–1432	MHz
n94	FDD	880–915	1432–1517	MHz
n95	SUL	2010–2025	-	MHz
n96	TDD	5925–7125	5925–7125	MHz
n97	SUL	2300–2400	-	MHz
n98	SUL	1880–1920	-	MHz
n99	SUL	1626.5–1660.5	-	MHz
n257	-	26.50–29.50	26.50–29.50	GHz
n258	-	24.25–27.50	24.25–27.50	GHz
n260	-	37.00–40.00	37.00–40.00	GHz
n261	-	27.50–28.35	27.50–28.35	GHz

Table 47: Operating Frequencies (2G + 3G + 4G)

2G	3G	4G	Duplex Mode	Uplink Operating Frequency	Downlink Operating Frequency	Unit
-	B1	B1	FDD	1920–1980	2110–2170	MHz
PCS1900	B2/BC1	B2	FDD	1850–1910	1930–1990	MHz
DCS1800	B3	B3	FDD	1710–1785	1805–1880	MHz
-	B4	B4	FDD	1710–1755	2110–2155	MHz
GSM850	B5/BC0	B5	FDD	824–849	869–894	MHz
-	B6	-	FDD	830–840	875–885	MHz
-	B7	B7	FDD	2500–2570	2620–2690	MHz
EGSM900	B8	B8	FDD	880–915	925–960	MHz

-	B9	B9	FDD	1749.9–1784.9	1844.9–1879.9	MHz
-	B10	B10	FDD	1710–1770	2110–2170	MHz
-	B11	B11	FDD	1427.9–1447.9	1475.9–1495.9	MHz
-	B12	B12	FDD	699–716	729–746	MHz
-	B13	B13	FDD	777–787	746–756	MHz
-	B14	B14	FDD	788–798	758–768	MHz
-	-	B17	FDD	704–716	734–746	MHz
-	-	B18	FDD	815–830	860–875	MHz
-	B19	B19	FDD	830–845	875–890	MHz
-	B20	B20	FDD	832–862	791–821	MHz
-	B21	B21	FDD	1447.9–1462.9	1495.9–1510.9	MHz
-	B22	B22	FDD	3410–3490	3510–3590	MHz
-	-	B24	FDD	1626.5–1660.5	1525–1559	MHz
-	B25	B25	FDD	1850–1915	1930–1995	MHz
-	B26	B26	FDD	814–849	859–894	MHz
-	-	B27	FDD	807–824	852–869	MHz
-	-	B28	FDD	703–748	758–803	MHz
-	-	B29	FDD [17]	-	717–728	MHz
-	-	B30	FDD	2305–2315	2350–2360	MHz
-	-	B31	FDD	452.5–457.5	462.5–467.5	MHz
-	-	B32	FDD [17]	-	1452–1496	MHz
-	B33	B33	TDD	1900–1920	1900–1920	MHz
-	B34	B34	TDD	2010–2025	2010–2025	MHz
-	B35	B35	TDD	1850–1910	1850–1910	MHz
-	B36	B36	TDD	1930–1990	1930–1990	MHz
	B37	B37	TDD	1910–1930	1910–1930	MHz

[17] Restricted to E-UTRA operation when carrier aggregation is configured. The downlink operating band is paired with the uplink operating band (external) of the carrier aggregation configuration that is supporting the configured Pcell.

-	B38	B38	TDD	2570–2620	2570–2620	MHz
-	B39	B39	TDD	1880–1920	1880–1920	MHz
-	B40	B40	TDD	2300–2400	2300–2400	MHz
-	-	B41	TDD	2496–2690	2496–2690	MHz
-	-	B42	TDD	3400–3600	3400–3600	MHz
-	-	B43	TDD	3600–3800	3600–3800	MHz
-	-	B44	TDD	703–803	703–803	MHz
-	-	B45	TDD	1447–1467	1447–1467	MHz
-	-	B46	TDD	5150–5925	5150–5925	MHz
-	-	B47	TDD	5855–5925	5855–5925	MHz
-	-	B48	TDD	3550–3700	3550–3700	MHz
-	-	B50	TDD	1432–1517	1432–1517	MHz
-	-	B51	TDD	1427–1432	1427–1432	MHz
-	-	B52	TDD	3300–3400	3300–3400	MHz
-	-	B65	FDD	1920–2010	2110–2200	MHz
-	-	B66	FDD [18]	1710–1780	2110–2200	MHz
-	-	B67	FDD [17]	-	738–758	MHz
-	-	B68	FDD	698–728	753–783	MHz
-	-	B69	FDD [17]	-	2570–2620	MHz
-	-	B70	FDD [19]	1695–1710	1995–2020	MHz
-	-	B71	FDD	663–698	617–652	MHz
-	-	B72	FDD	451–456	461–466	MHz
-	-	B73	FDD	450–455	460–465	MHz
-	-	B74	FDD	1427–1470	1475–1518	MHz
-	-	B75	FDD [17]	-	1432–1517	MHz
-	-	B76	FDD [17]	-	1427–1432	MHz

[18] The range 2180–2200 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured.

-	-	B85	FDD	698–716	728–746	MHz
-	-	B87	FDD	410–415	420–425	MHz
-	-	B88	FDD	412–417	422–427	MHz

Hereby, [Quectel Wireless Solutions Co., Ltd.] declares that the radio equipment type [RG255C-GL] is in compliance with Directive 2014/53/EU. The full text of the EU declaration of conformity is available at the following internet address: http://www.quectel.com/support/technical.htm
This equipment should be installed and operated with minimum distance 20cm between the radiator and your body；

Disposal of old electrical appliances

The European directive 2012/19/EU on Waste Electrical and Electronic Equipment (WEEE), requires that old household electrical appliances must not be disposed of in the normal unsorted municipal waste stream. Old appliances must be collected separately in order to optimize the recovery and recycling of the materials they contain, and reduce the impact on human health and the environment.
The crossed out "wheeled bin" symbol on the product reminds you of your obligation, that when you dispose of the appliance, it must be separately collected.
Consumers should contact their local authority or retailer for information concerning the correct disposal of their old appliance.

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[19] The range 2010–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and Tx-Rx separation is 300 MHz. The range 2005–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and Tx-Rx separation is 295 MHz.

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part
15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2024RG255CGL”
“Contains IC: 10224A-024RG255CGL “
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

FCC

Band	Antenna Type	Allowed Max Gain(dBi)
LTE Band 2	External Antenna	8.00

LTE Band 4	External Antenna	5.00
LTE Band 5	External Antenna	9.41
LTE Band 7	External Antenna	8.00
LTE Band 12	External Antenna	8.70
LTE Band 13	External Antenna	9.16
LTE Band 14	External Antenna	9.23
LTE Band 17	External Antenna	8.74
LTE Band 25	External Antenna	8.00
LTE Band 26 (814~824)	External Antenna	9.36
LTE Band 26 (824~849)	External Antenna	9.41
LTE Band 30	External Antenna	-0.02
LTE Band 38	External Antenna	5.00
LTE Band 41	External Antenna	5.00
LTE Band 42	External Antenna	2.00
LTE Band 42 Part 96	External Antenna	-5.00
LTE Band 43	External Antenna	2.00
LTE Band 43 Part 96	External Antenna	-5.00
LTE Band 48	External Antenna	-2.00
LTE Band 66	External Antenna	5.00
LTE Band 70	External Antenna	5.00
LTE Band 71	External Antenna	8.48
NR Band n2	External Antenna	8.00
NR Band n5	External Antenna	9.42
NR Band n7	External Antenna	8.00
NR Band n12	External Antenna	8.71
NR Band n13	External Antenna	9.16
NR Band n14	External Antenna	9.23
NR Band n25	External Antenna	8.00
NR Band n26 (814~824)	External Antenna	9.37
NR Band n26 (824~849)	External Antenna	9.42
NR Band n30	External Antenna	-0.02
NR Band n38	External Antenna	5.00
NR Band n41	External Antenna	5.00
NR Band n66	External Antenna	5.00
NR Band n70	External Antenna	5.00
NR Band n71	External Antenna	8.48
NR Band n77	External Antenna	2.00

(3450-3550)		
NR Band n77 (3700-3980)	External Antenna	2.00
NR Band n78 (3450-3550)	External Antenna	2.00
NR Band n78 (3700-3800)	External Antenna	2.00

IC

Band	Antenna Type	Antenna Gain(dBi)
LTE Band 2	External Antenna	1.80
LTE Band 4	External Antenna	1.20
LTE Band 5	External Antenna	0.30
LTE Band 7	External Antenna	1.40
LTE Band 12	External Antenna	-0.50
LTE Band 13	External Antenna	-0.70
LTE Band 14	External Antenna	-0.50
LTE Band 17	External Antenna	-0.50
LTE Band 25	External Antenna	1.80
LTE Band 26 (824~849)	External Antenna	0.30
LTE Band 30	External Antenna	-5.70
LTE Band 38	External Antenna	1.4
LTE Band 41	External Antenna	1.4
LTE Band 42	External Antenna	-2.01
LTE Band 43	External Antenna	-7.10
LTE Band 48	External Antenna	-6.12
LTE Band 66	External Antenna	1.50
LTE Band 71	External Antenna	-0.90
NR Band n2	External Antenna	1.80
NR Band n5	External Antenna	0.30
NR Band n7	External Antenna	1.40
NR Band n12	External Antenna	-0.50
NR Band n13	External Antenna	-0.70
NR Band n14	External Antenna	-0.50
NR Band n25	External Antenna	1.80
NR Band n26 (824~849)	External Antenna	0.30
NR Band n30	External Antenna	-5.70
NR Band n38	External Antenna	1.40
NR Band n41	External Antenna	1.40
NR Band n48	External Antenna	-6.12

NR Band n66	External Antenna	1.50
NR Band n71	External Antenna	-0.90
NR Band n77 (3450-3900)	External Antenna	-0.64
NR Band n77 (3900-3980)	External Antenna	-0.64
NR Band n78 (3450-3800)	External Antenna	-0.64

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, and part 96 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules)

listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

IC: 10224A-024RG255CGL

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 10224A-024RG255CGL”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 10224A-024RG255CGL ".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.