SC200R Series

Hardware Design

Multi-mode Smart LTE Module

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Our aim is to provide customers with timely and comprehensive service. For any assistance, please contact our company headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local office. For more information, please visit:
http://www.quectel.com/support/sales.htm

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About the Document

History

Revision	Date	Author	Description
1.0	2019-12-30	Arsene TONG	Initial

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1 Introduction

This document defines the SC200R module and its air interfaces and hardware interfaces which are connected with customers' application.

This document can help customers quickly understand module interface specifications, electrical and mechanical details as well as other related information of SC200R module. Associated with application note and user guide, customers can use SC200R module to design and set up mobile applications easily.

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

The final end product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID:XMR202005SC200RNA ; IC :10224A-20SC200RNA" or Contains FCC ID:XMR202005SC200RNA ; IC :10224A-20SC200RNA".

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution:

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) This device must accept any interference received, including interference that may cause undesired operation.

FCC Radiation Exposure Statement:

This equipment complies with FCC/IC radiation exposure limits set forth for an uncontrolled environment. This transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

The module must be installed in the host device.

This End equipment should be installed and operated with a minimum distance of 20cm centimeters between the radiator and your body.

Industry Canada Statement

This device complies with Industry Canada RSS-210 and CAN ICES-3(B)/NMB-3(B).

Operation is subject to the following two conditions:

(1) this device may not cause interference, and

(2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio RSS-210. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Cet émetteur ne doit pas être Co-placé ou ne fonctionnant en même temps qu'aucune autre antenne ou émetteur.

(i) the device for operation in the band 5150-5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;

(ii) the maximum antenna gain permitted for devices in the bands 5250-5350 MHz and

5470-5725 MHz shall comply with the e.i.r.p. limit; and
(iii) the maximum antenna gain permitted for devices in the band 5725-5825 MHz shall comply with the e.i.r.p. limits specified for point-to-point and non point-to-point operation as appropriate.

Le guide d'utilisation des dispositifs pour réseaux locaux doit inclure des instructions précises sur les restrictions susmentionnées, notamment :
(i) les dispositifs fonctionnant dans la bande 5 150-5 250 MHz sont réservés uniquement pour une utilisation à l'intérieur afin de réduire les risques de brouillage préjudiciable aux systèmes de satellites mobiles utilisant les mêmes canaux;
(ii) le gain maximal d'antenne permis pour les dispositifs utilisant les bandes 5 250-5 350 MHz et 5 470-5 725 MHz doit se conformer à la limite de p.i.r.e.;
(iii) le gain maximal d'antenne permis (pour les dispositifs utilisant la bande 5 725-5 825 MHz) doit se conformer à la limite de p.i.r les limites spécifiées pour un fonctionnement point à point et non point à point, selon le cas CAN ICES-3(B)/ NMB-3(B)

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating SC200R module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

SC200R is a series of 4G Smart LTE module based on Qualcomm platform and Android operating system, and provides industrial grade performance. Its general features are listed below:

- Support worldwide LTE-FDD, LTE-TDD, DC-HSPA+, HSPA+, HSDPA+, HSUPA, WCDMA, EVDO/CDMA, EDGE and GPRS coverage.
- Support short-range wireless communication via Wi-Fi 802.11a/b/g/n and BT4.2 LE.
- Integrate GPS/GLONASS/BeiDou satellite positioning systems.
- Support multiple audio and video codecs.
- Built-in high performance Adreno™ 308 graphics processing unit.
- Provide multiple audio and video input/output interfaces as well as abundant GPIO interfaces.

SC200R module is available in four variants: SC200R-CE, SC200R-EM*, SC200R-NA*, SC200R-JP*, SC200R-WF*.

2.2. Evaluation Board

To help customers design and test applications with Quectel SC200R modules, Quectel supplies an evaluation kit, which includes an evaluation board, a USB to RS232 converter cable, a USB T data cable, a power adapter, an earphone and antennas. For details, please refer the ***document [1]***

3 Application Interfaces

3.1. General Description

SC200R is an SMD type module with 146 LCC pins and 128 LGA pins. The following chapters provide the detailed description of pins/interfaces listed below.

- Power supply
- VRTC interface
- USB interface
- UART interfaces
- (U)SIM interfaces
- SD card interface
- GPIO interfaces
- I2C interface
- SPI interfaces
- ADC interfaces
- Motor drive interface
- LCM interface
- Touch panel interface
- Camera interfaces
- Sensor interfaces
- Audio interfaces
- Emergency download interface

3.2. Pin Assignment

The following figure shows the pin assignment of SC200R module.

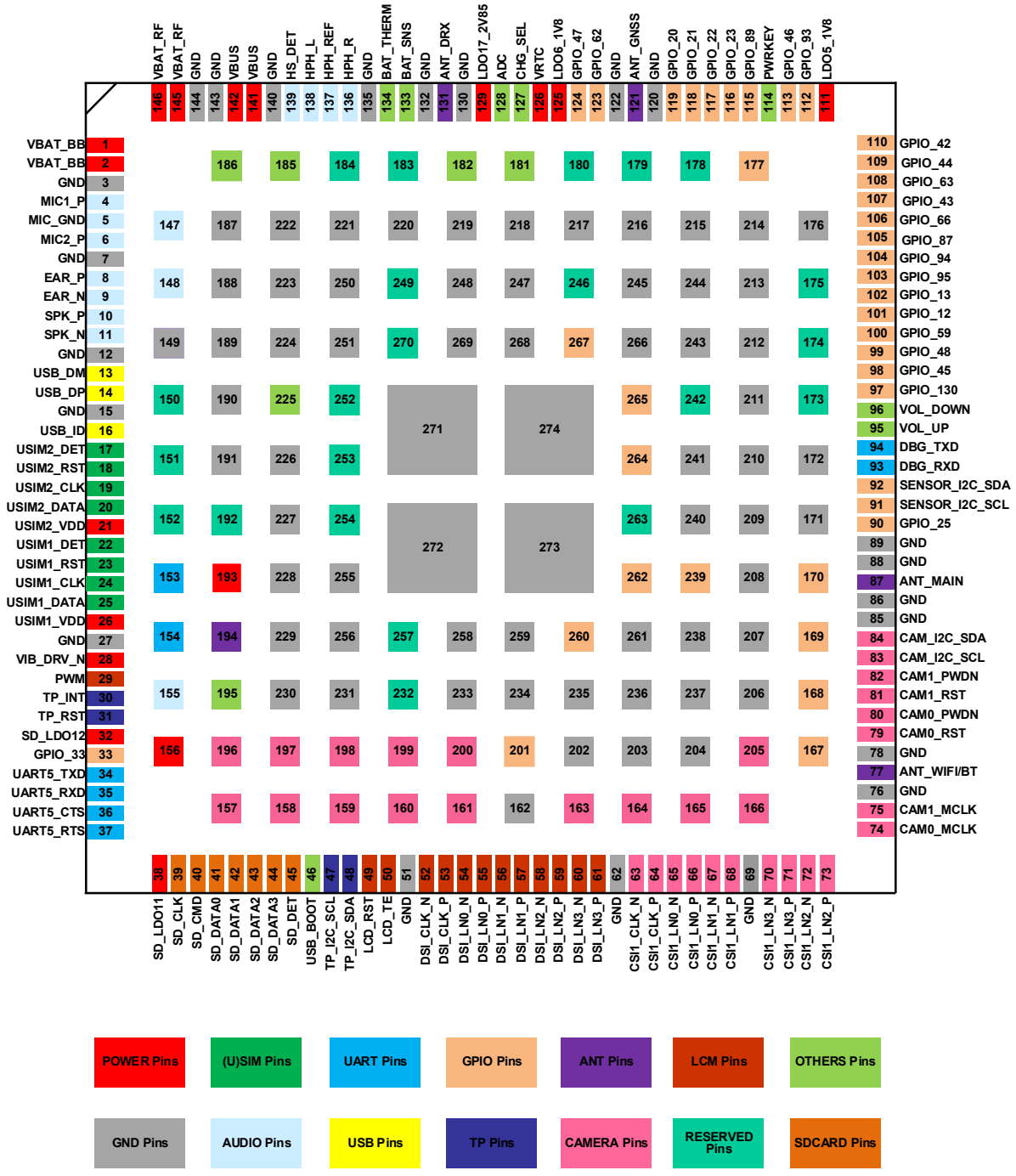


Figure 1: Pin Assignment (Top View)

3.3. Pin Description

The following tables show the SC200R's pin definition.

Table 1: I/O Parameters Definition

Type	Description
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
IO	Bidirectional
OD	Open drain
PI	Power input
PO	Power output

The following tables show the SC200R's pin definition and electrical characteristics.

Table 2: Pin Description

Power supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	1, 2	PI	Power supply for module's baseband part	Vmax=4.2V Vmin=3.55V Vnorm=3.8V	It must be provided with sufficient current up to 3.0A. It is suggested to use a TVS for external circuit.
VBAT_RF	145, 146	PI	Power supply for module's RF part.	Vmax=4.2V Vmin=3.55V Vnorm=3.8V	
VRTC	126	PI/PO	Power supply for internal RTC circuit.	VOmax=3.2V VI=2.0V~3.25V	If it is not used, keep this pin open.
LDO5_1V8	111	PO	1.8V output power supply	Vnorm=1.8V IOmax=20mA	Power supply for external GPIO's pull up circuits and

					level shift circuit.
LDO6_1V8	125	PO	1.8V output power supply	Vnorm=1.8V $I_O$max=150mA	Power supply for sensors, cameras, and I2C pull-up circuits. If it is used, it is recommended to connect an external 2.2μF~4.7μF capacitor to this pin in series. If it is not used, keep it open.
LDO10_2V85	156	PO	2.85V output power supply	Vnorm=2.85V IOmax=150mA	Reserved Power supply. If it is used, a 1μF~2.2μF bypass capacitor is recommended. If it is not used, keep it open.
LDO17_2V85	129	PO	2.85V output power supply	Vnorm=2.85V $I_O$max=450mA	Power supply for LCD, CTP, sensors and camera AVDD. If it is used, it is recommended to connect an external 2.2μF~4.7μF capacitor to this pin in series. If it is not used, keep this pin open.
LDO16_2V8	193	PO	2.8V output power supply	Vnorm=2.8V $I_O$max=55mA	Reserved Power supply. If it is used, a 1μF~2.2μF bypass capacitor is recommended. If it is not used, keep this pin open.
GND	3, 7, 12, 15, 27, 51, 62,		GND		

	69, 76, 78, 85, 86, 88, 89, 120, 122, 130, 132, 135, 140, 143, 144, 149, 162, 171,172, 176, 187~191, 202~204, 206~224, 226~231, 233~238, 240,241, 243~245, 247,248, 250,251, 255,256, 258,259, 261,266, 268,269, 271~274				
Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC1_P	4	AI	Microphone input for channel 1 (+)		
MIC_GND	5	AI	Microphone reference ground		If it is not used, connect to the ground.
MIC2_P	6	AI	icrophone input for headset (+)		
EAR_P	8	AO	Earpiece output (+)		
EAR_N	9	AO	Earpiece output (-)		
SPK_P	10	AO	Speaker output (+)		
SPK_N	11	AO	Speaker output (-)		

HPH_R	136	AO	Headphone right channel output		
HPH_REF	137	AI	Headphone reference ground		
HPH_L	138	AO	Headphone left channel output		
HS_DET	139	AI	Headset insertion detection		High level by default.
MIC_BIAS1	147	AO	Microphone bias1 voltage	V_O =1.6V~2.85V	
MIC3_P	148	AI	Microphone input for secondary microphone (+)		
MIC_BIAS2	155	AO	Microphone bias2 voltage	V_O =1.6V~2.85V	
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	141, 142	PI	USB power supply	Vmax=6.2V Vmin=4.35V Vnorm=5.0V	Used for USB 5V power input and USB detection.
USB_DM	13	AI/AO	USB differential data bus (-)	USB 2.0 standard compliant.	90Ω differential impedance.
USB_DP	14	AI/AO	USB differential data bus (+)		
USB_ID	16	DI	USB ID detection of the input		High level by default.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM2_DET	17	DI	(U)SIM2 card hot-plug detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active Low. Require external pull-up to 1.8V. If it is not used, keep it open. This function is disabled by default via software. It cannot be multiplexed into a Generic GPIO.

USIM2_RST	18	DO	(U)SIM2 card reset signal	V_{OL}max=0.4V V_{OH}min= 0.8 x USIM2_VDD	They cannot be multiplexed into a Generic GPIOs.
USIM2_CLK	19	DO	(U)SIM2 card clock signal	V_{OL}max=0.4V V_{OH}min= 0.8 × USIM2_VDD	
USIM2_DATA	20	IO	(U)SIM2 card data signal	V_{IL}max= 0.2 × USIM2_VDD V_{IH}min= 0.7×USIM2_VDD V_{OL}max=0.4V V_{OH}min= 0.8 × USIM2_VDD	
USIM2_VDD	21	PO	(U)SIM2 card power supply	**For 1.8V (U)SIM:** Vmax=1.85V Vmin=1.75V **For 2.95V (U)SIM:** Vmax=3.1V Vmin=2.8V	Either 1.8V or 2.95V (U)SIM card is supported.
USIM1_DET	22	DI	(U)SIM1 card hot-plug detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active Low. Require external pull-up to 1.8V. If it is not used, keep it open. This function is disabled by default via software. It cannot be multiplexed into a generic GPIO.
USIM1_RST	23	DO	(U)SIM1 card reset signal	V_{OL}max=0.4V V_{OH}min= 0.8 × USIM1_VDD	Cannot be multiplexed into generic GPIOs.
USIM1_CLK	24	DO	(U)SIM1 card clock signal	V_{OL}max=0.4V V_{OH}min= 0.8 × USIM1_VDD	
USIM1_DATA	25	IO	(U)SIM1 card data signal	V_{IL}max= 0.2 × USIM1_VDD V_{IH}min= 0.7 × USIM1_VDD V_{OL}max=0.4V V_{OH}min= 0.8 × USIM1_VDD	

USIM1_VDD	26	PO	(U)SIM1 card power supply	**For 1.8V (U)SIM:** Vmax=1.85V Vmin=1.75V **For 2.95V (U)SIM:** Vmax=3.1V Vmin=2.8V	Either 1.8V or 2.95V (U)SIM card is supported.
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART5_TXD	34	DO	UART5 transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If it is not used, keep these pins open.
UART5_RXD	35	DI	UART5 receive data	V_{IL}max=0.63V V_{IH}min=1.17V	
UART5_CTS	36	DI	UART5 clear to send	V_{IL}max=0.63V V_{IH}min=1.17V	
UART5_RTS	37	DO	UART5 request to send	V_{OL}max=0.45V V_{OH}min=1.35V	
DBG_RXD	93	DI	UART2 receive data. Debug port by default.	V_{IL}max=0.63V V_{IH}min=1.17V	
DBG_TXD	94	DO	UART2 transmit data. Debug port by default.	V_{OL}max=0.45V V_{OH}min=1.35V	
UART1_RXD	153	DI	UART1 receive data	V_{IL}max=0.63V V_{IH}min=1.17V	
UART1_TXD	154	DO	UART1 transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_LDO11	38	PO	2.95V output power supply	Vnorm=2.95V $I_O$max=800mA	Power supply for SD.
SD_LDO12	32	PO	1.8V/2.95V output power supply	Vnorm=1.8V/2.95V $I_O$max=50mA	Power supply for SD's pull up circuits.
SD_CLK	39	DO	High speed digital clock signal of SD card	**1.8V SD card:** V_{OL}max=0.45V V_{OH}min=1.4V **2.95V SD card:** V_{OL}max=0.37V	50Ω impedance

				V_{OH}min=2.2V	
SD_CMD	40	IO	Command signal of SD card	**1.8V SD card:** V_{IL}max=0.58V V_{IH}min=1.27V V_{OL}max=0.45V V_{OH}min=1.4V **2.95V SD card:** V_{IL}max=0.73V V_{IH}min=1.84V V_{OL}max=0.37V V_{OH}min=2.2V	
SD_DATA0	41	IO	High speed bidirectional digital signal lines of SD card	**1.8V SD card:** V_{IL}max=0.58V V_{IH}min=1.27V V_{OL}max=0.45V V_{OH}min=1.4V **2.95V SD card:** V_{IL}max=0.73V V_{IH}min=1.84V V_{OL}max=0.37V V_{OH}min=2.2V	
SD_DATA1	42	IO			
SD_DATA2	43	IO			
SD_DATA3	44	IO			
SD_DET	45	DI	SD card insertion detection	V_{IL}max=0.63V V_{IH}min=1.17V	SD card insert detection signal. Active low.
Touch Panel (TP) Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_INT	30	DI	Interrupt signal of TP	V_{IL}max=0.63V V_{IH}min=1.17V	1.8V power domain
TP_RST	31	DO	Reset signal of TP	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain Active low
TP_I2C_SCL	47	OD	I2C clock signal of TP		1.8V power domain
TP_I2C_SDA	48	OD	I2C data signal of TP		
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

PWM	29	DO	Adjust the backlight brightness. PWM control signal.	V_{OL}max=0.45V V_{OH}max=VBAT_BB	
LCD_RST	49	DO	LCD reset signal	VOLmax=0.45V VOHmin=1.35V	1.8V power domain
LCD_TE	50	DI	LCD tearing effect signal	VILmax=0.63V VIHmin=1.17V	1.8V power domain
DSI_ CLK_N	52	AO	MIPI DSI clock signal (-)		
DSI_ CLK_P	53	AO	MIPI DSI clock signal (+)		
DSI_LN0_N	54	AO	MIPI DSI data 0 signal (-)		
DSI_LN0_P	55	AO	MIPI DSI data 0 signal (+)		
DSI_LN1_N	56	AO	MIPI DSI data 1 signal (-)		
DSI_LN1_P	57	AO	MIPI DSI data 1 signal (+)		
DSI_LN2_N	58	AO	MIPI DSI data 2 signal (-)		
DSI_LN2_P	59	AO	MIPI DSI data 2 signal (+)		
DSI_LN3_N	60	AO	MIPI DSI data 3 signal (-)		
DSI_LN3_P	61	AO	MIPI DSI data 3 signal (+)		
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI1_CLK_N	63	AI	CAMERA MIPI clock signal (-)		
CSI1_CLK_P	64	AI	CAMERA MIPI clock signal (+)		

CSI1_LN0_N	65	AI	CAMERA MIPI data 0 signal (-)
CSI1_LN0_P	66	AI	CAMERA MIPI data 0 signal (+)
CSI1_LN1_N	67	AI	CAMERA MIPI data 1 signal (-)
CSI1_LN1_P	68	AI	CAMERA MIPI data 1 signal (+)
CSI1_LN3_N	70	AI	CAMERA MIPI data 3 signal (-)
CSI1_LN3_P	71	AI	CAMERA MIPI data 3 signal (+)
CSI1_LN2_N	72	AI	CAMERA MIPI data 2 signal (-)
CSI1_LN2_P	73	AI	CAMERA MIPI data 2 signal (+)
CSI0_CLK_N	157	AI	CAMERA MIPI clock signal (-)
CSI0_CLK_P	196	AI	CAMERA MIPI clock signal (+)
CSI0_LN0_N	158	AI	CAMERA MIPI data 0 signal (-)
CSI0_LN0_P	197	AI	CAMERA MIPI data 0 signal (+)
CSI0_LN1_N	159	AI	CAMERA MIPI data 1 signal (-)
CSI0_LN1_P	198	AI	CAMERA MIPI data 1 signal (+)
CSI0_LN2_N	160	AI	CAMERA MIPI data 2 signal (-)
CSI0_LN2_P	199	AI	CAMERA MIPI data 2 signal (+)

CSI0_LN3_N	161	AI	CAMERA MIPI data 3 signal (-)		
CSI0_LN3_P	200	AI	CAMERA MIPI data 3 signal (+)		
CAM0_MCLK	74	DO	Clock signal of camera	VOLmax=0.45V VOHmin=1.35V	1.8V power domain
CAM1_MCLK	75	DO	Clock signal of camera	VOLmax=0.45V VOHmin=1.35V	1.8V power domain
CAM0_RST	79	DO	Reset signal of camera	VOLmax=0.45V VOHmin=1.35V	1.8V power domain
CAM0_PWDN	80	DO	Power down signal of camera	VOLmax=0.45V VOHmin=1.35V	1.8V power domain
CAM1_RST	81	DO	Reset signal of camera	VOLmax=0.45V VOHmin=1.35V	1.8V power domain
CAM1_PWDN	82	DO	Power down signal of camera	VOLmax=0.45V VOHmin=1.35V	1.8V power domain
CAM_I2C_SCL	83	OD	I2C clock signal of camera		1.8V power domain
CAM_I2C_SDA	84	OD	I2C data signal of camera		1.8V power domain
CAM2_MCLK	165	DO	Clock signal of camera	VOLmax=0.45V VOHmin=1.35V	1.8V power domain
CAM2_RST	164	DO	Reset signal of camera	VOLmax=0.45V VOHmin=1.35V	1.8V power domain
CAM2_PWDN	163	DO	Power down signal of camera	VOLmax=0.45V VOHmin=1.35V	1.8V power domain
DCAM_I2C_SCL	166	OD	I2C clock signal of camera		1.8V power domain
DCAM_I2C_SDA	205	OD	I2C data signal of camera		1.8V power domain
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	114	DI	Turn on/off the module	V_{IL}max=0.63V V_{IH}min=1.17V	Pull-up to 1.8V internally. Active low.

RESET_N	225	DI	Reset the module		Off by default and can be enabled via software configuration.
VOL_UP	95	DI	Volume up	VILmax=0.63V VIHmin=1.17V	If it is not used, keep it open. Cannot be pull up. 1.8V power domain
VOL_ DOWN	96	DI	Volume down	VILmax=0.63V VIHmin=1.17V	If it is not used, keep it open. 1.8V power domain
SENSOR_I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SENSOR_I2C_SCL	91	OD	I2C clock signal for external sensor		1.8V power domain
SENSOR_I2C_SDA	92	OD	I2C data signal for external sensor		1.8V power domain
Charge Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BAT_SNS	133	AI	Battery voltage detection		Maximum input voltage is 4.2V.
BAT_THERM	134	AI	Battery temperature detection		Internally pulled up. Externally connected to GND via a NTC, If it is not used, connect a 47KΩ resistor.
BAT_ID	185	AI	Battery type detection	V_{OL}min=0.1V V_{OH}max=1.7V	Internal 100K pull down. If it is not used, keep it open.
CHG_SEL	127	DI	Used for charger selection		Keep it open, when charging with PM215. Connect this pin to GND when an external charging chip is used.

ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC	128	AI	Generic ADC		The maximum input voltage is 1.7V.
RF Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	87	AI/AO	Main antenna		50Ω impedance
ANT_DRX	131	AI	Diversity antenna		
ANT_GNSS	121	AI	GNSS antenna		
ANT_WIFI/BT	77	AI/AO	Wi-Fi/BT antenna		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_33	33	IO	GPIO	VILmax=0.63V VIHmin=1.17V VOLmax=0.45V VOHmin=1.4V	
GPIO_25	90	IO	GPIO		
GPIO_130	97	IO	GPIO		
GPIO_45	98	IO	GPIO		
GPIO_48	99	IO	GPIO		
GPIO_59	100	IO	GPIO		
GPIO_12	101	IO	GPIO		
GPIO_13	102	IO	GPIO		
GPIO_95	103	IO	GPIO		
GPIO_94	104	IO	GPIO		
GPIO_87	105	IO	GPIO		
GPIO_66	106	IO	GPIO		
GPIO_43	107	IO	GPIO		

GPIO_63	108	IO	GPIO		
GPIO_44	109	IO	GPIO		
GPIO_42	110	IO	GPIO		
GPIO_93	112	IO	GPIO		
GPIO_46	113	IO	GPIO		
GPIO_89	115	IO	GPIO		
GPIO_23	116	IO	GPIO		
GPIO_22	117	IO	GPIO		
GPIO_21	118	IO	GPIO		
GPIO_20	119	IO	GPIO		
GPIO_62	123	IO	GPIO		
GPIO_47	124	IO	GPIO		
GPIO_6	167	IO	GPIO		
GPIO_7	168	IO	GPIO		
GPIO_127	169	IO	GPIO		
GPIO_34	170	IO	GPIO		
GPIO_90	177	IO	GPIO		
GPIO_39	201	IO	GPIO		
GPIO_86	239	IO	GPIO		
GPIO_88	264	IO	GPIO		This GPIO pin cannot be pulled up when the module is turned on.
GPIO_85	265	IO	GPIO		
GPIO_61	267	IO	GPIO		
GNSS_LNA ENABLE Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

GNSS_LNA_EN	194	IO	External GNSS_LNA enable signal.		It cannot be multiplexed into a Generic GPIO.
GRFC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RFFE3_CLK	260	IO	GRFC can only be used for RF Tuner control.		It cannot be multiplexed into a Generic GPIO.
RFFE3_DATA	262	IO	GRFC can only be used for RF Tuner control.		
USB_BOOT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	46	DI	Force the module to enter emergency download mode		Pull up USB_BOOT to LDO5_1V8 will force the module enter emergency download mode.
Motor Drive Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VIB_DRV_N	28	PO	Motor drive	VO=1.2V~3.1V $I_O$max=175mA	Connected to the negative terminal of the motor.
Indication Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CHG_LED	195	AO	Charging indicator LED	$I_O$max=5mA	
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NFC_CLK	181	DO	NFC clock signal		
NFC_CLK_REQ	182	DI	NFC clock request signal		

CBL_PWR_N	186	DI	Pull down the pin to realize the power-on automatic startup function		It cannot be turned off when the pin is pulled down. If it is not used, keep it open.
Reserved Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	150~152, 173~175, 178~180, 183,184, 192,232, 242,246, 249, 252~254, 257,263, 270		Reserved pins		Keep these pins open.

3.4. Power Supply

3.4.1. Power Supply Pins

SC200R provides two VBAT_RF pins and two VBAT_BB pins for connecting with an external power supply. The VBAT_RF pins are used for the RF part of the module and the VBAT_BB pins are used for the baseband part of the module.

3.4.2. Decrease Voltage Drop

The power supply range of the module is 3.55V~4.2V, and the recommended value is 3.8V. The power supply performance, such as load capacity, voltage ripple, etc. directly influences the module's performance and stability. Under ultimate conditions, the transient peak current of the module may surge up to 3A. If the supply voltage is not enough, there will be voltage drops, and if the voltage drops below 3.1V, the module will be turned off automatically. Therefore, please make sure the input voltage will never drop below 3.1V.

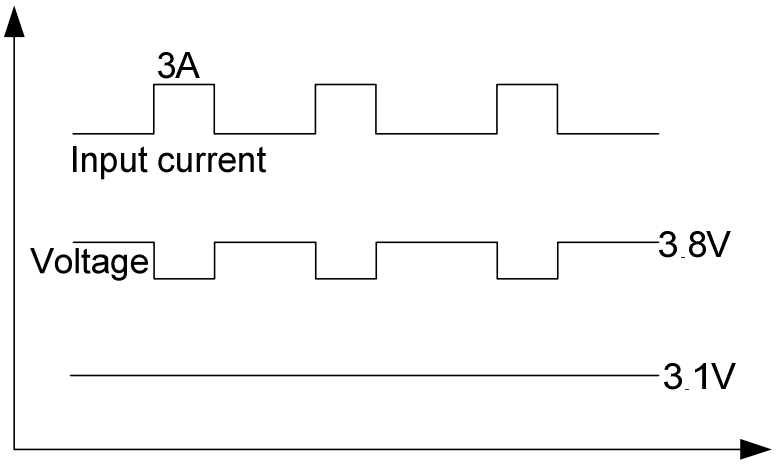


Figure 2: Voltage Drop Sample

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR (ESR=0.7Ω) should be used, and a multi-layer ceramic chip capacitor (MLCC) should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array and place these capacitors close to VBAT_BB/RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 3 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested to use a TVS and place it as close to the VBAT_BB/RF pins as possible to increase voltage surge withstand capability. The following figure shows the star structure of the power supply.

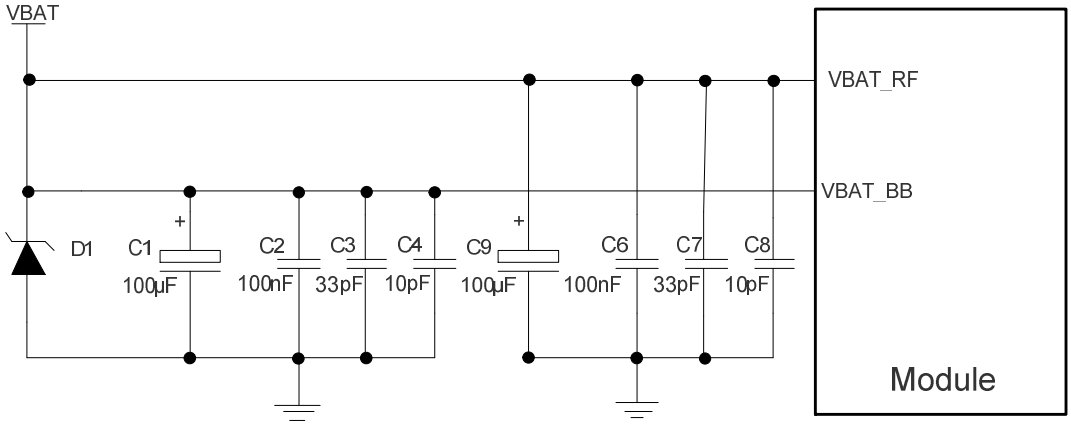


Figure 3: Star Structure of the Power Supply

3.4.3. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of SC200R should be able to provide sufficient current up to 3A at least. If the voltage drop between the input and output is not too high, it is suggested to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure shows a reference design for +5V input power source which adopts an LDO (MIC29502WU) from MICREL. The typical output voltage is 3.8V and the maximum load current is 5.0A.

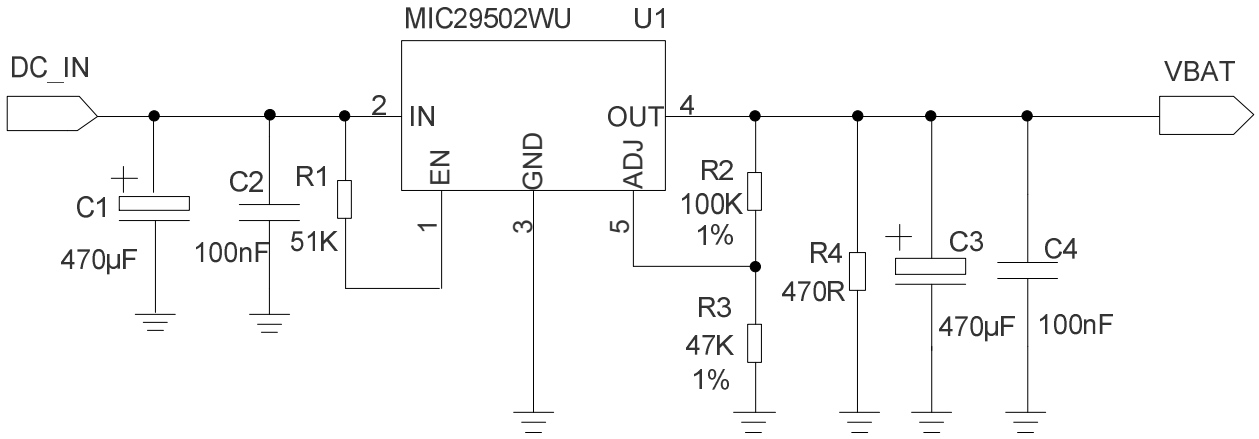


Figure 4: Reference Circuit of Power Supply

NOTES

1. It is suggested that customers should switch off the power supply for the module in an abnormal state, and then switch on the power to restart the module.
2. The module supports the battery charging function by default. If the above power supply design is adopted, please make sure the charging function is disabled by software or connect VBAT to Schottky diode in series to avoid the reverse current to the power supply chip.

3.5. Turn on and off Scenarios

3.5.1. Turn on Module Using the PWRKEY

The module can be turned on by driving the PWRKEY pin to a low level for at least 1.6s. PWRKEY pin is pulled to 1.8V internally. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

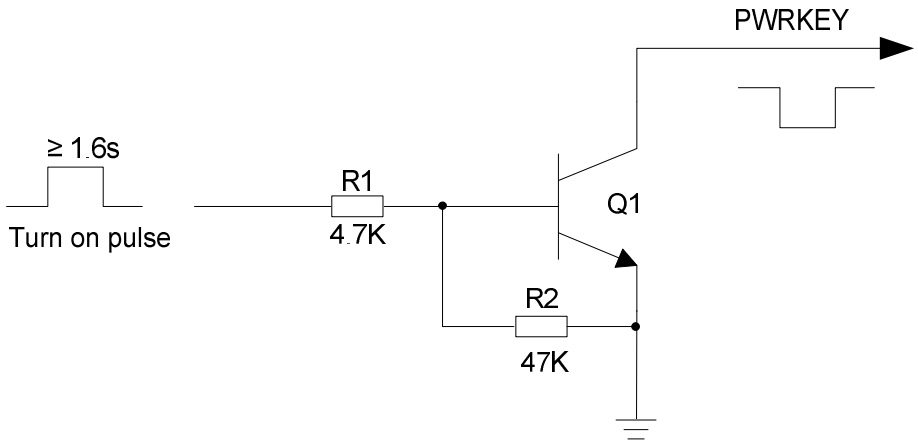


Figure 5: Turn on the Module Using Driving Circuit

The other way to control the PWRKEY is by using a button directly. A TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

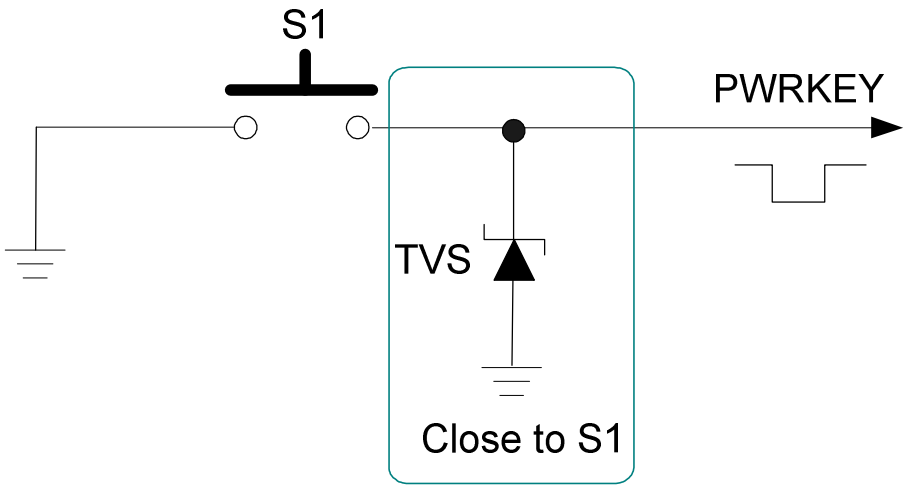


Figure 6: Turn on the Module Using Keystroke

The turning on the scenario is illustrated in the following figure.

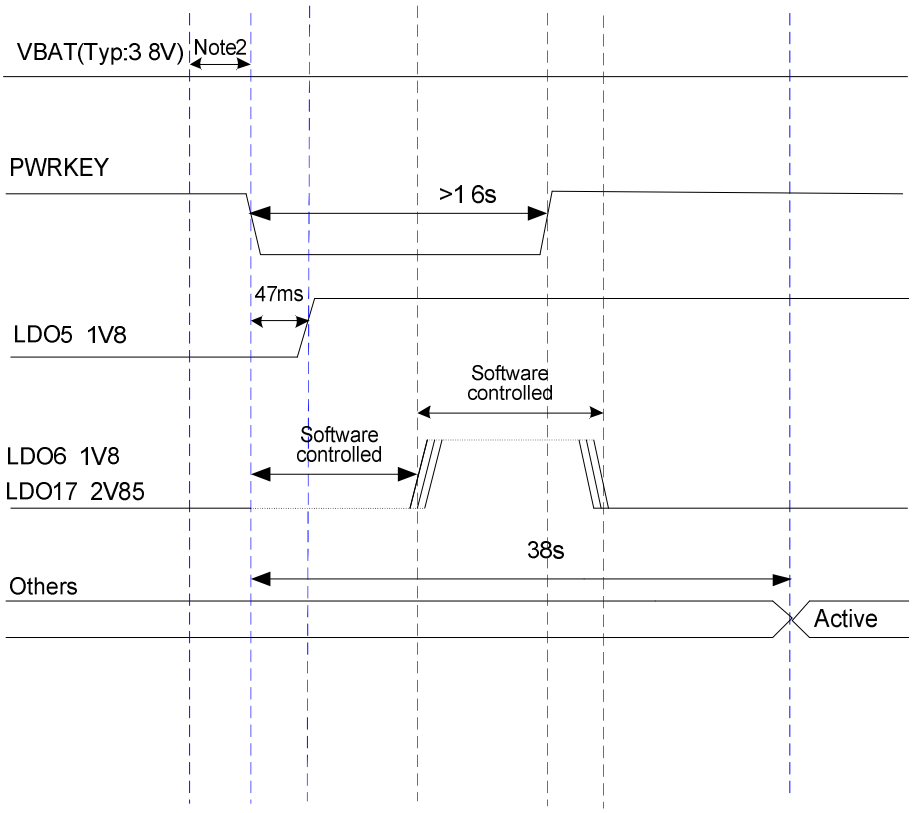


Figure 7: Timing of Turning on Module

NOTES

1. When the module is powered on for the first time, its timing of turning on may be different from that shown above.
2. Make sure that VBAT is stable before pulling down the PWRKEY pin. The recommended time between them is no less than 30ms. PWRKEY pin cannot be pulled down all the time.

3.5.2. Turn off Module

Set the PWRKEY pin low for at least 1s, and then choose to turn off the module when the prompt window comes up.

The other way to turn off the module is to drive PWRKEY to a low level for at least 8s. The module will execute the forced shutdown. The forced power-down scenario is illustrated in the following figure.

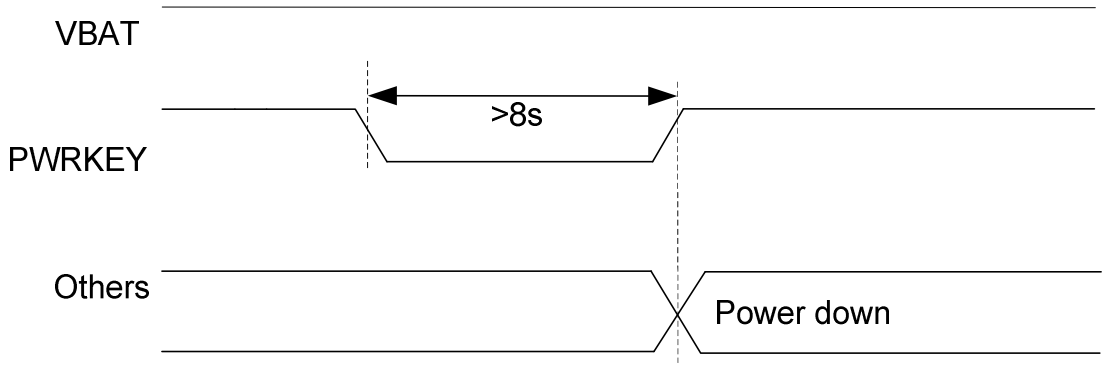


Figure 8: Timing of Turning off Module

3.6. VRTC Interface

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supply for the VBAT. The external power source can be a capacitor according to application demands. The following are some reference circuit designs when an external battery is utilized for powering RTC.

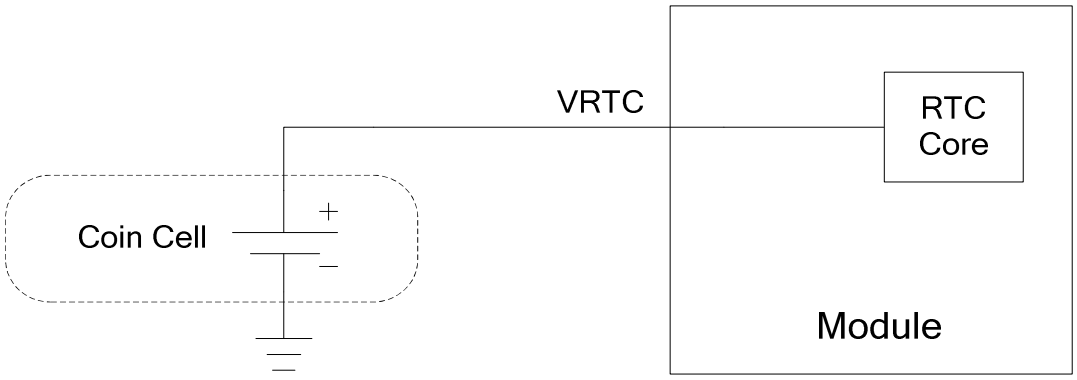


Figure 9: RTC Powered by Coin Cell

If RTC is ineffective, it can be synchronized through the network after the module is powered on. The recommended input voltage range for VRTC is 2.1V~3.25V and the recommended typical value is 3.0V.

3.7. Power Output

SC200R supports the output of regulated voltages for peripheral circuits. During application, it is recommended to use parallel capacitors (33pF and 10pF) in the circuit to suppress high-frequency noise.

Table 3: Power Description

Pin Name	Default Voltage (V)	Driving Current (mA)	IDLE
LDO5_1V8	1.8	20	KEEP
LDO6_1V8	1.8	150	/
LDO10_2V85	2.85	150	/
LDO17_2V85	2.85	450	/
LDO16_2V8	2.8	55	/
SD_LDO12	1.8/2.95	50	/
SD_LDO11	2.95	800	/
USIM1_VDD	1.8/2.95	55	
USIM2_VDD	1.8/2.95	55	

3.8. Battery Charge and Management

SC200R module can recharge batteries. The battery charger in the SC200R module supports trickle charging, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion batteries.

- **Trickle charging:** There are two steps in this mode. When the battery voltage is below 2.8V, a 90mA trickle charging current is applied to the battery. When the battery voltage is charged up and is between 2.8V and 3.2V, the charging current can be set to 450mA maximally.
- **Constant current mode (CC mode):** When the battery is increased to between 3.2V and 4.2V, the system will switch to CC mode. The maximum charging current is 1.44A when an adapter is used for

battery charging, and the maximum charging current is 450mA for USB charging.

- **Constant voltage mode (CV mode):** When the battery voltage reaches the final value 4.2V, the system will switch to CV mode and the charging current will decrease gradually. When the battery level reaches 100%, the charging is completed.

SC200R module supports battery temperature detection in the condition that the battery integrates a thermistor (47KΩ 1% NTC thermistor with a B-constant of 4050KΩ by default; SDNT1608X473F4050FTF of SUNLORD is recommended) and the thermistor is connected to VBAT_THERM pin. The default battery temperature range is -3.0 °C~48.5 °C. If the VBAT_THERM pin is not connected, there will be malfunctions such as battery charging failure, battery level display error, etc.

A reference design for the battery charging circuit is shown below.

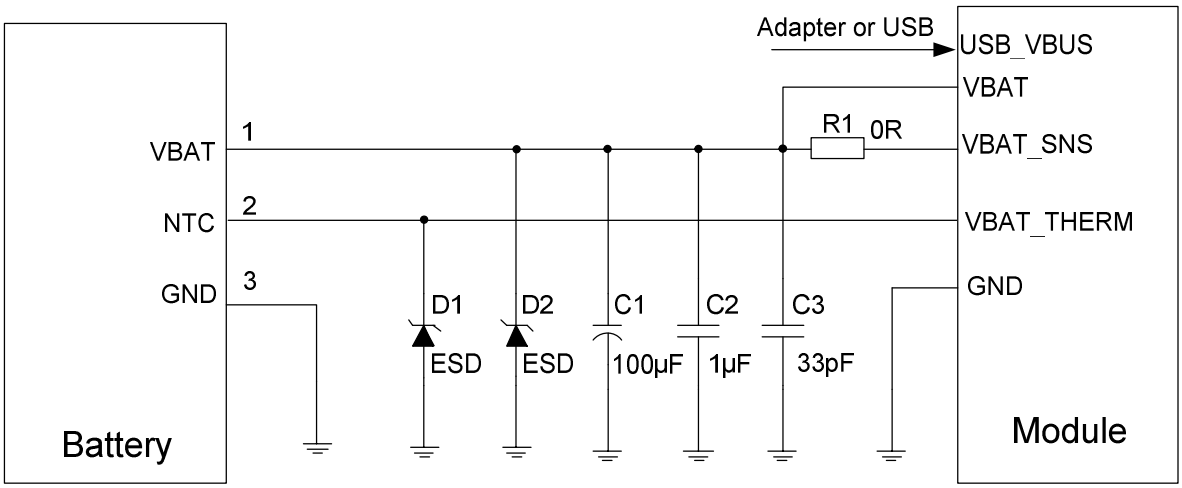


Figure 10: Reference Design for Battery Charging Circuit

Mobile devices such as mobile phones and handheld POS systems are powered by batteries. When different batteries are utilized, the charging and discharging curve has to be modified correspondingly so as to achieve the best effect.

If the thermistor is not available in the battery, or adapter is utilized for powering the module, then there is only a need for VBAT and GND connection. In this case, the system may mistakenly judge that the battery temperature is abnormal, which will cause battery charging failure. In order to avoid this, VBAT_THERM should be connected to GND via a 47KΩ resistor. If VBAT_THERM is unconnected, the system will be unable to detect the battery, making the battery cannot be charged.

VBAT_SNS pin must be connected. Otherwise, the module will have abnormalities in voltage detection, as well as an associated power on/off and battery charging and discharging issues.

3.9. USB Interface

SC200R contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high speed (480Mbps) and full-speed (12Mbps) modes. The USB interface is used for AT command communication, data transmission, software debugging and firmware upgrade.

The following table shows the pin definition of the USB interface.

Table 4: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	141, 142	PI	USB power supply	Vmax=6.2V Vmin=4.35V Vnorm=5.0V
USB_DM	13	AI/AO	USB 2.0 differential data bus (-)	USB 2.0 standard compliant. 90Ω differential impedance.
USB_DP	14	AI/AO	USB differential data bus (+)	
USB_ID	16	AI	USB ID detection of the input	

For USB 2.0 interface design, it is recommended that USB_ID should be directly connected to the USB_ID pin of an external USB port for USB ID detection. When a device inserts an external USB port, if it pulls down the USB_ID pin of the module, the module will enter the Host mode.

The following are two USB interface reference designs for customers to choose from.

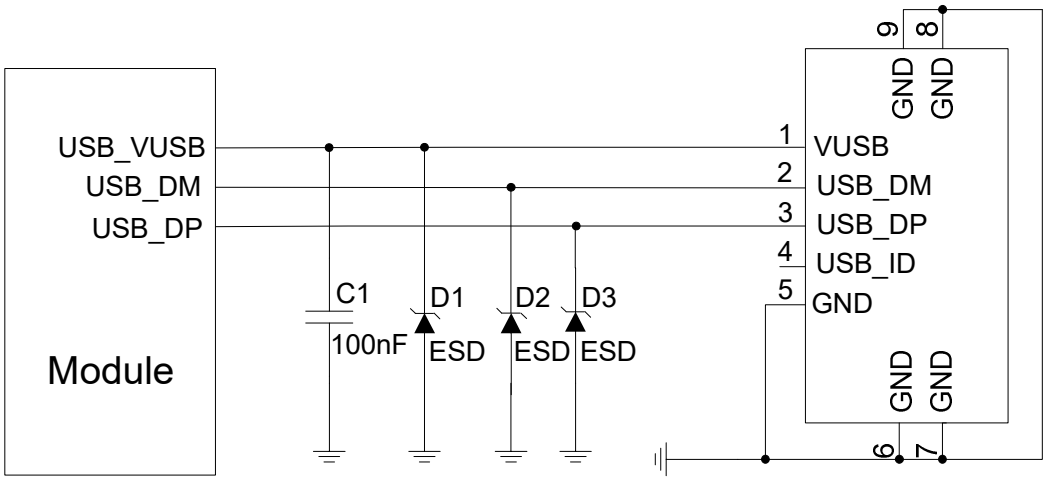


Figure 11: USB Interface Reference Design (OTG is not Supported)

SC200R supports OTG protocol. If the OTG function is needed, customers can refer to the above figure for the reference design. In this design, AW3605DNR is recommended. It is a high-efficiency DC-DC chip manufactured by AWINIC, and customers can choose according to their own demands.

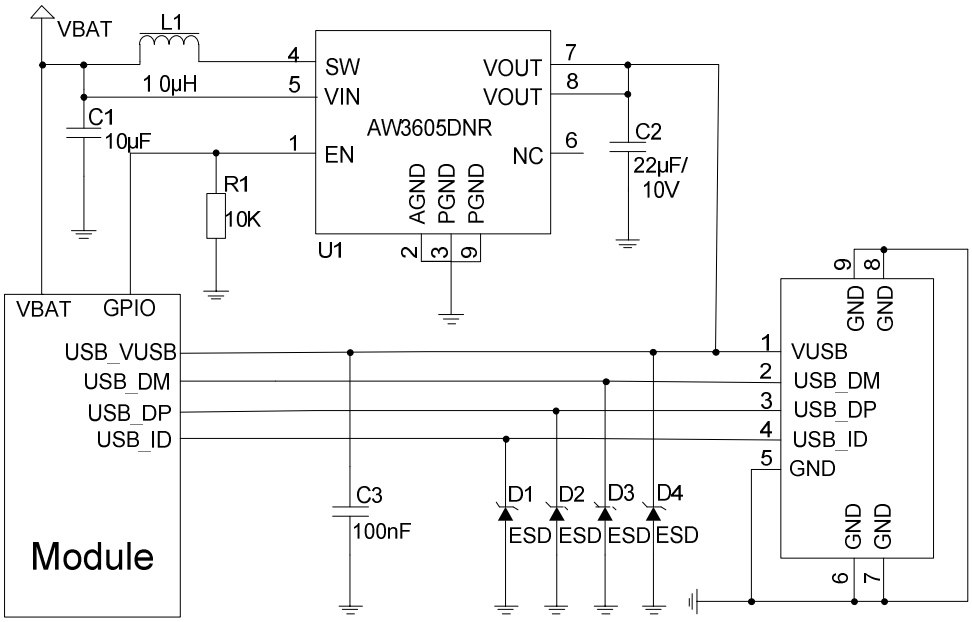


Figure 12: USB Interface Reference Design (OTG is Supported)

In order to ensure USB performance, please comply with the following principles while designing a USB interface.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- Keep the ESD protection devices as close as possible to the USB connector. Pay attention to the influence of junction capacitance of ESD protection devices on USB data lines. Typically, the capacitance value should be less than 2pF.
- Do not route signal traces under crystals, oscillators, magnetic devices, and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only the upper and lower layers but also the right and left sides.
- Make sure the trace length difference of USB 2.0 is not exceeding 0.7 mm.

Table 5: USB Trace Length Inside the Module

PIN	Signal	Length (mm)	Length Difference (DP-DM)
13	USB_DM	32.25	-0.10
14	USB_DP	32.15	

3.10. UART Interfaces

SC200R provides three UART interfaces:

- **UART5:** 4-wire UART interface, hardware flow control supported.
- **UART2（DEBUG）:** 2-wire UART interface; used for debugging by default.
- **UART1:** 2-wire UART interface

Table 6: Pin Definition of UART Interfaces

Pin Name	Pin No	I/O	Description	Comment
UART5_TXD	34	DO	UART5 transmit data	1.8V power domain. If unused, keep it open.
UART5_RXD	35	DI	UART5 receive data	
UART5_CTS	36	DI	UART5 clear to send	
UART5_RTS	37	DO	UART5 request to send	
DBG_RXD	93	DI	UART2 receive data. Debug port by default.	
DBG_TXD	94	DO	UART2 transmit data. Debug port by default.	
UART1_RXD	153	DI	UART1 receive data	
UART1_TXD	154	DO	UART1 transmit data	

UART5 is a 4-wire UART interface with 1.8V power domain. A level translator should be used if customers' application is equipped with a 3.3V UART interface. A level translator TXS0104PWR provided by Texas Instruments is recommended. The following figure shows the reference design.

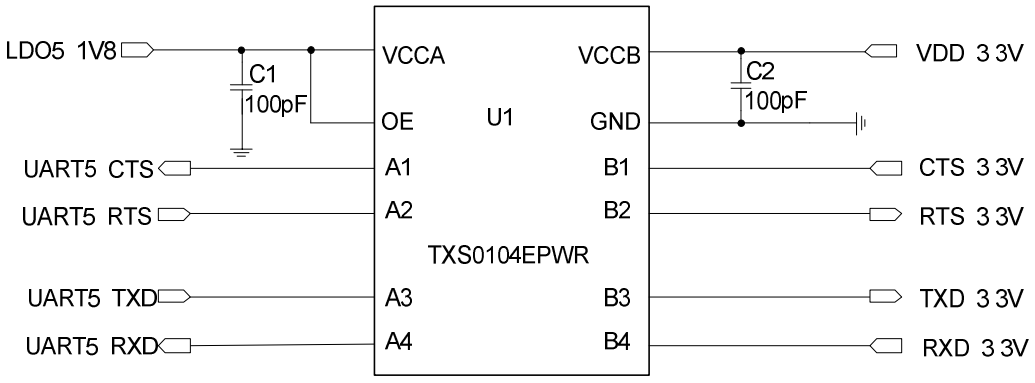


Figure 13: Reference Circuit with Level Translator Chip (for UART5)

The following figure is an example of a connection between SC200R and PC. A voltage level translator and an RS-232 level translator chip are also recommended to be added between the module and PC. The following figure shows the reference design.

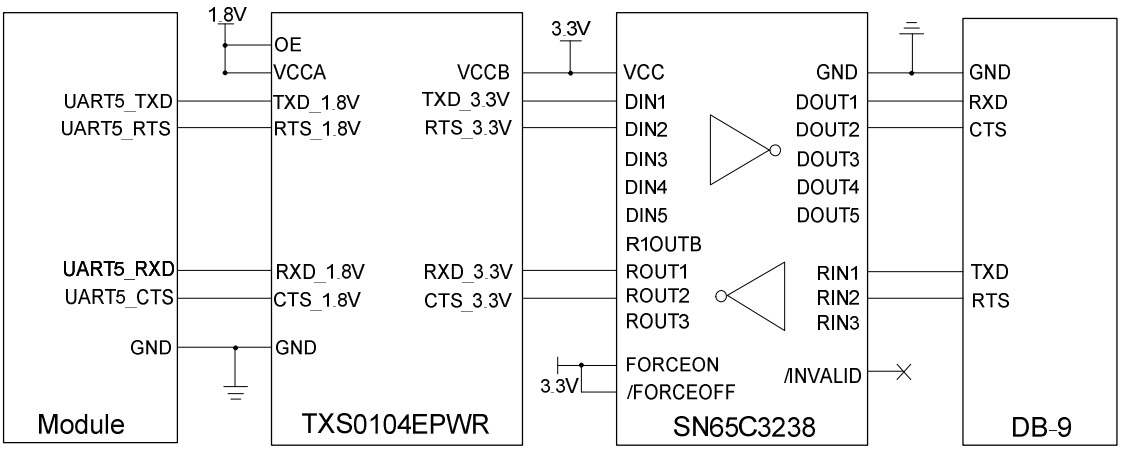


Figure 14: RS-232 Level Match Circuit (for UART5)

NOTE

UART2 and UART1 is similar to UART5. Please refer to UART5 reference circuit design for that of UART2 and UART1.

3.11. (U)SIM Interfaces

SC200R provides 2 (U)SIM interfaces that meet ETSI and IMT-2000 requirements. Dual SIM Card Dual Standby is supported by default. Both 1.8V and 2.95V (U)SIM cards are supported, and the (U)SIM card interfaces are powered by the internal power supply of the SC200R module.

Table 7: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No	I/O	Description	Comment
USIM2_DET	17	DI	(U)SIM2 card hot-plug detection	Active Low. An external pull-up resistor is required. If it is not used, keep it open. Enabled by default via software. It cannot be multiplexed into

				a generic GPIO.
USIM2_RST	18	DO	(U)SIM2 card reset signal	It cannot be multiplexed into a generic GPIO.
USIM2_CLK	19	DO	(U)SIM2 card clock signal	It cannot be multiplexed into a generic GPIO.
USIM2_DATA	20	IO	(U)SIM2 card data signal	It cannot be multiplexed into a generic GPIO.
USIM2_VDD	21	PO	(U)SIM2 card power supply	Either 1.8V or 2.95V (U)SIM card is supported.
USIM1_DET	22	DI	(U)SIM1 card hot-plug detection	Active low. An external pull-up resistor is required. If it is not used, keep it open. Enabled by default via software. It cannot be multiplexed into a generic GPIO.
USIM1_RST	23	DO	(U)SIM1 card reset signal	It cannot be used as a generic GPIO.
USIM1_CLK	24	DO	(U)SIM1 card clock signal	It cannot be multiplexed into a generic GPIO.
USIM1_DATA	25	IO	(U)SIM1 card data signal	It cannot be multiplexed into a generic GPIO.
USIM1_VDD	26	PO	(U)SIM1 card power supply	Either 1.8V or 2.95V (U)SIM card is supported.

SC200R supports (U)SIM card hot-plug via the USIM_DET pin. A reference circuit for (U)SIM interface with an 8-pin (U)SIM card connector is shown below.

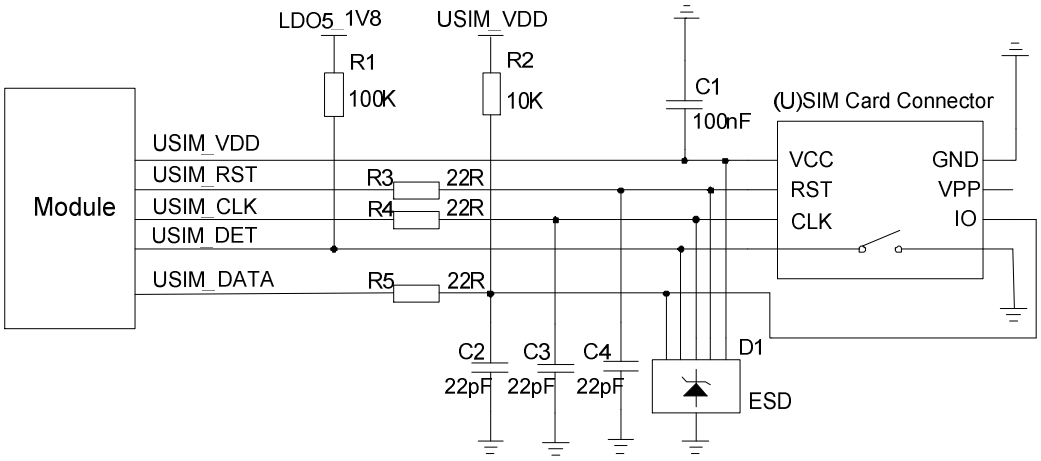


Figure 15: Reference Circuit for (U)SIM Interface with an 8-pin (U)SIM Card Connector

If there is no need to use USIM_DET, please keep this pin open. The following is a reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector.

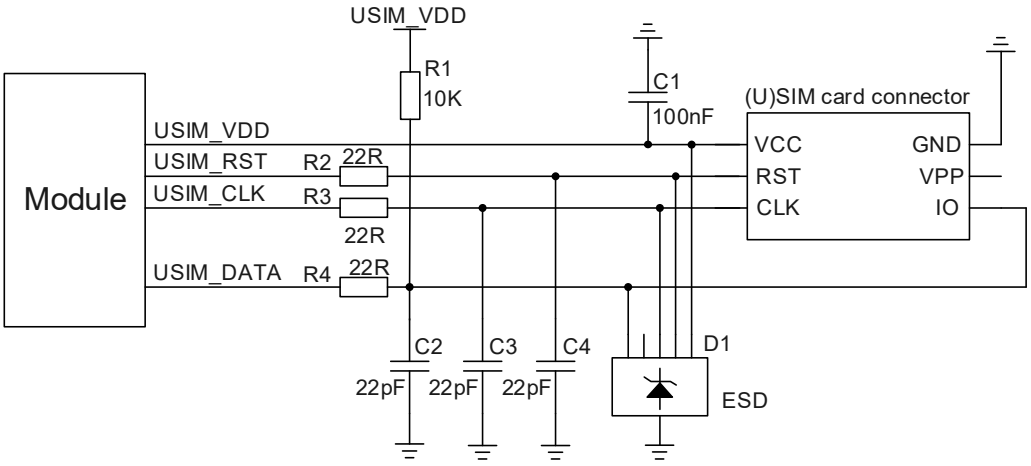


Figure 16: Reference Circuit for (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to ensure good performance and avoid damage of (U)SIM cards, please follow the criteria listed below during (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length of (U)SIM card signals as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- A filter capacitor shall be reserved for USIM_VDD, and its maximum capacitance should not exceed 1μF. The capacitor should be placed near to (U)SIM card.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground. USIM_RST also needs ground protection.
- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 50pF. The 22Ω resistors should be added in series between the module and (U)SIM card so as to suppress EMI spurious transmission and enhance ESD protection. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The 22pF capacitors should be added in parallel on USIM_DATA, USIM_VDD, USIM_CLK and USIM_RST signal lines so as to filter RF interference, and they should be placed as close to the (U)SIM card connector as possible.

3.12. SD Card Interface

SC200R SD Card Interface supports the SD 3.0 protocol. The pin definition of the SD card interface is shown below.

Table 8: Pin Definition of SD Card Interface

Pin Name	Pin No	I/O	Description	Comment
SD_CLK	39	DO	High-speed digital clock signal of SD card	50Ω characteristic impedance
SD_CMD	40	I/O	Command signal of SD card	
SD_DATA0	41	I/O	High-speed bidirectional digital signal lines of SD card	
SD_DATA1	42	I/O		
SD_DATA2	43	I/O		
SD_DATA3	44	I/O		
SD_DET	45	DI	SD card insertion detection	Active low
SD_LDO11	38	PO	2.95V output power supply	Power supply for SD card
SD_LDO12	32	PO	1.8V/2.95V output power supply	Pull up for SD card only

A reference circuit for the SD card interface is shown below.

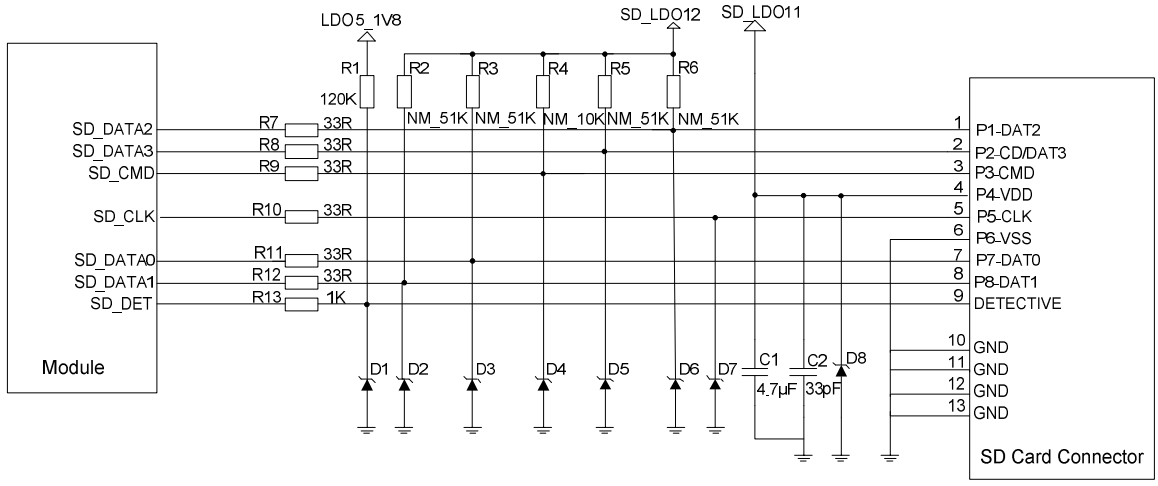


Figure 17: Reference Circuit for SD Card Interface

SD_VDD is a peripheral driver power supply for an SD card. The maximum drive current is 800mA. Because of the high drive current, it is recommended that the trace width is 0.8 mm or above. In order to ensure the stability of drive power, a 4.7μF and a 33pF capacitor should be added in parallel near the SD card connector.

CMD, CLK, DATA0, DATA1, DATA2, and DATA3 are all high-speed signal lines. In PCB design, please control the characteristic impedance of them to 50Ω, and do not cross them with other traces. It is recommended to route the trace on the inner layer of PCB and keep the same trace length for CLK, CMD, DATA0, DATA1, DATA2 and DATA3. CLK needs separate ground shielding.

Layout guidelines:

- Control impedance to 50Ω ±10% and ground shielding is required.
- The total trace length difference between CLK and other signal line traces like CMD and DATA should not exceed 1 mm.

Table 9: SD Card Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Comment
39	SD_CLK	21.50	
40	SD_CMD	21.40	
41	SD_DATA0	21.45	
42	SD_DATA1	21.60	
43	SD_DATA2	21.40	
44	SD_DATA3	21.35	

3.13. GPIO Interfaces

SC200R has abundant GPIO interfaces with a power domain of 1.8V. The pin definition is listed below.

Table 10: Pin Definition of GPIO Interfaces

Pin Name	Pin No	GPIO	Default state	Comment
GPIO_6	167	GPIO_6	B-PD:nppukp [1)]	
GPIO_7	168	GPIO_7	B-PD:nppukp	
GPIO_12	101	GPIO_12	B-PD:nppukp	Wakeup[2)]
GPIO_13	102	GPIO_13	B-PD:nppukp	Wakeup
GPIO_20	119	GPIO_20	B-PD:nppukp	
GPIO_21	118	GPIO_21	B-PD:nppukp	Wakeup
GPIO_22	117	GPIO_22	B-PD:nppukp	
GPIO_23	116	GPIO_23	B-PD:nppukp	
GPIO_25	90	GPIO_25	B-PD:nppukp	Wakeup
GPIO_33	33	GPIO_33	B-PD:nppukp	
GPIO_34	170	GPIO_34	B-PD:nppukp	Wakeup
GPIO_39	201	GPIO_39	B-PD:nppukp	
GPIO_42	110	GPIO_42	B-PD:nppukp	Wakeup
GPIO_43	107	GPIO_43	B-PD:nppukp	Wakeup
GPIO_44	109	GPIO_44	B-PD:nppukp	Wakeup
GPIO_45	98	GPIO_45	B-PD:nppukp	Wakeup
GPIO_46	113	GPIO_46	B-PD:nppukp	Wakeup
GPIO_47	124	GPIO_47	B-PD:nppukp	
GPIO_48	99	GPIO_48	B-PD:nppukp	Wakeup
GPIO_59	100	GPIO_59	B-PD:nppukp	Wakeup
GPIO_61	267	GPIO_61	B-PD:nppukp	Wakeup

GPIO_62	123	GPIO_62	B-PD:nppukp	Wakeup
GPIO_63	108	GPIO_63	B-PD:nppukp	Wakeup
GPIO_66	106	GPIO_66	B-PD:nppukp	
GPIO_85	265	GPIO_85	B-PD:nppukp	
GPIO_86	239	GPIO_86	B-PD:nppukp	Wakeup
GPIO_87	105	GPIO_87	B-PD:nppukp	
GPIO_88	264	GPIO_88	B-PD:nppukp	
GPIO_89	115	GPIO_89	B-PD:nppukp	
GPIO_90	177	GPIO_90	B-PD:nppukp	Wakeup
GPIO_93	112	GPIO_93	B-PD:nppukp	Wakeup
GPIO_94	104	GPIO_94	B-PD:nppukp	
GPIO_95	103	GPIO_95	B-PD:nppukp	
GPIO_127	169	GPIO_127	B-PD:nppukp	Wakeup
GPIO_130	97	GPIO_130	B-PD:nppukp	Wakeup
SD_DET	45	GPIO_67	B-PD:nppukp	Wakeup
TP_INT	30	GPIO_65	B-PD:nppukp	Wakeup
TP_RST	31	GPIO_64	B-PD:nppukp	
TP_I2C_SCL	47	GPIO_11	B-PD:nppukp	
TP_I2C_SDA	48	GPIO_10	B-PD:nppukp	
LCD_RST	49	GPIO_60	B-PD:nppukp	
LCD_TE	50	GPIO_24	B-PD:nppukp	
CAM0_MCLK	74	GPIO_26	B-PD:nppukp	
CAM1_MCLK	75	GPIO_28	B-PD:nppukp	Wakeup
CAM0_RST	79	GPIO_128	B-PD:nppukp	Wakeup
CAM0_PWDN	80	GPIO_126	B-PD:nppukp	Wakeup
CAM1_RST	81	GPIO_129	B-PD:nppukp	
CAM1_PWDN	82	GPIO_125	B-PD:nppukp	

CAM2_MCLK	165	GPIO_27	B-PD:nppukp	
CAM2_RST	164	GPIO_38	B-PD:nppukp	Wakeup
CAM2_PWDN	163	GPIO_41	B-PD:nppukp	Wakeup
VOL_UP	95	GPIO_91	B-PD:nppukp	Wakeup
VOL_DOWN	96	GPIO_50	B-PD:nppukp	Wakeup
UART5_TXD	34	GPIO_16	B-PD:nppukp	
UART5_RXD	35	GPIO_17	B-PD:nppukp	Wakeup
UART5_CTS	36	GPIO_18	B-PD:nppukp	
UART5_RTS	37	GPIO_19	B-PD:nppukp	
UART1_TXD	154	GPIO_0	B-PD:nppukp	
UART1_RXD	153	GPIO_1	B-PD:nppukp	Wakeup

NOTES

1. [1)] B: Bidirectional digital with CMOS input; PD:nppukp = default pulldown with programmable options following the colon (:).
2. [2)] Wakeup: interrupt pins that can wake up the system.
3. More details about GPIO configuration, please refer to ***document [2]***.

3.14. I2C Interfaces

SC200R module provides four I2C interfaces. As an open-drain signal, the I2C interfaces need a pull-up resistor on its external circuit, and the recommended power domain is 1.8V. The SENSOR_I2C interface only supports sensors of the aDSP architecture. CAM_I2C/CAM2_I2C bus is controlled by Linux Kernel code, they can mount devices related to the video output.

Table 11: Pin Definition of I2C Interfaces

Pin Name	Pin No	I/O	Description	Comment
TP_I2C_SCL	47	OD	I2C clock signal of touch panel	Used for touch panel
TP_I2C_SDA	48	OD	I2C data signal of touch panel	

CAM_I2C_SCL	83	OD	I2C clock signal of camera	Used for camera
CAM_I2C_SDA	84	OD	I2C data signal of camera	
DCAM_I2C_ SCL	166	OD	I2C clock signal of camera	Used for camera
DCAM_I2C_ SDA	205	OD	I2C data signal of camera	
SENSOR_I2C_SCL	91	OD	I2C clock signal for external sensor	Used for external sensor
SENSOR_I2C_SDA	92	OD	I2C data signal for external sensor	

3.15. SPI Interfaces

SC200R provides three SPI interfaces, which are multiplexed from UART and GPIO interfaces. These interfaces can only support the master mode. SPI interfaces can be used for fingerprint recognition.

Table 12: Pin Definition of SPI Interfaces

Pin Name	Pin No	I/O	Description	Comment
UART5_RXD	35	DI	SPI5 data input	Can be multiplexed into SPI5_MISO
UART5_TXD	34	DO	SPI5 data output	Can be multiplexed into SPI5_MOSI
UART5_RTS	37	DO	SPI5 clock signal	Can be multiplexed into SPI5_CLK
UART5_CTS	36	DO	SPI5 chip select signal	Can be multiplexed into SPI5_CS
GPIO_22	117	DO	SPI6 chip select signal	Can be multiplexed into SPI6_CS
GPIO_23	116	DO	SPI6 clock signal	Can be multiplexed into SPI6_CLK
GPIO_20	119	DO	SPI6 data output	Can be multiplexed into SPI6_MOSI
GPIO_21	118	DI	SPI6 data input	Can be multiplexed into SPI6_MISO
GPIO_87	105	DO	SPI7 chip select signal	Can be multiplexed into SPI7_CS
GPIO_85	265	DO	SPI7 data output	Can be multiplexed into SPI7_MOSI
GPIO_88	264	DO	SPI7 clock signal	Can be multiplexed into SPI7_CLK
GPIO_86	239	DI	SPI7 data input	Can be multiplexed into SPI7_MISO

3.16. ADC Interface

SC200R supports a analog-to-digital converter (ADC) interface, and the pin definition is shown below.

Table 13: Pin Definition of ADC Interfaces

Pin Name	Pin No	I/O	Description	Comment
ADC	128	AI	Generic ADC	The maximum input voltage is 1.7V.

The resolution of the ADC is up to 15 bits.

3.17. Motor Drive Interface

The pin of the motor drive interface is listed below.

Table 14: Pin Definition of Motor Drive Interface

Pin Name	Pin No	I/O	Description	Comment
VIB_DRV_N	28	PO	Motor drive	Connected to the negative pole of the motor

The motor is driven by an exclusive circuit, and a reference circuit is shown below.

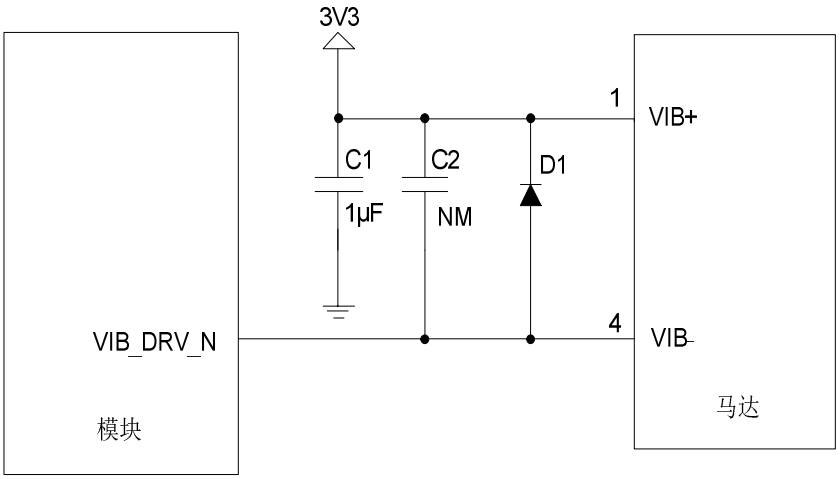


Figure 18: Reference Circuit for Motor Connection

When the motor stops working and the VIB_DRV is disconnected, the redundant electricity on the motor can be discharged from the circuit loop formed by diodes, thus avoiding component damages.

3.18. LCM Interface

SC200R provides an LCM interface, which is MIPI_DSI standard compliant. The interface supports high-speed differential data transmission and supports HD+ display (1440x720 @60fps). The pin definition of the LCM interface is shown below.

Table 15: Pin Definition of LCM Interface

Pin Name	Pin No	I/O	Description	Comment
LDO17_2V85	129	PO	2.85V output power supply for LCM VCC	
PWM	29	DO	Adjust the backlight brightness PWM control signal	
LCD_RST	49	DO	LCD reset signal	
LCD_TE	50	DI	LCD tearing effect signal	
DSI_ CLK_N	52	AO	LCD MIPI clock signal (-)	
DSI_ CLK_P	53	AO	LCD MIPI clock signal (+)	
DSI_LN0_N	54	AO	LCD MIPI data signal 0 (-)	
DSI_LN0_P	55	AO	LCD MIPI data signal 0 (+)	
DSI_LN1_N	56	AO	LCD MIPI data signal 1 (-)	
DSI_LN1_P	57	AO	LCD MIPI data signal 1 (+)	
DSI_LN2_N	58	AO	LCD MIPI data signal 2 (-)	
DSI_LN2_P	59	AO	LCD MIPI data signal 2 (+)	
DSI_LN3_N	60	AO	LCD MIPI data signal 3 (-)	
DSI_LN3_P	61	AO	LCD MIPI data signal 3 (+)	

A reference circuit for the LCM interface is shown below.

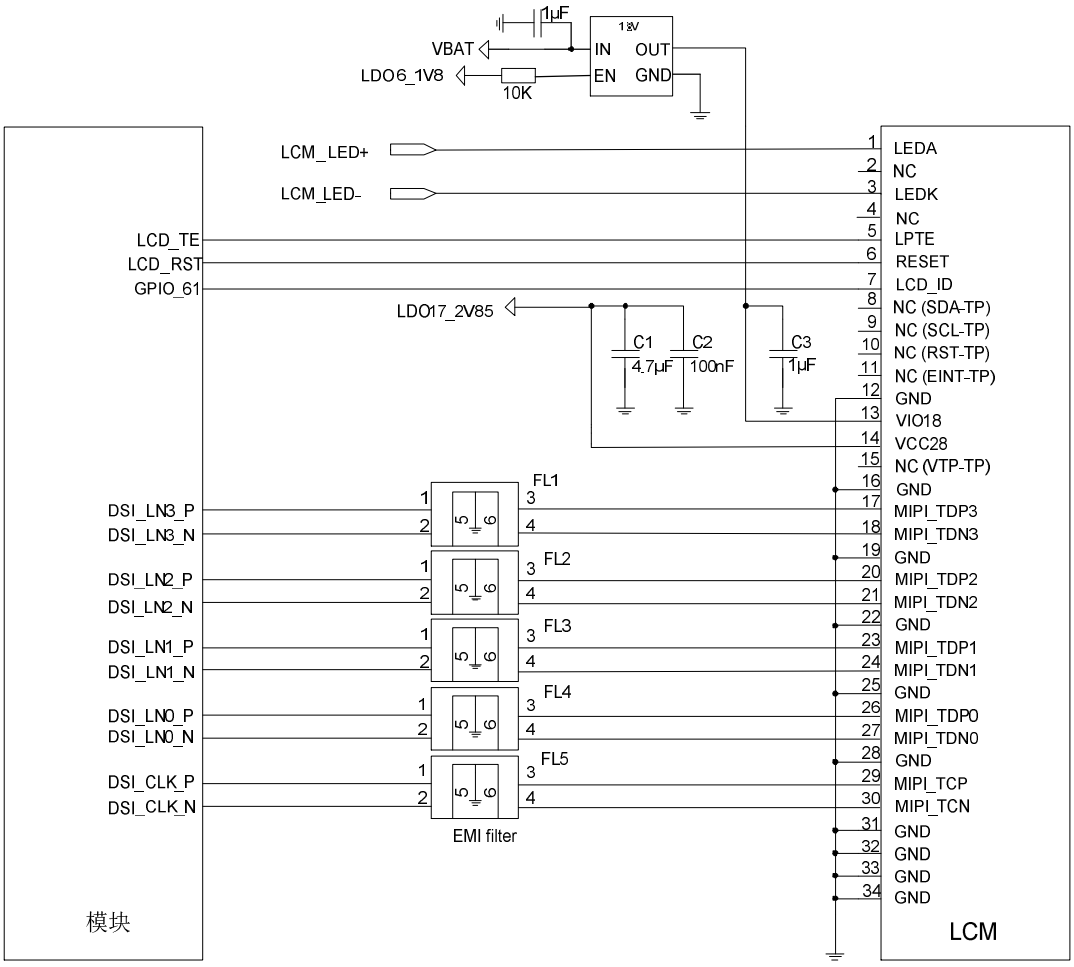


Figure 19: Reference Circuit Design for LCM Interface

MIPI is high-speed signal lines. It is recommended that common-mode filters should be added in series near the LCM connector, so as to improve protection against electromagnetic radiation interference. ICMEF112P900MFR using ICT is recommended.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCM models share the same IC, it is recommended that the LCM module factory burn the OTP register to distinguish different screens. Customers can also select the LCD_ID pin of LCM to connect the ADC pin of the SC200R module, but it should be noted that the output voltage of LCD_ID should not exceed the voltage range of the ADC pin.

The external backlight driving circuit needs to be designed for LCM, and a reference circuit design is shown in the following figure. The backlight brightness adjustment can be realized by the PWM pin of the SC200R module by adjusting the duty ratio.

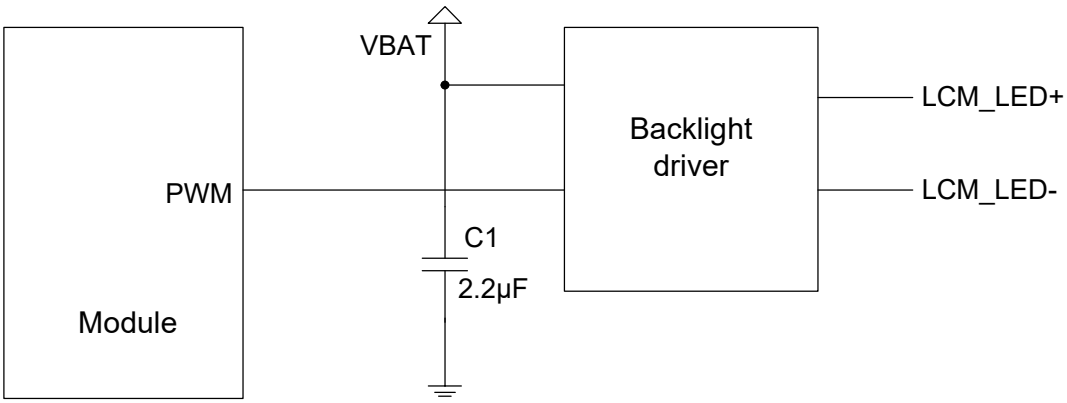


Figure 20: Reference Design for External Backlight Driving Circuit

3.19. Touch Panel Interface

SC200R provides one I2C interface for connection with Touch Panel (TP), and also provides the corresponding power supply and interrupt pins. The definitions of TP interface pins are illustrated below.

Table 16: Pin Definition of Touch Panel Interface

Pin Name	Pin No	I/O	Description	Comment
LDO17_2V85	129	PO	2.85V output power supply for TP VDD	Vnorm=2.85V $I_O$max=450mA
LDO6_1V8	125	PO	1.8V output power supply for TP I/O power	The pull-up power supply of I2C.
TP_INT	30	DI	Interrupt signal of TP	V_{IL}max=0.63V V_{IH}min=1.17V
TP_RST	31	DO	Reset signal of TP	
TP_I2C_SCL	47	OD	I2C clock signal of TP	1.8V voltage domain
TP_I2C_SDA	48	OD	I2C data signal of TP	1.8V voltage domain

A reference circuit for the TP interface is shown below.

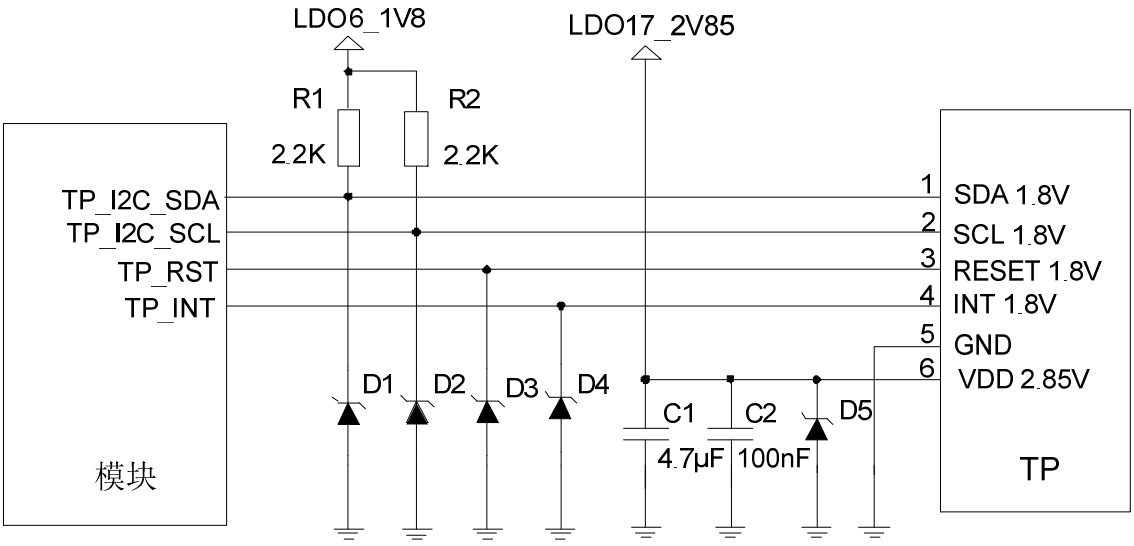


Figure 21: Reference Circuit Design for TP Interface

3.20. Camera Interfaces

Based on the standard MIPI CSI video input interface, the SC200R module supports two cameras (4-lane + 4-lane) or three cameras (4-lane + 2-lane + 1-lane), and the maximum pixel of the camera can be up to 13MP. The video and photo quality is determined by various factors such as the camera sensor, camera lens quality, etc.

Table 17: Pin Definition of Camera Interface

Pin Name	Pin No	I/O	Description	Comment
LDO6_1V8	125	PO	1.8V output power supply for DOVDD of camera	Vnorm=1.8V $I_O$max=150mA
LDO17_2V85	129	PO	2.85V output power supply for AVDD of camera	Vnorm=2.85V $I_O$max=450mA
CSI1_CLK_N	63	AI	CAMERA MIPI clock signal (-)	
CSI1_CLK_P	64	AI	CAMERA MIPI clock signal (+)	
CSI1_LN0_N	65	AI	CAMERA MIPI data0 signal (-)	

CSI1_LN0_P	66	AI	CAMERA MIPI data0 signal (+)
CSI1_LN1_N	67	AI	CAMERA MIPI data1 signal (-)
CSI1_LN1_P	68	AI	CAMERA MIPI data1 signal (+)
CSI1_LN3_N	70	AI	CAMERA MIPI data3 signal (-)
CSI1_LN3_P	71	AI	CAMERA MIPI data3 signal (+)
CSI1_LN2_N	72	AI	CAMERA MIPI data2 signal (-)
CSI1_LN2_P	73	AI	CAMERA MIPI data2 signal (+)
CSI0_CLK_N	157	AI	CAMERA MIPI clock signal (-)
CSI0_CLK_P	196	AI	CAMERA MIPI clock signal (+)
CSI0_LN0_N	158	AI	CAMERA MIPI data0 signal (-)
CSI0_LN0_P	197	AI	CAMERA MIPI data0 signal (+)
CSI0_LN1_N	159	AI	CAMERA MIPI data1 signal (-)
CSI0_LN1_P	198	AI	CAMERA MIPI data1 signal (+)
CSI0_LN2_N	160	AI	CAMERA MIPI data2 signal (-)
CSI0_LN2_P	199	AI	CAMERA MIPI data2 signal (+)
CSI0_LN3_N	161	AI	CAMERA MIPI data3 signal (-)
CSI0_LN3_P	200	AI	CAMERA MIPI data3 signal (+)
CAM0_MCLK	74	DO	Clock signal of camera
CAM1_MCLK	75	DO	Clock signal of camera
CAM0_RST	79	DO	Reset signal of camera
CAM0_PWDN	80	DO	Power down signal of camera
CAM1_RST	81	DO	Reset signal of camera
CAM1_PWDN	82	DO	Power down signal of camera
CAM_I2C_SCL	83	OD	I2C clock signal of camera
CAM_I2C_SDA	84	OD	I2C data signal of camera

CAM2_MCLK	165	DO	Clock signal of camera
CAM2_RST	164	DO	Reset signal of camera
CAM2_PWDN	163	DO	Power down signal of camera
DCAM_I2C_SDA	205	OD	I2C data signal of camera
DCAM_I2C_SCL	166	OD	I2C clock signal of camera

The following is a reference circuit design for cameras.

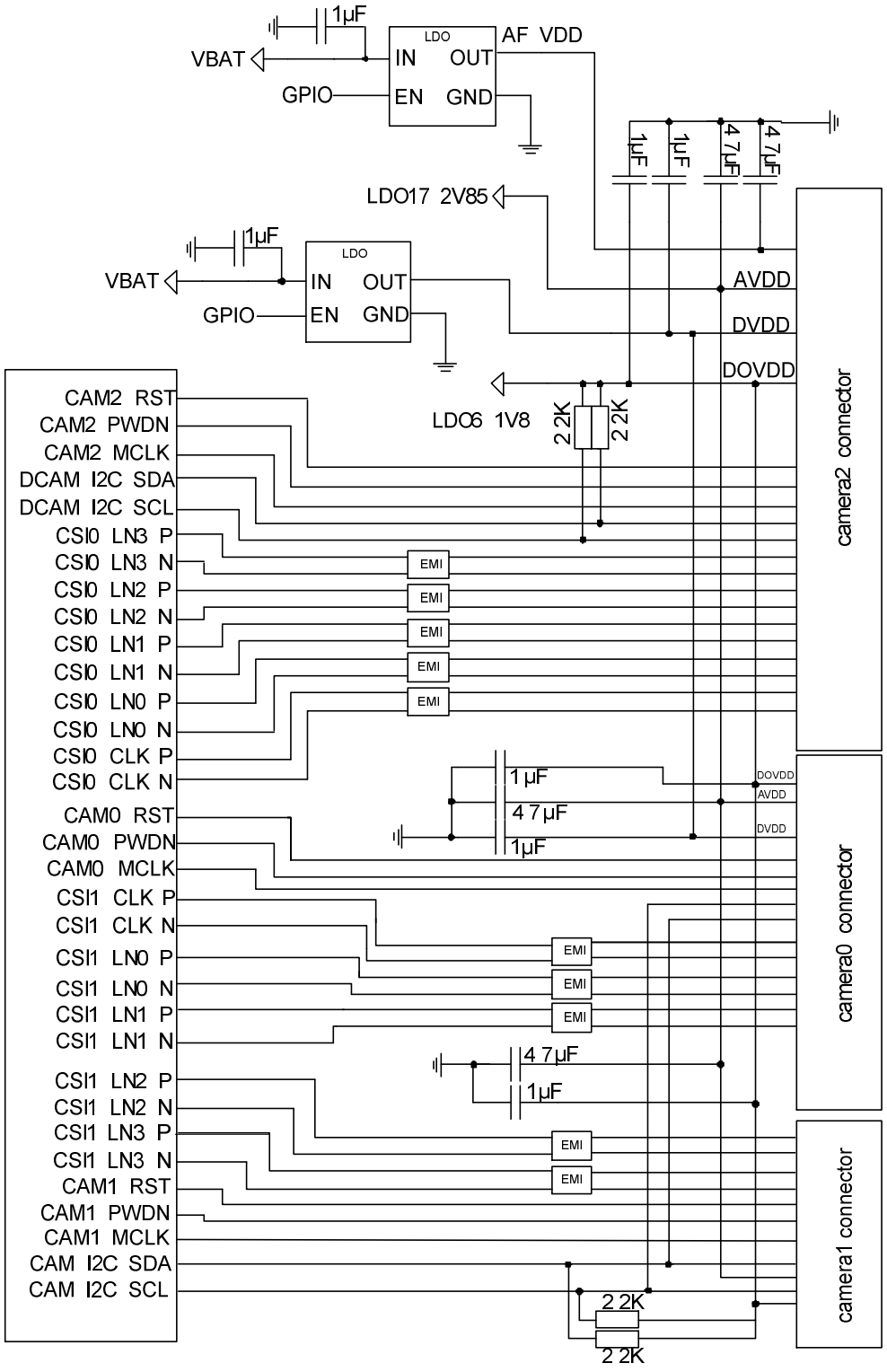


Figure 22: Reference Circuit Design for Cameras

NOTE

CSI1_LN3_P and CSI1_LN3_N of CSI1 can be used as the CLK_P and CLK_N of the camera 1, CSI1_LN2_P and CSI1_LN2_N can be used as the LN_P and LN_N of the camera 1.

3.20.1. Design Considerations

- Special attention should be paid to the pin definition of LCM/camera connectors. Assure the SC200R and the connectors are correctly connected .
- MIPI is high speed signal lines, supporting maximum data rate up to 2.1Gbps. The differential impedance should be controlled to 100Ω. Additionally, it is recommended to route the trace on the inner layer of PCB, and do not cross it with other traces. For the same group of DSI or CSI signals, all the MIPI traces should keep the same length. In order to avoid crosstalk, a distance of 1.5 times the trace width among MIPI signal lines is recommended. During impedance matching, do not connect GND on different planes so as to ensure impedance consistency.
- It is recommended to select a low capacitance TVS for ESD protection and the recommended parasitic capacitance should be below 1pF.
- Route MIPI traces according to the following rules:
  a) The total trace length should not exceed 305mm;
  b) Control the differential impedance to 100Ω ±10%;
  c) Control intra-lane length difference within 0.67 mm;
  d) Control inter-lane length difference within 1.3 mm.

Table 18: MIPI Trace Length Inside the Module

Pin Name	Pin No	Length (mm)	Length Difference (P-N)
52	DSI_CLK_N	12.40	0.00
53	DSI_CLK_P	12.40	
54	DSI_LN0_N	11.75	-0.10
55	DSI_LN0_P	11.65	
56	DSI_LN1_N	9.40	-0.10
57	DSI_LN1_P	9.30	
58	DSI_LN2_N	9.60	0.00
59	DSI_LN2_P	9.60	
60	DSI_LN3_N	12.35	0.00

61	DSI_LN3_P	12.35	
63	CSI1_CLK_N	18.10	-0.05
64	CSI1_CLK_P	18.05	
65	CSI1_LN0_N	18.05	0.05
66	CSI1_LN0_P	18.10	
67	CSI1_LN1_N	18.15	0.05
68	CSI1_LN1_P	18.20	
70	CSI1_LN3_N	18.10	0.10
71	CSI1_LN3_P	18.20	
72	CSI1_LN2_N	18.05	0.05
73	CSI1_LN2_P	18.10	
157	CSI0_CLK_N	22.60	-0.05
196	CSI0_CLK_P	22.55	
158	CSI0_LN0_N	22.55	-0.05
197	CSI0_LN0_P	22.50	
159	CSI0_LN1_N	20.25	0.05
198	CSI0_LN1_P	20.30	
160	CSI0_LN2_N	20.50	0.00
199	CSI0_LN2_P	20.50	
161	CSI0_LN3_N	12.95	0.00
200	CSI0_LN3_P	12.95	

3.21. Sensor Interfaces

SC200R module supports communication with sensors via I2C interfaces, and it supports ALS/PS, compass, G-sensor, and gyroscopic sensors.

Table 19: Pin Definition of Sensor Interfaces

Pin Name	Pin No	I/O	Description	Comment
SENSOR_I2C_SCL	91	OD	I2C clock signal for external sensor	Dedicated for external sensors; cannot be used on touch panel, NFC, I2C keyboard, etc.
SENSOR_I2C_SDA	92	OD	I2C data signal for external sensor	
GPIO_43	107	DI	Light sensor interrupt signal	
GPIO_44	109	DI	Compass sensor interrupt signal	
GPIO_42	110	DI	Accelerate sensor interrupt signal	
GPIO_63	108	DI	Gyroscope sensor interrupt signal	

3.22. Audio Interfaces

SC200R module provides three analog input channels and three analog output channels. The following table shows the pin definition.

Table 20: Pin Definition of Audio Interfaces

Pin Name	Pin No	I/O	Description	Comment
MIC1_P	4	AI	Main microphone input (+)	
MIC_GND	5		MIC reference ground	If unused, connect to ground
MIC2_P	6	AI	Headphone microphone input (+)	
MIC_BIAS2	155		Microphone bias voltage 2	

MIC3_P	148	AI	Secondary microphone input (+)	
MIC_BIAS1	147		Microphone bias voltage 1	
EAR_P	8	AO	Earpiece output (+)	
EAR_N	9	AO	Earpiece output (-)	
SPK_P	10	AO	Speaker output (+)	
SPK_N	11	AO	Speaker output (-)	
HPH_R	136	AO	Headphone right channel output	
HPH_REF	137		Headphone reference ground	
HPH_L	138	AO	Headphone left channel output	
HS_DET	139	AI	Headset insertion detection	High level by default

- The module offers three audio input channels, including three single-ended channels.
- The output voltage range of two MIC_BIAS is programmable between 1.6V and 2.85V, and the maximum output current is 3mA.
- The earpiece interface uses differential output.
- The loudspeaker interface uses the differential output as well. The output channel is available with a Class-D amplifier whose output power is 1362mW when load is 8Ω.
- The headphone interface features stereo left and right channel output, and headphone insert detection function is supported.

3.22.1. Reference Circuit Design for Microphone Interfaces

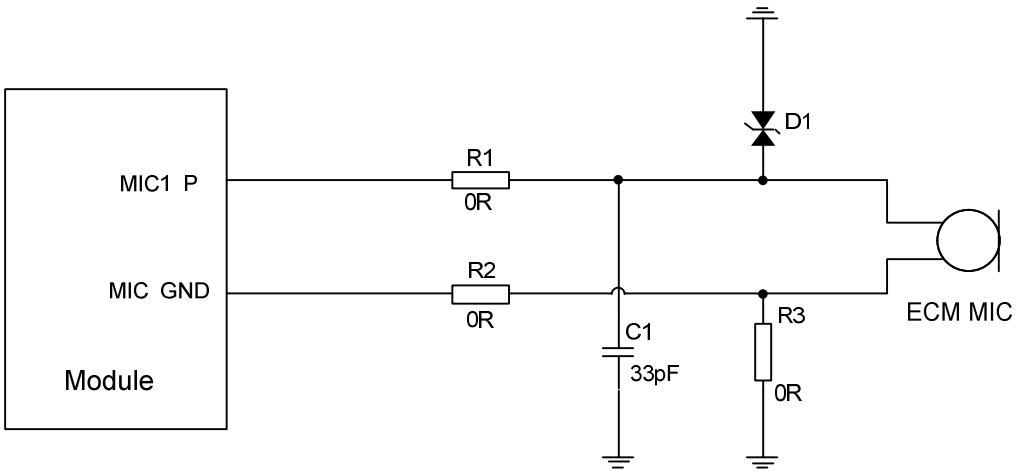


Figure 23: Reference Circuit Design for ECM Microphone Interfaces

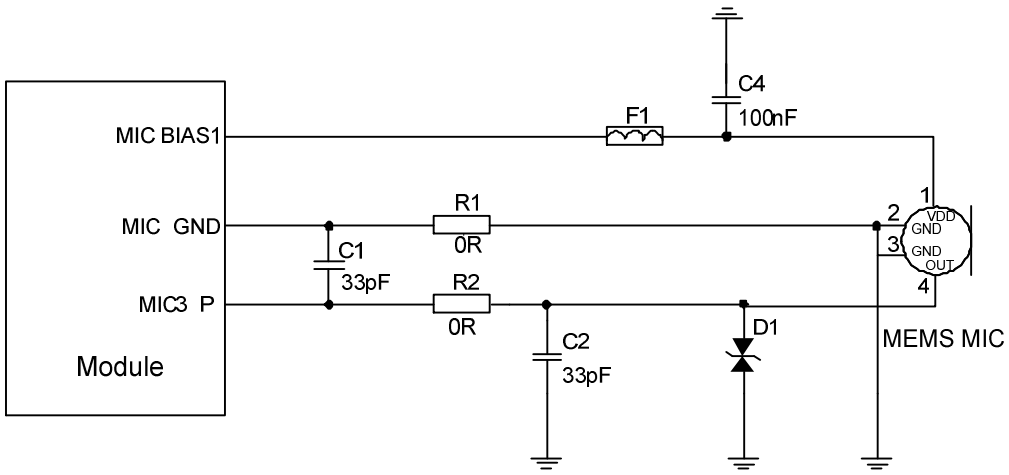


Figure 24: Reference Circuit Design for MEMS Microphone Interfaces

3.22.2. Reference Circuit Design for Receiver Interface

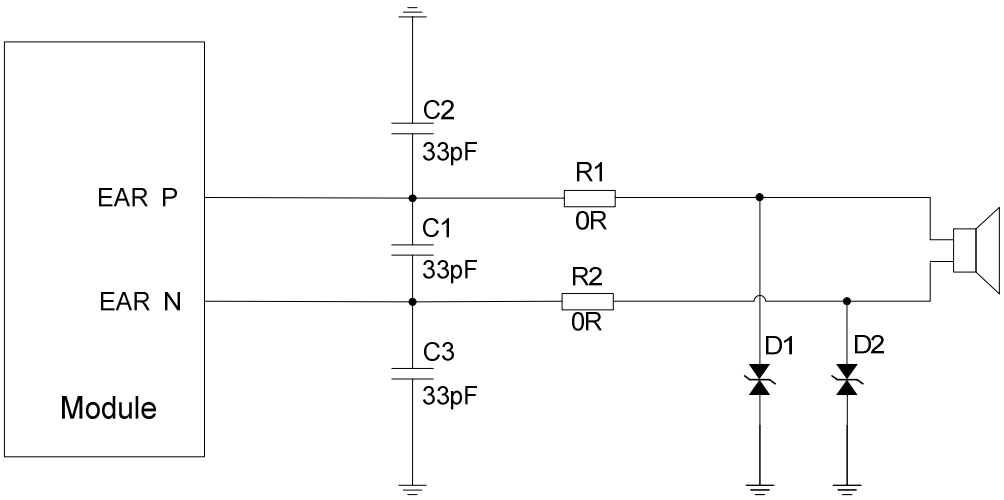


Figure 25: Reference Circuit Design for Receiver Interface

3.22.3. Reference Circuit Design for Headphone Interface

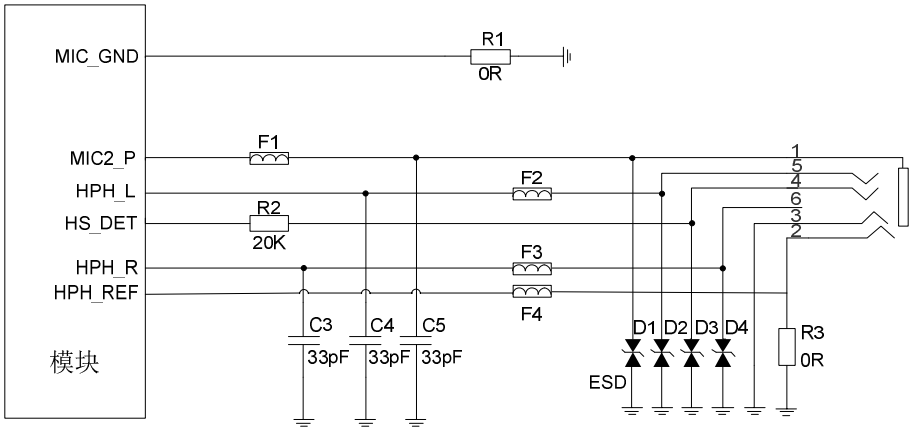


Figure 26: Reference Circuit Design for Headphone Interface

3.22.4. Reference Circuit Design for Loudspeaker Interface

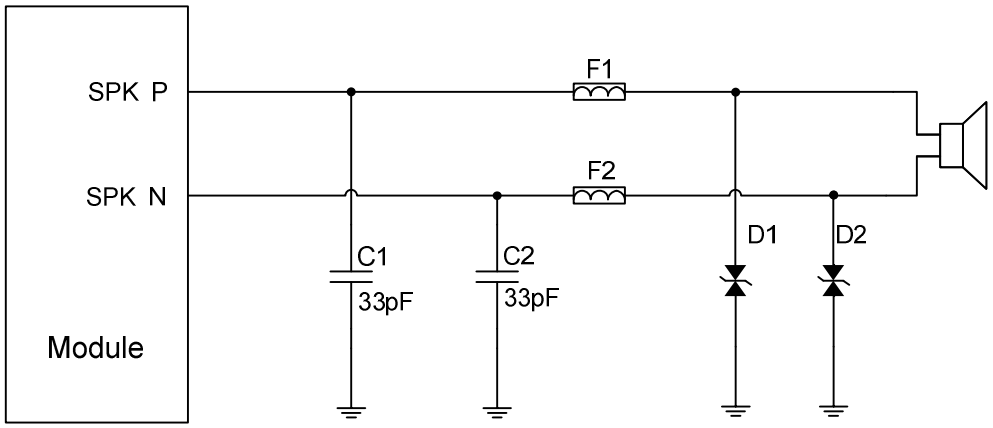


Figure 27: Reference Circuit Design for Loudspeaker Interface

3.22.5. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10pF and 33pF) for filtering out RF interference, thus reducing TDD noise. The 33pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10pF capacitor here is used for filtering out RF interference at DCS1800. Please note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, customers would have to discuss with their capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor should be selected based on the test results. Sometimes, even no RF filtering capacitor is required.

In order to decrease radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces cannot be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

3.23. Emergency Download Interface

USB_BOOT is an emergency download interface. Pull up to LDO5_1V8 during power-up will force the module to enter emergency download mode. There is an emergency option when failures such as abnormal start-up or running occur. For the convenient firmware upgrade and debugging in the future, please reverse this pin. The reference circuit design is shown below.

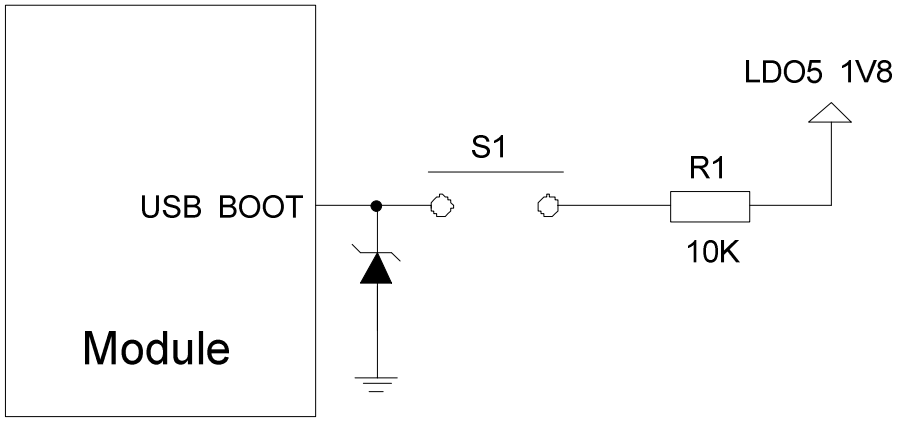


Figure 28: Reference Circuit Design for Emergency Download Interface

4 Wi-Fi and BT

SC200R provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth (BT) functions. The interface impedance is 50Ω. External antennas such as PCB antenna, sucker antenna, and ceramic antenna can be connected to the module via the interface, so as to achieve Wi-Fi and BT functions.

4.1. Wi-Fi Overview

SC200R supports 2.4GHz/5GHz double-band WLAN wireless communication based on IEEE 802.11a/b/g/n standard protocols. The maximum data rate is up to 150Mbps. The features are as below:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI SMS4 hardware encryption
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40

4.1.1. Wi-Fi Performance

The following table lists the Wi-Fi transmitting and receiving performance of the SC200R module.

Table 21: Wi-Fi Transmitting Performance

	Standard	Rate	Output Power
2.4GHz	802.11b	1Mbps	16dBm ±2.5dB
	802.11b	11Mbps	16dBm ±2.5dB
	802.11g	6Mbps	16dBm ±2.5dB
	802.11g	54Mbps	14dBm ±2.5dB
	802.11n HT20	MCS0	15dBm ±2.5dB
	802.11n HT20	MCS7	13dBm ±2.5dB

	802.11n HT40	MCS0	14dBm ±2.5dB
	802.11n HT40	MCS7	13dBm ±2.5dB
5GHz	802.11a	6Mbps	15dBm ±2.5dB
	802.11a	54Mbps	13dBm ±2.5dB
	802.11n HT20	MCS0	14dBm ±2.5dB
	802.11n HT20	MCS7	12dBm ±2.5dB
	802.11n HT40	MCS0	14dBm ±2.5dB
	802.11n HT40	MCS7	12dBm ±2.5dB

Table 22: Wi-Fi Receiving Performance

	Standard	Rate	Sensitivity
2.4GHz	802.11b	1Mbps	-96
	802.11b	11Mbps	-87
	802.11g	6Mbps	-91
	802.11g	54Mbps	-73
	802.11n HT20	MCS0	-90
	802.11n HT20	MCS7	-72
	802.11n HT40	MCS0	TBD
	802.11n HT40	MCS7	TBD
5GHz	802.11a	6Mbps	-89
	802.11a	54Mbps	-73
	802.11n HT20	MCS0	TBD
	802.11n HT20	MCS7	TBD
	802.11n HT40	MCS0	-89
	802.11n HT40	MCS7	-71

Referenced specifications are listed below:

- IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11d, IEEE Std 802.11e, IEEE Std 802.11g, IEEE Std 802.11i: IEEE 802.11-2007 WLAN MAC and PHY, June 2007

4.2. BT Overview

SC200R module supports BT4.2 (BR/EDR+BLE) specification, as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally support up to 7 wireless connections.
- Maximally support up to 3.5 PICONETs at the same time.
- Support one SCO (Synchronous Connection Oriented) or eSCO connection.

The BR/EDR channel bandwidth is 1MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2MHz, and can accommodate 40 channels.

Table 23: BT Data Rate and Version

Version	Data rate	Maximum Application Throughput	Comment
1.2	1 Mbit/s	> 80 Kbit/s	
2.0+EDR	3 Mbit/s	> 80 Kbit/s	
3.0+HS	24 Mbit/s	Reference 3.0 + HS	
4.0	24 Mbit/s	Reference 4.0 LE	

Referenced specifications are listed below:

- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009

4.2.1. BT Performance

The following table lists the BT transmitting and receiving performance of SC200R module.

Table 24: BT Transmitting and Receiving Performance

Transmitter Performance			
Packet Types	DH5	2-DH5	3-DH5
Transmitting Power	10dBm±2.5dB	8dBm±2.5dB	8dBm±2.5dB
Receiver Performance			
Packet Types	DH5	2-DH5	3-DH5
Receiving Sensitivity	-93	-92	-88

5 GNSS

SC200R integrates a Qualcomm IZat™ GNSS engine (GEN 8C) which supports multiple positioning and navigation systems including GPS, GLONASS, and BeiDou. With an embedded LNA, the module provides greatly improved positioning accuracy.

5.1. GNSS Performance

The following table lists the GNSS performance of the SC200R module in conduction mode.

Table 25: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity (GNSS)	Cold start	-145	dBm
	Reacquisition	-157	dBm
	Tracking	-157	dBm
TTFF (GNSS)	Cold start	30	s
	Warm start	23	s
	Hot start	3.3	s
Static Drift (GNSS)	CEP-50	<2.5	m

5.2. GNSS RF Design Guidelines

Bad design of antenna and layout may cause reduced GPS receiving sensitivity, longer GPS positioning time, or reduced positioning accuracy. In order to avoid this, please follow the reference design rules as below:

- Maximize the distance between the GNSS RF part and the GPRS RF part (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, GNSS RF signal lines and RF components should be placed far away from high-speed circuits, switched-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with a harsh electromagnetic environment or with high requirement on ESD protection, it is recommended to add ESD protection diodes for the antenna interface. Only diodes with ultra-low junction capacitance such as 0.5pF can be selected. Otherwise, there will be effects on the impedance characteristic of the RF circuit loop or attenuation of the bypass RF signal may be caused.
- Control the impedance of either feeder line or PCB trace to 50Ω, and keep the trace length as short as possible.
- Refer to ***Chapter 6.3*** for the GNSS reference circuit design.

6 Antenna Interfaces

SC200R provides four antenna interfaces for the main antenna, Rx-diversity/MIMO antenna, GNSS antenna and Wi-Fi/BT antenna, respectively. The antenna ports have an impedance of 50Ω.

6.1. Main/Rx-diversity Antenna Interfaces

The pin definition of main/Rx-diversity antenna interfaces is shown below.

Table 26: Pin Definition of Main/Rx-diversity Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	87	IO	Main antenna	50Ω impedance
ANT_DRX	131	AI	Diversity antenna	

The operating frequencies of SC200R are listed in the following tables

Table 27: SC200R-CE Operating Frequencies

3GPP Band	Receive	Transmit	Unit
EGSM900	925~960	880~915	MHz
DCS1800	1805~1880	1710~1785	MHz
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B8	925~960	880~915	MHz
EVDO/CDMA BC0	869~894	824~849	MHz
LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz

LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-TDD B34	2010~2025	2010~2025	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41	2555~2655	2555~2655	MHz

Table 28: SC200R-EM* Operating Frequencies

3GPP Band	Receive	Transmit	Unit
GSM850	869~894	824~849	MHz
EGSM900	925~960	880~915	MHz
DCS1800	1805~1880	1710~1785	MHz
PCS1900	1930~1990	1850~1910	MHz
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B2	1930~1990	1850~1910	MHz
WCDMA B5	869~894	824~849	MHz
WCDMA B8	925~960	880~915	MHz
LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B2	1930~1990	1850~1910	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B7	2620~2690	2500~2570	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-FDD B20	791~821	832~862	MHz

LTE-FDD B28 ()A+B)	758~803	703~748	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41	2555~2655	2555~2655	MHz

Table 29: SC200R-NA* Operating Frequencies

3GPP Band	Receive	Transmit	Unit
WCDMA B2	1930~1990	1850~1910	MHz
WCDMA B4	2110~2155	1710~1755	MHz
WCDMA B5	869~894	824~849	MHz
LTE-FDD B2	1930~1990	1850~1910	MHz
LTE-FDD B4	2110~2155	1710~1755	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B7	2620~2690	2500~2570	MHz
LTE-FDD B12	729~746	699~716	MHz
LTE-FDD B13	746~756	777~787	MHz
LTE-FDD B14	758~768	788~798	MHz
LTE-FDD B17	734~746	704~716	MHz
LTE-FDD B25	1930~1995	1850~1915	MHz
LTE-FDD B26	859~894	814~849	MHz
LTE-FDD B66	2100~2200	1710~1780	MHz
LTE-FDD B71	663~698	617~652	MHz
LTE-TDD B41	2496~2690	2496~2690	MHz

Table 30: SC200R-JP* Operating Frequencies

3GPP Band	Receive	Transmit	Unit
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B6	875~885	830~840	MHz
WCDMA B8	925~960	880~915	MHz
WCDAM B19	875~890	830~845	MHz
LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-FDD B11	1428~1447	1475~1495	MHz
LTE-FDD B18	860~875	815~830	MHz
LTE-FDD B19	875~890	830~845	MHz
LTE-FDD B26	859~894	814~849	MHz
LTE-FDD B28	758~803	703~748	MHz
LTE-TDD B41	2496~2690	2496~2690	MHz

NOTE

"*" means under development.

6.1.1. Main and Rx-diversity Antenna Interfaces Reference Design

A reference circuit design for main and Rx-diversity antenna interfaces is shown as below. A π-type matching circuit should be reserved for better RF performance. The π-type matching components (R1/C1/C2, R2/C3/C4) should be placed as close to the antennas as possible and are mounted according to the actual debugging. The C1, C2, C3, and C4 are not mounted and a 0Ω resistor is mounted on R1 and R2 respectively by default.

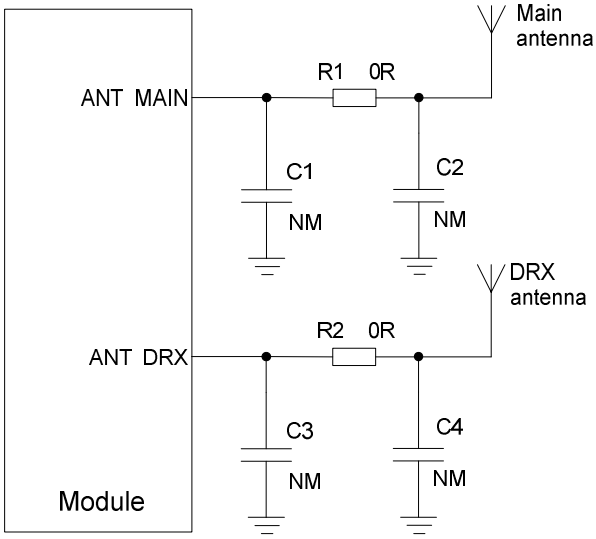


Figure 29: Reference Circuit Design for Main and Rx-diversity Antenna Interfaces

6.1.2. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the clearance between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip line or coplanar waveguide with different PCB structures.

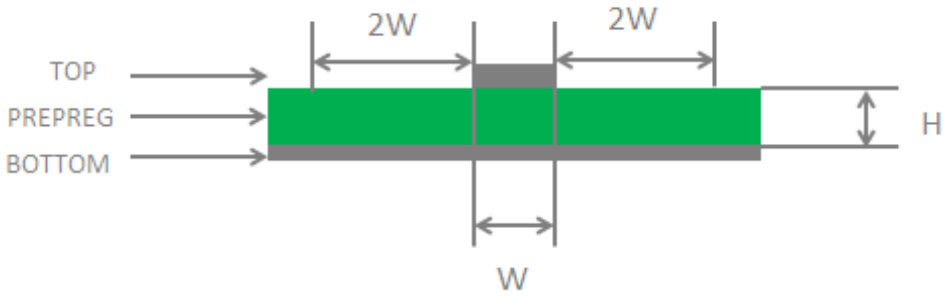


Figure 30: Microstrip Design on a 2-layer PCB

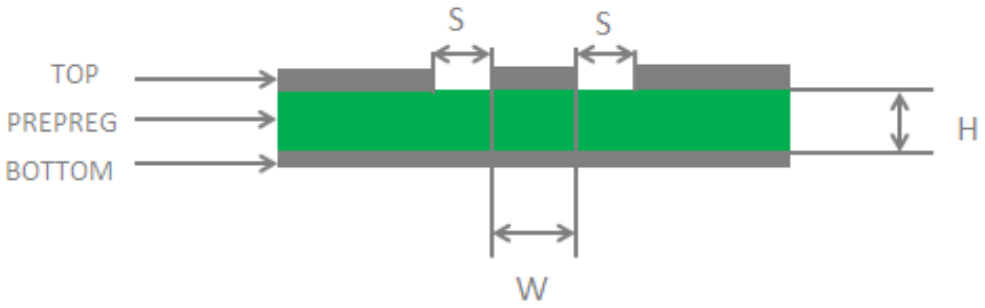


Figure 31: Coplanar Waveguide Design on a 2-layer PCB

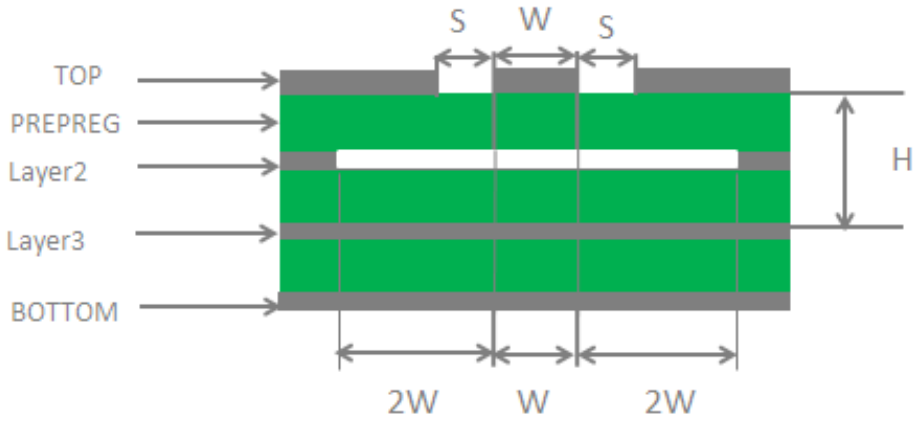


Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

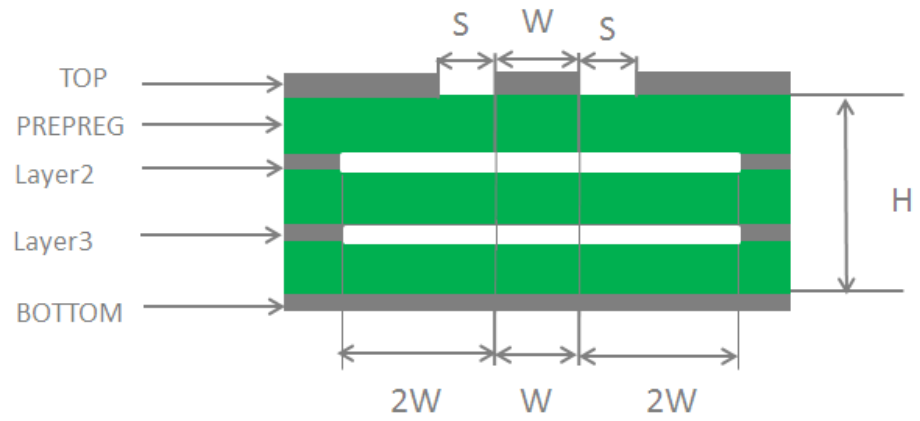


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times as wide as RF signal traces (2 x W).

For more details about the RF layout, please refer to the ***document [3]***.

6.2. Wi-Fi/BT Antenna Interface

The following tables show the pin definition and frequency specification of the Wi-Fi/BT antenna interface.

Table 31: Pin Definition of Wi-Fi/BT Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	77	IO	Wi-Fi/BT antenna interface	50Ω impedance

Table 32: Wi-Fi/BT Frequency

Type	Frequency	Unit
Wi-Fi (2.4GHz)	2402~2482	MHz
Wi-Fi (5GHz)	5180~5825	MHz
BT4.2 LE	2402~2480	MHz

A reference circuit design for Wi-Fi/BT antenna interface is shown as below. C1 and C2 are not mounted and a 0Ω resistor is mounted on R1 by default.

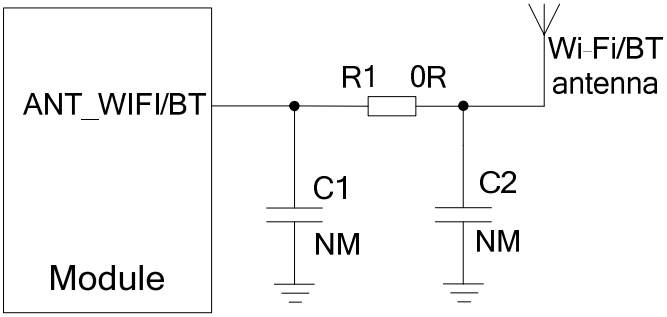


Figure 34: Reference Circuit Design for Wi-Fi/BT Antenna

6.3. GNSS Antenna Interface

The following tables show pin definition and frequency specification of GNSS antenna interface.

Table 33: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	121	AI	GNSS antenna interface	50Ω impedance

Table 34: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098 ±2.046	MHz

6.3.1. Recommended Circuit for Passive Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference circuit design is given below.

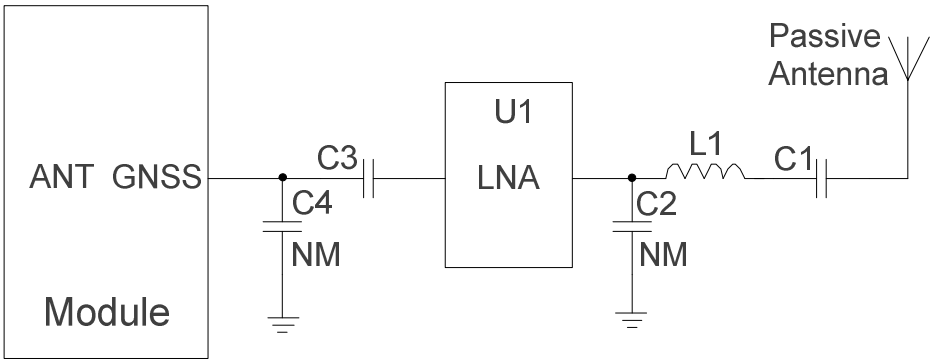


Figure 35: Reference Circuit Design for GNSS Passive Antenna

NOTE

When the passive antenna is placed far away from the module (that is, the antenna trace is long), it is recommended to add an external LNA circuit for better GNSS receiving performance, and the LNA should be placed close to the antenna.

6.3.2. Recommended Circuit for Active Antenna

The active antenna is powered by a 56nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3V to 5.0V. Although featuring low power consumption, the active antenna still requires stable and clean power supplies. It is recommended to use high-performance LDO as the power supply. A reference design of the GNSS active antenna is shown below.

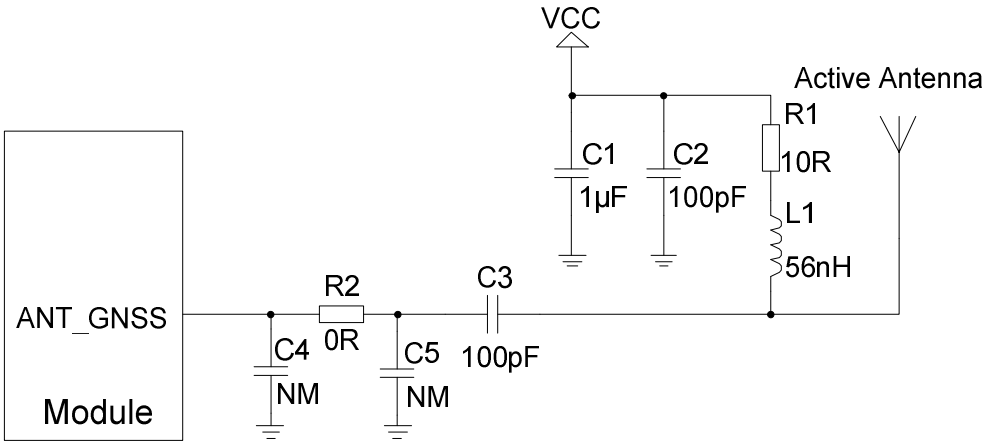


Figure 36: Reference Circuit Design for GNSS Active Antenna

6.4. Antenna Installation

6.4.1. Antenna Requirements

The following table shows the requirement on the main antenna, RX-diversity antenna, Wi-Fi/BT antenna and a GNSS antenna.

Table 35: Antenna Requirements

Type	Requirements
GSM/WCDMA/TD-SCDMA/ LTE	VSWR:> ≤ 2 Gain (dBi): 1 Max Input Power (W): 50 Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: < 1dB (GSM850, EGSM900, WCDMA B5/B6/B8/B19, EVDO/CDMA BC0, LTE B5/B8/B12/B13/B14/B17/B18/B19/B20/B26/B28A/B28B/B71) Cable Insertion Loss: < 1.5dB (DCS1800, PCS1900, WCDMA B1/B2/B4, LTE B1/B2/B3/B4/B11/B21/B25/B34/B39/B66) Cable Insertion Loss: < 2dB (LTE-FDD B7, LTE-TDD B38/B40/B41)
Wi-Fi/BT	VSWR: ≤ 2 Gain (dBi): 1 Max Input Power (W): 50 Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: < 1dB
GNSS [1)]	Frequency range: 1559MHz~1609MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive Antenna Gain: > 0dBi Active Antenna Noise Figure: < 1.5dB Active Antenna Total Gain: < 17dBi (Typ.)

NOTE

[1)] It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

6.4.2. Recommended RF Connector for Antenna Installation

If an RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by HIROSE.

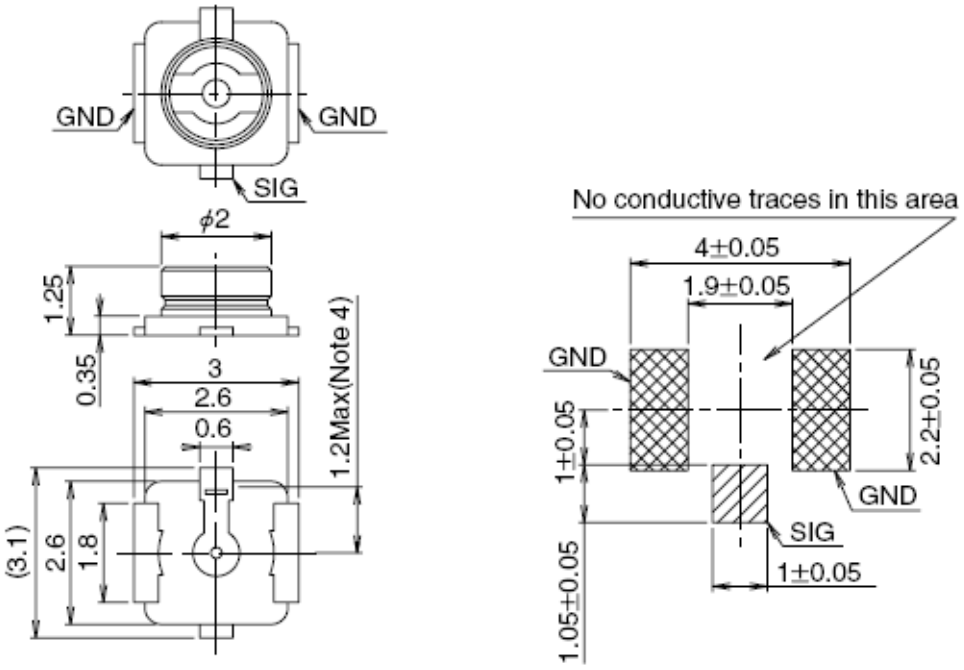


Figure 37: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

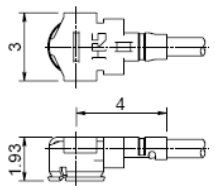
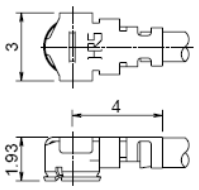
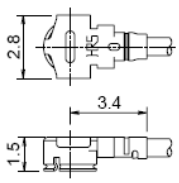
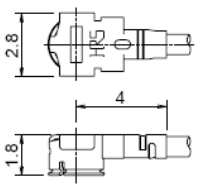
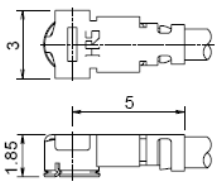
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 38: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

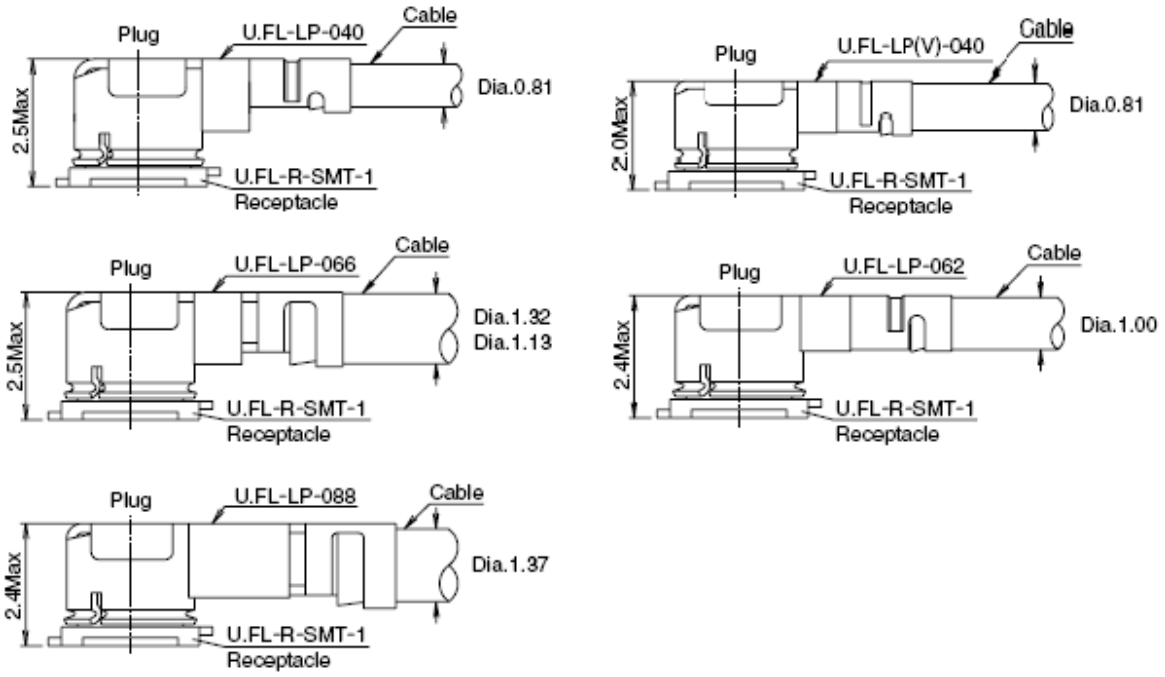


Figure 39: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://www.hirose.com.

7 Electrical, Reliability and Radio Characteristics

7.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 36: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.5	6	V
USB_VBUS	-0.5	16	V
Peak Current of VBAT	0	3	A
Voltage on Digital Pins	-0.3	2.16	V

7.2. Power Supply Ratings

Table 37: SC200R Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltages must stay between the minimum and maximum values	3.55	3.8	4.2	V
	Voltage drop during transmitting burst	Maximum power control level at EGSM900			400	mV

I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level at EGSM900		1.8	3.0	A
USB_VBUS	USB detection		4.35	5.0	6.2	V
VRTC	Power supply voltage of the backup battery		2.0	3.0	3.25	V

7.3. Operation and Storage Temperatures

The operating temperature is listed in the following table.

Table 38: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating temperature range [1)]	-35	+25	+75	ºC
Storage Temperature Range	-40		+90	ºC

NOTE

[1)] Within the operation temperature range, the module is 3GPP compliant. At present, this temperature range is only for reference and needs to be further tested

7.4. Current Consumption

The values of current consumption are shown below.

Table 39: SC200R-CE Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{VBAT}	OFF state	Power down		20		uA
	GSM/GPRS supply current	Sleep (USB disconnected) @DRX=2		TBD		mA

		Sleep (USB disconnected) @DRX=5	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	mA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6	TBD	mA
		Sleep (USB disconnected) @DRX=7	TBD	mA
		Sleep (USB disconnected) @DRX=8	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	mA
	CDMA supply current	BC0 CH283 @ Slot Cycle Index=1	TBD	mA
		BC0 CH283 @ Slot Cycle Index=7	TBD	mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=5	TBD	mA
		Sleep (USB disconnected) @DRX=6	TBD	mA
		Sleep (USB disconnected) @DRX=7	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=5	TBD	mA
		Sleep (USB disconnected) @DRX=6	TBD	mA
		Sleep (USB disconnected) @DRX=7	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	mA
	GSM voice call	EGSM900 @PCL 5	TBD	mA
		EGSM900 @PCL 12	TBD	mA
		EGSM900 @PCL 19	TBD	mA
		DCS1800 @PCL 0	TBD	mA
		DCS1800 @PCL 7	TBD	mA
		DCS1800 @PCL 15	TBD	mA

	WCDMA voice call	B1 @max power	TBD	mA
		B8 @max power	TBD	mA
	GPRS data transfer	EGSM900 (1UL/4DL) @PCL 5	TBD	mA
		EGSM900 (2UL/3DL) @PCL 5	TBD	mA
		EGSM900 (3UL/2DL) @PCL 5	TBD	mA
		EGSM900 (4UL/1DL) @PCL 5	TBD	mA
		DCS1800 (1UL/4DL) @PCL 0	TBD	mA
		DCS1800 (2UL/3DL) @PCL 0	TBD	mA
		DCS1800 (3UL/2DL) @PCL0	TBD	mA
		DCS1800 (4UL/1DL) @PCL 0	TBD	mA
	EDGE data transfer	EGSM900 (1UL/4DL) @PCL 8	TBD	mA
		EGSM900 (2UL/3DL) @PCL 8	TBD	mA
		EGSM900 (3UL/2DL) @PCL 8	TBD	mA
		EGSM900 (4UL/1DL) @PCL 8	TBD	mA
		DCS1800 (1UL/4DL) @PCL 2	TBD	mA
		DCS1800 (2UL/3DL) @PCL 2	TBD	mA
		DCS1800 (3UL/2DL) @PCL 2	TBD	mA
		DCS1800 (4UL/1DL) @PCL 2	TBD	mA
	WCDMA data transfer	B1 (HSDPA) @max power	TBD	mA
		B8 (HSDPA) @max power	TBD	mA
		B1 (HSUPA) @max power	TBD	mA
		B8 (HSUPA) @max power	TBD	mA
	EVDO/CDMA data transfer	BC0 @max power	TBD	mA
	LTE data transfer	LTE-FDD B1 @max power	TBD	mA
		LTE-FDD B3 @max power	TBD	mA

	LTE-FDD B5 @max power	TBD	mA
	LTE-FDD B8 @max power	TBD	mA
	LTE-TDD B34 @max power	TBD	mA
	LTE-TDD B38 @max power	TBD	mA
	LTE-TDD B39 @max power	TBD	mA
	LTE-TDD B40 @max power	TBD	mA
	LTE-TDD B41 @max power	TBD	mA

Table 40: SC200R-EM* Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{VBAT}	OFF state	Power down		20		uA
	GSM/GPRS supply current	Sleep (USB disconnected) @DRX=2		TBD		mA
		Sleep (USB disconnected) @DRX=5		TBD		mA
		Sleep (USB disconnected) @DRX=9		TBD		mA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6		TBD		mA
		Sleep (USB disconnected) @DRX=8		TBD		mA
		Sleep (USB disconnected) @DRX=9		TBD		mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=6		TBD		mA
		Sleep (USB disconnected) @DRX=8		TBD		mA
		Sleep (USB disconnected) @DRX=9		TBD		mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6		TBD		mA
		Sleep (USB disconnected) @DRX=8		TBD		mA
		Sleep (USB disconnected) @DRX=9		TBD		mA

	GSM voice call	EGSM850 @PCL 5	TBD	mA
		EGSM850 @PCL 12	TBD	mA
		EGSM850 @PCL 19	TBD	mA
		EGSM900 @PCL 5	TBD	mA
		EGSM900 @PCL 12	TBD	mA
		EGSM900 @PCL 19	TBD	mA
		DCS1800 @PCL 0	TBD	mA
		DCS1800 @PCL 7	TBD	mA
		DCS1800 @PCL 15	TBD	mA
		DCS1900 @PCL 0	TBD	mA
		DCS1900 @PCL 7	TBD	mA
		DCS1900 @PCL 15	TBD	mA
	WCDMA voice call	B1 @max power	TBD	mA
		B2 @max power	TBD	mA
		B5 @max power	TBD	mA
		B8 @max power	TBD	mA
	GPRS data transfer	EGSM850(1UL/4DL) @PCL 5	TBD	mA
		EGSM850 (2UL/3DL) @PCL 5	TBD	mA
		EGSM850 (3UL/2DL) @PCL 5	TBD	mA
		EGSM850 (4UL/1DL) @PCL 5	TBD	mA
		EGSM900 (1UL/4DL) @PCL 5	TBD	mA
		EGSM900 (2UL/3DL) @PCL 5	TBD	mA
		EGSM900 (3UL/2DL) @PCL 5	TBD	mA
		EGSM900 (4UL/1DL) @PCL 5	TBD	mA
		DCS1800 (1UL/4DL) @PCL 0	TBD	mA

		DCS1800 (2UL/3DL) @PCL 0	TBD	mA
		DCS1800 (3UL/2DL) @PCL0	TBD	mA
		DCS1800 (4UL/1DL) @PCL 0	TBD	mA
		DCS1900 (1UL/4DL) @PCL 0	TBD	mA
		DCS1900 (2UL/3DL) @PCL 0	TBD	mA
		DCS1900 (3UL/2DL) @PCL0	TBD	mA
		DCS1900 (4UL/1DL) @PCL 0	TBD	mA
	EDGE data transfer	EGSM850(1UL/4DL) @PCL 8	TBD	mA
		EGSM850 (2UL/3DL) @PCL 8	TBD	mA
		EGSM850 (3UL/2DL) @PCL 8	TBD	mA
		EGSM850 (4UL/1DL) @PCL 8	TBD	mA
		EGSM900 (1UL/4DL) @PCL 8	TBD	mA
		EGSM900 (2UL/3DL) @PCL 8	TBD	mA
		EGSM900 (3UL/2DL) @PCL 8	TBD	mA
		DCS1800 (1UL/4DL) @PCL 2	TBD	mA
		DCS1800 (2UL/3DL) @PCL 2	TBD	mA
		DCS1800 (3UL/2DL) @PCL 2	TBD	mA
		DCS1800 (4UL/1DL) @PCL 2	TBD	mA
		DCS1900 (1UL/4DL) @PCL 2	TBD	mA
		DCS1900 (2UL/3DL) @PCL 2	TBD	mA
		DCS1900 (3UL/2DL) @PCL 2	TBD	mA
		DCS1900 (4UL/1DL) @PCL 2	TBD	mA
	WCDMA data transfer	B1 (HSDPA) @max power	TBD	mA
		B2 (HSDPA) @max power	TBD	mA
		B5 (HSDPA) @max power	TBD	mA

		B8 (HSDPA) @max power	TBD	mA
		B1 (HSUPA) @max power	TBD	mA
		B2 (HSUPA) @max power	TBD	mA
		B5 (HSUPA) @max power	TBD	mA
		B8 (HSUPA) @max power	TBD	mA
	LTE data transfer	LTE-FDD B1 @max power	TBD	mA
		LTE-FDD B2 @max power	TBD	mA
		LTE-FDD B3 @max power	TBD	mA
		LTE-FDD B5 @max power	TBD	mA
		LTE-FDD B7 @max power	TBD	mA
		LTE-FDD B8 @max power	TBD	mA
		LTE-FDD B20 @max power	TBD	mA
		LTE-FDD B28 @max power	TBD	mA
		LTE-TDD B38 @max power	TBD	mA
		LTE-TDD B39 @max power	TBD	mA
		LTE-TDD B40 @max power	TBD	mA
		LTE-TDD B41 @max power	TBD	mA

Table 41: SC200R-NA* Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{VBAT}	OFF state	Power down		20		uA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6		3.9		mA
		Sleep (USB disconnected) @DRX=8		3		mA
		Sleep (USB disconnected) @DRX=9		2.7		mA
	LTE-FDD	Sleep (USB disconnected)		4.7		mA

	supply current	@DRX=6		
		Sleep (USB disconnected) @DRX=8	3.1	mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6	4.8	mA
		Sleep (USB disconnected) @DRX=8	3.1	mA
	WCDMA voice call	B2 @max power	645	mA
		B4 @max power	560	mA
		B5 @max power	480	mA
	WCDMA data transfer	B2 (HSDPA) @max power	600	mA
		B4 (HSDPA) @max power	560	mA
		B5 (HSDPA) @max power	450	mA
		B2 (HSUPA) @max power	530	mA
		B4 (HSUPA) @max power	530	mA
		B5 (HSUPA) @max power	445	mA
	LTE data transfer	LTE-FDD B2 @max power	830	mA
		LTE-FDD B4 @max power	720	mA
		LTE-FDD B5 @max power	550	mA
		LTE-FDD B7 @max power	965	mA
		LTE-FDD B12 @max power	610	mA
		LTE-FDD B13 @max power	655	mA
		LTE-FDD B14 @max power	665	mA
		LTE-FDD B17@max power	585	mA
		LTE-FDD B25 @max power	837	mA
		LTE-FDD B26 @max power	620	mA
		LTE-FDD B66 @max power	750	mA
		LTE-FDD B71 @max power	750	mA

	LTE-TDD B41 @max power	481	mA

Table 42: SC200R-JP* Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{VBAT}	OFF state	Power down		20		uA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6		TBD		mA
		Sleep (USB disconnected) @DRX=8		TBD		mA
		Sleep (USB disconnected) @DRX=9		TBD		mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=6		TBD		mA
		Sleep (USB disconnected) @DRX=8		TBD		mA
		Sleep (USB disconnected) @DRX=9		TBD		mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6		TBD		mA
		Sleep (USB disconnected) @DRX=8		TBD		mA
		Sleep (USB disconnected) @DRX=9		TBD		mA
	WCDMA voice call	B1 @max power		TBD		mA
		B6 @max power		TBD		mA
		B8 @max power		TBD		mA
		B19 @max power		TBD		mA
	WCDMA data transfer	B1 (HSDPA) @max power		TBD		mA
		B6 (HSDPA) @max power		TBD		mA
		B8 (HSDPA) @max power		TBD		mA
		B19 (HSDPA) @max power		TBD		mA
		B1 (HSUPA) @max power		TBD		mA

		B6 (HSUPA) @max power	TBD	mA
		B8 (HSUPA) @max power	TBD	mA
		B19 (HSUPA) @max power	TBD	mA
	LTE data transfer	LTE-FDD B1 @max power	TBD	mA
		LTE-FDD B3 @max power	TBD	mA
		LTE-FDD B5 @max power	TBD	mA
		LTE-FDD B8 @max power	TBD	mA
		LTE-FDD B11 @max power	TBD	mA
		LTE-FDD B18 @max power	TBD	mA
		LTE-FDD B19 @max power	TBD	mA
		LTE-FDD B21 @max power	TBD	mA
		LTE-FDD B26 @max power	TBD	mA
		LTE-FDD B28 @max power	TBD	mA
		LTE-TDD B41 @max power	TBD	mA

NOTE

"*" means under development.

7.5. RF Output Power

The following table shows the RF output power of SC200R module.

Table 43: SC200R-CE RF Output Power

Frequency	Max.	Min.
EGSM900	33dBm ±2dB	5dBm ±5dB
DCS1800	30dBm ±2dB	0dBm ±5dB
WCDMA B1	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
EVDO/CDMA BC0	24dBm+3/-1dB	<-49dBm
LTE-FDD B1	23dBm ±2dB	<-39dBm
LTE-FDD B3	23dBm ±2dB	<-39dBm
LTE-FDD B5	23dBm ±2dB	<-39dBm
LTE-FDD B8	23dBm ±2dB	<-39dBm
LTE-FDD B34	23dBm ±2dB	<-39dBm
LTE-TDD B38	23dBm ±2dB	<-39dBm
LTE-TDD B39	23dBm ±2dB	<-39dBm
LTE-TDD B40	23dBm ±2dB	<-39dBm
LTE-TDD B41	23dBm ±2dB	<-39dBm

Table 44: SC200R-EM* RF Output Power

Frequency	Max.	Min.
GSM850	TBD	TBD
EGSM900	TBD	TBD
DCS1800	TBD	TBD
PCS1900	TBD	TBD
WCDMA B1	TBD	TBD
WCDMA B2	TBD	TBD
WCDMA B5	TBD	TBD
WCDMA B8	TBD	TBD
LTE-FDD B1	TBD	TBD
LTE-FDD B2	TBD	TBD
LTE-FDD B3	TBD	TBD
LTE-FDD B5	TBD	TBD
LTE-FDD B7	TBD	TBD
LTE-FDD B8	TBD	TBD
LTE-FDD B20	TBD	TBD
LTE-FDD B28	TBD	TBD
LTE-TDD B38	TBD	TBD
LTE-TDD B39	TBD	TBD
LTE-TDD B40	TBD	TBD
LTE-TDD B41	TBD	TBD

Table 45: SC200R-NA* RF Output Power

Frequency	Max.	Min.
WCDMA B2	24dBm+1/-3dB	<-49dBm
WCDMA B4	24dBm+1/-3dB	<-49dBm
WCDMA B5	24dBm+1/-3dB	<-49dBm
LTE-FDD B2	23dBm±2dB	<-39dBm
LTE-FDD B4	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B7	23dBm±2dB	<-39dBm
LTE-FDD B12	23dBm±2dB	<-39dBm
LTE-FDD B13	23dBm±2dB	<-39dBm
LTE-FDD B14	23dBm±2dB	<-39dBm
LTE-FDD B17	23dBm±2dB	<-39dBm
LTE-FDD B25	23dBm±2dB	<-39dBm
LTE-FDD B26	23dBm±2dB	<-39dBm
LTE-FDD B66	23dBm±2dB	<-39dBm
LTE-FDD B71	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

Table 46: SC200R-JP* RF Output Power

Frequency	Max.	Min.
WCDMA B1	TBD	TBD
WCDMA B6	TBD	TBD
WCDMA B8	TBD	TBD
WCDAM B19	TBD	TBD
LTE-FDD B1	TBD	TBD
LTE-FDD B3	TBD	TBD
LTE-FDD B5	TBD	TBD
LTE-FDD B8	TBD	TBD
LTE-FDD B11	TBD	TBD
LTE-FDD B18	TBD	TBD
LTE-FDD B19	TBD	TBD
LTE-FDD B21	TBD	TBD
LTE-FDD B26	TBD	TBD
LTE-FDD B28	TBD	TBD
LTE-TDD B41	TBD	TBD

NOTES

1. In GPRS 4 slots TX mode, the maximum output power is reduced by 3dB. This design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.
2. "*" means under development.

7.6. RF Receiving Sensitivity

The following table shows the RF receiving sensitivity of SC200R module.

Table 47: SC200R-CE RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
EGSM900	TBD	/	/	-102.4dBm
DCS1800	TBD	/	/	-102.4dBm
WCDMA B1	TBD	TBD	TBD	-106.7dBm
WCDMA B8	TBD	TBD	TBD	-103.7dBm
EVDO/CDMA BC0	TBD	/	/	-104dBm
LTE-FDD B1 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-FDD B3 (10M)	TBD	TBD	TBD	-93.3dBm
LTE-FDD B5 (10M)	TBD	TBD	TBD	-94.3dBm
LTE-FDD B8 (10M)	TBD	TBD	TBD	-93.3dBm
LTE-TDD B34 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-TDD B38 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-TDD B39 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-TDD B40 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-TDD B41 (10M)	TBD	TBD	TBD	-94.3dBm

Table 48: SC200R-EM RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	TBD	/	/	-102.4dBm
EGSM900	TBD	/	/	-102.4dBm
DCS1800	TBD	/	/	-102.4dBm
PCS1900	TBD	/	/	-102.4dBm
WCDMA B1	TBD	TBD	TBD	-106.7dBm
WCDMA B2	TBD	TBD	TBD	-104.7dBm
WCDMA B5	TBD	TBD	TBD	-104.7dBm
WCDMA B8	TBD	TBD	TBD	-103.7dBm
LTE-FDD B1 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-FDD B2 (10M)	TBD	TBD	TBD	-94.3dBm
LTE-FDD B3 (10M)	TBD	TBD	TBD	-93.3dBm
LTE-FDD B5 (10M)	TBD	TBD	TBD	-94.3dBm
LTE-FDD B7 (10M)	TBD	TBD	TBD	-94.3dBm
LTE-FDD B8 (10M)	TBD	TBD	TBD	-93.3dBm
LTE-FDD B20 (10M)	TBD	TBD	TBD	-93.3dBm
LTE-FDD B28(10M)	TBD	TBD	TBD	-94.8dBm
LTE-TDD B38 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-TDD B39 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-TDD B40 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-TDD B41 (10M)	TBD	TBD	TBD	-94.3dBm

Table 49: SC200-NA* RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B2	-110	-110	-111	-104.7dBm
WCDMA B4	-110.5	-110.5	-111	-106.7dBm
WCDMA B5	-111	-111	-111.5	-104.7dBm
LTE-FDD B2 (10M)	-98	-98	-100	-94.3dBm
LTE-FDD B4 (10M)	-98.5	-98	-101	-96.3dBm
LTE-FDD B5 (10M)	-99.5	-99.5	-102.5	-94.3dBm
LTE-FDD B7 (10M)	-96	-98	-100	-93.3dBm
LTE-FDD B12 (10M)	-97	-98	-100	-93.3dBm
LTE-FDD B13 (10M)	-99	-97	-101	-93.3dBm
LTE-FDD B14 (10M)	-98	-97	-100	-93.3dBm
LTE-FDD B17 (10M)	-96.5	-98	-100	-93.3dBm
LTE-FDD B25 (10M)	-97	-97	-100	-92.8dBm
LTE-FDD B26 (10M)	-99	-99	-102	-93.8dBm
LTE-FDD B66 (10M)	-98	-98	-101	-96.3dBm
LTE-FDD B71 (10M)	-97.5	-97	-100	-93.5dBm
LTE-TDD B41 (10M)	-98	-98	-101	-94.3dBm

Table 50: SC200-JP*RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B1	TBD	TBD	TBD	-102.4dBm
WCDMA B6	TBD	TBD	TBD	-102.4dBm
WCDMA B8	TBD	TBD	TBD	-106.7dBm
WCDAM B19	TBD	TBD	TBD	-103.7dBm
LTE-FDD B1 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-FDD B3 (10M)	TBD	TBD	TBD	-93.3dBm
LTE-FDD B5 (10M)	TBD	TBD	TBD	-94.3dBm
LTE-FDD B8 (10M)	TBD	TBD	TBD	-93.3dBm
LTE-FDD B11 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-FDD B18 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-FDD B19 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-FDD B21 (10M)	TBD	TBD	TBD	-96.3dBm
LTE-FDD B26 (10M)	TBD	TBD	TBD	-93.8dBm
LTE-FDD B28 (10M)	TBD	TBD	TBD	-94.8dBm
LTE-TDD B41 (10M)	TBD	TBD	TBD	-94.3dBm

NOTE

"*" means under development.

7.7. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it should be subject to ESD handling precautions that are typically applied to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the electrostatic discharge characteristics of SC200R module.

Table 51: ESD Characteristics (Temperature: 25 ºC, Humidity: 45%)

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	+/-5	+/-10	KV
All Antenna Interfaces	+/-5	+/-10	KV
Other Interfaces	+/-0.5	+/-1	KV

8 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the tolerances for dimensions without tolerance values are ±0.05 mm.

8.1. Mechanical Dimensions of the Module

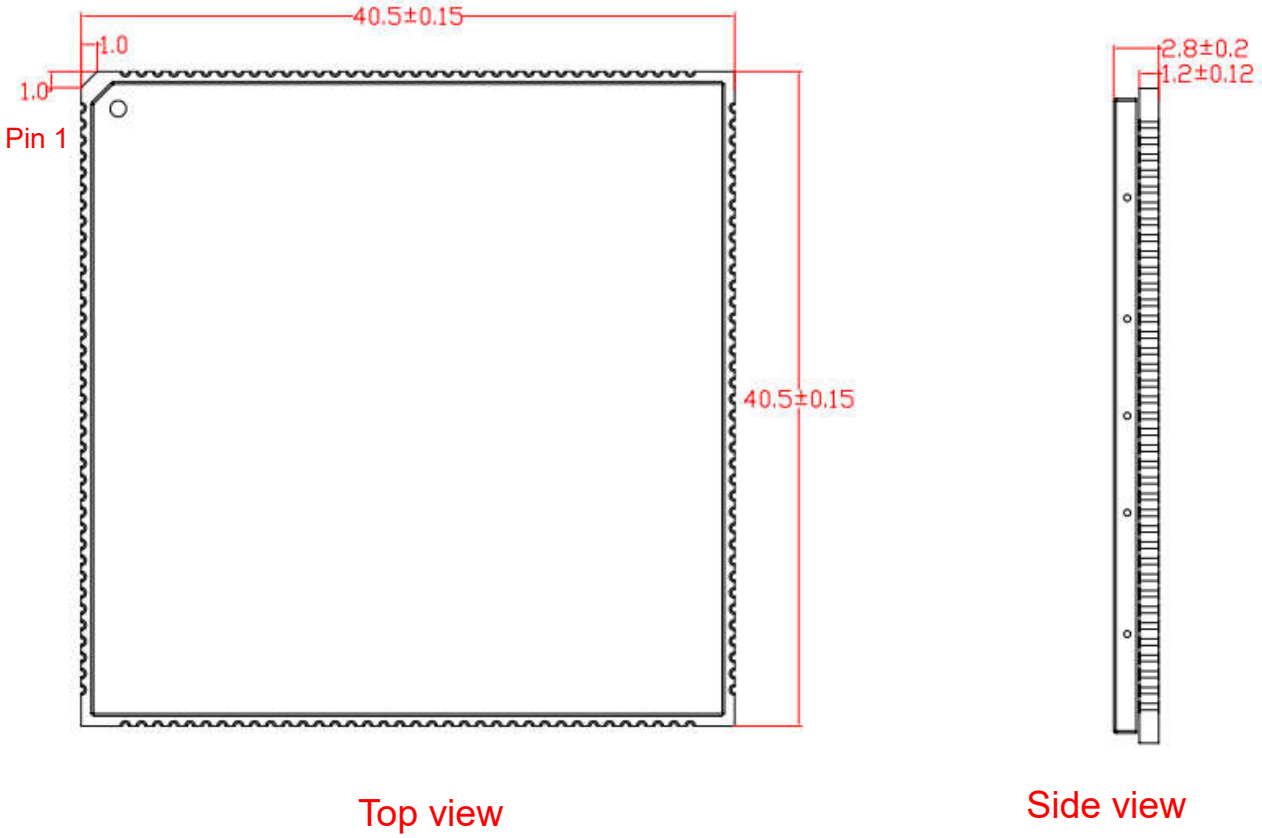


Figure 40: SC200R Module Top and Side Dimensions

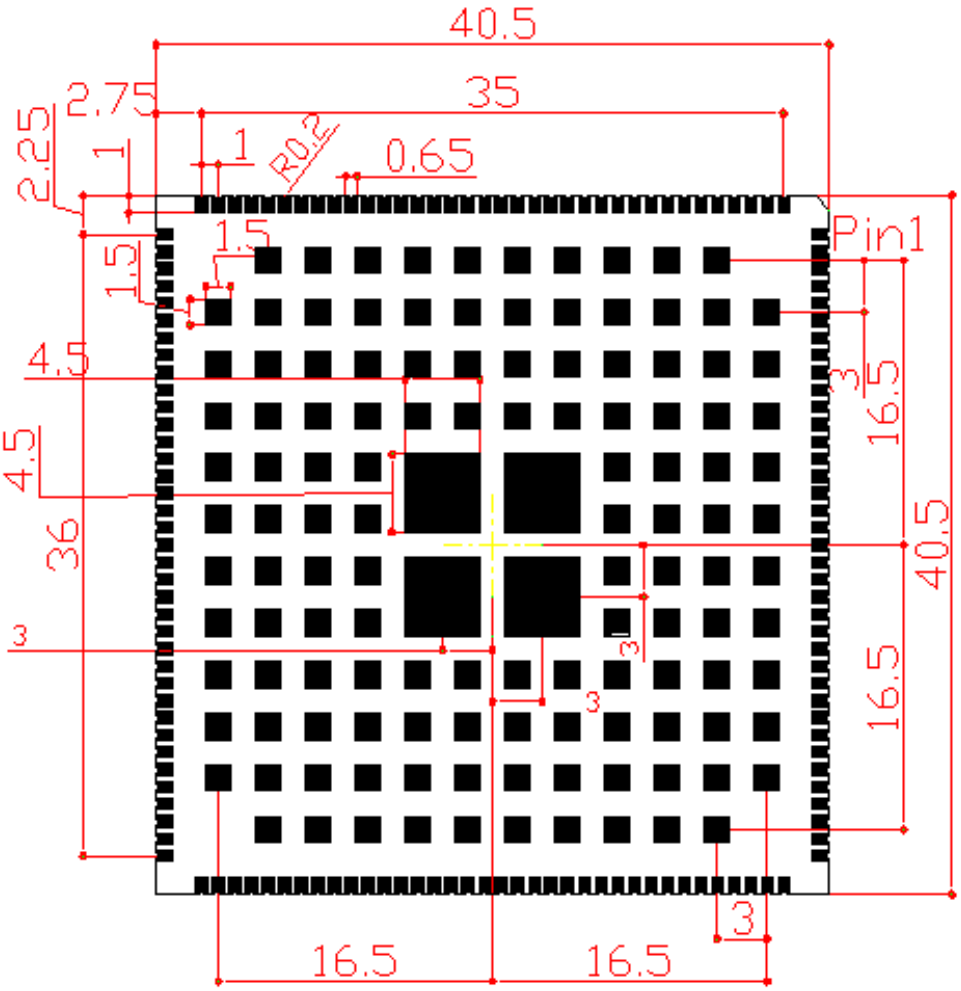


Figure 41: SC200R Module Bottom Dimensions (Top View)

8.2. Recommended Footprint

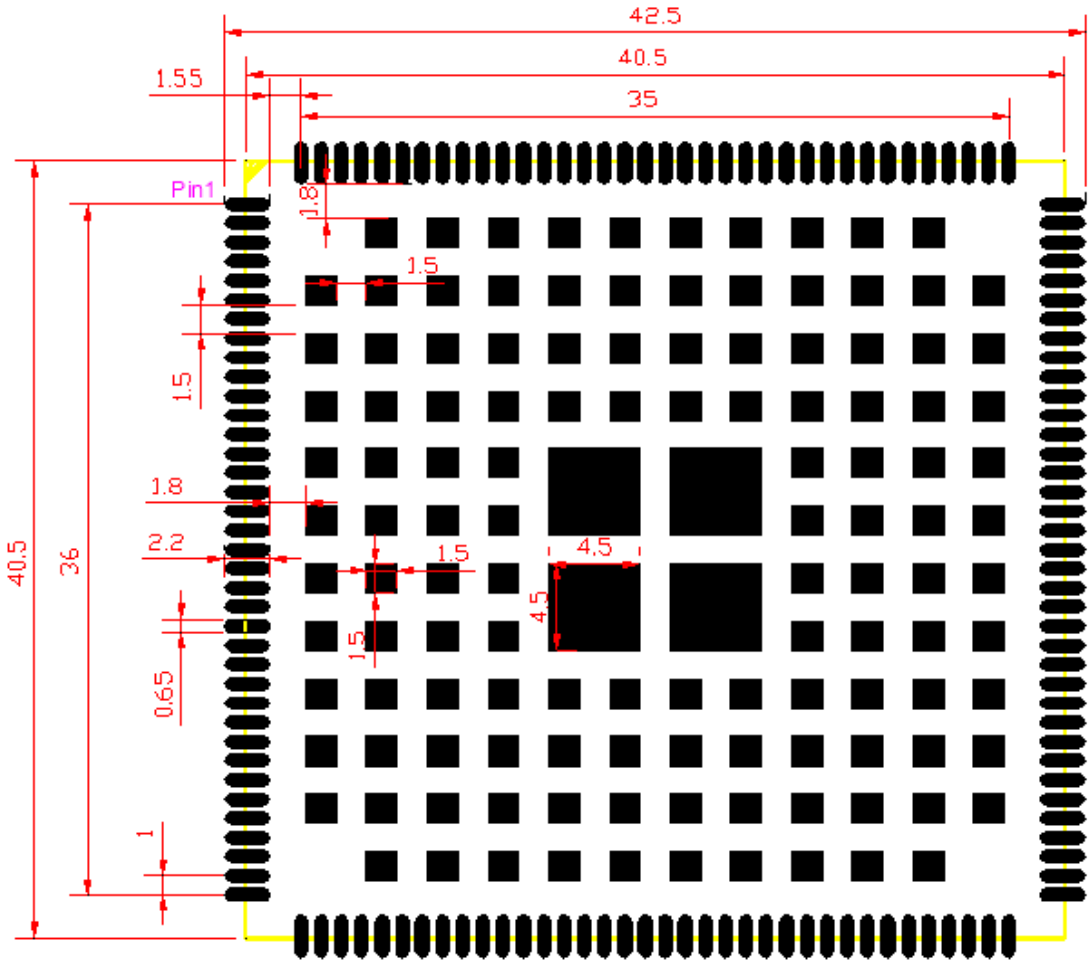


Figure 42: Recommended Footprint (Top View)

NOTES

1. For easy maintenance of the module, keep about 3 mm between the module and other components on the host PCB.
2. All RESERVED pins should be kept open and MUST NOT be connected to ground.

8.3. Top and Bottom Views of the Module

Figure 43: Top View of the Module

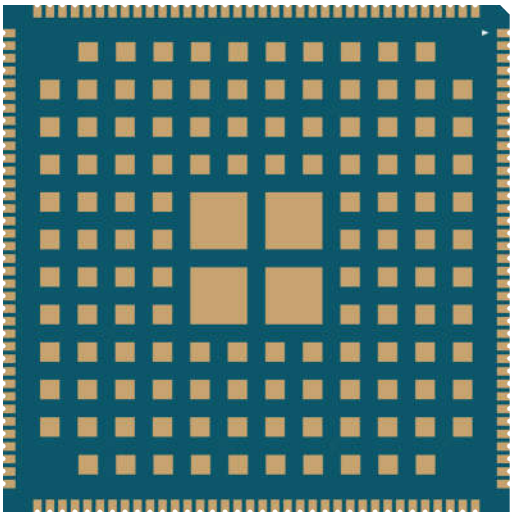


Figure 44: Bottom View of the Module

NOTE

These are renderings of SC200R module. For authentic dimension and appearance, please refer to the module that you receive from Quectel.

9 Storage, Manufacturing and Packaging

9.1. Storage

SC200R is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
   - Mounted within 168 hours at the factory environment of ≤30 ºC/60%RH.
   - Stored at <10%RH.

3. Devices require baking before mounting, if any circumstance below occurs.
   - When the ambient temperature is 23 ºC ±5 ºC and the humidity indication card shows the humidity is > 10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤ 30 ºC/60%RH.

4. If baking is required, devices may be baked for 8 hours at 120 °C ±5 °C.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devic es before high temperature (120 °C) baking. If shorter baking time is desired, please refer to *IPC /JEDECJ-STD-033* for the baking procedure.

9.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18 mm~0.20 mm. It is recommended to slightly reduce the amount of solder paste for LGA pads, thus avoiding short-circuit. For more details, please refer to ***document [4]***.

It is suggested that the peak reflow temperature is 238~245 ºC, and the absolute maximum reflow temperature is 245 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

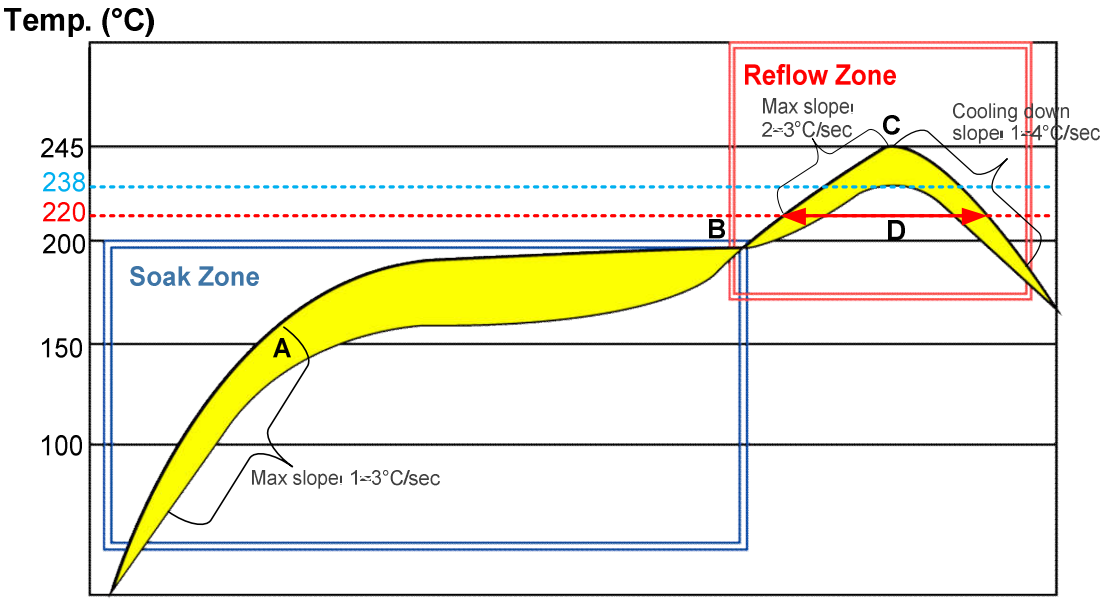


Figure 45: Recommended Reflow Soldering Thermal Profile

Table 52: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3 °C/sec

Soak time (between A and B: 150 °C and 200 °C)	60 to 120 sec
Reflow Zone	
Max slope	2 to 3 °C/sec
Reflow time (D: over 220 °C)	40 to 60 sec
Max temperature	238 °C ~ 245 °C
Cooling down slope	1 to 4 °C/sec
Reflow Cycle	
Max reflow cycle	1

9.3. Packaging

SC200R is packaged in tape and reel carriers, and sealed in the vacuum-sealed bag. It is not recommended to open the vacuum package before using the module for actual production. Each reel is 380 mm in diameter and contains 200 modules. The following figures show the package details, measured in mm.

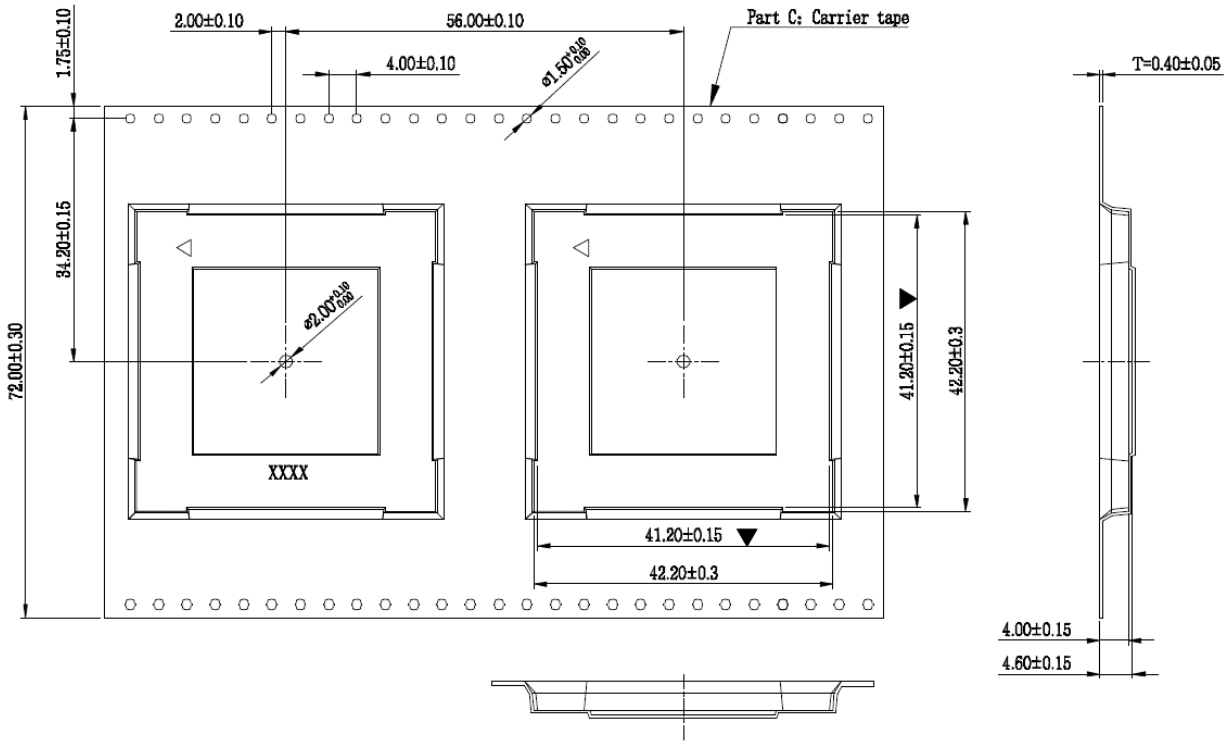


Figure 46: Tape Dimensions（Unit: mm）

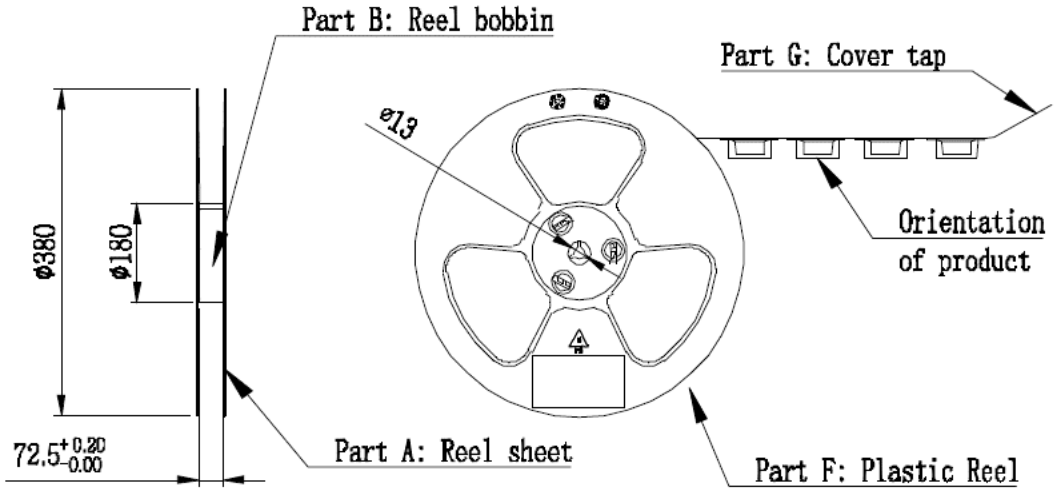


Figure 47: Reel Dimensions (Unit: mm)

Table 53: Reel Packaging

Model Name	MOQ for MP	Minimum Package: 200pcs	Minimum Package × 4=800pcs
SC200R	200	Size: 405 mm × 390 mm × 83 mm N.W: TBD G.W: TBD	Size: 425 mm × 358 mm × 410 mm N.W: TBD G.W: TBD

10 Appendix A References

Table 54: Related Documents

SN	Document Name	Remark
[1]	Quectel_Smart_EVB-G2_User_Guide	Smart EVB user guide
[2]	Quectel_SC200R_GPIO_Configuration	SC200R GPIO Configuration
[3]	Quectel_RF_Layout_Application_Note	RF layout application note
[4]	Quectel_Module_Secondary_SMT_User_Guide	Module secondary SMT user guide
[5]	Quectel_SC200R_Reference_Design	SC200R reference design

Table 55: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
CS	Coding Scheme
CTS	Clear to Send
DRX	Discontinuous Reception
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
GMSK	Gaussian Minimum Shift Keying
GPS	Global Positioning System
GPU	Graphics Processing Unit

GSM	Global System for Mobile Communications
HR	Half Rate
I/O	Input/Output
Imax	Maximum Load Current
Inorm	Normal Current
LCD	Liquid Crystal Display
LCM	LCD Module
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LRA	Linear Resonant Actuator
MIPI	Mobile Industry Processor Interface
MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RTC	Real Time Clock
Rx	Receive
SAW	Surface Acoustic Wave
SMS	Short Message Service
TDMA	Time Division Multiple Access

TE	Terminal Equipment
TX	Transmit
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_I	Voltage Input
$V_{IH}max$	Maximum Input High Level Voltage Value
$V_{IH}min$	Minimum Input High Level Voltage Value
$V_{IL}max$	Maximum Input Low Level Voltage Value
$V_{IL}min$	Minimum Input Low Level Voltage Value
V_Imax	Absolute Maximum Input Voltage Value
V_Imin	Absolute Minimum Input Voltage Value
V_O	Voltage Output
$V_{OH}max$	Maximum Output High Level Voltage Value
$V_{OH}min$	Minimum Output High Level Voltage Value
$V_{OL}max$	Maximum Output Low Level Voltage Value
$V_{OL}min$	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

11 Appendix B GPRS Coding Schemes

Table 56: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	C4-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

12 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 57: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA
14	4	4	NA

15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

13 Appendix D EDGE Modulation and Coding Schemes

Table 58: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps