SC66 Hardware Design

Smart LTE Module Series

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About the Document

History

Revision	Date	Author	Description
1.0	2019-03-08	Jian WU	Initial

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1 Introduction

This document defines the SC66 module and describes its air interface and hardware interface which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details as well as other related information of SC66 module. Associated with application note and user guide, customers can use SC66 module to design and set up mobile applications easily.

Hereby, [Quectel Wireless Solutions Co., Ltd.] declares that the radio equipment type [SC66-MW] is in compliance with Directive 2014/53/EU.
The full text of the EU declaration of conformity is available at the following internet address: http://www.quectel.com/support/technical.htm

The device is restricted to indoor use only when operating in the 5150 to 5350 MHz frequency range.

	AT	BE	BG	HR	CY	CZ	DK
	EE	FI	FR	DE	EL	HU	IE
	IT	LV	LT	LU	MT	NL	PL
	PT	RO	SK	SI	ES	SE	UK

The device could be used with a separation distance of 20cm to the human body.

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part
15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR201905SC66MW”
“Contains IC: 10224A-20195SC66MW “
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.
(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna type	2.4GHz band Peak Gain (dBi)	5.2GHz band Peak Gain (dBi)	5.3GHz band Peak Gain (dBi)	5.5GHz band Peak Gain (dBi)	5.8GHz band Peak Gain (dBi)
External antenna	5.38	4.48	4.48	5.05	4.54

In the event that these conditions cannot be met (for example certain laptop configurations or co-location

with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

The device could automatically discontinue transmission in case of absence of information to transmit, or operational failure. Note that this is not intended to prohibit transmission of control or signaling information or the use of repetitive codes where required by the technology.

The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;
The maximum antenna gain permitted for devices in the bands 5250–5350 MHz and 5470–5725 MHz shall comply with the e.i.r.p. limit; and
The maximum antenna gain permitted for devices in the band 5725–5825 MHz shall comply with the e.i.r.p. limits specified for point-to-point and non point-to-point operation as appropriate.

L'appareil peut interrompre automatiquement la transmission en cas d'absence d'informations à transmettre ou de panne opérationnelle. Notez que ceci n'est pas destiné à interdire la transmission d'informations de contrôle ou de signalisation ou l'utilisation de codes répétitifs lorsque cela est requis par la technologie.

Le dispositif utilisé dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur afin de réduire le risque de brouillage préjudiciable aux systèmes mobiles par satellite dans le même canal;
Le gain d'antenne maximal autorisé pour les dispositifs dans les bandes 5250-5350 MHz et 5470-5725 MHz doit être conforme à la norme e.r.p. limite; et
Le gain d'antenne maximal autorisé pour les appareils de la bande 5725-5825 MHz doit être conforme à la norme e.i.r.p. les limites spécifiées pour un fonctionnement point à point et non point à point, selon le cas.

CAN ICES-3(B)/ NMB-3(B)

Radiation Exposure Statement

This equipment complies with FCC/IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating SC66 module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

SC66 is a series of Smart LTE module based on Qualcomm platform and Android operating system, and provides industrial grade performance. Its general features are listed below:

- Support worldwide LTE-FDD, LTE-TDD, DC-HSDPA, DC-HSUPA, HSPA+, HSDPA, HSUPA, WCDMA, TD-SCDMA, EVDO/CDMA, EDGE and GPRS coverage
- Support short-range wireless communication via Wi-Fi 802.11a/b/g/n/ac and BT5.0 LE standards
- Integrate GPS/GLONASS/BeiDou satellite positioning systems
- Support multiple audio and video codecs
- Built-in high performance Adreno™ 512 graphics processing unit
- Provide multiple audio and video input/output interfaces as well as abundant GPIO interfaces

SC66 are available in six variants: SC66-MW*, SC66-CE*, SC66-A*, SC66-J*, SC66-E*, SC66-W*.

The following table shows the supported frequency bands of SC66.

Table 1: SC66-CE* Frequency Bands

Type	Frequency Bands
LTE-FDD	B1/B3/B5/B8
LTE-TDD	B34/B38/B39/B40/B41
WCDMA	B1/B8
TD-SCDMA	B34/B39
EVDO/CDMA	BC0
GSM	900/1800MHz
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz

BT5.0	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

Table 2: SC66-A* Frequency Bands

Type	Frequency Bands
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B66/B71
LTE-TDD	B41(200M)
WCDMA	B2/B4/B5
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz
BT 5.0	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

Table 3: SC66-J* Frequency Bands

Type	Frequency Bands
LTE-FDD	B1/B3/B5/B8/B11/B18/B19/B21/B26/B28(A+B)
LTE-TDD	B41(120M)
WCDMA	B1/B6/B8/B19
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz
BT 5.0	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

Table 4: SC66-E* Frequency Bands

Type	Frequency Bands
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B20/B28(A+B)
LTE-TDD	B38/B39/B40/B41(200M)
WCDMA	B1/B2/B4/B5/B8
GSM	B2/B3/B5/B8
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz
BT 5.0	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

Table 5: SC66-W* Frequency Bands

Type	Frequency Bands
LTE-FDD	/
LTE-TDD	/
WCDMA	/
TD-SCDMA	/
CDMA	/
GSM	/
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz
BT 5.0	2402MHz~2480MHz
GNSS	/

Table 6: SC66-MW*(2*2 MIMO WIFI) Frequency Bands

Type	Frequency Bands
LTE-FDD	/
LTE-TDD	/
WCDMA	/
TD-SCDMA	/
CDMA	/
GSM	/
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz
BT 5.0	2402MHz~2480MHz
GNSS	/

NOTE

"*" means under development. SC66-A、SC66-J、SC66-E、SC66-MW support WIFI_MIMO

SC66 is an SMD type module which can be embedded into applications through its 324 pins (including 152 LCC pads and 172 LGA pads). With a compact profile of 43.0mm × 44.0mm × 2.85mm, SC66 can meet almost all requirements for M2M applications such as smart metering, smart home, security, routers, wireless POS, mobile computing devices, PDA phone, tablet PC, etc.

2.2. Key Features

The following table describes the detailed features of SC66 module.

Table 7: SC66 Key Features

Features	Details
Application Processor	Customized 64-bit ARM v8-compliant applications processorCustomized 64-bit ARM v8-compliant applications processor ● Kryo Gold: quad high-performance cores targeting 2.2 GHz ● Kryo Silver: quad low-power cores targeting 1.843 GHz ● two quad-core processors with 1MB L2 cache
Modem system	LTE Cat 6(FDD and TDD), 2*20 CA(40MHz)
GPU	Adreno 512 up to 650 MHzAdreno 512 up to 650 MHz
Memory	32GB eMMC + 3GB LPDDR4x(default) 64GB eMMC + 4GB LPDDR4x (optional)
Operating System	Android 9
Power Supply	VBAT Supply Voltage: 3.55V~4.4V Typical 4.0V
Transmitting Power	Class 4 (33dBm±2dB) for EGSM900 Class 1 (30dBm±2dB) for DCS1800 Class E2 (27dBm±3dB) for EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (24dBm+3/-1dB) for EVDO/CDMA BC0 Class 2 (24dBm+1/-3dB) for TD-SCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands Class 3 (23dBm±2dB) for LTE-TDD bands
LTE Features	Support 3GPP R12 Cat 6* and Cat 4 Support 1.4 MHz to 20MHz RF bandwidth Support Multiuser MIMO in DL direction ● Cat 6* FDD: Max 300Mbps (DL)/Max 50Mbps (UL) ● Cat 6* TDD: Max 265Mbps (DL)/Max 30Mbps (UL) ● Cat 4 FDD: Max 150Mbps (DL)/Max 50Mbps (UL) ● Cat 4 TDD: Max 130Mbps (DL)/Max 30Mbps (UL)
UMTS Features	Support 3GPP R9 DC-HSDPA/DC-HSUPA/HSPA+/HSDPA/HSUPA/WCDMA Support QPSK, 16-QAM and 64-QAM modulation ● DC-HSDPA: Max 42Mbps (DL) ● DC-HSUPA: Max 11.2Mbps (UL)

	• WCDMA: Max 384Kbps (DL)/Max 384Kbps (UL)
TD-SCDMA Features	Support CCSA Release 3 TD-SCDMA • Max 4.2Mbps (DL)/Max 2.2Mbps (UL)
CDMA2000 Features	Support 3GPP2 CDMA2000 1X Advanced, CDMA2000 1x EV-DO Rev.A • EVDO: Max 3.1Mbps (DL)/Max 1.8 Mbps (UL) • 1X Advanced: Max 307.2Kbps (DL)/Max 307.2Kbps (UL)
GSM Features	**R99** CSD: 9.6kbps, 14.4kbps **GPRS** Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max 107Kbps (DL), 85.6Kbps (UL) **EDGE** Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max 296Kbps (DL), 236.8Kbps (UL)
WLAN Features	2.4GHz/5GHz, support 802.11a/b/g/n/ac, maximally up to 433Mbps Support AP and STA mode
Bluetooth Features	BT5.0 LE
GNSS Features	GPS/GLONASS/BeiDou
SMS	Text and PDU mode Point-to-point MO and MT SMS cell broadcast
LCM Interfaces	Support for MIPI_DSI and DP overTYPE-C for dual screen display MIPI_DSI Supports up to 2560x1600@60fps DP supports 4K@30fps
Camera Interfaces	Support three groups of 4-lane MIPI_CSI, up to 2.1Gbps per lane Support 3 cameras (4-lane + 4-lane + 4-lane) or 4 cameras (4-lane + 4-lane + 2-lane + 1-lane) up to 24MP with dual ISP
Video Codec	Video encoding and decoding: up to 4K @30fps Concurrency: encoding up to 1080P @30fps; decoding up to 1080P @60fps
Audio Interfaces	**Audio Input** Three analog microphone inputs, integrating internal bias voltage **Audio Output** Class AB stereo headphone output Class AB earpiece differential output Class D speaker differential amplifier output

Audio Codec	EVRC, EVRC-B, EVRC-WB; G.711, G.729A/AB; GSM-FR, GSM-EFR, GSM-HR; AMR-NB, AMR-WB, AMR-eAMR, AMR-BeAMR
USB Interface	Compliant with USB 3.1 and 2.0 specifications, with transmission rates up to 10Gbps on USB 3.1 and 480Mbps on USB 2.0. Support USB OTG Used for AT command communication, data transmission, software debugging and firmware upgrade
UART Interfaces	4 UART Interfaces: DEBUG UART、UART6、UART1 and LPI_UART_2 ● UART6: 4-wire UART interface with RTS/CTS hardware flow control, max rate up to 4Mbps ● UART1: terface ● DEBUG: 2-wire UART interface used for debugging ● LPI_UART_2:low power uart, use is not recommended for the time being
SD Card Interface	Support SD 3.0 Support SD card hot-plug
(U)SIM Interfaces	2 (U)SIM interfaces Support USIM/SIM card: 1.8V/2.95V Support Dual SIM Dual Standby (supported by default)
I2C Interfaces	It supports up to five I2C interfaces, used for peripherals such as TP, camera, sensor, etc.
I2S Interface	Supports two I2S, one of which is low power I2S
ADC Interfaces	2 general purpose ADC interfaces
SPI Interfaces	One SPI interfaces, only support master mode
Real Time Clock	Supported
Antenna Interfaces	Main antenna, Rx-diversity antenna, GNSS antenna and Wi-Fi/BT antenna interfaces
Physical Characteristics	Size: (43.0±0.15)mm × (44.0±0.15)mm × (2.85±0.2)mm Package: LCC + LGA Weight: approx. 13.0g
Temperature Range	Operating temperature range: -35°C ~ +65°C [1)] Extended temperature range: -40°C ~ +75°C [2)] Storage temperature range: -40°C ~ +90°C
Firmware Upgrade	Over USB interface
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

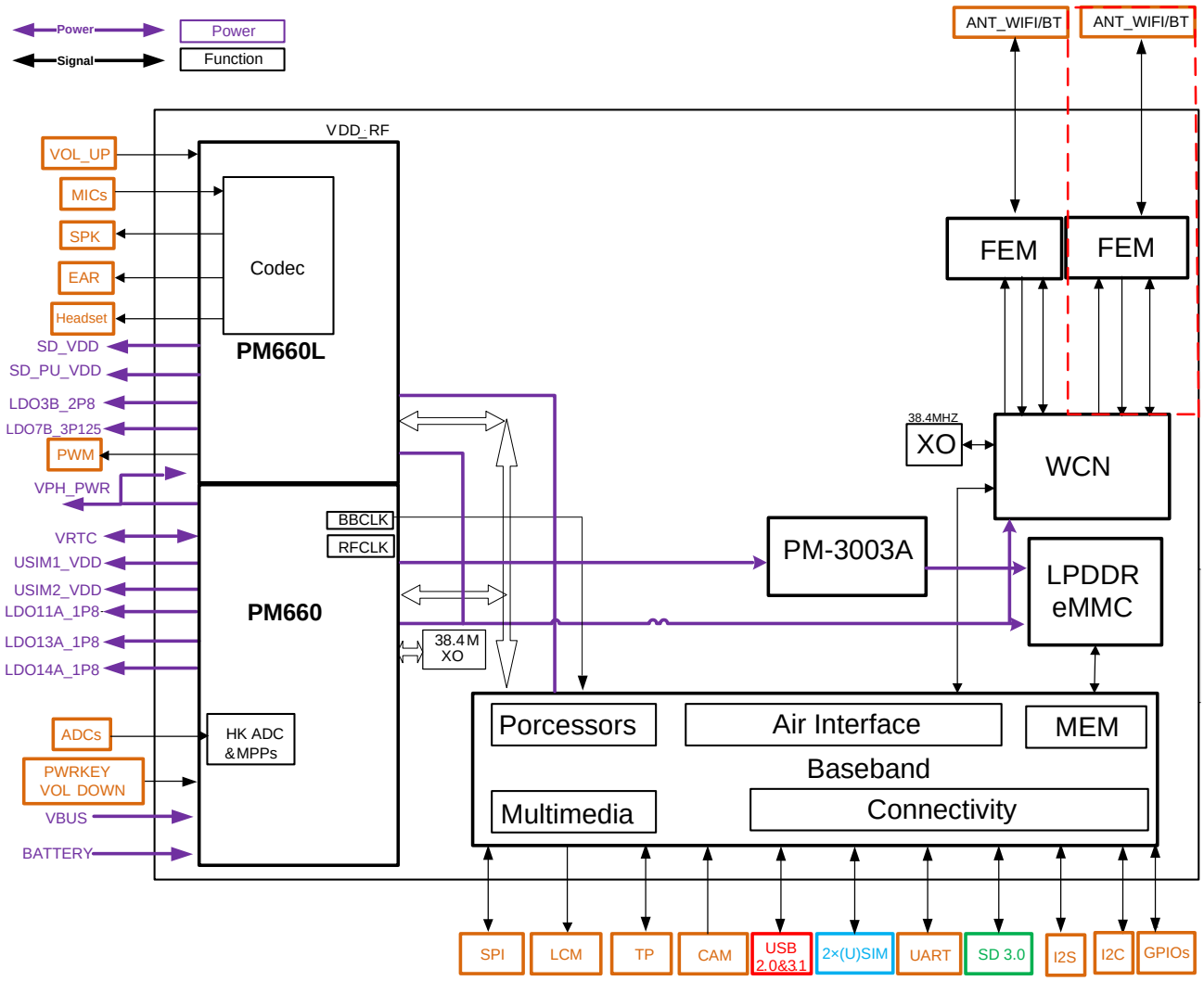
1. [1)] Within operation temperature range, the module is 3GPP compliant.

2. [2] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of SC66 and illustrates the major functional parts.

- Power management
- Radio frequency
- Baseband
- LPDDR4X+eMMC flash
- Peripheral interfaces
  -- USB interface
  -- (U)SIM interfaces
  -- UART interfaces
  -- SD card interface
  -- I2C interfaces
  - I2S interfaces
  -- SPI interfaces
  --ADC interfaces
  -- LCM (MIPI) interfaces
  -- TP (touch panel) interfaces
  -- Camera (MIPI) interfaces
  -- Audio interfaces



This diagram just used for SC66-MW

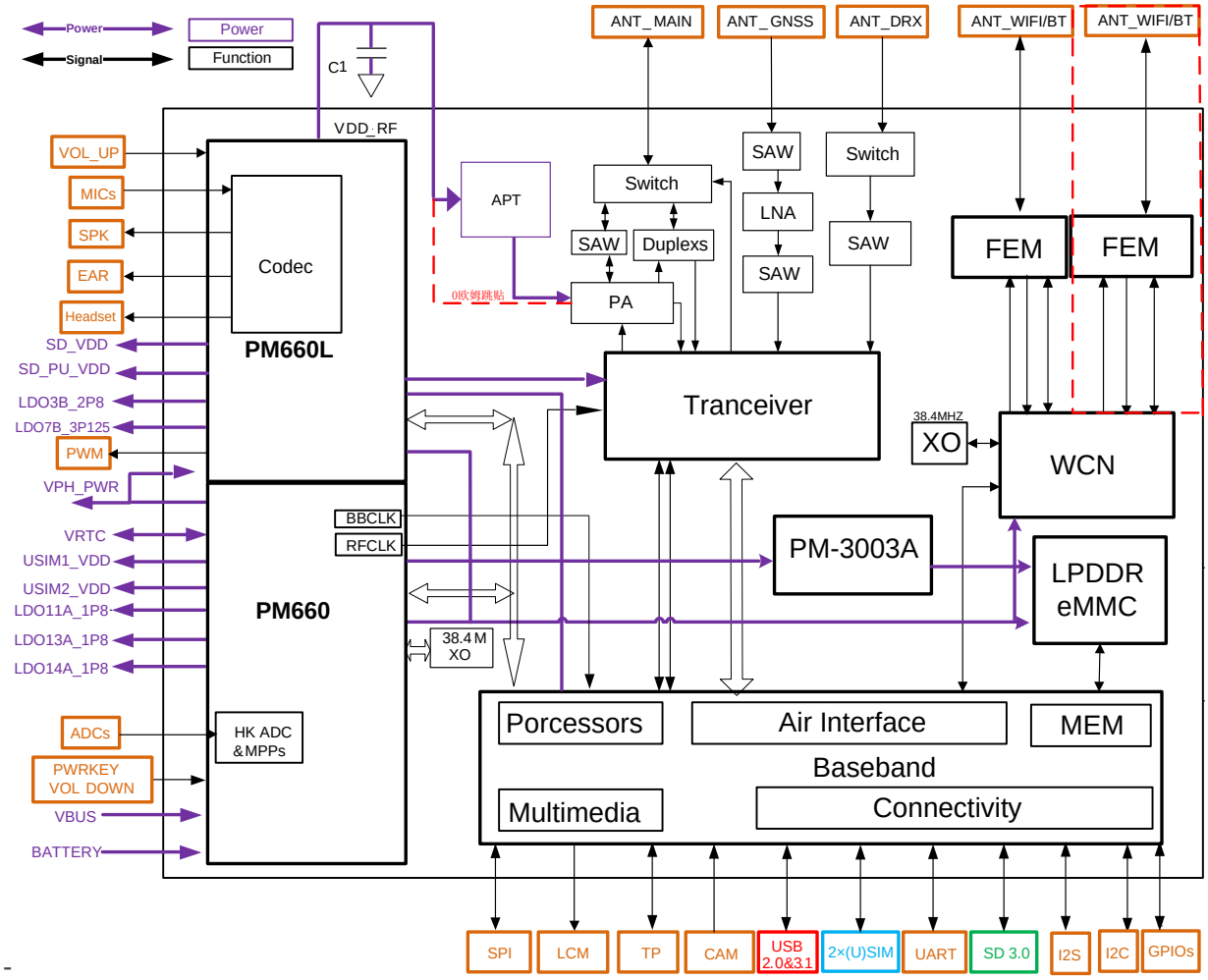


Figure 1: Functional Diagram

NOTE

The red dotted frame is WIFI_MIMO path, which is not supported by SC66-CE and SC66-W.

2.4. Evaluation Board

In order to help customers develop applications with SC66 conveniently, Quectel supplies the evaluation board, USB to RS232 converter cable, USB Type-C data cable, power adapter, earphone, antenna and other peripherals to control or test the module.

3 Application Interfaces

3.1. General Description

SC66 is equipped with 324-pin 1.0mm pitch SMT pads that can be embedded into cellular application platform. The following chapters provide the detailed description of pins/interfaces listed below.

- Power supply
- Turn on and off function
- VRTC interface
- Power Output
- Charging interface
- USB interface
- UART interfaces
- (U)SIM interfaces
- SD card interface
- GPIO interfaces
- I2C interfaces
- I2S interfaces
- SPI interfaces
- ADC interfaces
- LCM interfaces
- TP (touch panel) interfaces
- Camera interfaces
- Sensor interfaces
- Audio interfaces
- Emergency download interface

3.2. Pin Assignment

The following figure shows the pin assignment of SC66 module.

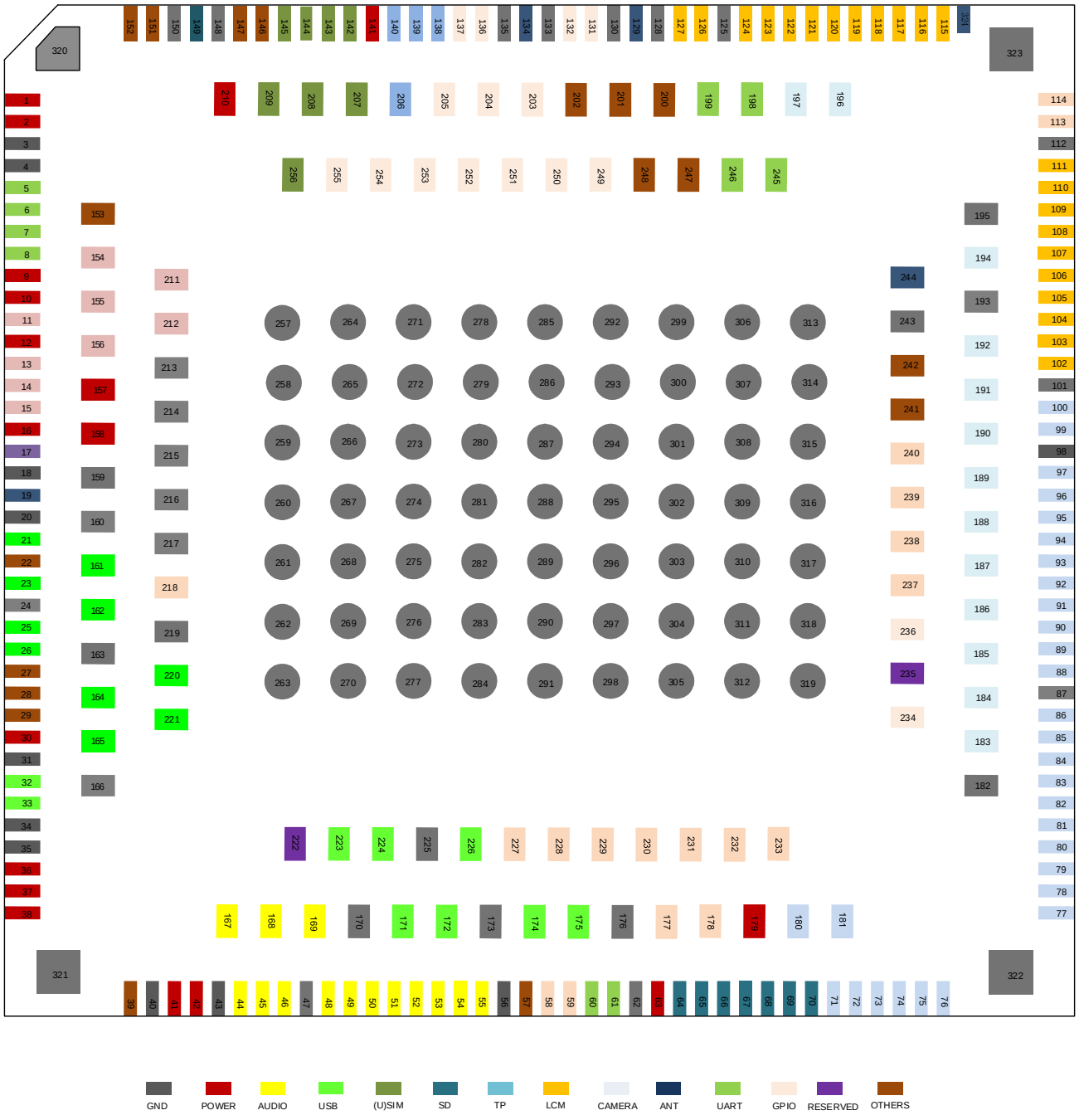


Figure 2: Pin Assignment (Top View)

3.3. Pin Description

Table 8: I/O Parameters Definition

Type	Description
IO	Bidirectional
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

The following tables show the SC66's pin definition and electrical characteristics.

Table 9: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	36,37, 38	PI/PO	Power supply for the module	Vmax=4.4V Vmin=3.55V Vnorm=4.0V	It must be able to provide sufficient current up to 3.0A. It is suggested to use a TVS to increase voltage surge withstand capability.
VDD_RF	1, 2	PO	Connect to external bypass capacitors to eliminate voltage fluctuation of RF part.	Vmax=4.4V Vmin=3.55V Vnorm=4.0V	Do not load externally.
VRTC	16	PI/P	Power supply for	$V_O$max=3.2V；	

		O	internal RTC circuit	When VBAT is not connected : V_I=2.1V~3.25V	
LDO13A_1P8	9	PO	1.8V output power supply	Vnorm=1.8V $I_O$max=20mA	Power supply for external GPIO's pull up circuits and level shift circuit.
LDO7B_3P125	157	PO	3.125V output power supply	Vnorm=3.125V $I_O$max=150mA	Power supply only for DP switch
LDO11A_1P8	10	PO	1.8V output power supply	Vnorm=1.8V $I_O$max=150mA	Power supply for I/O VDD of cameras, LCDs and TP etc.
LDO14A_1P8	158	PO	1.8V output power supply	Vnorm=1.8V $I_O$max=150mA	Power supply for Sensors. Add a 1.0uF~4.7uF bypass capacitor if used. If unused, keep this pin open.
LDO3B_2P8	12	PO	2.8V output power supply	Vnorm=2.8V $I_O$max=600mA	Power supply for sensor and LCM. Add a 1.0uF~2.2uF bypass capacitor if used. If unused, keep this pin open.
VPH_PWR	30	PO	VBAT output power supply	Vnorm=VBAT $I_O$max=1000mA	Power supply for other ICs.ICs
GND	3，4，18，20，24，31，34，35，40，		Ground		

	43 , 47 , 56 , 62 , 87 , 98 , 101 , 112 , 125 , 128 , 130 , 133 , 135 , 148 , 150 , 159 , 160 , 163 , 166 , 170 , 173 , 176 , 182 , 193 , 195 , 219 , 225 , 243 , 257~323				
Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_BIAS	167	AO	Microphone bias voltage	V_O=1.6V~2.9V	
MIC1_P	44	AI	Microphone positive input for channel 1		
MIC1_M	45	AI	Microphone negative input for channel 1		
MIC_GND	168		Microphone reference ground		If unused, it should be connected to GND
MIC2_P	46	AI	Microphone		Headset mic input

			positive input for headset		
MIC3_P	169	AI	Microphone positive input for second mic		Second mic input
EAR_P	53	AO	Earpiece positive output		
EAR_M	52	AO	Earpiece negative output		
SPK_P	55	AO	Speaker positive output		
SPK_M	54	AO	Speaker negative output		
HPH_R	51	AO	Headphone right channel output		
HPH_REF	50	AI	Headphone reference ground		It should be connected to main GND
HPH_L	49	AO	Headphone left channel output		
HS_DET	48	AI	Headset insertion detection		Default high level
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	41, 42	PI/PO	Charging power input. Power supply output for OTG device. USB/charger insertion detection.	Vmax=10V Vmin=3.6V Vnorm=5.0V	
USB2_HS_DM	25	IO	USB 2.0 differential data bus (minus)	USB 2.0 standard compliant	90Ω differential impedance.
USB2_HS_DP	26	IO	USB 2.0 differential data bus (plus)		
USB1_HS_DM	33	IO	USB 2.0 differential data bus (minus)	USB 2.0 standard compliant	90Ω differential impedance; One part of the

USB1_HS_DP	32	IO	USB 2.0 differential data bus (plus)		TYPE-C.
USB_SS2_TX_P	165	IO	USB 3.1 differential transmit (plus)	USB 3.1 channel2 standard compliant	90Ω differential impedance.
USB_SS2_TX_M	164	IO	USB 3.1 differential transmit (minus)		
USB_SS2_RX_P	162	IO	USB 3.1 differential receive (plus)		
USB_SS2_RX_M	161	IO	USB 3.1 differential receive (minus)		
USB_SS1_RX_P	171	IO	USB 3.1 differential receive (plus)	USB 3.1 channel1 standard compliant	90Ω differential impedance.
USB_SS1_RX_M	172	IO	USB 3.1 differential receive (minus)		
USB_SS1_TX _P	174	IO	USB 3.1 differential transmit (plus)		90Ω differential impedance.
USB_SS1_TX _M	175	IO	USB 3.1 differential transmit (minus)		
USB_CC1	224	AI	USB Type-C detection channel 1		When micro usb is used ,it can be used as ID pin
USB_CC2	223	AI	USB Type-C detection channel 2		
UUSB_TYPEC	23	DI	TYPE-C&uUSB configuration control pin		When USB TYPE-C is used, it should be connected to VPH_PWR through 10K resistor. When uUSB is used, it should be connected to GND

					through 10K resistor.
SS_DIR_IN	21	DI	CC status detection pin		When USB TYPE-C is used, it should be connected to SS_DIR_OUT. When uUSB is used, it should be connected to GND.
SS_DIR_OUT	226	DO	CC status output pin		When USB TYPE-C is used, it should be connected to SS_DIR_IN. When uUSB is used, it should be kept open.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_DET	145	DI	(U)SIM1 card hot-plug detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active Low. Require external pull-up to 1.8V. If unused, keep this pin open.
USIM1_RST	144	DO	(U)SIM1 card reset signal	V_{OL}max=0.4V V_{OH}min= 0.8 × USIM1_VDD	
USIM1_CLK	143	DO	(U)SIM1 card clock signal		
USIM1_DATA	142	IO	(U)SIM1 card data signal	V_{IL}max= 0.2 × USIM1_VDD V_{IH}min= 0.7 × USIM1_VDD V_{OL}max=0.4V V_{OH}min= 0.8 × USIM1_VDD	
USIM1_VDD	141	PO	(U)SIM1 card power supply		Either 1.8V or 2.95V (U)SIM card is supported.
USIM2_DET	256	DI	(U)SIM2 card detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active Low. Need external

					pull-up to 1.8V. If unused, keep this pin open.
USIM2_RST	207	DO	(U)SIM2 card reset signal	V_{OL}max=0.4V V_{OH}min= 0.8 × USIM2_VDD	
USIM2_CLK	208	DO	(U)SIM2 card clock signal	V_{OL}max=0.4V V_{OH}min= 0.8 × USIM2_VDD	
USIM2_DATA	209	IO	(U)SIM2 card data signal	V_{IL}max= 0.2 × USIM2_VDD V_{IH}min= 0.7 × USIM2_VDD V_{OL}max=0.4V V_{OH}min= 0.8 × USIM2_VDD	
USIM2_VDD	210	PO	(U)SIM2 card power supply		Either 1.8V or 2.95V (U)SIM card is supported.
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DEBUG_TXD	5	DO	DEBUG transmit data. Debug port by default.	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep these pins open.
DEBUG_RXD	6	DI	DEBUG receive data. Debug port by default.	V_{IL}max=0.63V V_{IH}min=1.17V	
UART1_TXD	7	DO	UART1 transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	
UART1_RXD	8	DI	UART1 receive data	V_{IL}max=0.63V V_{IH}min=1.17V	
UART6_RXD	198	DI	UART6 receive data	V_{IL}max=0.63V V_{IH}min=1.17V	
UART6_TXD	199	DO	UART6 transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	
UART6_RTS	245	DO	UART6 request to send	V_{OL}max=0.45V V_{OH}min=1.35V	
UART6_CTS	246	DI	UART6 clear to send	V_{IL}max=0.63V V_{IH}min=1.17V	

LPI_UART_2_TXD	60	DO	UART2 transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	
LPI_UART_2_RXD	61	DI	UART2 receive data	V_{IL}max=0.63V V_{IH}min=1.17V	
SD Card Interface					
Pin Name	**Pin N.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	70	DO	High speed digital clock signal of SD card	**1.8V SD card:** V_{OL}max=0.45V V_{OH}min=1.4V **2.95V SD card:** V_{OL}max=0.368V V_{OH}min=2.125V	
SD_CMD	69	IO	Command signal of SD card		
SD_DATA0	68	IO	High speed bidirectional digital signal lines of SD card	**1.8V SD card:** V_{IL}max=0.58V V_{IH}min=1.27V V_{OL}max=0.45V V_{OH}min=1.4V **2.95V SD card:** V_{IL}max=0.737V V_{IH}min=1.843V V_{OL}max=0.368V V_{OH}min=2.125V	
SD_DATA1	67	IO			
SD_DATA2	66	IO			
SD_DATA3	65	IO			
SD_DET	64	DI	SD card insertion detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active low.
SD_VDD	63	PO	Power supply for SD card	Vnorm=2.95V $I_O$max=600mA	
SD_PU_VDD	179	PO	2.95V output	Vnorm=1.8V/2.95V $I_O$max=50mA	Power supply for SD card's pull-up circuit.
TP (Touch Panel) Interfaces					
Pin Name	**Pin N**	**I/O**	**Description**	**DC Characteristics**	**Comment**

TP0_RST	138	DO	Reset signal of touch panel (TP0)	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active low.
TP0_INT	139	DI	Interrupt signal of touch panel (TP0)	V_{IL}max=0.63V V_{IH}min=1.17V	1.8V power domain.
TP0_I2C_SCL	140	OD	I2C clock signal of touch panel (TP0)		1.8V power domain.
TP0_I2C_SDA	206	OD	I2C data signal of touch panel (TP0)		1.8V power domain.
LCM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWM	152	DO	PWM Output		
LCD0_RST	127	DO	LCD0 reset signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain It should not be pulled up.
LCD0_TE	126	DI	LCD0 tearing effect signal	V_{IL}max=0.63V V_{IH}min=1.17V	1.8V power domain.
DSI0_CLK_N	116	AO	LCD0 MIPI clock signal (negative)		85Ω differential impedance.
DSI0_CLK_P	115	AO	LCD0 MIPI clock signal (positive)		
DSI0_LN0_N	118	AO	LCD0 MIPI lane 0 data signal (negative)		85Ω differential impedance.
DSI0_LN0_P	117	AO	LCD0 MIPI lane 0 data signal (positive)		
DSI0_LN1_N	120	AO	LCD0 MIPI lane 1 data signal (negative)		85Ω differential impedance.
DSI0_LN1_P	119	AO	LCD0 MIPI lane 1 data signal (positive)		
DSI0_LN2_N	122	AO	LCD0 MIPI lane 2 data signal (negative)		85Ω differential impedance.
DSI0_LN2_P	121	AO	LCD0 MIPI lane 2 data signal (positive)		
DSI0_LN3_N	124	AO	LCD0 MIPI lane 3 data signal (negative)		85Ω differential impedance.
DSI0_LN3_P	123	AO	LCD0 MIPI lane 3 data signal (positive)		
Camera Interfaces					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
CSI1_CLK_N	89	AI	MIPI clock signal of rear camera (negative)		85Ω differential impedance.
CSI1_CLK_P	88	AI	MIPI clock signal of rear camera (positive)		
CSI1_LN0_N	91	AI	MIPI lane 0 data signal of rear camera (negative)		85Ω differential impedance.
CSI1_LN0_P	90	AI	MIPI lane 0 data signal of rear camera (positive)		
CSI1_LN1_N	93	AI	MIPI lane 1 data signal of rear camera (negative)		85Ω differential impedance.
CSI1_LN1_P	92	AI	MIPI lane 1 data signal of rear camera (positive)		
CSI1_LN2_N	95	AI	MIPI lane 2 data signal of rear camera (negative)		85Ω differential impedance.
CSI1_LN2_P	94	AI	MIPI lane 2 data signal of rear camera (positive)		
CSI1_LN3_N	97	AI	MIPI lane 3 data signal of rear camera (negative)		85Ω differential impedance.
CSI1_LN3_P	96	AI	MIPI lane 3 data signal of rear camera (positive)		
CSI2_CLK_N	184	AI	MIPI clock signal of depth camera (negative)		85Ω differential impedance.
CSI2_CLK_P	183	AI	MIPI clock signal of depth camera (positive)		
CSI2_LN0_N	186	AI	MIPI lane 0 data signal of depth camera (negative)		85Ω differential impedance.
CSI2_LN0_P	185	AI	MIPI lane 0 data signal of depth camera (positive)		
CSI2_LN1_N	188	AI	MIPI lane 1 data signal of depth camera (negative)		85Ω differential impedance.
CSI2_LN1_P	187	AI	MIPI lane 1 data signal of depth camera (positive)		
CSI2_LN2_N	190	AI	MIPI lane 2 data signal of depth camera (negative)		85Ω differential impedance.
CSI2_LN2_P	189	AI	MIPI lane 2 data signal of depth camera (positive)		
CSI2_LN3_N	192	AI	MIPI lane 3 data signal of depth camera (negative)		85Ω differential impedance.
CSI2_LN3_P	191	AI	MIPI lane 3 data signal of depth camera (positive)		

CSI0_CLK_N	78	AI	MIPI clock signal of front camera (negative)		85Ω differential impedance.
CSI0_CLK_P	77	AI	MIPI clock signal of front camera (positive)		
CSI0_LN0_N	80	AI	MIPI lane 0 data signal of front camera (negative)		85Ω differential impedance.
CSI0_LN0_P	79	AI	MIPI lane 0 data signal of front camera (positive)		
CSI0_LN1_N	82	AI	MIPI lane 1 data signal of front camera (negative)		85Ω differential impedance.
CSI0_LN1_P	81	AI	MIPI lane 1 data signal of front camera (positive)		
CSI0_LN2_N	84	AI	MIPI lane 2 data signal of front camera (negative)		85Ω differential impedance.
CSI0_LN2_P	83	AI	MIPI lane 2 data signal of front camera (positive)		
CSI0_LN3_N	86	AI	MIPI lane 3 data signal of front camera (negative)		85Ω differential impedance.
CSI0_LN3_P	85	AI	MIPI lane 3 data signal of front camera (positive)		
MCAM_MCLK	99	DO	Master clock signal of rear camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
SCAM_MCLK	100	DO	Master clock signal of front camera		1.8V power domain.
MCAM_RST	74	DO	Reset signal of rear camera		1.8V power domain.
MCAM_PWDN	73	DO	Power down signal of rear camera		1.8V power domain.
SCAM_RST	72	DO	Reset signal of front camera		1.8V power domain.
SCAM_PWDN	71	DO	Power down signal of front camera		1.8V power domain.
CAM_I2C_SCL0	75	OD	I2C clock signal of camera		1.8V power domain.
CAM_I2C_SDA0	76	OD	I2C data signal of camera		1.8V power domain.
DCAM_MCLK	194	DO	Master clock signal of depth camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain

DCAM_RST	180	DO	Reset signal of depth camera		1.8V power domain
DCAM_PWDN	181	DO	Power down signal of depth camera		1.8V power domain
CAM_I2C_SDA1	197	OD	I2C data signal of depth camera		1.8V power domain
CAM_I2C_SCL1	196	OD	I2C data signal of depth camera		1.8V power domain.
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	39	DI	Turn on/off the module		1.8V power domain
VOL_UP	146	DI	Volume up		The voltage follows VBAT
VOL_DWN	147	DI	Volume down		1.8V power domain
SENSOR_I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SENSOR_I2C_SCL	131	OD	I2C clock signal of external sensors		1.8V power domain.
SENSOR_I2C_SDA	132	OD	I2C data signal of external sensors		1.8V power domain.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	151	AI			Max input voltage:1.8V
ADC1	153	AI			Max input voltage:1.8V
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	19	IO	Main antenna interface		50Ω impedance

ANT_DRX	149	AI	Diversity antenna interface		
ANT_GNSS	134	AI	GNSS antenna interface		
ANT_WIFI/BT	129	IO	Wi-Fi/BT antenna interface		
ANT_WIFI_MIMO	324	IO	Wi-Fi_MIMO antenna interface		SC66-CE、SC66-W is not supported
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_20	113	IO	GPIO		Can be used as LCD1_RST
GPIO_21	231	IO	GPIO		
GPIO_34	236	IO	GPIO		
GPIO_40	238	IO	GPIO		
GPIO_41	237	IO	GPIO		
GPIO_42	137	IO	GPIO		Can be used as TP1_INT
GPIO_43	136	IO	GPIO		Can be used as TP1_RST
GPIO_55	178	IO	GPIO	V_{IL}max=0.63V V_{IH}min=1.17V V_{OL}max=0.45V V_{OL}min=1.35V	
GPIO_56	177	IO	GPIO		
GPIO_72	239	IO	GPIO		
GPIO_73	59	IO	GPIO		
GPIO_74	58	IO	GPIO		
GPIO_76	232	IO	GPIO		
GPIO_77	240	IO	GPIO		
ACCL_INT	252	IO	GPIO		
GYRO_INT	255	IO	GPIO		
MAG_INT	254	IO	GPIO		
ALPS_INT	253	IO	GPIO		

HALL_INT	218	IO	GPIO		
GPIO_22	204	IO	GPIO		
GPIO_23	205	IO	GPIO		
GPIO_12	228	IO	GPIO		
GPIO_13	227	IO	GPIO		
GPIO_14	230	IO	GPIO		
GPIO_15	229	IO	GPIO		
GPIO_61	234	IO	GPIO		
GPIO_03B	11	IO	GPIO		
GPIO_08B	13	IO	GPIO		
GPIO_04B	14	IO	GPIO		
GPIO_05B	15	IO	GPIO		
GPIO_11A	211	IO	GPIO		
GPIO_13A	233	IO	GPIO		
GRFC Interfaces					
Pin Name	**Pin No.**		**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC_19	242		IO	GPIO		Only for RF debug. It should not be pulled up.
GRFC_18	241		IO	GPIO		
SPI Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	201	DO	Chip selection signal		Only support master mode
SPI_CLK	200	DO	Clock signal		
SPI_MOSI	248	DO	Data output signal		
SPI_MISO	247	DI	Data input signal		
I2S Interfaces					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MI2S_2_WS	203	DO	I2S Word selection signal		
MI2S_2_DATA0	249	IO	I2S DATA0 signal		
MI2S_2_SCK	250	DO	I2S Serial clock signal		
MI2S_2_DATA1	251	IO	I2S DATA1 signal		
MI2S_2_MCLK	114	DO	I2S Main clock signal		
LPI_MI2S_SCLK	212	DO	LPI_I2S serial clock signal		
LPI_MI2S_WS	156	DO	LPI_I2S word selection signal		
LPI_MI2S_DATA0	154	IO	LPI_I2S DATA0 signal		
LPI_MI2S_DATA1	155	IO	LPI_I2S DATA1 signal		
Emergency Download Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	57	DI	Force the module to enter into emergency download mode		Pulled up to LDO13A_1P8 during power-up will force the module to enter into emergency download mode.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GNSS_PPS_OUT	202	DO	LNA enable control		LNA enable control
CBL_PWR_N	22	DI	Used for configuring auto power-on		If customers require automatic power-on, this pin should be shorted-to-ground.
Reserved Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RESERVED	17,213，214，215，216，217，222，235		Reserved pins		Keep these pins open.

3.4. Power Supply

3.4.1. Power Supply Pins

SC66 provides three VBAT pins、VDD_RF pins and one VPH_PWR pin. VBAT pins are dedicated for connection with an external power supply. VDD_RF pins are designed for module's RF part, and are used to connect bypass capacitors so as to eliminate voltage fluctuation of RF part, VPH_PWR is used for powering other devices.

3.4.2. Decrease Voltage Drop

The power supply range of the module is from 3.55V to 4.4V, and the recommended value is 4.0V. The power supply performance, such as load capacity, voltage ripple, etc. directly influences the module's performance and stability. Under ultimate conditions, the module may have a transient peak current up to 3A. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 3.55V, the module will be powered off automatically. Therefore, please make sure the input voltage will never drop below 3.55V.

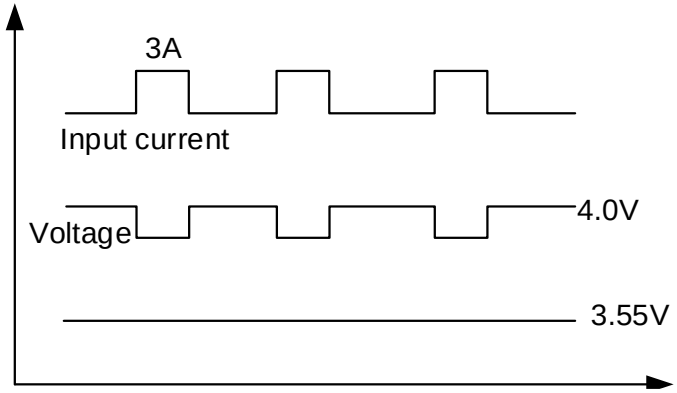


Figure 3: Voltage Drop Sample

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR (ESR=0.7Ω) should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to VBAT/VDD_RF pins. The width of VBAT trace should be no less than 3mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested to use a 0.5W TVS and place it as close to the VBAT pins as possible to increase voltage surge withstand capability. The following figure shows the structure of the power supply.

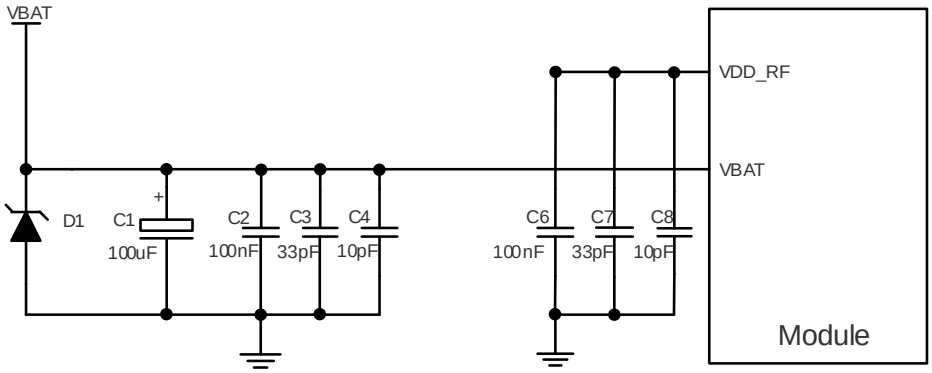


Figure 4: Structure of Power Supply

3.4.3. Reference Design for Power Supply

The power design for the module is very important, as the performance of module largely depends on the power source. The power supply of SC66 should be able to provide sufficient current up to 3A at least. By default, it is recommended to use a battery to supply power for SC66. But if battery is not intended to be used, it is recommended to use a regulator for SC66. If the voltage difference between the input and output is not too high, it is suggested to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source which adopts an LDO (MIC29502WU) from MICROCHIP. The typical output voltage is 4.0V and the maximum rated current is 5.0A.

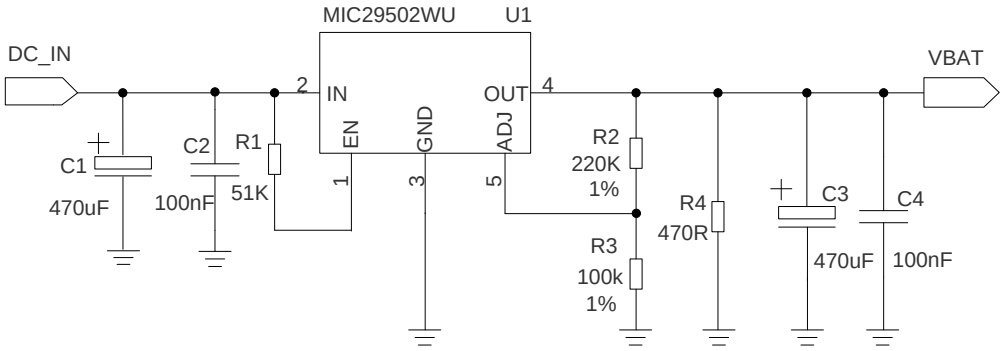


Figure 5: Reference Circuit of Power Supply

NOTES

1. It is recommended to switch off the power supply for module in abnormal state, and then switch on the power to restart the module.
2. The module supports battery charging function by default. If the above power supply design is adopted, please make sure the charging function is disabled by software, or connect VBAT to Schottky diode in series to avoid the reverse current to the power supply chip.
3. When the battery power is reduced to 0%, the system will trigger automatic shutdown, so the design of power supply should be consistent with the configuration of fuel gauge driver.

3.5. Turn on and off Scenarios

3.5.1. Turn on Module Using the PWRKEY

The module can be turned on by driving PWRKEY pin to a low level for at least 1.6s. PWRKEY pin is pulled to 1.8V internally. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

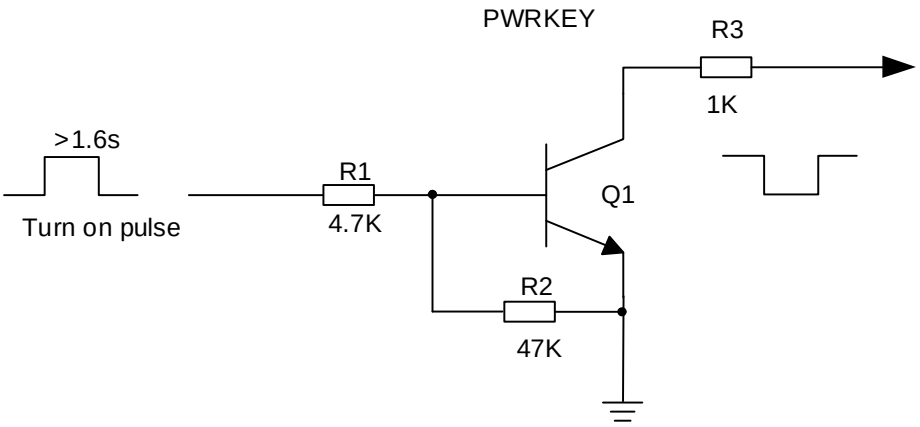


Figure 6: Turn on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. A TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

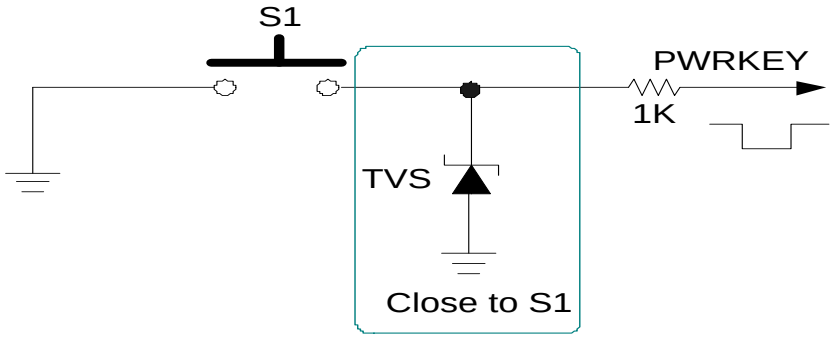


Figure 7: Turn on the Module Using Keystroke

In addition, when VBAT is powered on, the module will be powered on automatically. The reference circuit is shown below:

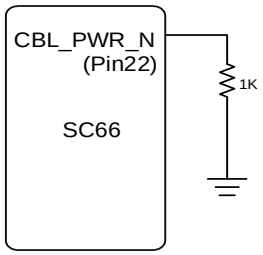


Figure 8: Automatic Boot Reference Circuit

NOTE

Make sure that VBAT is stable before pulling down PWRKEY pin. The recommended time between them is no less than 30ms. PWRKEY cannot be pulled down all the time.

3.5.2. Restart the Module

Pull down PWRKEY for at least 1s, and then choose to turn off or restart the module when the prompt window comes up.

Another way to Restart the module is to drive PWRKEY to a low level for at least 8s. The module will execute Restart. The restart scenario is illustrated in the following figure.

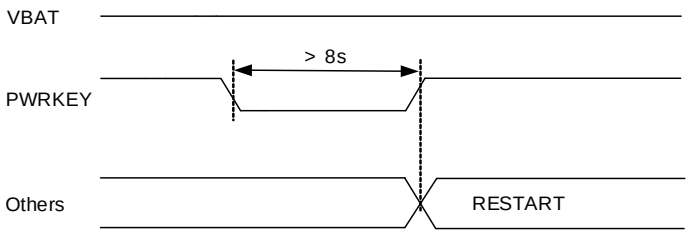


Figure 9: Timing of Restarting Module

3.6. VRTC Interface

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supply for the VBAT. The external power source can be rechargeable battery (such as button cells) according to application demands. The following reference circuit design when an external battery is utilized for powering RTC.

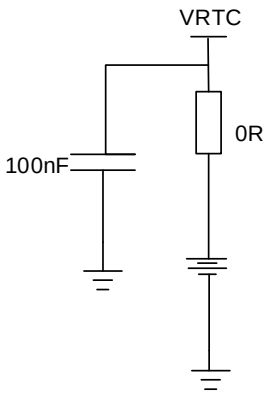


Figure 10: RTC Powered by Rechargeable Button Cell

NOTES

1. 2.1V~3.25V input voltage range and 3.0V typical value for VRTC, when VBAT is disconnected.
2. When powered by VBAT, the RTC error is 100ppm. When powered by VRTC, the RTC error is about 200ppm.
3. If the rechargeable battery is used, the ESR of battery should be less than 2K, and it is recommended to use the MS621FE FL11E of SEIKO.

3.7. Power Output

SC66 supports output of regulated voltages for peripheral circuits. During application, it is recommended to use parallel capacitors (33pF and 10pF) in the circuit to suppress high frequency noise.

Table 10: Power Description

Pin Name	Default Voltage (V)	Drive Current (mA)	Idle
LDO13A_1P8	1.8	20	Keep
LDO11A_1P8	1.8	150	/
LDO3B_2P8	2.8	600	/
LDO7B_3P125	3.125	150	/
LDO14A_1P8	1.8	150	Keep
SD_VDD	2.95	600	/
SD_PU_VDD	2.95	50	/
USIM1_VDD	1.8/2.95	150	/
USIM2_VDD	1.8/2.95	150	/
VPH_PWR	Follow VBAT	1000	Keep

3.8. Battery Charge and Management

SC66 module supports a fully programmable switch-mode Li-ion battery charge function.It can charge single-cell Li-ion and Li-polymer battery. Switching charging with Quick Charge 3.0 and 4.0 supports up to 3 A.The battery charger of SC66 module supports trickle charging, pre-charge, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion batteries.

- **Trickle charging:** When the battery voltage is below 2.1V, a 45mA trickle charging current is applied to the battery.
- **Pre-charge:** When the battery voltage is charged up and is between 2.4V and 3.0V (the maximum pre-charge voltage is 2.4V~3.0V programmable, 3.0V by default), the system will enter into pre-charge mode. The charging current is 500mA (100mA~1500mA programmable, 500mA by default).

- **Constant current mode (CC mode):** When the battery voltage is increased to between the maximum pre-charge voltage and 4.35V (3.6V~4.5V programmable, 4.35V by default), the system will switch to CC mode. The charging current is programmable from 0mA~3000mA. The default charging current is 500mA for USB charging and 2A for adapter.
- **Constant voltage mode (CV mode):** When the battery voltage reaches the final value 4.35V, the system will switch to CV mode and the charging current will decrease gradually. When the charging current reduces to about 100mA, the charging is completed.

Table 11: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	41, 42	PI/PO	Charging power input. Power supply output for OTG device. USB/charger insertion detection.	Vmax=10V Vmin=3.6V Vnorm=5.0V
VBAT	36,37, 38	PI/PO	Power supply for the module	Vmax=4.4V Vmin=3.55V Vnorm=4.0V
BAT_PLUS	27	AI	Differential input signal of battery voltage detection (plus)	Must be connected.
BAT_MINUS	28	AI	Differential input signal of battery voltage detection (minus)	Must be connected.
BAT_THERM	29	AI	Battery temperature detection	Internally pulled up. Externally connected to GND via a 47K NTC resistor.

SC66 module supports battery temperature detection in the condition that the battery integrates a thermistor (47K 1% NTC thermistor with B-constant of 4050K by default; SDNT1608X473F4050FTF of SUNLORD is recommended) and the thermistor is connected to VBAT_THERM pin. If VBAT_THERM pin is not connected, there will be malfunctions such as boot error, battery charging failure, battery level display error, etc.
A reference design for battery charging circuit is shown as below.

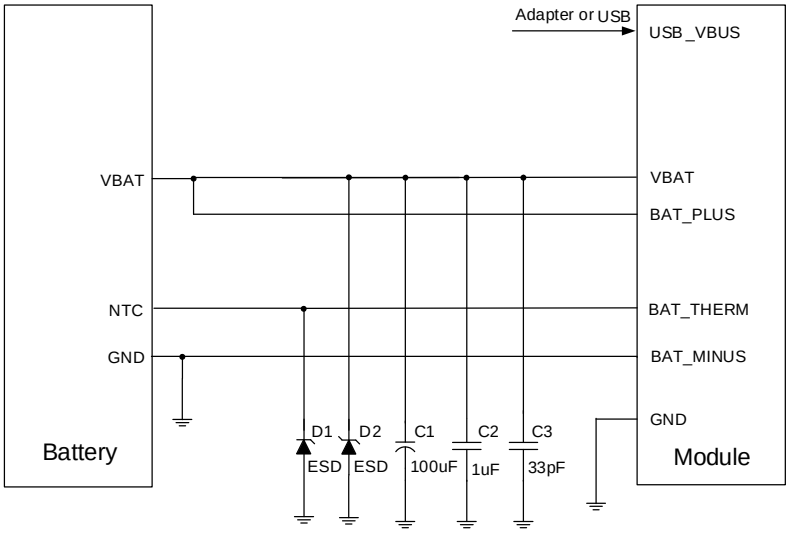


Figure 11: Reference Design for Battery Charging Circuit

SC66 offers a fuel gauge algorithm that is able to accurately estimate the battery's state by current and voltage monitor techniques. Using precise measurements of battery voltage, current, and temperature, the fuel gauge provides a dependable state of charge estimate throughout the entire life of the battery and across a broad range of operating conditions. It effectively protects the battery from over-discharging, and also allows users to estimate the battery life based on the battery level so as to timely save important data before completely power-down.

Mobile devices such as mobile phones and handheld POS systems are powered by batteries. When different batteries are utilized, the charging and discharging curve has to be modified correspondingly so as to achieve the best effect.

If thermistor is not available in the battery, or adapter is utilized for powering the module, then there is only a need for VBAT and GND connection. In this case, the system may be unable to detect the battery, which will cause power-on failure. In order to avoid this, VBAT_THERM should be connected to GND with a 47KΩ resistor. BAT_PLUS and BAT_MINUS must be connected, otherwise there may be abnormalities in use of the module. Among them, BAT_PLUS and BAT_MINUS are used for battery level detection, and they should be routed as differential pair to ensure accuracy.

USB_VBUS can be powered by external power or USB adapter, mainly used for USB detection and battery charging. The input of USB_VBUS is 3.6v ~10V, and the typical working voltage is 5V. The SC66 module supports the charge management of lithium ion batteries, but different types or capacities of batteries require different charging parameters, and the maximum charging current can reach 3A.

3.9. USB Interface

SC66 provides two USB interfaces,The interface is compatible with the USB 3.1/2.0 specification, and can be used for USB OTG,TYPE-C,DP function. USB 3.1 has a maximum speed of 10Gbps, USB 2.0 supports up to 480Mbps with full speed (12Mbps) down compatibility. USB interface can be used for AT command transmission, data transmission, software debugging and software upgrading.

SC66 also supports USB on-go(OTG) function. CC1 pin is used to detect whether the OTG device is connected or not. CC1 is opened by default and high level is maintained. If a slave device is inserted, CC1 will be pulled down and SC66 will be configured as host mode.

3.9.1. TYPE-C Interfaces

The TYPE-C interface has one set of usb2.0-compatible HS interfaces (USB1_HS_DP/M), and two sets of SS interfaces that support USB3.1 (USB_SS1_RXP/M,USB_SS1_TXP/M& USB_SS2_RXP/M,USB_SS2_TXP/M).

When TYPE-C is forward inserted, USB_CC1 detects the external device, and the data is transmitted through USB_SS1;Conversely, when TYPE-C is inverted, USB_CC2 detects the external device, and the data is transmitted through USB_SS2.

The following table shows the pin definition of USB interface.

Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	41，42	PI/PO	Charging power input. Power supply output for OTG device. USB/Charger insertion detection.	Vnorm=5.0V
USB1_HS_DM	33	IO	USB 2.0 differential data	Requires 90R differential routing
USB1_HS_DP	32	IO		
USB_SS1_RX_P	171	AI	USB 3.1 channel1 differential data	
USB_SS1_RX_M	172	AI		
USB_SS1_TX_P	174	AO		
USB_SS1_TX_M	175	AO		
USB_SS2_RX_M	161	AI	USB 3.1 channel2 differential data	

USB_SS2_RX_P	162	AI		
USB_SS2_TX_M	164	AO		
USB_SS2_TX_P	165	AO		
UUSB_TYPEC	23	AI	uUSB&USB TYPE-C configure slection pin	When USB TYPE-C is used, it should be connected to VPH_PWR through 10K resistor. When uUSB is used, it should be connected to GND through 10K resistor.
USB_CC2	223	AI	USB TYPE-C Configure2	
USB_CC1	224	AI	USB TYPE-C Configure1	When Micro usb is used, it should be used as ID pin
SS_DIR_IN	21	DI	CC status detection pin	When USB TYPE-C is used, it should be connected to SS_DIR_OUT.When uUSB is used,it should be connected to GND.
SS_DIR_OUT	226	DO	CC status output pin	When USB TYPE-C is used, it should be connected to SS_DIR_IN.When uUSB is used,it should be huang up.

The following is a reference design for TYPE-C interface:

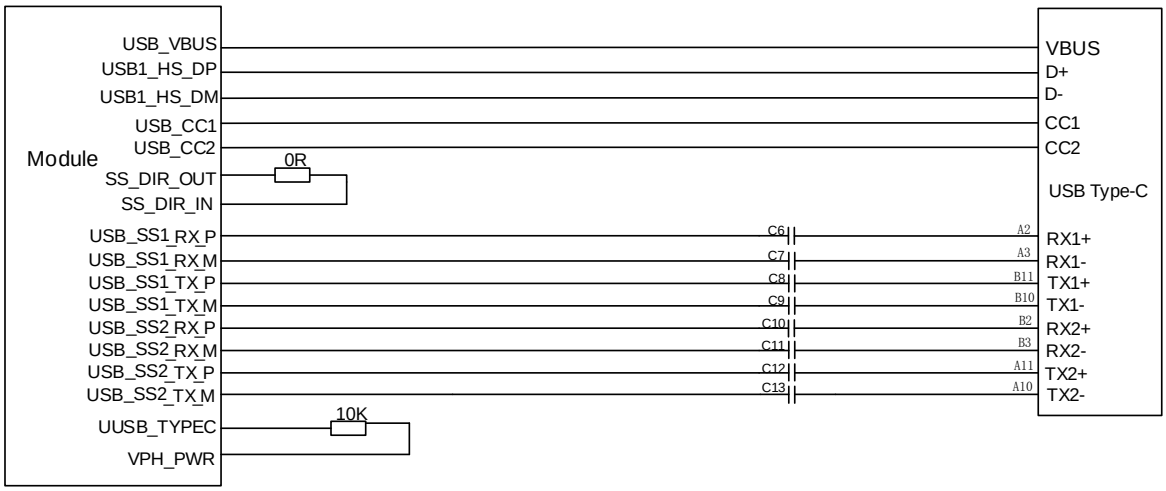


Figure 12: USB Type-C Interface Reference Design

In order to ensure USB performance, please follow the following principles while designing USB interface.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- The ground reference plane must be continuous,without any cuts or any holes under the USB signals,to ensure impedance continuity.
- Pay attention to the influence of junction capacitance of ESD protection devices on USB data lines. Typically, the capacitance value should be less than 2pF for USB 2.0 and less than 0.5pF for USB 3.1. besides.Keep the ESD protection devices as close as possible to the USB connector.
- Do not route signal traces under crystals, oscillators, magnetic devices ,audio signal,and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Keep USB3.1 signal routing away from RF signal. Crossing and parallel with RF signal line is forbidden. The isolation between USB3.0 signal and RF signal should be more than 90 db. Otherwise, it will interfere with RF signal strongly.
- Make sure the trace length difference between USB 3.1 RX/TX differential pairs do not exceed 0.7mm.
- Make sure the trace length difference between USB 2.0 DP/DM differential pairs do not exceed 2mm.

- For USB3.1，the Rx-to-Tx spacing should be three times the line width, Rx-and-Tx to other signals spacing should be four times the line width;For USB2.0, the DP-to-DM spacing shouled be three times the line width, DP-and-DM to other signals spacing should be four times line width.
- For DisplayPort, The routing length difference between DP_AUX_N and DP_AUX_P should be less than 7mm.

Table 13: USB Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Length Difference (DP-DM)
33	USB1_HS_DM	50.88	-0.32
32	USB1_HS_DP	51.20	
171	USB_SS1_RX_P	39.96	0.00
172	USB_SS1_RX_M	39.96	
174	USB_SS1_TX_P	39.69	-0.01
175	USB_SS1_TX_M	39.70	
162	USB_SS2_RX_P	39.40	-0.18
161	USB_SS2_RX_M	39.57	
165	USB_SS2_TX_P	39.85	-0.05
164	USB_SS2_TX_M	39.90	
25	USB2_HS_DM	37.80	-0.26
26	USB2_HS_DP	37.54	
220	DP_AUX_N	42.88	-0.94
221	DP_AUX_P	41.94	

3.9.2. DP Interfaces

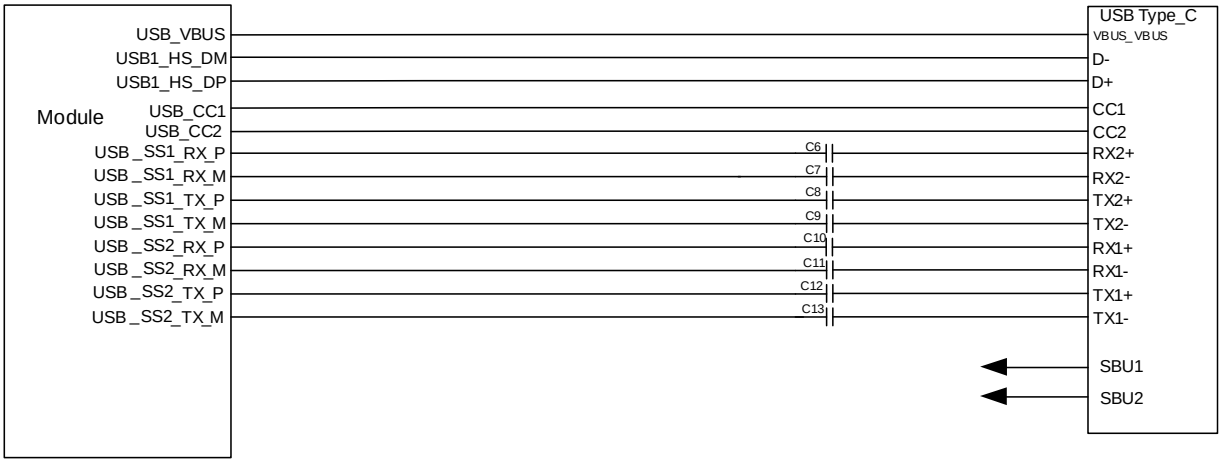
SC66 also supports DisplayPort mode with 4 lanes up to 4K@30ps. It should be noticed that Display mode cannot be supported with USB1 together, but it can be used with USB2 together.

The differences between USB mode and DisplayPort Mode are listed below：

Table 14: The Differences between USB Mode and DisplayPort Mode

Module Pin Name	USB Mode	DisplayPort Mode
USB_SS2_RX_P/M	USB_SS2_RX_P/M	DP_LANE0_P/M
USB_SS2_TX_P/M	USB_SS2_TX_P/M	DP_LANE1_P/M
USB_SS1_RX_P/M	USB_SS1_RX_P/M	DP_LANE3_P/M
USB_SS1_TX_P/M	USB_SS1_TX_P/M	DP_LANE2_P/M
DP_AUX_P/N	SBU1/2	AUX_P/N
USB1_HS_DP/DM	USB1_HS_DP/DM	USB1_HS_DP/M
USB_CC1/CC2	USB_CC1/CC2	HOTPLUG_DET/Vconn
VBUS	VBUS	VBUS
GND	GND	GND

The design of Display Port is shown as below:



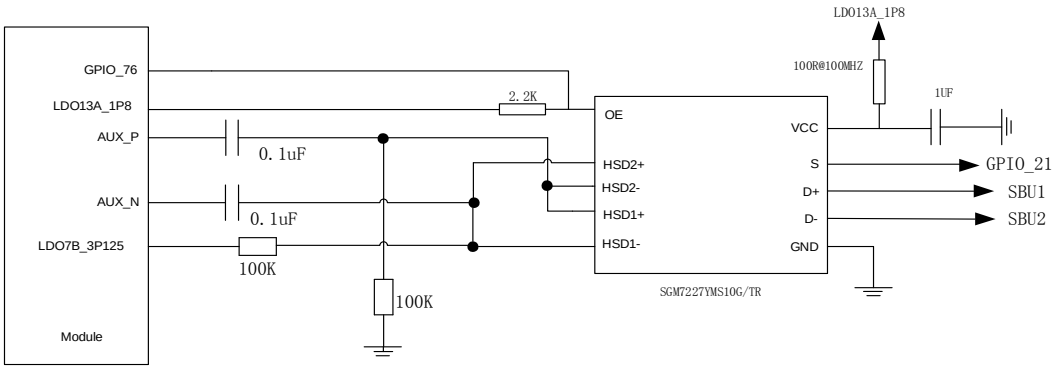


Figure 13: Display Port interfaces

3.9.3. Host

SC66 supports two groups of USB, and USB1 is part of TYPE-C compatibility, USB2 is a separate part that supports only the Host mode.

Table 15: USB2 configuration

Pin Name	Pin No.	Comment
USB2_HS_DM	25	USB Differential Signal (minus)
USB2_HS_DP	26	USB Differential Signal (positive)

USB2 realizes the reference circuit of Host mode:

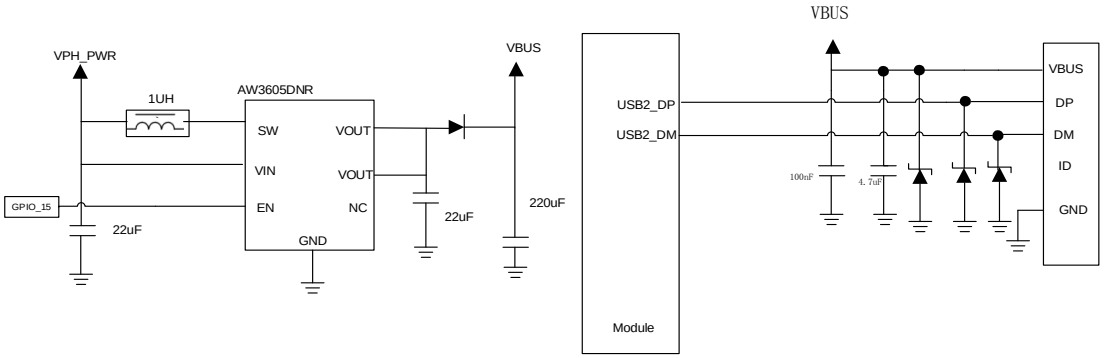


Figure 14: USB2 Host

3.10. UART Interfaces

The module provides the following four UART interfaces:

- UART6: 4-wire UART interface, hardware flow control supported
- DEBUG UART: 2-wire UART interface, used for debugging by default
- UART1: 2-wire UART interface
- LPI_ UART _2: low power UART interface

The following table shows the pin definition of UART interfaces.

Table 16: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
DEBUG_TXD	5	DO	UART for Debug	1.8 power domain
DEBUG_RXD	6	DI		1.8 power domain
UART1_TXD	7	DO	UART1	1.8 power domain
UART1_RXD	8	DI		1.8 power domain
UART6_RXD	198	DI	UART6 Receive data	1.8 power domain
UART6_TXD	199	DO	UART6 Send data	1.8 power domain
UART6_CTS	246	DI	UART6 Clear sending	1.8 power domain
UART6_RTS	245	DO	UART6 Request sending	1.8 power domain
LPI_UART_2_TXD	60	DO	UART2 Send data	1.8 power domain
LPI_UART_2_RXD	61	DI	UART2 Receive data	1.8 power domain

UART6 is a 4-wire UART interface with 1.8V power domain. A level translator chip should be used if customers' application is equipped with a 3.3V UART interface. A level translator chip TXS0104EPWR provided by Texas Instruments is recommended.

The following figure shows a reference design.

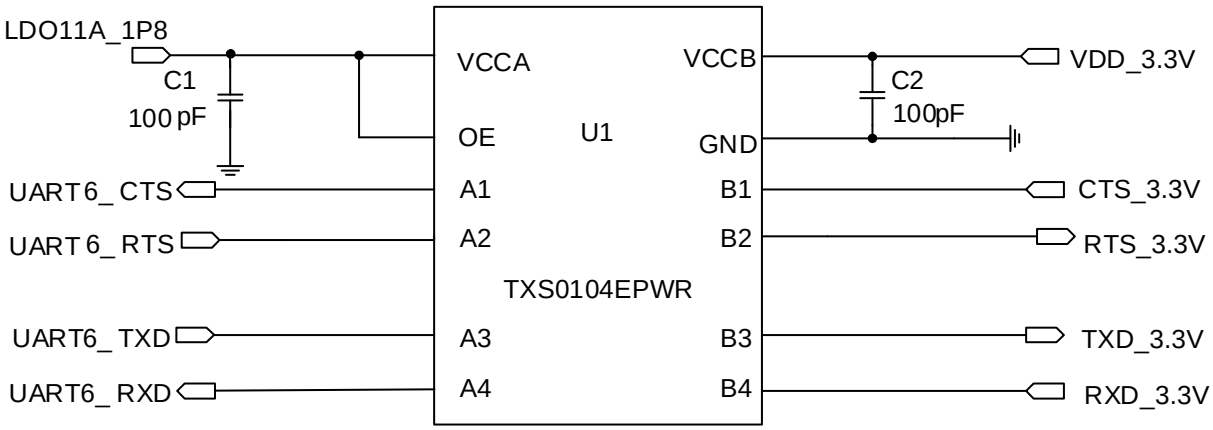


Figure 15: Reference Circuit with Level Translator Chip (for UART6)

The following figure is an example of connection between SC66 and PC. A voltage level translator and a RS-232 level translator chip are recommended to be added between the module and PC, as shown below:

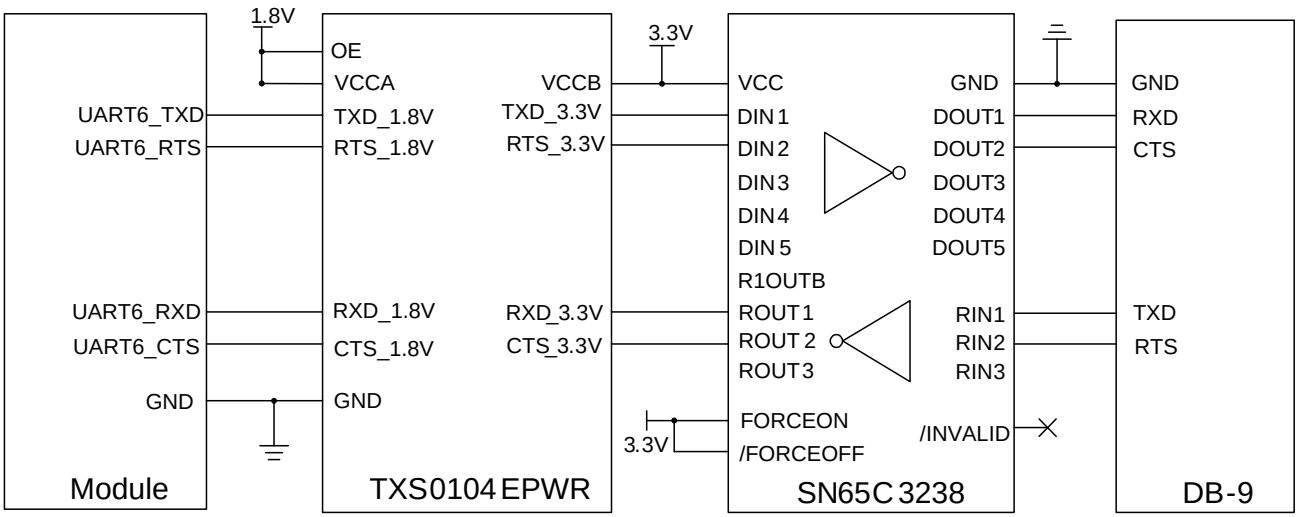


Figure 16: RS232 Level Match Circuit (for UART5)

NOTE

1. DEBUG UART, UART1,LPI_UART_2 are similar to UART6. Please refer to UART6 reference circuit design for DEBUG UART, UART1,LPI_UART_2.
2. LPI_UART_2 is a low power UART and it is not recommended for the time being.

3.11. (U)SIM Interfaces

SC66 provides two (U)SIM interfaces which both meet ETSI and IMT-2000 requirements. Dual SIM Dual Standby is supported by default. Both 1.8V and 2.95V (U)SIM cards are supported, and the (U)SIM interfaces are powered by the dedicated low dropout regulators from SC66 module.

Table 17: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DET	145	DI	(U)SIM1 card detection	Active Low. Need external pull-up to 1.8V. If unused, keep this pin open. Disabled by default, and can be enabled through software configuration.
USIM1_RST	144	DO	(U)SIM1 card reset signal	
USIM1_CLK	143	DO	(U)SIM1 card clock signal	
USIM1_DATA	142	IO	(U)SIM1 card data signal	Pull up to USIM1 with a 10K resistor.
USIM1_VDD	141	PO	(U)SIM1 card power supply	Either 1.8V or 2.95V (U)SIM card is supported.
USIM2_DET	256	DI	(U)SIM2 card insertion detection	Active low. Need external pull-up to1.8V If unused, keep this pin open.
USIM2_RST	207	DO	(U)SIM2 card reset signal	
USIM2_CLK	208	DO	(U)SIM2 card clock signal	
USIM2_DATA	209	IO	(U)SIM2 card data signal	Pull-up to USIM2 with a 10K resistor.
USIM2_VDD	210	PO	(U)SIM2 card power supply	Either 1.8V or 2.95V (U)SIM card is supported.

SC66 supports (U)SIM card hot-plug via the USIM_DET pin, which is disabled by default and can be enabled through software configuration. A reference circuit for (U)SIM interface with an 8-pin (U)SIM card connector is shown as below.

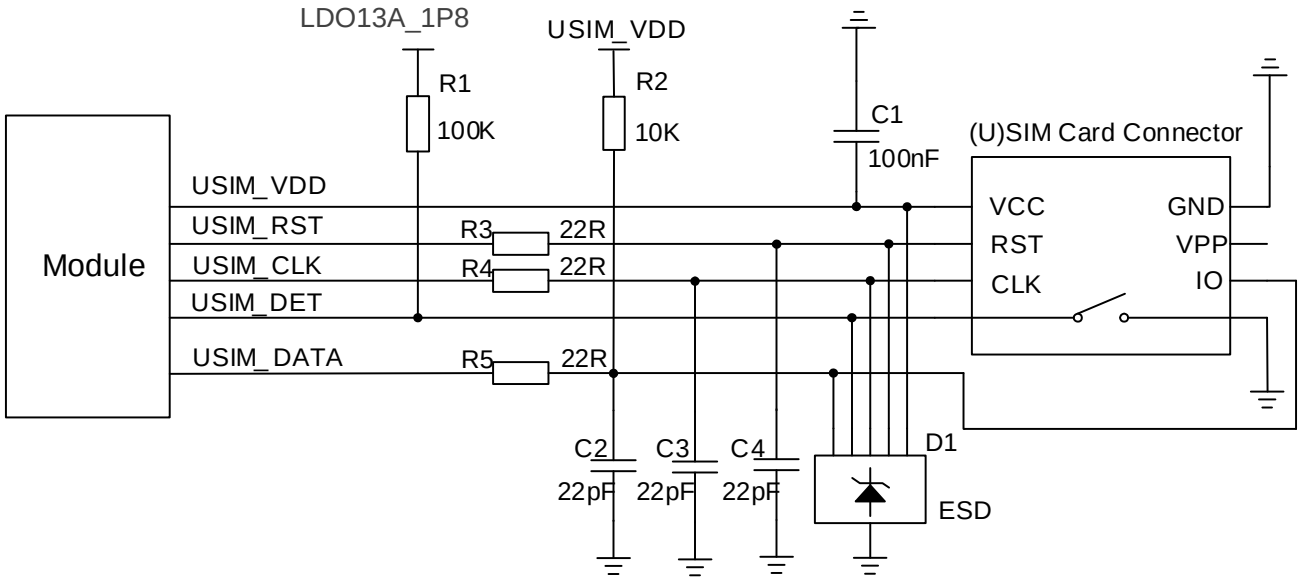


Figure 17: Reference Circuit for (U)SIM Interface with an 8-pin (U)SIM Card Connector

If there is no need to use USIM_DET, please keep it open. The following is a reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector.

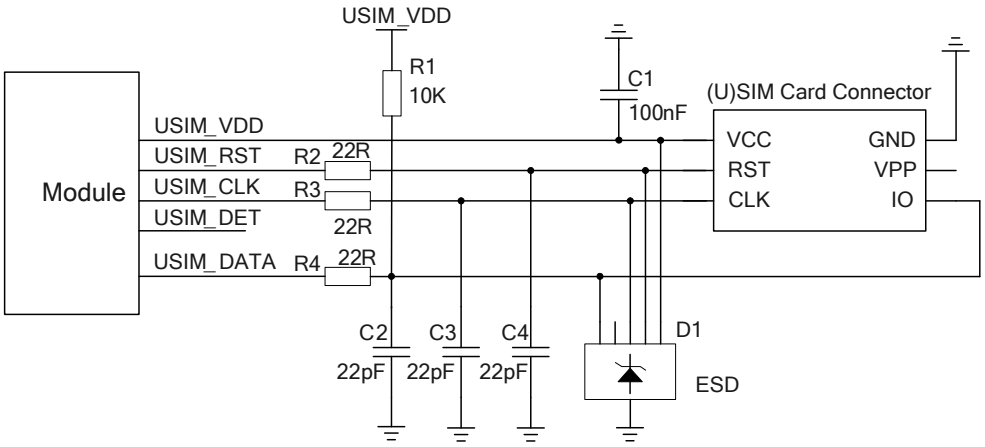


Figure 18: Reference Circuit for (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to ensure good performance and avoid damage of (U)SIM cards, please follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length of (U)SIM card signals as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- A filter capacitor shall be reserved for USIM_VDD, and its maximum capacitance should not exceed 1uF. The capacitor should be placed near to (U)SIM card.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground. USIM_RST also needs ground protection.

- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 50pF. The 22Ω resistors should be added in series between the module and (U)SIM card so as to suppress EMI spurious transmission and enhance ESD protection. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The 22pF capacitors should be added in parallel on USIM_DATA, USIM_VDD, USIM_CLK and USIM_RST signal lines so as to filter RF interference, and they should be placed as close to the (U)SIM card connector as possible.

3.12. SD Card Interface

SC66 module supports SD 3.0 specifications. The pin definition of the SD card interface is shown below.

Table 18: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_VDD	63	PO	Power supply for SD card	Vnorm=2.95V $I_O$max=600mA
SD_PU_VDD	179	PO	SD card pull-up power supply	Support 1.8V/2.95V power supply. The maximum drive current is 50mA.
SD_CLK	70	DO	High speed digital clock signal of SD card	Control characteristic impedance as 50Ω.
SD_CMD	69	I/O	Command signal of SD card	
SD_DATA0	68	I/O	High speed bidirectional digital signal lines of SD card	
SD_DATA1	67	I/O		
SD_DATA2	66	I/O		
SD_DATA3	65	I/O		
SD_DET	64	DI	SD card insertion detection	Active low.

A reference circuit for SD card interface is shown as below.

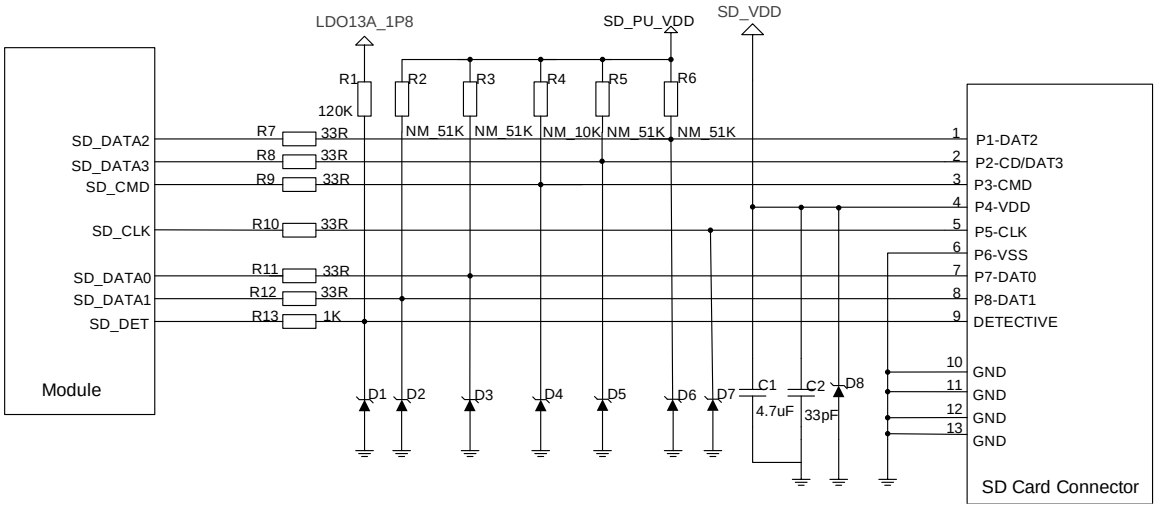


Figure 19: Reference Circuit for SD Card Interface

SD_VDD is a peripheral driver power supply for SD card. The maximum drive current is 600mA. Because of the high drive current, it is recommended that the trace width is 0.5mm or above. In order to ensure the stability of drive power, a 4.7uF and a 33pF capacitor should be added in parallel near the SD card connector.

CMD, CLK, DATA0, DATA1, DATA2 and DATA3 are all high speed signal lines. In PCB design, please control the characteristic impedance of them as 50Ω, and do not cross them with other traces. It is recommended to route the trace on the inner layer of PCB, and keep the same trace length for CLK, CMD, DATA0, DATA1, DATA2 and DATA3. CLK additionally needs ground shielding.

Layout guidelines:

- Control impedance as 50Ω±10%, and ground shielding is required.
- The difference in trace lengths among the clock, data, and command signals should be less than 2 mm.
- The Bus length should be less than 100mm.
- The spacing to all other signals and lane-to-lane should be at least one and a half times the line width.

Table 19: SD Card Signal Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Comment
70	SD_CLK	24.58	
69	SD_CMD	24.32	
68	SD_DATA0	24.33	

67	SD_DATA1	24.33
66	SD_DATA2	24.21
65	SD_DATA3	24.25

3.13. GPIO Interfaces

SC66 has abundant GPIO interfaces with power domain of 1.8V. The pin definition is listed below.

Table 20: Pin Definition of GPIO Interfaces

引脚名	引脚号	GPIO	复位状态	备注
GPIO_20	113	GPIO_20	B-PD:nppukp [1)]	
GPIO_21	231	GPIO_21	B-PD:nppukp	Wakeup [2)]
GPIO_34	236	GPIO_34	B-PD:nppukp	
GPIO_40	238	GPIO_40	B-PD:nppukp	Wakeup
GPIO_41	237	GPIO_41	B-PD:nppukp	Wakeup
GPIO_42	137	GPIO_42	B-PD:nppukp	Wakeup
GPIO_43	136	GPIO_43	B-PD:nppukp	Wakeup
GPIO_55	178	GPIO_55	B-PD:nppukp	Wakeup
GPIO_56	177	GPIO_56	B-PD:nppukp	Wakeup
GPIO_72	239	GPIO_72	B-PD:nppukp	Wakeup
GPIO_73	59	GPIO_73	B-PD:nppukp	Wakeup
GPIO_74	58	GPIO_74	B-PD:nppukp	Wakeup
GPIO_76	232	GPIO_76	B-PD:nppukp	Wakeup
GPIO_77	240	GPIO_77	B-PD:nppukp	Wakeup
ACCL_INT	252	GPIO_68	B-PD:nppukp	Wakeup
GYRO_INT	255	GPIO_69	B-PD:nppukp	Wakeup

MAG_INT	254	GPIO_70	B-PD:nppukp	Wakeup
ALPS_INT	253	GPIO_71	B-PD:nppukp	Wakeup
HALL_INT	218	GPIO_75	B-PD:nppukp	Wakeup
GPIO_22	204	GPIO_22	B-PD:nppukp	Wakeup
GPIO_23	205	GPIO_23	B-PD:nppukp	
GPIO_12	228	GPIO_12	B-PD:nppukp	
GPIO_13	227	GPIO_13	B-PD:nppukp	Wakeup
GPIO_14	230	GPIO_14	B-PD:nppukp	
GPIO_15	229	GPIO_15	B-PD:nppukp	
GPIO_61	234	GPIO_61	B-PD:nppukp	
GPIO_03B	11	GPIO_03B	B-PD:nppukp	
GPIO_08B	13	GPIO_08B	B-PD:nppukp	
GPIO_04B	14	GPIO_04B	B-PD:nppukp	
GPIO_05B	15	GPIO_05B	B-PD:nppukp	
GPIO_11A	211	GPIO_11A	B-PD:nppukp	
GPIO_13A	233	GPIO_13A	B-PD:nppukp	

1. [1)] B: Bidirectional digital with CMOS input; PD:nppukp = Contains an internal pull-down.
2. [2)] Wakeup: interrupt pins that can wake up the system.
3. More details about GPIO configuration, please refer to the GPIO_Configuration.

3.14. I2C Interfaces

SC66 can provide up to 5 groups of I2C Interfaces. As an open drain output, each I2C interface should be pulled up to 1.8V voltage. The SENSOR_I2C interface supports only sensors of the aDSP architecture. CAM_I2C bus is controlled by Linux Kernel code and supports connection to video output related devices.

Table 21: Pin Definition of I2C Interfaces

Pin Name	Pin No	I/O	Description	Comment
TP0_I2C_SCL	140	OD	TP I2C clock	Used for TP0
TP0_I2C_SDA	206	OD	TP I2C data	
CAM_I2C_SCL0	75	OD	CAM I2C clock	Used for main and front camera
CAM_I2C_SDA0	76	OD	CAM I2C data	
CAM_I2C_SCL1	196	OD	CAM I2C clock	Used for depth camera
CAM_I2C_SDA1	197	OD	CAM I2C data	
SENSOR_I2C_SCL	131	OD	Sensor I2C clock	Used for sensor
SENSOR_I2C_SDA	132	OD	Sensor I2C data	
GPIO_22	204	OD	TP I2C data	The default configuration is GPIO port, which can be reused as I2C for TP1
GPIO_23	205	OD	TP I2C clock	

3.15. I2S Interface

SC66 provides two I2S interfaces. The reference voltage field of the interface is 1.8v, and one group is low-power I2S.

Table 22: Pin Definition of I2S Interface

Pin Name	Pin No	I/O	Description	Comment
MI2S_2_WS	203	DO	I2S word selection signal	I2S word selection (L/R)
MI2S_2_DATA0	249	IO	I2S Data0 signal	I2S serial data0 channel
MI2S_2_SCK	250	DO	I2S serial signal	I2S serial clock
MI2S_2_DATA1	251	IO	I2S Data1 signal	I2S serial data1 channel
MI2S_2_MCLK	114	DO	I2S Main clock signal	I2S main clock

LPI_MI2S_SCLK	212	DO	LPI_I2S serial clock signal	I2S serial clock
LPI_MI2S_WS	156	DO	LPI_I2S word selection signal	I2S word selection (L/R)
LPI_MI2S_DATA0	154	IO	LPI_I2S Data0 signal	I2S serial data0 channel
LPI_MI2S_DATA1	155	IO	LPI_I2S Data1 signal	I2S serial data1 channel

3.16. SPI Interfaces

SC66 provides SPI interfaces which only support master mode.

Table 23: Pin Definition of SPI Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SPI3_MOSI	248	DO	Master out slave in of SPI interface	
SPI3_MISO	247	DI	Master in salve out of SPI interface	
SPI3_CS_N	201	DO	Chip selection signal of SPI interface	
SPI3_CLK	200	DO	Clock signal of SPI interface	

3.17. ADC Interfaces

SC66 provides two analog-to-digital converter (ADC) interfaces, and the pin definition is shown below.

Table 24: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	151	AI	Universal ADC interface	The maximum input voltage is 1.7v
ADC1	153	AI	Universal ADC interface	The maximum input voltage is 1.7v

The resolution of the ADC is up to 15 bits.

3.18. LCM Interfaces

SC66 video output interface (LCM interface) is based on MIPI_DSI standard and supports 8 groups of high-speed differential data transmission and WQXGA display (resolution: 2560*1600),Support double screen display, default DSI+DP (type-c), optional DSI0+DSI1. Note that DSI1 does not support screens with command mode.

Table 25: Pin Definition of LCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
LDO11A_1P8	10	PO	1.8V output power supply for LCM logic circuit and DSI	
LDO3B_2P8	12	PO	2.8V output power supply for LCM analog circuits	
PWM	152	DO	PWM signal output	
LCD0_RST	127	DO	LCD0 reset signal	
LCD0_TE	126	DI	LCD0 tearing effect signal	
DSI0_CLK_N	116	AO	LCD0 MIPI clock signal (negative)	
DSI0_CLK_P	115	AO	LCD0 MIPI clock signal (positive)	
DSI0_LN0_N	118	AO	LCD0 MIPI lane 0 data signal (negative)	
DSI0_LN0_P	117	AO	LCD0 MIPI lane 0 data signal (positive)	
DSI0_LN1_N	120	AO	LCD0 MIPI lane 1 data signal (negative)	
DSI0_LN1_P	119	AO	LCD0 MIPI lane 1 data signal (positive)	

DSI0_LN2_N	122	AO	LCD0 MIPI lane 2 data signal (negative)	
DSI0_LN2_P	121	AO	LCD0 MIPI lane 2 data signal (positive)	
DSI0_LN3_N	124	AO	LCD0 MIPI lane 3 data signal (negative)	
DSI0_LN3_P	123	AO	LCD0 MIPI lane 3 data signal (positive)	
DSI1_CLK_N	103	AO	LCD1 MIPI clock signal (negative)	
DSI1_CLK_P	102	AO	LCD1 MIPI clock signal (positive)	
DSI1_LN0_N	105	AO	LCD1 MIPI lane 0 data signal (negative)	
DSI1_LN0_P	104	AO	LCD1 MIPI lane 0 data signal (positive)	
DSI1_LN1_N	107	AO	LCD1 MIPI lane 1 data signal (negative)	
DSI1_LN1_P	106	AO	LCD1 MIPI lane 1 data signal (positive)	
DSI1_LN2_N	109	AO	LCD1 MIPI lane 2 data signal (negative)	
DSI1_LN2_P	108	AO	LCD1 MIPI lane 2 data signal (positive)	
DSI1_LN3_N	111	AO	LCD1 MIPI lane 3 data signal (negative)	
DSI1_LN3_P	110	AO	LCD1 MIPI lane 3 data signal (positive)	
GPIO_20	113	DO	LCD1 复位信号	默认为 GPIO 口
GPIO_40	238	DO	LCD1 PWM 输出	默认为 GPIO 口

The following are the reference designs for LCM interfaces.
LCM can use external backlight drive circuit according to customer requirement. The reference design of the external backlight drive circuit is shown in the figure below, in which pins PWM (PIN152&PIN238) can be used for backlight brightness adjustment.

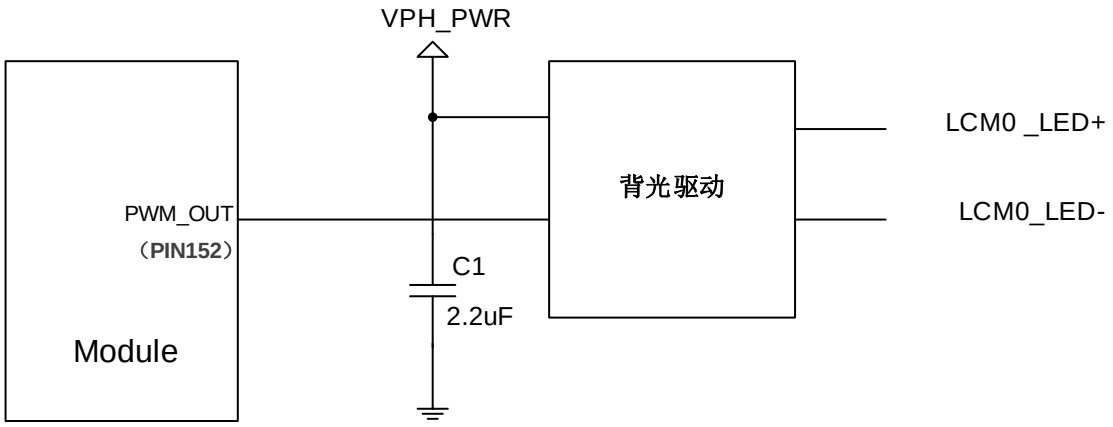


Figure 20: LCM0 external backlight drive reference circuit

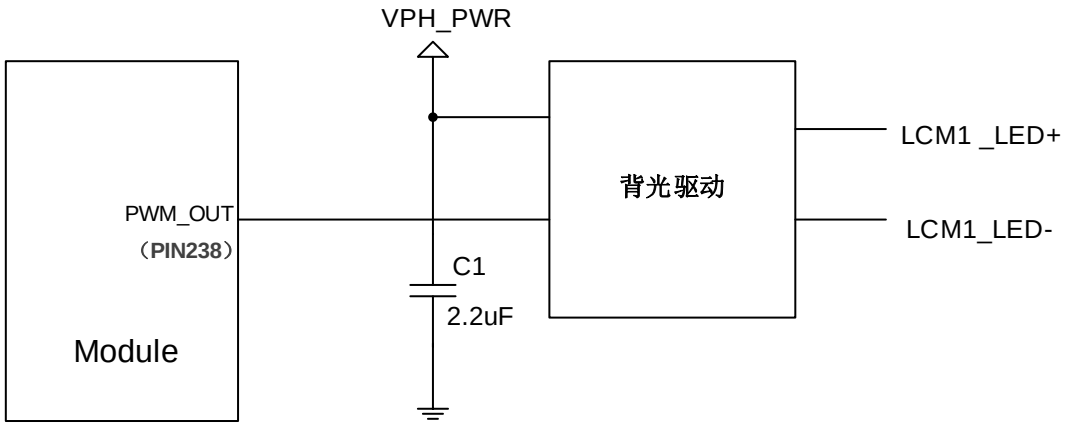


Figure 21: Reference Circuit Design for LCM1 Interface

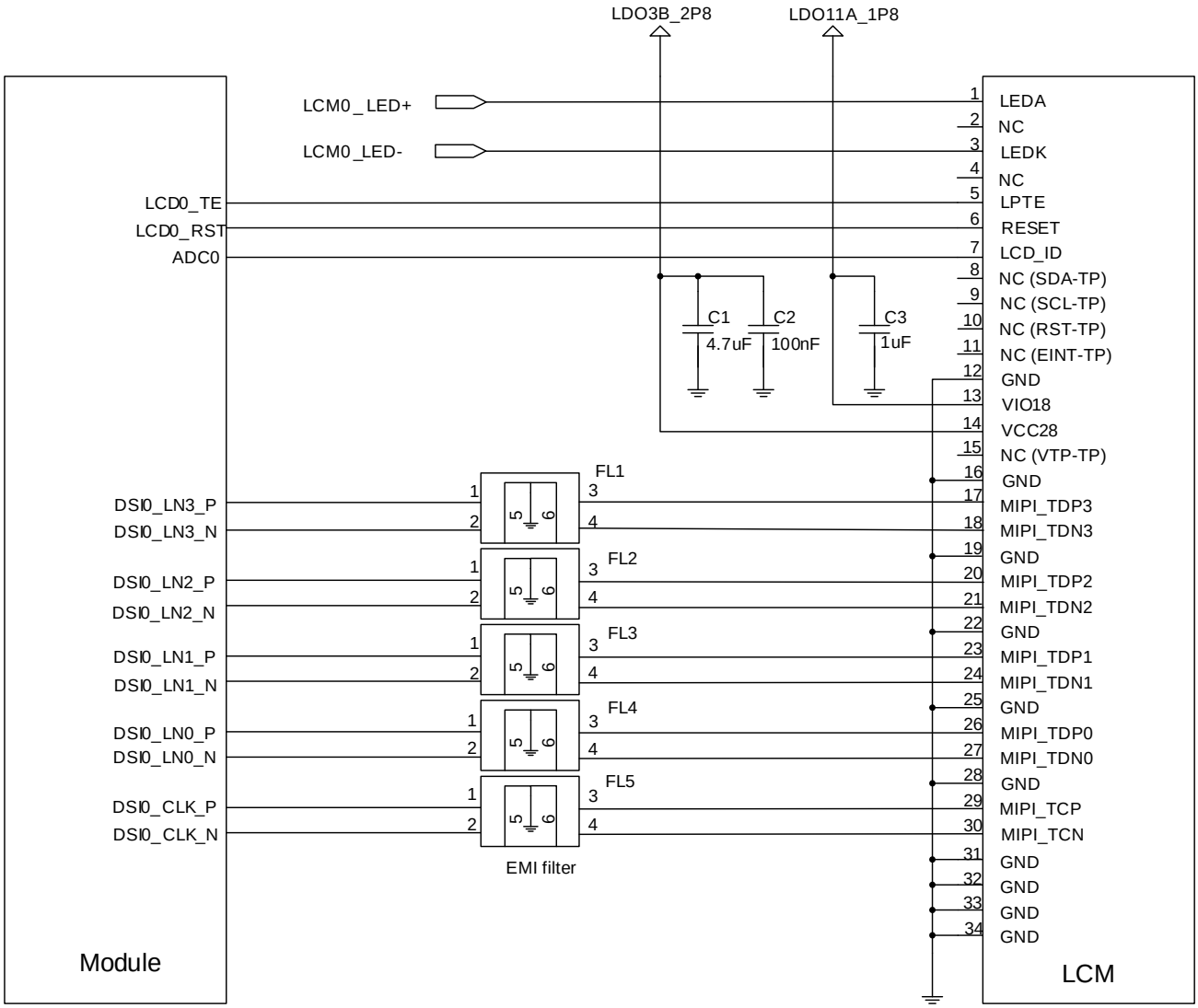


Figure 22: Reference Circuit Design for LCM0 Interface

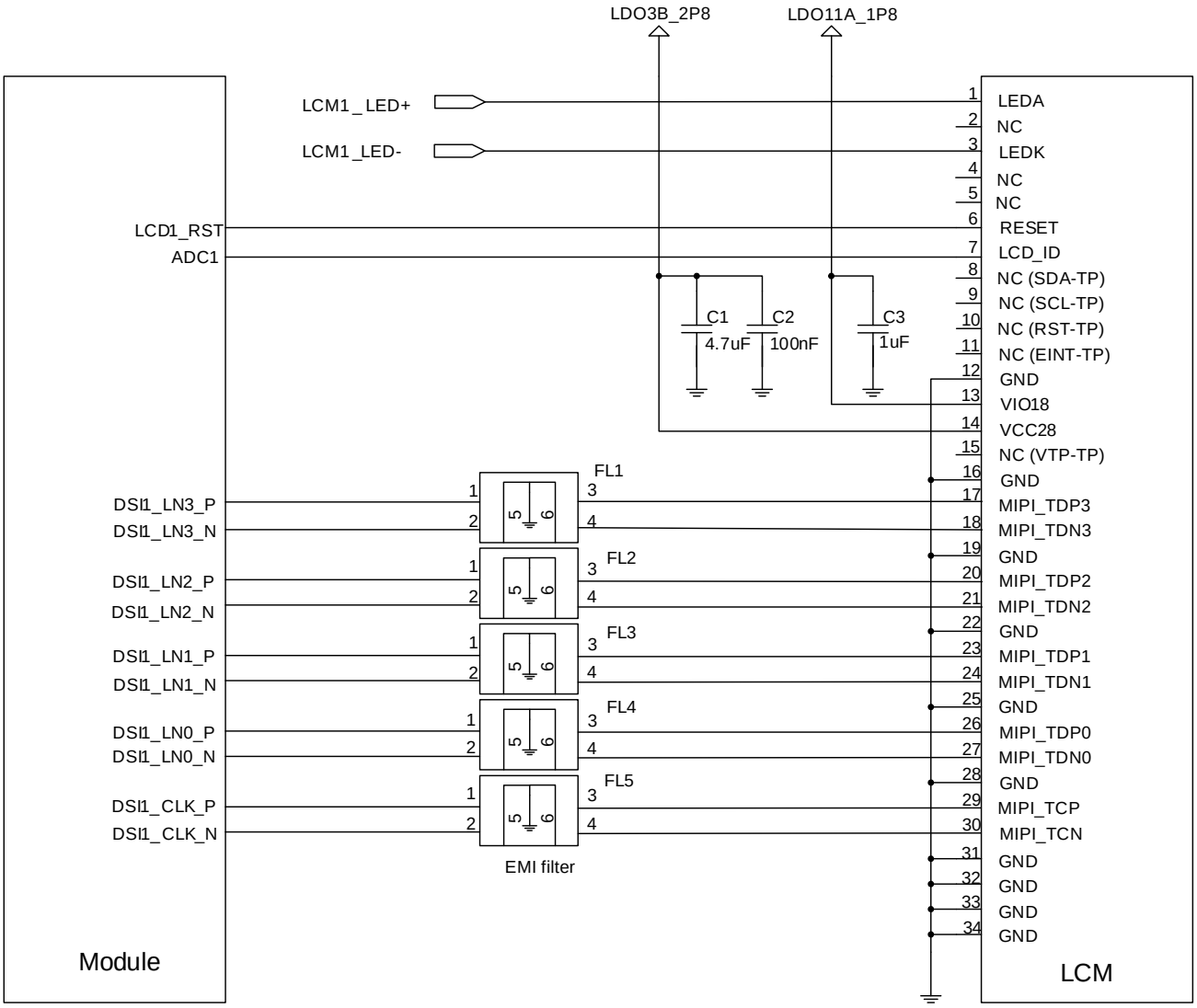


Figure 23: Reference Circuit Design for LCM1 Interface

MIPI are high speed signal lines. It is recommended that common-mode filters should be added in series near the LCM connector, so as to improve protection against electromagnetic radiation interference. ICMEF112P900MFR using ICT is recommended.

When compatible design with other displays is required, please connect the LCD_ID pin of LCM to the module's ADC pin, and please note that the output voltage of LCD_ID cannot exceed the voltage range of ADC pin.

3.19. Touch Panel Interfaces

SC66 provides two I2C interfaces for connection with Touch Panel (TP), and also provides the

corresponding power supply and interrupt pins. The pin definition of touch panel interfaces is illustrated below.

Table 26: Pin Definition of Touch Panel Interfaces

Pin Name	Pin No	I/O	Description	Comment
GPIO_03B	11	PO	TP VDD power supply enable pin	Use external LDO power supply
LDO11A_1P8	10	PO	1.8V output power supply	Pull-up power supply of I2C Vnorm=1.8V $I_O$max=300mA
TP0_INT	139	DI	Interrupt signal of touch panel (TP0)	
TP0_RST	138	DO	Reset signal of touch panel (TP0)	
TP0_I2C_SCL	140	OD	I2C clock signal of touch panel (TP0)	
TP0_I2C_SDA	206	OD	I2C data signal of touch panel (TP0)	

A reference design for touch panel interfaces is shown below.

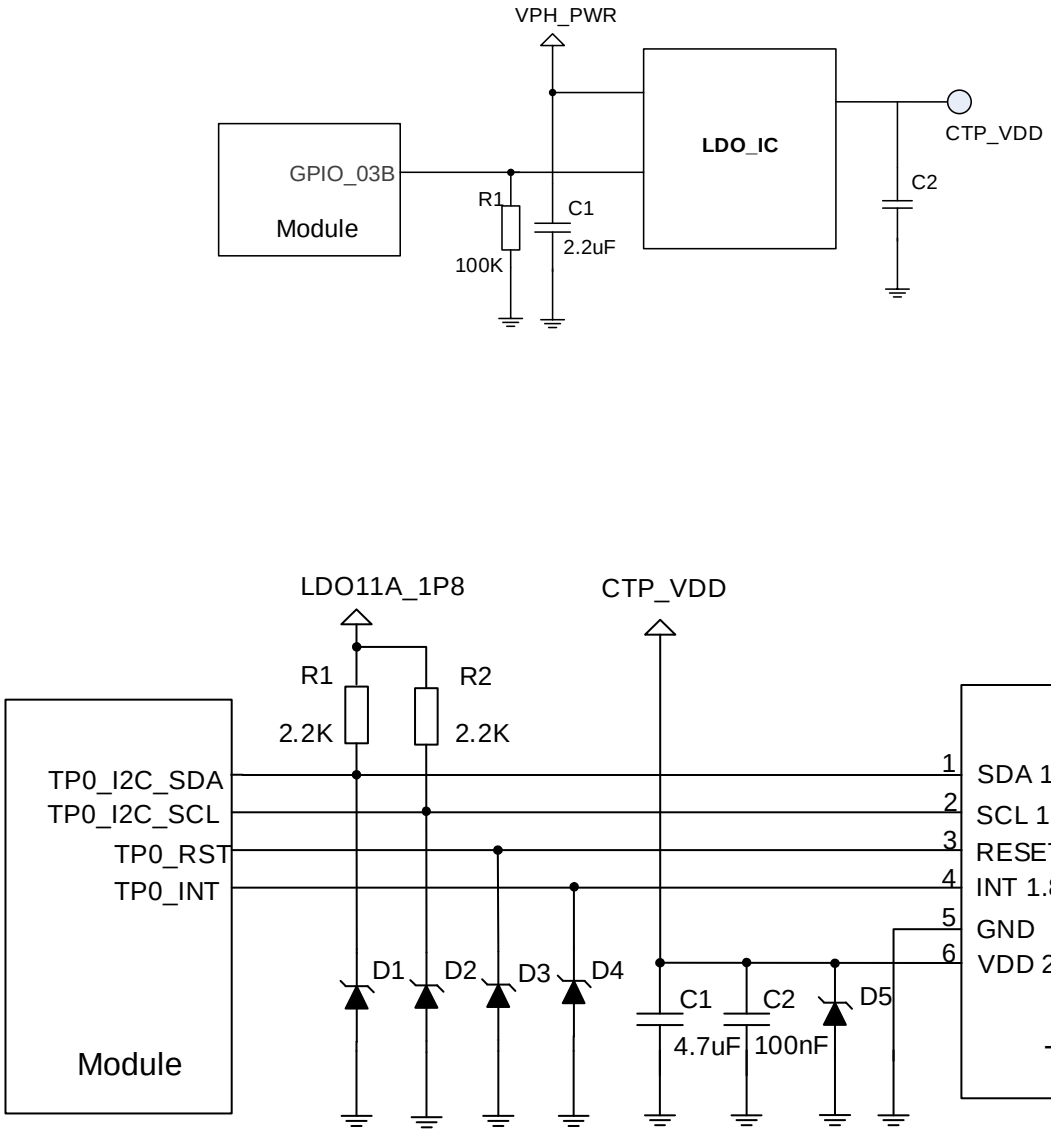


Figure 24: Reference Circuit Design for Touch Panel Interfaces

3.20. Camera Interfaces

Based on standard MIPI CSI input interface, SC66 module supports 3 cameras (4-lane + 4-lane + 4-lane) or 4 cameras (4-lane + 4-lane + 2-lane + 1-lane), with maximum pixels up to 24MP for SC66. The video and photo quality are determined by various factors such as camera sensor, camera lens quality, etc.

Table 27: Pin Definition of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GPIO_08B	13	DO	后置摄像头 DVDD 供电 LDO 使能管脚	
GPIO_05B	15	DO	前置摄像头 DVDD 供电 LDO 使能管脚	Vnorm=1.8V $I_O$max=150mA
LDO11A_1P8	10	PO	输出 1.8V； 给摄像头的 DOVDD 供电	Vnorm=2.8V $I_O$max=600mA
LDO3B_2P8	12	PO	输出 2.8V； 摄像头 AF_VDD 电路供电	
GPIO_04B	14	DO	摄像头 AVDD 供电 LDO 使能管脚	
CSI0_CLK_N	78	AI	前摄 MIPI 时钟负	
CSI0_CLK_P	77	AI	前摄 MIPI 时钟正	
CSI0_LN0_N	80	AI	前摄 MIPI 数据 0 负	
CSI0_LN0_P	79	AI	前摄 MIPI 数据 0 正	
CSI0_LN1_N	82	AI	前摄 MIPI 数据 1 负	
CSI0_LN1_P	81	AI	前摄 MIPI 数据 1 正	
CSI0_LN2_N	84	AI	前摄 MIPI 数据 2 负	
CSI0_LN2_P	83	AI	前摄 MIPI 数据 2 正	
CSI0_LN3_N	86	AI	前摄 MIPI 数据 3 负	
CSI0_LN3_P	85	AI	前摄 MIPI 数据 3 正	
CSI1_CLK_N	89	AI	后摄 MIPI 时钟负	
CSI1_CLK_P	88	AI	后摄 MIPI 时钟正	
CSI1_LN0_N	91	AI	后摄 MIPI 数据 0 负	
CSI1_LN0_P	90	AI	后摄 MIPI 数据 0 正	
CSI1_LN1_N	93	AI	后摄 MIPI 数据 1 负	
CSI1_LN1_P	92	AI	后摄 MIPI 数据 1 正	
CSI1_LN2_N	95	AI	后摄 MIPI 数据 2 负	

CSI1_LN2_P	94	AI	后摄 MIPI 数据 2 正
CSI1_LN3_N	97	AI	后摄 MIPI 数据 3 负
CSI1_LN3_P	96	AI	后摄 MIPI 数据 3 正
CSI2_CLK_N	184	AI	景深 MIPI 时钟负
CSI2_CLK_P	183	AI	景深 MIPI 时钟正
CSI2_LN0_N	186	AI	景深 MIPI 数据 0 负
CSI2_LN0_P	185	AI	景深 MIPI 数据 0 正
CSI2_LN1_N	188	AI	景深 MIPI 数据 1 负
CSI2_LN1_P	187	AI	景深 MIPI 数据 1 正
CSI2_LN2_N	190	AI	景深 MIPI 数据 2 负
CSI2_LN2_P	189	AI	景深 MIPI 数据 2 正
CSI2_LN3_N	192	AI	景深 MIPI 数据 3 负
CSI2_LN3_P	191	AI	景深 MIPI 数据 3 正
MCAM_MCLK	99	DO	后置摄像头时钟信号
SCAM_MCLK	100	DO	前置摄像头时钟信号
DCAM_MCLK	194	DO	景深摄像头时钟信号
MCAM_RST	74	DO	后置摄像头复位信号
SCAM_RST	72	DO	前置摄像头复位信号
DCAM_RST	180	DO	景深摄像头复位信号
MCAM_PWDN	73	DO	后置摄像头关断信号
SCAM_PWDN	71	DO	前置摄像头关断信号
DCAM_PWDN	181	DO	景深摄像头关断信号
CAM_I2C_SCL0	75	OD	前后摄 I2C 时钟信号
CAM_I2C_SDA0	76	OD	前后摄 I2C 数据信号
CAM_I2C_SDA1	197	OD	景深摄像头 I2C 数据信号

CAM_I2C_SCL1	196	OD	景深摄像头 I2C 时钟信号

The following is a reference circuit design for two-camera applications.

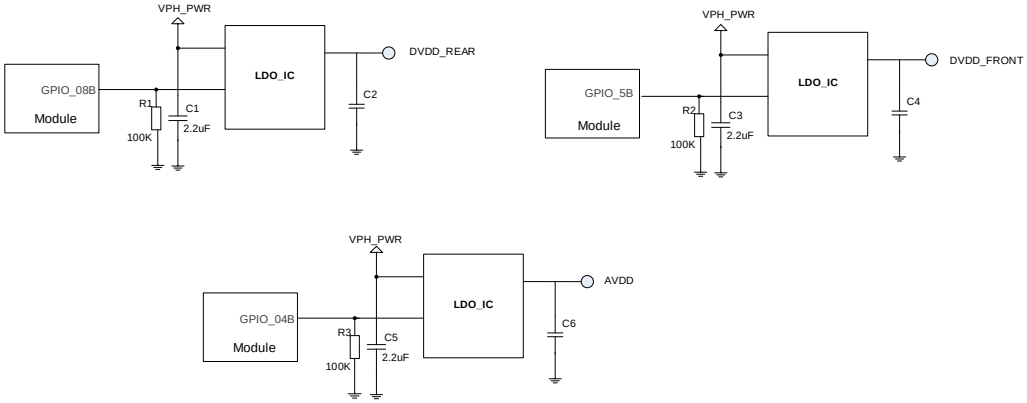


Figure 25: Reference Circuit Design for Two-Camera Applications

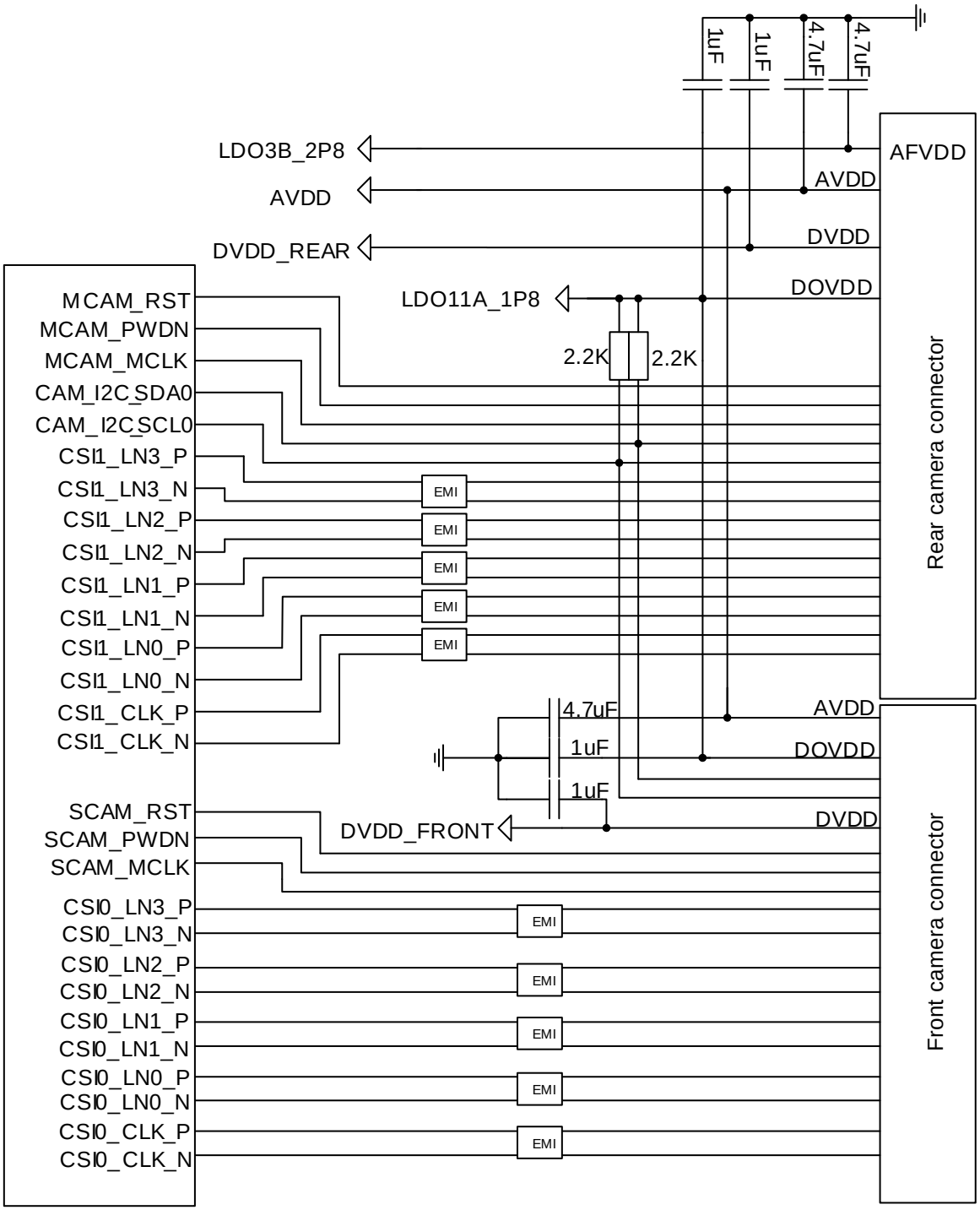


Figure 26: Reference Circuit Design for Two-Camera Applications

NOTE

CSI1 is used for rear camera, CSI2 is used for depth camera, and CSI0 is used for front camera,and LN2 as DATA, LN3 as CLK.

The following is a reference circuit design for three-camera applications.

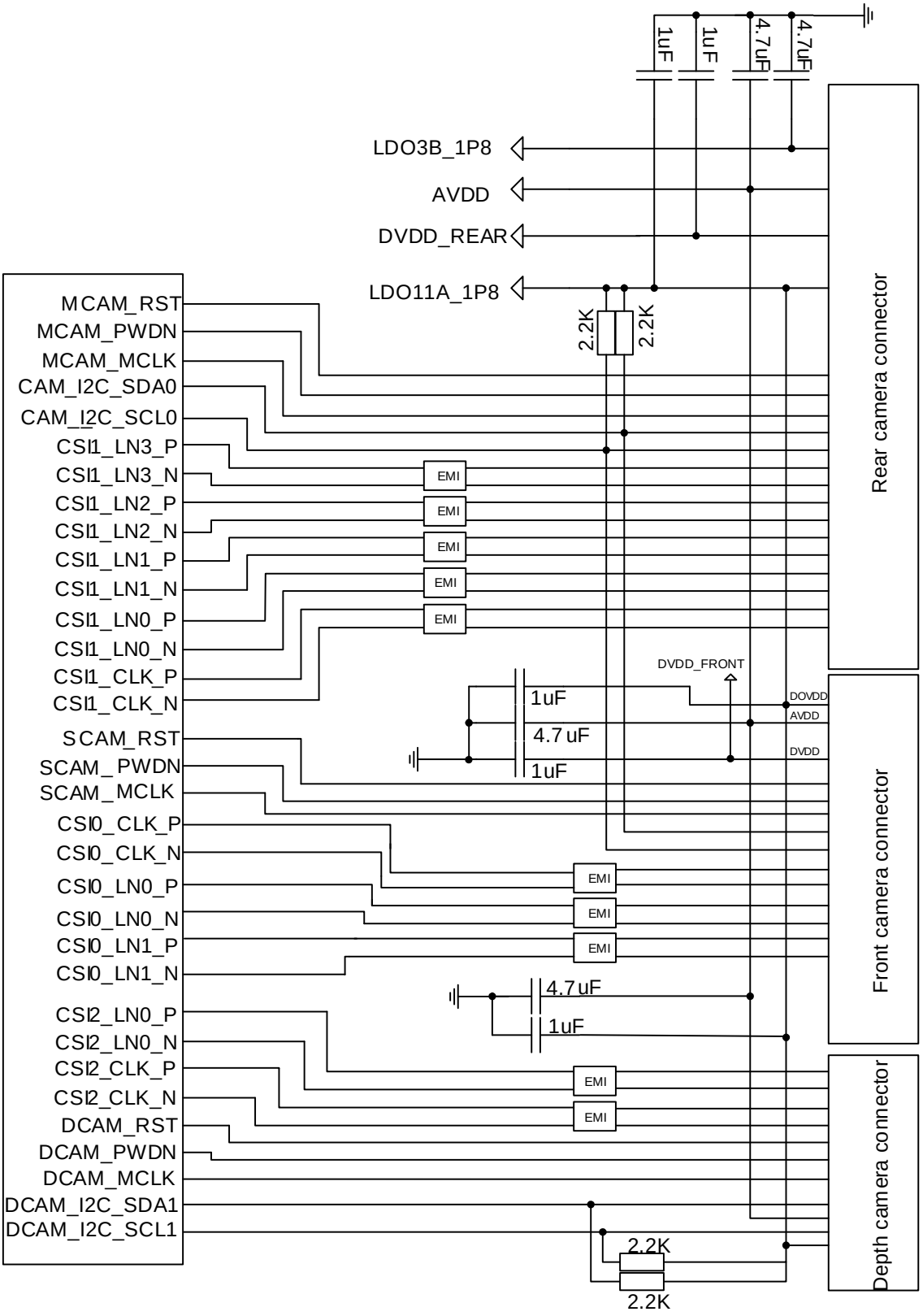


Figure 27: Reference Circuit Design for Three-Camera Applications

NOTE

CSI2 data lines CSI1_LN2_P, CSI_LN2_N, CSI_LN3_P and CSI_LN3_N can be multiplexed into MIPI signals for the fourth camera in four-camera application.

3.20.1. Design Considerations

- Special attention should be paid to the pin definition of LCM/camera connectors. Assure the SC66 and the connectors are correctly connected.
- MIPI are high speed signal lines, supporting maximum data rate up to 2.1Gbps. The differential impedance should be controlled as 85Ω. Additionally, it is recommended to route the trace on the inner layer of PCB, and do not cross it with other traces. For the same group of DSI or CSI signals, all the MIPI traces should keep the same length.
- CSI/DSI should reference the ground at all times,ground cuts and voids in the path of CSI/DSI signals should be avoided or removed.
- Route the camera CLK signal in the inner layer of the PCB between ground fills
- Spacing of the Lanes according to the following rules:
  a) intrapair p to n : 1*trace width
  b) Lane to Lane : 1.5*trace width
  c) to all other signals : 2.5*trace width
- Route MIPI traces according to the following rules:
  a) The CSI trace length should not exceed 170mm and the DSI trace length should not exceed 110mm;
  b) Control the differential impedance as 85Ω±10%;
  c) Control intra-lane length difference within 0.7mm;
  d) Control inter-lane length difference within 1.4mm.

Table 28: MIPI Trace Length Inside the Module

Pin	Signal	length	Length（P-N）
116	DSI0_CLK_N	27.37	-0.10
115	DSI0_CLK_P	27.27	
118	DSI0_LN0_N	27.03	0.04
117	DSI0_LN0_P	27.07	
120	DSI0_LN1_N	26.65	-0.05
119	DSI0_LN1_P	26.60	
122	DSI0_LN2_N	26.54	-0.01

121	DSI0_LN2_P	26.53	
124	DSI0_LN3_N	27.31	-0.01
123	DSI0_LN3_P	27.30	
103	DSI1_CLK_N	23.20	0.34
102	DSI1_CLK_P	23.54	
105	DSI1_LN0_N	27.89	0.14
104	DSI1_LN0_P	28.03	
107	DSI1_LN1_N	30.21	-0.30
106	DSI1_LN1_P	29.91	
109	DSI1_LN2_N	33.56	0.16
108	DSI1_LN2_P	33.40	
111	DSI1_LN3_N	37.35	-0.02
110	DSI1_LN3_P	37.33	
89	CSI1_CLK_N	16.00	0.02
88	CSI1_CLK_P	15.98	
91	CSI1_LN0_N	14.94	0.02
90	CSI1_LN0_P	14.96	
93	CSI1_LN1_N	12.23	-0.16
92	CSI1_LN1_P	12.07	
95	CSI1_LN2_N	10.69	-0.06
94	CSI1_LN2_P	10.75	
97	CSI1_LN3_N	9.42	-0.01
96	CSI1_LN3_P	9.43	
184	CSI2_CLK_N	17.46	-0.21
183	CSI2_CLK_P	17.67	
186	CSI2_LN0_N	15.33	0..02

185	CSI2_LN0_P	15.35	
188	CSI2_LN1_N	7.29	-0.03
187	CSI2_LN1_P	7.26	
190	CSI2_LN2_N	3.73	0.52
189	CSI2_LN2_P	4.25	
192	CSI2_LN3_N	6.77	0.27
191	CSI2_LN3_P	7.04	
78	CSI0_CLK_N	25.37	-0.03
77	CSI0_CLK_P	25.34	
80	CSI0_LN0_N	23.33	-0.10
79	CSI0_LN0_P	23.23	
82	CSI0_LN1_N	22.19	0.36
81	CSI0_LN1_P	22.55	
84	CSI0_LN2_N	20.06	-0.02
83	CSI0_LN2_P	20.04	
86	CSI0_LN3_N	18.33	-0.28
85	CSI0_LN3_P	18.05	

3.21. Sensor Interfaces

SC66 module supports communication with sensors via I2C interface, and it supports various sensors such as acceleration sensor, gyroscopic sensor, compass, optical sensor, temperature sensor.

Table 29: Pin Definition of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SENSOR_I2C_SCL	131	OD	I2C clock signal of external sensor	Dedicated

				used for sensors.
SENSOR_I2C_SDA	132	OD	I2C data signal of external sensor	It cannot be used for touch panel, NFC, I2C keyboard.
ALPS_INT	253	DI	Interrupt signal of optical sensor	
MAG_INT	254	DI	Interrupt signal of direction sensor (compass)	
ACCL_INT	252	DI	Interrupt signal of acceleration sensor	
GYRO_INT	255	DI	Interrupt signal of gyroscopic sensor	
HALL_INT	218	DI	Interrupt signal of Hall sensor	

3.22. Audio Interfaces

SC66 module provides three analog input channels and three analog output channels. The following table shows the pin definition.

Table 30: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC1_P	44	AI	Microphone positive input for Main Mic	
MIC1_N	45	AI	Microphone negative input for Main Mic	
MIC_GND	168		Microphone reference ground	If unused, connect this pin to the ground.
MIC2_P	46	AI	Microphone positive input for headset	
MIC3_P	169	AI	Microphone positive input for secondary mic	
MIC_BIAS	167	AO	Microphone bias voltage	
EAR_P	53	AO	Earpiece positive output	
EAR_N	52	AO	Earpiece negative output	
SPK_P	55	AO	Speaker positive output	

SPK_N	54	AO	Speaker negative output	
HPH_R	51	AO	Headphone right channel output	
HPH_REF	50	AI	Headphone reference ground	
HPH_L	49	AO	Headphone left channel output	
HS_DET	48	AI	Headset insertion detection	High level by default.

- The module offers three audio input channels, including one differential input pair and two single-ended channels. The three sets of MICs are integrated with internal bias voltage.
- The output voltage range of MIC_BIAS is programmable between 1.6V and 2.9V, and the maximum output current is 3mA.
- The earpiece interface uses differential output.
- The loudspeaker interface uses differential output as well. The output channel is available with a Class-D amplifier whose maximum output power is 1.5W when load is 8Ω.
- The headphone interface features stereo left and right channel output, and headphone insertion detection function is supported.

3.22.1. Reference Circuit Design for Microphone Interfaces

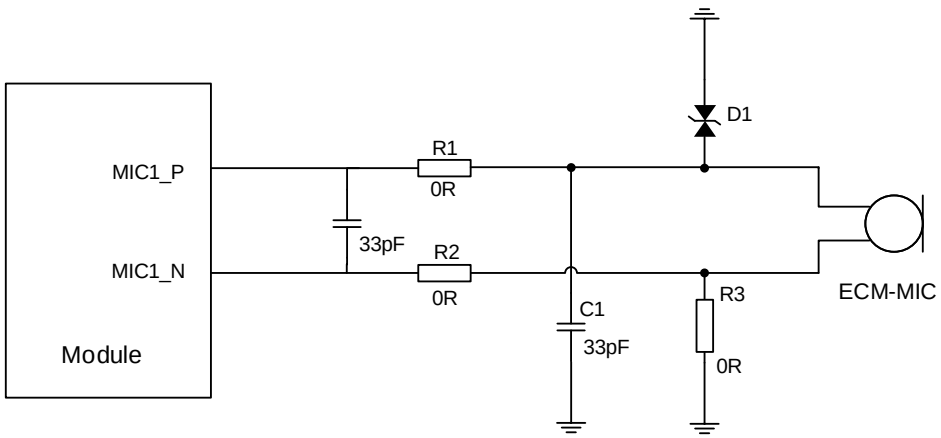


Figure 28: Reference Circuit Design for Analog ECM-type Microphone

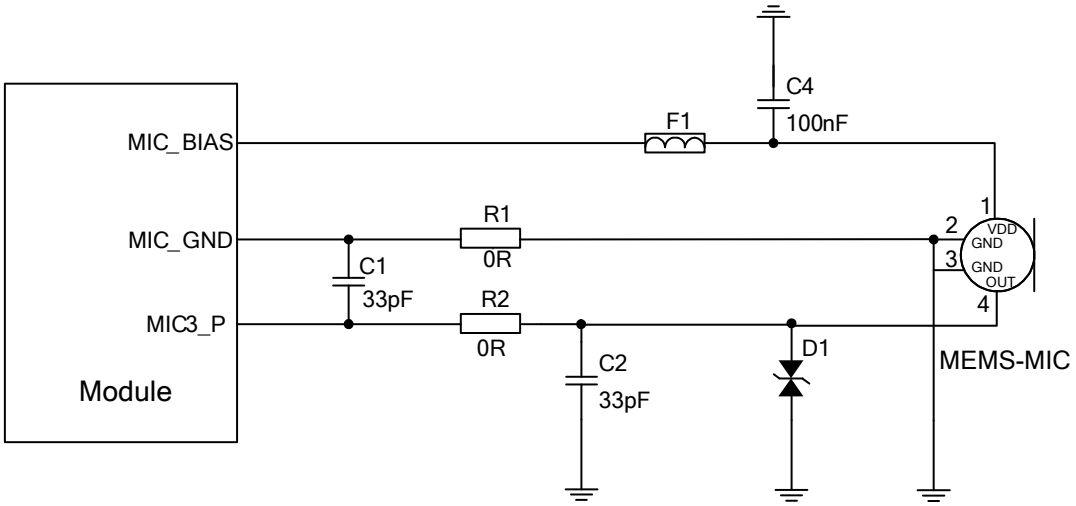


Figure 29: Reference Circuit Design for MEMS-type Microphone

3.22.2. Reference Circuit Design for Earpiece Interface

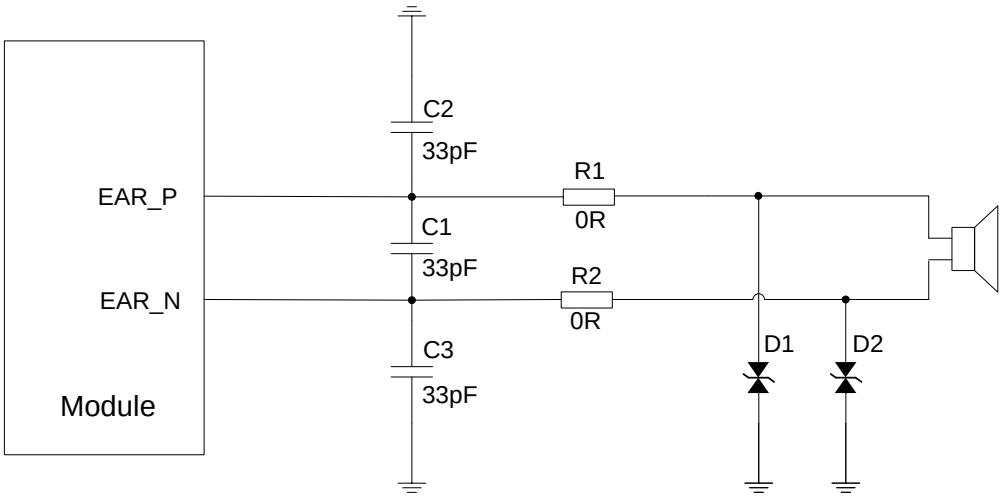


Figure 30: Reference Circuit Design for Earpiece IInterface

3.22.3. Reference Circuit Design for Headphone Interface

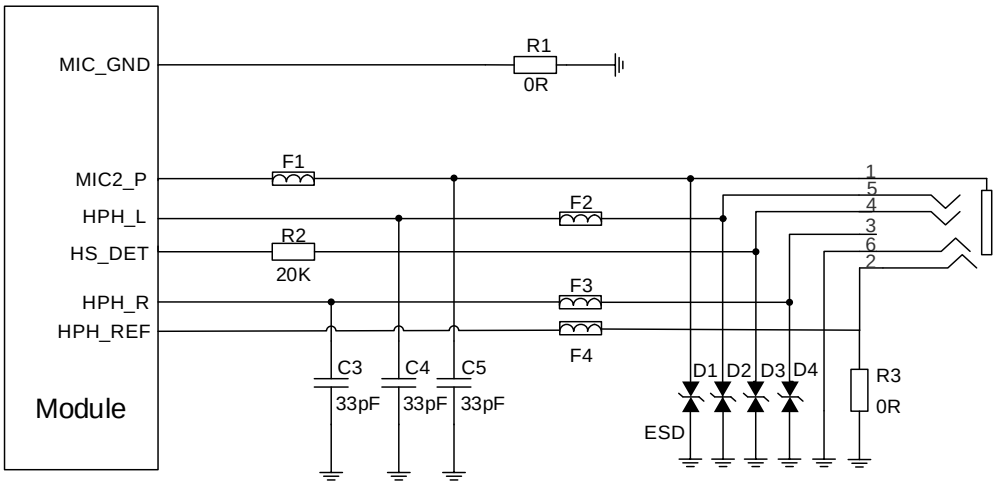


Figure 31: Reference Circuit Design for Headphone Interface

3.22.4. Reference Circuit Design for Loudspeaker Interface

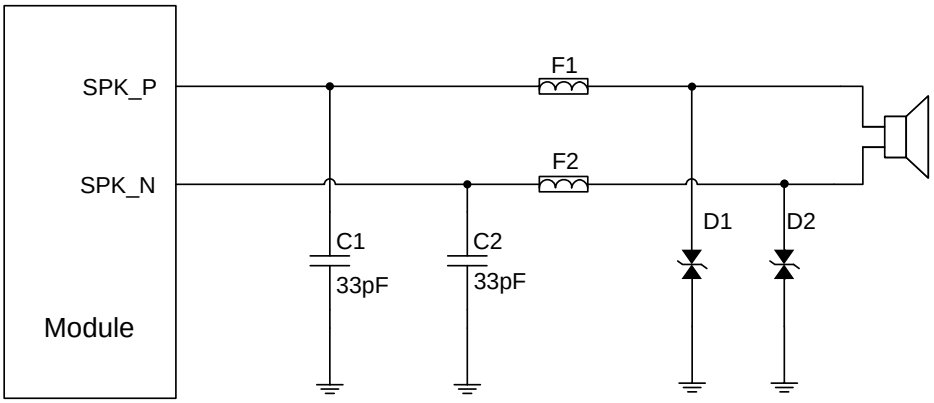


Figure 32: Reference Circuit Design for Loudspeaker Interface

3.22.5. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10pF and 33pF) for filtering out RF interference, thus reducing TDD noise. The 33pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10pF capacitor here is used for filtering out RF interference at DCS1800. Please note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, customers would have to discuss with their capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required.

In order to decrease radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces cannot be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

3.23. Emergency Download Interface

USB_BOOT is an emergency download interface. Pull up to LDO13A_1P8 during power-up will force the module enter into emergency download mode. This is an emergency option when there are failures such as abnormal startup or operation. For convenient firmware upgrade and debugging in the future, please reverse the reference circuit design shown as below.

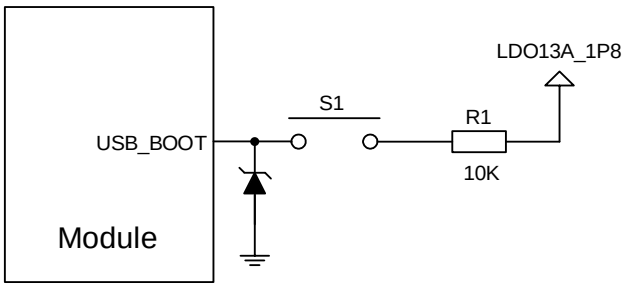


Figure 33: Reference Circuit Design for Emergency Download Interface

4 Wi-Fi and BT

SC66 module provides two shared antenna interface ANT_WIFI/BT and ANT_WIFI_MIMO for Wi-Fi and Bluetooth (BT) functions(SC66-CE and SC66-W just support ANT_WIFI/BT). The interface impedance is 50Ω. External antennas such as PCB antenna, sucker antenna and ceramic antenna can be connected to the module via the interface, so as to achieve Wi-Fi and BT functions.

4.1. Wi-Fi Overview

SC66 module supports 2.4GHz and 5GHz dual-band WLAN wireless communication based on IEEE 802.11a/b/g/n/ac standard protocols. The maximum data rate is up to 433Mbps.

The features are as below:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI SMS4 hardware encryption
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40
- Support MCS 0-8 for VHT20
- Support MCS 0-9 for VHT40 and VHT80

4.1.1. Wi-Fi Performance

The following table lists the Wi-Fi transmitting and receiving performance of SC66 module.

Table 31: Wi-Fi Transmitting Performance

	Standard	Rate	Output Power
2.4GHz	802.11b	1Mbps	16dBm±2.5dB
	802.11b	11Mbps	16dBm±2.5dB
	802.11g	6Mbps	16dBm±2.5dB

	802.11g	54Mbps	14dBm±2.5dB
	802.11n HT20	MCS0	15dBm±2.5dB
	802.11n HT20	MCS7	13dBm±2.5dB
	802.11n HT40	MCS0	14dBm±2.5dB
	802.11n HT40	MCS7	13dBm±2.5dB
5GHz	802.11a	6Mbps	15dBm±2.5dB
	802.11a	54Mbps	13dBm±2.5dB
	802.11n HT20	MCS0	15dBm±2.5dB
	802.11n HT20	MCS7	13dBm±2.5dB
	802.11n HT40	MCS0	15dBm±2.5dB
	802.11n HT40	MCS7	13dBm±2.5dB
	802.11ac VHT20	MCS0	14dBm±2.5dB
	802.11ac VHT20	MCS8	13dBm±2.5dB
	802.11ac VHT40	MCS0	13dBm±2.5dB
	802.11ac VHT40	MCS9	12dBm±2.5dB
	802.11ac VHT80	MCS0	13dBm±2.5dB
	802.11ac VHT80	MCS9	12dBm±2.5dB

Table 32: Wi-Fi Receiving Performance

	Standard	Rate	Sensitivity
2.4GHz	802.11b	1Mbps	-96dBm
	802.11b	11Mbps	-87dBm
	802.11g	6Mbps	-91dBm
	802.11g	54Mbps	-73dBm
	802.11n HT20	MCS0	-90dBm

	802.11n HT20	MCS7	-72dBm
	802.11n HT40	MCS0	-87dBm
	802.11n HT40	MCS7	-68dBm
5GHz	802.11a	6Mbps	-90dBm
	802.11a	54Mbps	-70dBm
	802.11n HT20	MCS0	-88dBm
	802.11n HT20	MCS7	-69dBm
	802.11n HT40	MCS0	-86dBm
	802.11n HT40	MCS7	-66dBm
	802.11ac VHT20	MCS8	-68dBm
	802.11ac VHT40	MCS9	-64dBm
	802.11ac VHT80	MCS9	-60dBm

Reference specifications are listed below:

- IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11d, IEEE Std 802.11e, IEEE Std 802.11g, IEEE Std 802.11i: IEEE 802.11-2007 WLAN MAC and PHY, June 2007

4.2. BT Overview

SC66 module supports BT4.2 (BR/EDR+BLE) specifications, as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally support up to 7 wireless connections
- Maximally support up to 3.5 piconets at the same time
- Support one SCO or eSCO (Extended Synchronous Connection Oriented) connection

The BR/EDR channel bandwidth is 1MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2MHz, and can accommodate 40 channels.

Table 33: BT Data Rate and Versions

Version	Data rate	Maximum Application	Throughput	Comment
1.2	1Mbit/s	> 80Kbit/s		
2.0+EDR	3Mbit/s	> 80Kbit/s		
3.0+HS	24Mbit/s	Reference to 3.0+HS		
4.0	24Mbit/s	Reference to 4.0 LE		
5.0	48Mbit/S	Reference to 5.0 LE		

Reference specifications are listed below:

- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth 5.0 RF-PHY Cover Standard：RF-PHY.TS.5.0.0, December 06, 2016

4.2.1. BT Performance

The following table lists the BT transmitting and receiving performance of SC66 module.

Table 34: BT Transmitting and Receiving Performance

Transmitter Performance			
Packet Types	DH5	2-DH5	3-DH5
Transmitting Power	10dBm±2.5dB	8dBm±2.5dB	8dBm±2.5dB
Receiver Performance			
Packet Types	DH5	2-DH5	3-DH5
Receiving Sensitivity	-92dBm	-91dBm	-83dBm

5 GNSS

SC66 module integrates a Qualcomm IZat™ GNSS engine (Gen 9) which supports multiple positioning and navigation systems including GPS, GLONASS and BeiDou. With an embedded LNA, the module provides greatly improved positioning accuracy.

5.1. GNSS Performance

The following table lists the GNSS performance of SC66 module in conduction mode.

Table 35: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity (GNSS)	Cold start	TBD	dBm
	Reacquisition	TBD	dBm
	Tracking	TBD	dBm
TTFF (GNSS)	Cold start	TBD	s
	Warm start	TBD	s
	Hot start	TBD	s
Static Drift (GNSS)	CEP-50	TBD	m

5.2. GNSS RF Design Guidelines

Bad design of antenna and layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, or reduced positioning accuracy. In order to avoid these, please follow the design rules listed below:

- Maximize the distance between the GNSS RF part and the GPRS RF part (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, GNSS RF signal lines and RF components should be placed far away from high speed circuits, switched-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with harsh electromagnetic environment or high ESD-protection requirements, it is recommended to add ESD protective diodes for the antenna interface. Only diodes with ultra-low junction capacitance such as 0.5pF can be selected. Otherwise, there will be effects on the impedance characteristic of RF circuit loop, or attenuation of bypass RF signal may be caused.
- Control the impedance of either feeder line or PCB trace as 50Ω, and keep the trace length as short as possible.
- Refer to ***Chapter 6.3*** for GNSS antenna reference circuit designs.

6 Antenna Interfaces

SC66 provides five antenna interfaces for main antenna, Rx-diversity/MIMO antenna, GNSS antenna, Wi-Fi/BT antenna and WIFI_MIMO antenna. respectively. The antenna ports have an impedance of 50Ω.

6.1. Main/Rx-diversity Antenna Interfaces

The pin definition of main/Rx-diversity antenna interfaces is shown below.

Table 36: Pin Definition of Main/Rx-diversity Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	19	IO	Main antenna interface	50Ω impedance
ANT_DRX	149	AI	Diversity and MIMO antenna interface	50Ω impedance

The operating frequencies of SC66 module are listed in the following table.

Table 37: SC66-CE* Module Operating Frequencies

3GPP Band	Receive	Transmit	Unit
EGSM900	925~960	880~915	MHz
DCS1800	1805~1880	1710~1785	MHz
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B8	925~960	880~915	MHz
EVDO/CDMA BC0	869~894	824~849	MHz
TD-SCDMA B34	2010~2025	2010~2025	MHz
TD-SCDMA B39	1880~1920	1880~1920	MHz

LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz
LTE-FDD B5	824~849	869~894	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-TDD B34	2010~2025	2010~2025	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41 [1)]	2555~2655	2555~2655	MHz

Table 38: SC66-A* Module Operating Frequencies

频段	下行	上行	单位
WCDMA B2	1930~1990	1850~1910	MHz
WCDMA B4	2110~2155	1710~1755	MHz
WCDMA B5	871~892	826~847	MHz
LTE-FDD B2	1930~1990	1850~1910	MHz
LTE-FDD B4	2110~2155	1710~1755	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B7	2620~2690	2500~2570	MHz
LTE-FDD B12	729~746	699~716	MHz
LTE-FDD B13	746~756	777~787	MHz
LTE-FDD B14	758~768	788~798	MHz
LTE-FDD B17	734~746	704~716	MHz
LTE-FDD B25	1930~1995	1850~1915	MHz
LTE-FDD B26	859~894	814~849	MHz

LTE-FDD B66	2110~2200	1710~1780	MHz
LTE-FDD B71	617~652	663~698	MHz
LTE-TDD B41 [2)]	2496~2690	2496~2690	MHz

Table 39: SC66-J* Module Operating Frequencies

频段	下行	上行	单位
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B6	877~883	832~838	MHz
WCDMA B8	925~960	880~915	MHz
WCDMA B19	877~888	832~843	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-FDD B11	1476~1496	1428~1448	MHz
LTE-FDD B18	860~875	815~830	MHz
LTE-FDD B19	875~890	830~845	MHz
LTE-FDD B21	1496~1511	1448~1463	MHz
LTE-FDD B26	859~894	814~849	MHz
LTE-FDD B28	758~803	703~748	MHz
LTE-TDD B41 [1)]	2535~2655	2535~2655	MHz
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B6	877~883	832~838	MHz
WCDMA B8	925~960	880~915	MHz

Table 40: SC66-E* Module Operating Frequencies

频段	下行	上行	单位
GSM850	869~894	824~849	MHz
EGSM900	925~960	880~915	MHz
DCS1800	1805~1880	1710~1785	MHz
PCS1900	1930~1990	1850~1910	MHz
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B2	1930~1990	1850~1910	MHz
WCDMA B4	2110~2155	1710~1755	MHz
WCDMA B5	871~892	826~847	MHz
WCDMA B8	925~960	880~915	MHz
LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B2	1930~1990	1850~1910	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz
LTE-FDD B4	2110~2155	1710~1755	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B7	2620~2690	2500~2570	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-FDD B20	791~821	832~862	MHz
LTE-FDD B28	758~803	703~748	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41 [2)]	2496~2690	2496~2690	MHz

NOTE

1) The bandwidth of LTE-TDD B41 for SC66-CE and SC66-J is 120MHz (2535MHz~2655MHz), and the corresponding channel ranges from 40040 to 41240.

2) The bandwidth of LTE-TDD B41 for SC66-A and SC66-E is 200MHz (2496MHZ~2690MHz) , and the corresponding channel ranges from 39650~41589.

6.1.1. Main and Rx-diversity Antenna Interfaces Reference Design

A reference circuit design for main and Rx-diversity antenna interfaces is shown as below. A π-type matching circuit should be reserved for better RF performance, and the π-type matching components (R1/C1/C2, R2/C3/C4) should be placed as close to the antennas as possible. The capacitors are not mounted by default and resistors are 0Ω.

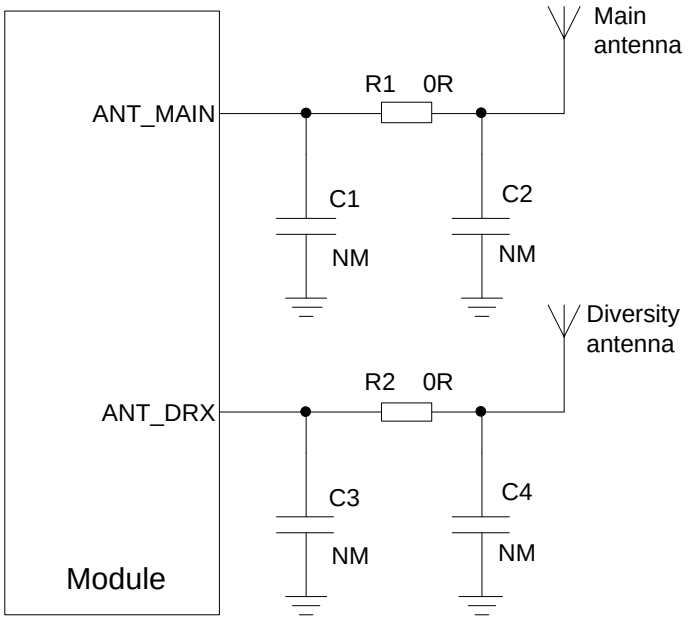


Figure 34: Reference Circuit Design for Main and Rx-diversity Antenna Interfaces

6.1.2. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the distance between signal layer and reference ground (H), and the clearance between RF trace and ground (S). Microstrip line or coplanar waveguide line is typically used in RF layout for characteristic

impedance control. The following are reference designs of microstrip line or coplanar waveguide line with different PCB structures.

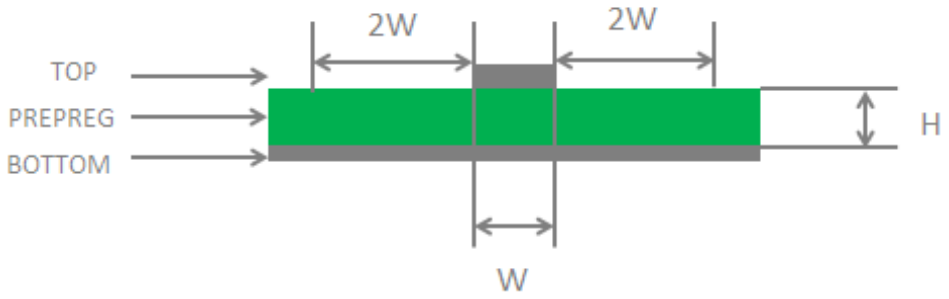


Figure 35: Microstrip Line Design on a 2-layer PCB

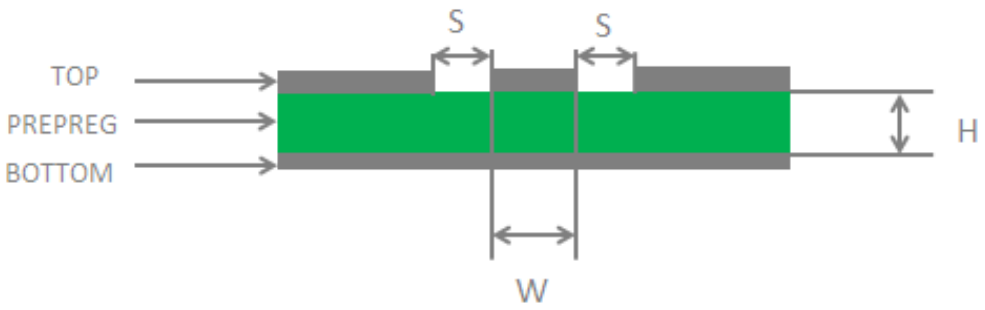


Figure 36: Coplanar Waveguide Line Design on a 2-layer PCB

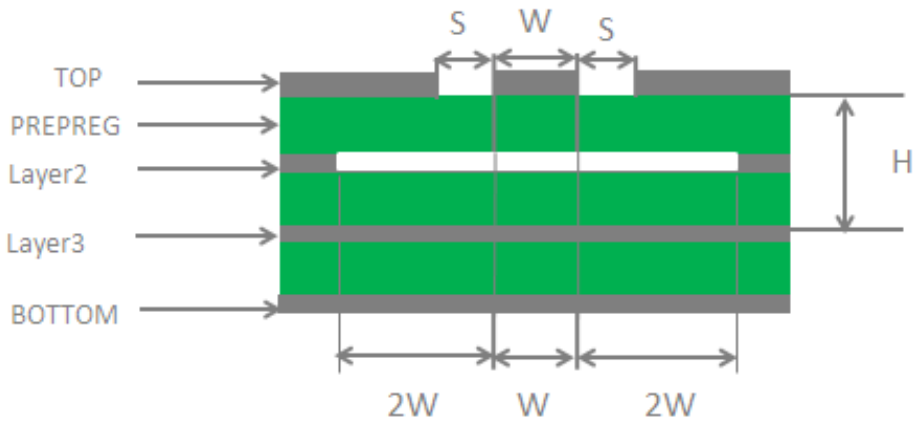


Figure 37: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

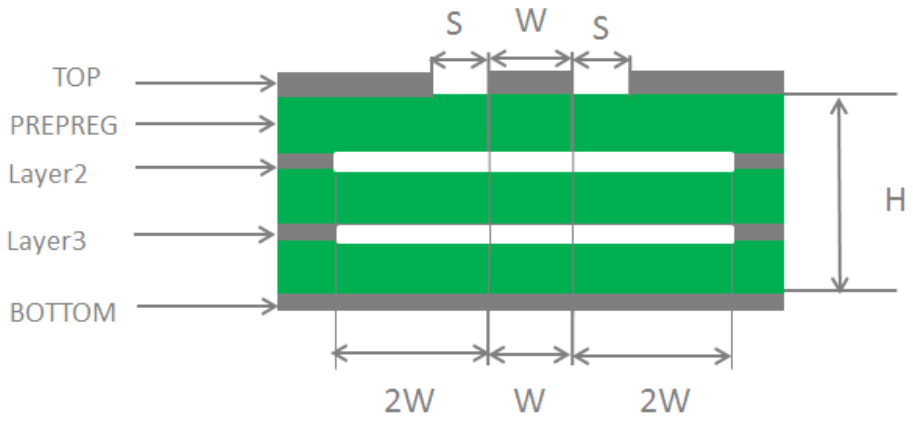


Figure 38: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedance of RF traces to 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [3]***.

6.2. Wi-Fi/BT Antenna Interface

Table 41: Pin Definition of Wi-Fi/BT Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	129	IO	Wi-Fi/BT antenna interface	50Ω impedance
ANT_WIFI_MIMO[1)]	324	IO	Wi-Fi_MIMO antenna interface	50Ω impedance

NOTE

1) SC66-CE and SC66-W do not support ANT_WIFI_MIMO

Table 42: Wi-Fi/BT Frequency

Type	Frequency	Unit
802.11a/b/g/n/ac	2402~2482 5180~5825	MHz
BT5.0	2402~2480	MHz

A reference circuit design for Wi-Fi/BT antenna interface is shown as below. A π-type matching circuit is recommended to be reserved for better RF performance. The capacitors are not mounted by default and resistors are 0Ω.

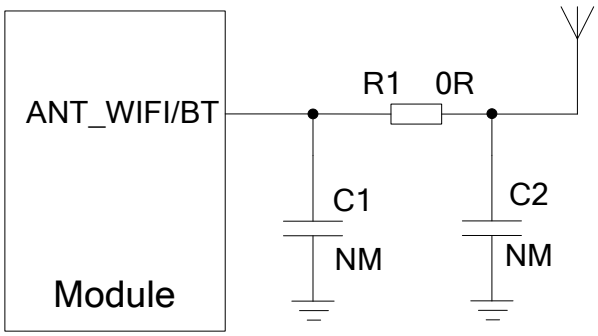


Figure 39: Reference Circuit Design for Wi-Fi/BT Antenna Interface

6.3. GNSS Antenna Interface

Table 43: Pin Definition of GNSS Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	134	AI	GNSS antenna Interface	50Ω impedance

GNSS_LNA_EN	202	DO	LNA enable control	For test purpose only. If unused, keep it open.

Table 44: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098±2.046	MHz

6.3.1. Recommended Circuit for Passive Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference circuit design is given below.

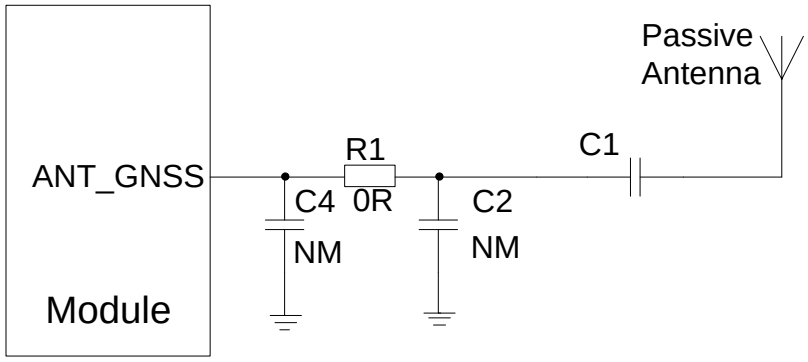


Figure 40: Reference Circuit Design for GNSS Passive Antenna

NOTE

When the passive antenna is placed far away from the module (that is, the antenna trace is long), it is recommended to add an external LNA circuit for better GNSS receiving performance, and the LNA should be placed close to the antenna.

6.3.2. Recommended Circuit for Active Antenna

The active antenna is powered by a 56nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3V to 5.0V. Although featuring low power consumption, the active antenna still requires stable and clean power supplies. It is recommended to use high performance LDO as the power supply. A reference design of GNSS active antenna is shown below.

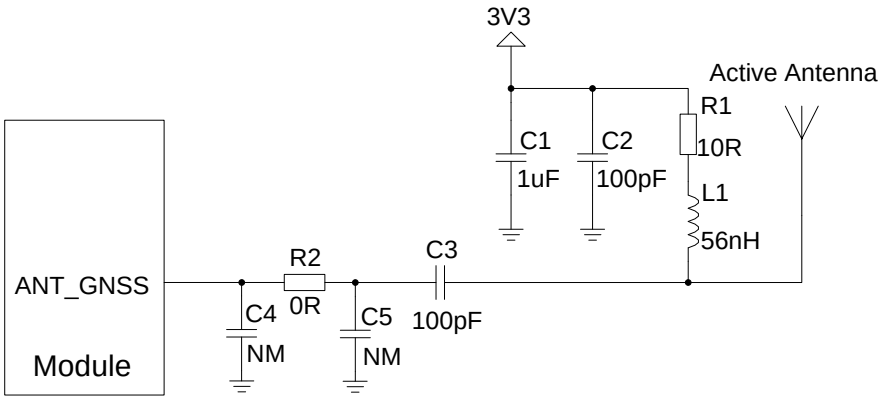


Figure 41: Reference Circuit Design for GNSS Active Antenna

6.4. Antenna Installation

6.4.1. Antenna Requirements

The following table shows the requirements on main antenna, Rx-diversity, Wi-Fi/BT antenna and GNSS antenna.

Table 45: Antenna Requirements

Antenna Type	Requirements
GSM/WCDMA/TD-SCDMA/ LTE	VSWR: ≤ 2 Gain (dBi): 1 Max Input Power (W): 50 Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: < 1dB (frequency：663-960 MHz) Cable Insertion Loss: < 1.5dB(frequency：1427-2200 MHz) Cable Insertion Loss: < 2dB (frequency：2300-2690 MHz)
Wi-Fi/BT	VSWR: ≤ 2 Gain (dBi): 1 Max Input Power (W): 50

	Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: < 1dB
GNSS [1)]	Frequency range: 1559MHz~1609MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive Antenna Gain: > 0dBi Active Antenna Noise Figure: < 1.5dB (Typ.) Active Antenna Gain: > -2dBi Active Antenna Embedded LNA Gain: < 17dB (Typ.) Active Antenna Total Gain: < 17dBi (Typ.)

NOTE

[1)] It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

6.4.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by HIROSE.

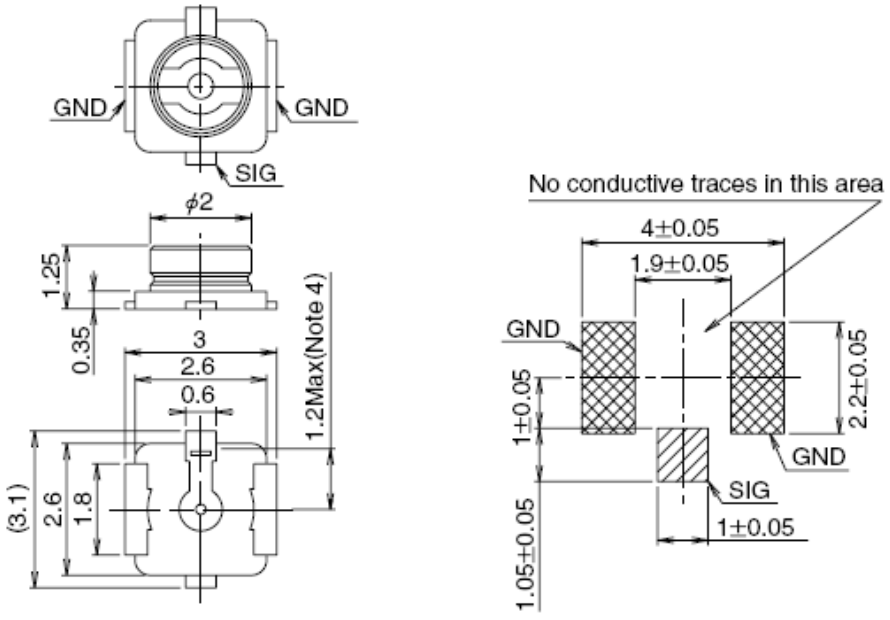


Figure 42: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

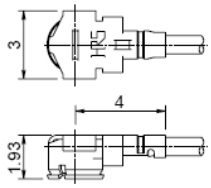
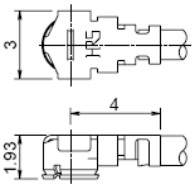
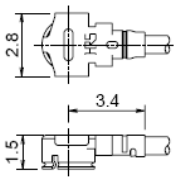
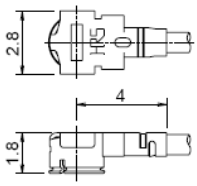
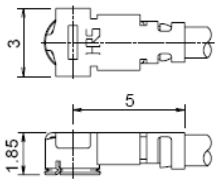
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 43: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

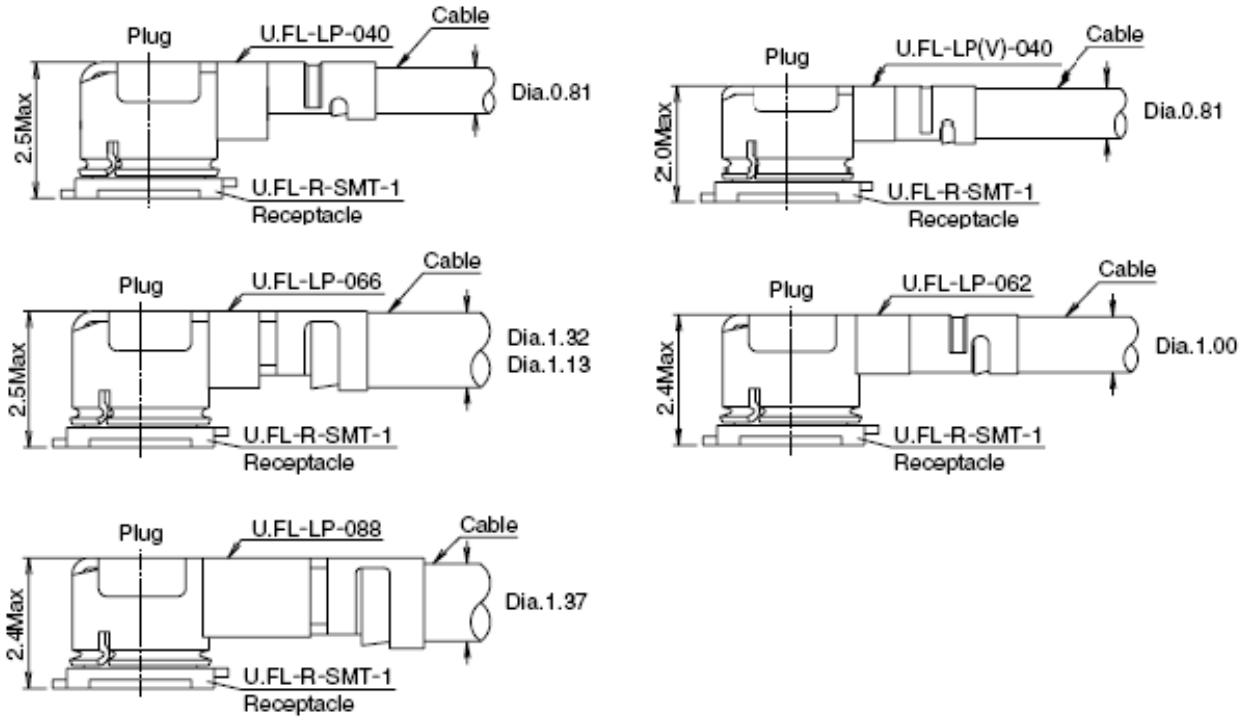


Figure 44: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

7 Electrical, Reliability and Radio Characteristics

7.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 46: Absolute Maximum Ratings

Parameter	Min	Max	Unit
VBAT	-0.5	6	V
USB_VBUS	-0.5	16	V
Current on VBAT	0	3	A
Voltage on Digital Pins	-0.3	2.3	V

7.2. Power Supply Ratings

Table 47: SC66 Module Power Supply Ratings

Parameter	Description	Conditions	Min	Typ.	Max	Unit
VBAT	VBAT	The actual input voltages must stay between the minimum and maximum values.	3.55	4.0	4.4	V
	Voltage drop during transmitting burst	Maximum power control level at EGSM900			400	mV

I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level at EGSM900		1.8	3.0	A
USB_VBUS			3.6	5.0	10	V
VRTC	Power supply voltage of backup battery.		2.0	3.0	3.25	V

7.3. Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 48: Operation and Storage Temperatures

Parameter	Min	Typ.	Max	Unit
Operating temperature range [1)]	-35	+25	+65	°C
Extended temperature range [2)]	-40		+75	°C
Storage temperature range	-40		+90	°C

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

7.4. Current Consumption

Table 49: SC66-CE* Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{VBAT}	OFF state	Power down		70		uA
	GSM/GPRS supply current	Sleep (USB disconnected) @DRX=2		4.3		mA
		Sleep (USB disconnected) @DRX=5		3.4		mA
		Sleep (USB disconnected) @DRX=9		3.3		mA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6		3.98		mA
		Sleep (USB disconnected) @DRX=8		3.2		mA
		Sleep (USB disconnected) @DRX=9		3.08		mA
	CDMA supply current	BC0 CH283 @Slot Cycle Index=1		4.67		mA
		BC0 CH283 @Slot Cycle Index=7		3.84		mA
	TD-SCDMA supply current	Sleep (USB disconnected) @DRX=6		4.4		mA
		Sleep (USB disconnected) @DRX=8		3.6		mA
		Sleep (USB disconnected) @DRX=9		3.3		mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=6		7.2		mA
		Sleep (USB disconnected) @DRX=8		4.8		mA
		Sleep (USB disconnected) @DRX=9		4.3		mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6		7.8		mA
		Sleep (USB disconnected) @DRX=8		5.2		mA
		Sleep (USB disconnected) @DRX=9		4.2		mA

	GSM voice call	EGSM900 @PCL 5	280	mA
		EGSM900 @PCL 12	140	mA
		EGSM900 @PCL 19	120	mA
		DCS1800 @PCL 0	200	mA
		DCS1800 @PCL 7	150	mA
		DCS1800 @PCL 15	130	mA
	WCDMA voice call	B1 @max power	600	mA
		B8 @max power	650	mA
	GPRS data transfer	EGSM900 (1UL/4DL) @PCL 5	300	mA
		EGSM900 (2UL/3DL) @PCL 5	460	mA
		EGSM900 (3UL/2DL) @PCL 5	590	mA
		EGSM900 (4UL/1DL) @PCL 5	630	mA
		DCS1800 (1UL/4DL) @PCL 0	220	mA
		DCS1800 (2UL/3DL) @PCL 0	320	mA
		DCS1800 (3UL/2DL) @PCL 0	430	mA
		DCS1800 (4UL/1DL) @PCL 0	540	mA
	EDGE data transfer	EGSM900 (1UL/4DL) @PCL 8	250	mA
		EGSM900 (2UL/3DL) @PCL 8	430	mA
		EGSM900 (3UL/2DL) @PCL 8	510	mA
		EGSM900 (4UL/1DL) @PCL 8	600	mA
		DCS1800 (1UL/4DL) @PCL 2	200	mA
		DCS1800 (2UL/3DL) @PCL 2	300	mA
		DCS1800 (3UL/2DL) @PCL 2	380	mA
		DCS1800 (4UL/1DL) @PCL 2	480	mA
	WCDMA data transfer	B1 (HSDPA) @max power	570	mA
		B8 (HSDPA) @max power	540	mA
		B1 (HSUPA) @max power	550	mA
		B8 (HSUPA) @max power	620	mA
	EVDO/CDMA data transfer	BC0 @max power	550	mA
	TD-SCDMA data transfer	TD-SCDMA B34 @max power	160	mA
		TD-SCDMA B39 @max power	160	mA

	LTE data transfer	LTE-FDD B1 @max power	550	mA
		LTE-FDD B3 @max power	550	mA
		LTE-FDD B5 @max power	550	mA
		LTE-FDD B8 @max power	580	mA
		LTE-TDD B34 @max power	300	mA
		LTE-TDD B38 @max power	350	mA
		LTE-TDD B39 @max power	280	mA
		LTE-TDD B40 @max power	330	mA
		LTE-TDD B41 @max power	350	mA

Table 50: SC66-A* Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
OFF state	Power down	OFF state				uA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6				mA
		Sleep (USB disconnected) @DRX=8				mA
		Sleep (USB disconnected) @DRX=9				mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=6				mA
		Sleep (USB disconnected) @DRX=8				mA
		Sleep (USB disconnected) @DRX=9				mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6				mA
		Sleep (USB disconnected) @DRX=8				mA
		Sleep (USB disconnected) @DRX=9				mA
	WCDMA voice call	B2 @max power				mA
		B4 @max power				mA
		B5 @max power				mA

	WCDMA data transfer	B2 (HSDPA) @max power	mA
		B4 (HSDPA) @max power	mA
		B5 (HSDPA) @max power	mA
		B2 (HSUPA) @max power	mA
		B4 (HSUPA) @max power	mA
		B5(HSUPA) @max power	mA
	LTE data transfer	LTE-FDD B2 @max power	mA
		LTE-FDD B4 @max power	mA
		LTE-FDD B5 @max power	mA
		LTE-FDD B7 @max power	mA
		LTE-TDD B12 @max power	mA
		LTE-TDD B13 @max power	mA
		LTE-TDD B14 @max power	mA
		LTE-TDD B17 @max power	mA
		LTE-TDD B25 @max power	mA
		LTE-TDD B26 @max power	mA
		LTE-TDD B66 @max power	mA
		LTE-TDD B71 @max power	mA
		LTE-TDD B41 @max power	mA

Table 51: SC66-J* Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
OFF	Power down	OFF state				uA

state	WCDMA supply current	Sleep (USB disconnected) @DRX=6	mA
		Sleep (USB disconnected) @DRX=8	mA
		Sleep (USB disconnected) @DRX=9	mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=6	mA
		Sleep (USB disconnected) @DRX=8	mA
		Sleep (USB disconnected) @DRX=9	mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6	mA
		Sleep (USB disconnected) @DRX=8	mA
		Sleep (USB disconnected) @DRX=9	mA
	WCDMA voice call	B1 @max power	mA
		B6 @max power	mA
		B8 @max power	mA
		B19 @max power	mA
	WCDMA data transfer	B1 (HSDPA) @max power	mA
		B6 (HSDPA) @max power	mA
		B8 (HSDPA) @max power	mA
		B19 (HSDPA) @max power	mA
		B1 (HSUPA) @max power	mA
		B6 (HSUPA) @max power	mA
		B8 (HSUPA) @max power	mA
		B19 (HSUPA) @max power	mA
	LTE data transfer	LTE-FDD B1 @max power	mA
		LTE-FDD B3 @max power	mA

	LTE-FDD B5 @max power	mA
	LTE-FDD B8 @max power	mA
	LTE-FDD B11 @max power	mA
	LTE-FDD B18 @max power	mA
	LTE-TDD B19 @max power	mA
	LTE-TDD B21 @max power	mA
	LTE-TDD B26 @max power	mA
	LTE-TDD B28 @max power	mA
	LTE-TDD B41 @max power	mA

Table 52: SC66-E* Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
OFF state	Power down	OFF state				uA
	GSM/GPRS supply current	Sleep (USB disconnected) @DRX=2				mA
		Sleep (USB disconnected) @DRX=5				mA
		Sleep (USB disconnected) @DRX=9				mA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6				mA
		Sleep (USB disconnected) @DRX=8				mA
		Sleep (USB disconnected) @DRX=9				mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=6				mA
		Sleep (USB disconnected) @DRX=8				mA
		Sleep (USB disconnected) @DRX=9				mA

	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6	mA
		Sleep (USB disconnected) @DRX=8	mA
		Sleep (USB disconnected) @DRX=9	mA
	GSM voice call	GSM850 @PCL 5	mA
		GSM850 @PCL 12	mA
		GSM850 @PCL 19	mA
		EGSM900 @PCL 5	mA
		EGSM900 @PCL 12	mA
		EGSM900 @PCL 19	mA
		DCS1800 @PCL 0	mA
		DCS1800 @PCL 7	mA
		DCS1800 @PCL 15	mA
		PCS1900 @PCL 0	mA
		PCS1900 @PCL 7	mA
		PCS1900 @PCL 15	mA
	WCDMA voice call	B1 @max power	mA
		B2 @max power	mA
		B4 @max power	mA
		B5 @max power	mA
		B8 @max power	mA
	GPRS data transfer	GSM850 (1UL/4DL) @PCL 5	mA
		GSM850 (2UL/3DL) @PCL 5	mA
		GSM850 (3UL/2DL) @PCL 5	mA
		GSM850 (4UL/1DL) @PCL 5	mA
		EGSM900 (1UL/4DL) @PCL 5	mA

		EGSM900 (2UL/3DL) @PCL 5	mA
		EGSM900 (3UL/2DL) @PCL 5	mA
		EGSM900 (4UL/1DL) @PCL 5	mA
		DCS1800 (1UL/4DL) @PCL 0	mA
		DCS1800 (2UL/3DL) @PCL 0	mA
		DCS1800 (3UL/2DL) @PCL 0	mA
		DCS1800 (4UL/1DL) @PCL 0	mA
		PCS1900 (1UL/4DL) @PCL 0	mA
		PCS1900 (2UL/3DL) @PCL 0	mA
		PCS1900 (3UL/2DL) @PCL 0	mA
		PCS1900 (4UL/1DL) @PCL 0	mA
	EDGE data transfer	GSM850 (1UL/4DL) @PCL 8	mA
		GSM850 (2UL/3DL) @PCL 8	mA
		GSM850 (3UL/2DL) @PCL 8	mA
		GSM850 (4UL/1DL) @PCL 8	mA
		EGSM900 (1UL/4DL) @PCL 8	mA
		EGSM900 (2UL/3DL) @PCL 8	mA
		EGSM900 (3UL/2DL) @PCL8	mA
		EGSM900 (4UL/1DL) @PCL 8	mA
		DCS1800 (1UL/4DL) @PCL 2	mA
		DCS1800 (2UL/3DL) @PCL 2	mA
		DCS1800 (3UL/2DL) @PCL 2	mA
		DCS1800 (4UL/1DL) @PCL 2	mA
		PCS1900 (1UL/4DL) @PCL 2	mA
		PCS1900 (2UL/3DL) @PCL 2	mA

		PCS1900 (3UL/2DL) @PCL 2	mA
		PCS1900 (4UL/1DL) @PCL 2	mA
	WCDMA data transfer	B1 (HSDPA) @max power	mA
		B2 (HSDPA) @max power	mA
		B4 (HSDPA) @max power	mA
		B5 (HSDPA) @max power	mA
		B8 (HSDPA) @max power	mA
		B1 (HSUPA) @max power	mA
		B2 (HSUPA) @max power	mA
		B4 (HSUPA) @max power	mA
		B5 (HSUPA) @max power	mA
		B8 (HSUPA) @max power	mA
	LTE data transfer	LTE-FDD B1 @max power	mA
		LTE-FDD B2 @max power	mA
		LTE-FDD B3 @max power	mA
		LTE-FDD B4 @max power	mA
		LTE-FDD B5 @max power	mA
		LTE-FDD B7 @max power	mA
		LTE-FDD B8 @max power	mA
		LTE-FDD B20 @max power	mA
		LTE-FDD B28 @max power	mA
		LTE-TDD B41 @max power	mA

7.5. RF Output Power

The following table shows the RF output power of SC66 module.

Table 53: SC66-CE* RF Output Power

Frequency	Max	Min
EGSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
WCDMA B1	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
EVDO/CDMA BC0	24dBm+3/-1dB	<-49dBm
TD-SCDMA B34	24dBm+1/-3dB	<-49dBm
TD-SCDMA B39	24dBm+1/-3dB	<-49dBm
LTE-FDD B1	23dBm±2dB	<-39dBm
LTE-FDD B3	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B8	23dBm±2dB	<-39dBm
LTE-FDD B34	23dBm±2dB	<-39dBm
LTE-TDD B38	23dBm±2dB	<-39dBm
LTE-TDD B39	23dBm±2dB	<-39dBm
LTE-TDD B40	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

Table 54: SC66-A* RF Output Power

Frequency	Max	Min
WCDMA B2	24dBm+1/-3dB	<-49dBm
WCDMA B4	24dBm+1/-3dB	<-49dBm

WCDMA B5	24dBm+1/-3dB	<-49dBm
LTE-FDD B2	23dBm±2dB	<-39dBm
LTE-FDD B4	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B7	23dBm±2dB	<-39dBm
LTE-FDD B12	23dBm±2dB	<-39dBm
LTE-FDD B13	23dBm±2dB	<-39dBm
LTE-FDD B14	23dBm±2dB	<-39dBm
LTE-FDD B17	23dBm±2dB	<-39dBm
LTE-FDD B25	23dBm±2dB	<-39dBm
LTE-FDD B66	23dBm±2dB	<-39dBm
LTE-TDD B71	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

Table 55: SC66-J* RF Output Power

Frequency	Max	Min
WCDMA B1	24dBm+1/-3dB	<-49dBm
WCDMA B6	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
WCDMA B19	24dBm+1/-3dB	<-49dBm
LTE-FDD B1	23dBm±2dB	<-39dBm
LTE-FDD B3	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B8	23dBm±2dB	<-39dBm

LTE-FDD B11	23dBm±2dB	<-39dBm
LTE-FDD B18	23dBm±2dB	<-39dBm
LTE-FDD B19	23dBm±2dB	<-39dBm
LTE-FDD B21	23dBm±2dB	<-39dBm
LTE-TDD B26	23dBm±2dB	<-39dBm
LTE-TDD B28	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

Table 56: SC66-E* RF Output Power

Frequency	Max	Min
GSM850	33dBm±2dB	5dBm±5dB
EGSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
PCS1900	30dBm±2dB	0dBm±5dB
WCDMA B1	24dBm+1/-3dB	<-49dBm
WCDMA B2	24dBm+1/-3dB	<-49dBm
WCDMA B4	24dBm+1/-3dB	<-49dBm
WCDMA B5	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
LTE-FDD B1	23dBm±2dB	<-39dBm
LTE-FDD B2	23dBm±2dB	<-39dBm
LTE-FDD B3	23dBm±2dB	<-39dBm
LTE-FDD B4	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm

LTE-FDD B7	23dBm±2dB	<-39dBm
LTE-FDD B8	23dBm±2dB	<-39dBm
LTE-FDD B20	23dBm±2dB	<-39dBm
LTE-FDD B28	23dBm±2dB	<-39dBm
LTE-TDD B38	23dBm±2dB	<-39dBm
LTE-TDD B39	23dBm±2dB	<-39dBm
LTE-TDD B40	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

In GPRS 4 slots TX mode, the maximum output power is reduced by 3dB. This design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

7.6. RF Receiving Sensitivity

The following table shows the conducted RF receiving sensitivity of SC66 module.

Table 57: SC66-CE* RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
EGSM900	-109dBm	/	/	-102.4dBm
DCS1800	-108dBm	/	/	-102.4dBm
WCDMA B1	-110dBm	/	/	-106.7dBm
WCDMA B8	-110dBm	/	/	-103.7dBm
EVDO/CDMA BC0	-109dBm	/	/	-104dBm

TD-SCDMA B34	-109dBm	/	/	-108dBm
TD-SCDMA B39	-109dBm	/	/	-108dBm
LTE-FDD B1 (10M)	-98dBm	-98.5dBm	-101.2dBm	-96.3dBm
LTE-FDD B3 (10M)	-98dBm	-98.5dBm	-101.2dBm	-93.3dBm
LTE-FDD B5 (10M)	-98dBm	-99dBm	-101.5dBm	-94.3dBm
LTE-FDD B8 (10M)	-98dBm	-99dBm	-101.5dBm	-93.3dBm
LTE-TDD B34 (10M)	-98dBm	-98dBm	-101dBm	-96.3dBm
LTE-TDD B38 (10M)	-97.5dBm	-98dBm	-100.5dBm	-96.3dBm
LTE-TDD B39 (10M)	-98dBm	-98dBm	-101dBm	-96.3dBm
LTE-TDD B40 (10M)	-97.5dBm	-98dBm	-100.5dBm	-96.3dBm
LTE-TDD B41 (10M)	-97.5dBm	-98dBm	-100.5dBm	-94.3dBm

Table 58: SC66-A* RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B2	/	/	/	-104.7dBm
WCDMA B4	/	/	/	-106.7dBm
WCDMA B5	/	/	/	-104.7dBm
LTE-FDD B2 (10M)	/	/	/	-94.3dBm
LTE-FDD B4 (10M)	/	/	/	-96.3dBm
LTE-FDD B5 (10M)	/	/	/	-94.3dBm
LTE-FDD B7 (10M)	/	/	/	-94.3dBm
LTE-FDD B12 (10M)	/	/	/	-93.3dBm
LTE-FDD B13 (10M)	/	/	/	-93.3dBm
LTE-FDD B14 (10M)	/	/	/	-93.3dBm
LTE-FDD B17 (10M)	/	/	/	-93.3dBm

LTE-FDD B25 (10M)	/	/	/	-92.8dBm
LTE-FDD B66 (10M)	/	/	/	-95.8dBm
LTE-TDD B71 (10M)	/	/	/	-93.5dBm
LTE-TDD B41 (10M)	/	/	/	-94.3dBm

Table 59: SC66-J* RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B1	/	/	/	-106.7dBm
WCDMA B6	/	/	/	-106.7dBm
WCDMA B8	/	/	/	-103.7dBm
WCDMA B19	/	/	/	-106.7dBm
LTE-FDD B1 (10M)	/	/	/	-96.3dBm
LTE-FDD B3 (10M)	/	/	/	-93.3dBm
LTE-FDD B5 (10M)	/	/	/	-94.3dBm
LTE-FDD B8 (10M)	/	/	/	-93.3dBm
LTE-FDD B11 (10M)	/	/	/	-96.3dBm
LTE-FDD B18 (10M)	/	/	/	-96.3dBm
LTE-FDD B19 (10M)	/	/	/	-96.3dBm
LTE-FDD B21 (10M)	/	/	/	-96.3dBm
LTE-TDD B26 (10M)	/	/	/	-93.8dBm
LTE-TDD B28 (10M)	/	/	/	-94.8dBm
LTE-TDD B41 (10M)	/	/	/	-94.3dBm

Table 60: SC66-E* RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	/	/	/	-102.4dBm
EGSM900	/	/	/	-102.4dBm
DCS1800	/	/	/	-102.4dBm
PCS1900	/	/	/	-102.4dBm
WCDMA B1	/	/	/	-106.7dBm
WCDMA B2	/	/	/	-104.7dBm
WCDMA B4	/	/	/	-106.7dBm
WCDMA B5	/	/	/	-104.7dBm
WCDMA B8	/	/	/	-103.7dBm
LTE-FDD B1 (10M)	/	/	/	-96.3dBm
LTE-FDD B2 (10M)	/	/	/	-94.3dBm
LTE-FDD B3 (10M)	/	/	/	-93.3dBm
LTE-FDD B4 (10M)	/	/	/	-96.3dBm
LTE-FDD B5 (10M)	/	/	/	-94.3dBm
LTE-FDD B7 (10M)	/	/	/	-94.3dBm
LTE-FDD B8 (10M)	/	/	/	-93.3dBm
LTE-FDD B20 (10M)	/	/	/	-93.3dBm
LTE-FDD B28 (10M)	/	/	/	-94.8dBm
LTE-TDD B38 (10M)	/	/	/	-96.3dBm
LTE-TDD B39 (10M)	/	/	/	-96.3dBm
LTE-TDD B40 (10M)	/	/	/	-96.3dBm
LTE-TDD B41 (10M)	/	/	/	-94.3dBm

7.7. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it should be subject to ESD handling precautions that are typically applied to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the electrostatic discharge characteristics of SC66 module.

Table 61: ESD Characteristics (Temperature: 25°C, Humidity: 45%)

Test Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	+/-5	+/-10	KV
All Antenna Interfaces	+/-5	+/-10	KV
Other Interfaces	+/-0.5	+/-1	KV

8 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the tolerances for dimensions without tolerance values are ±0.05mm.

8.1. Mechanical Dimensions of the Module

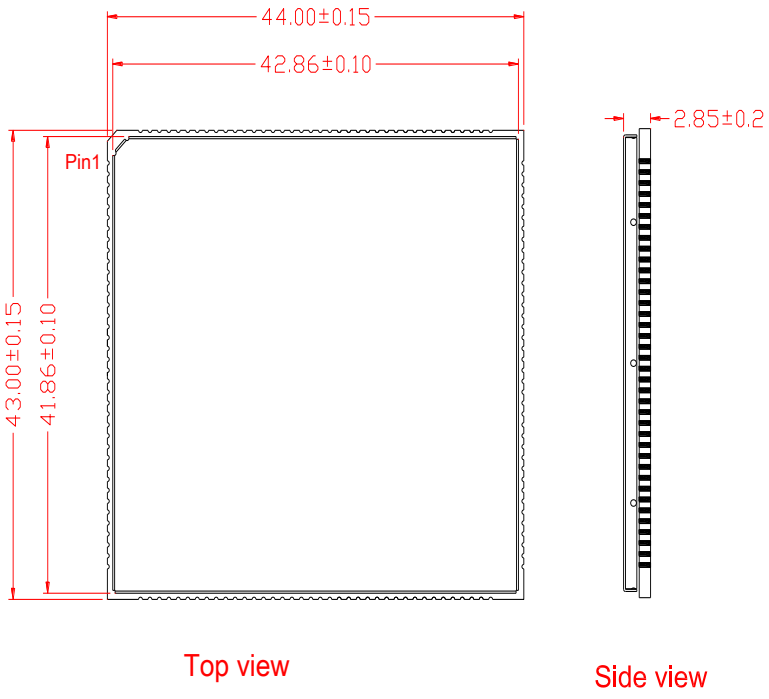


Figure 45: Module Top and Side Dimensions

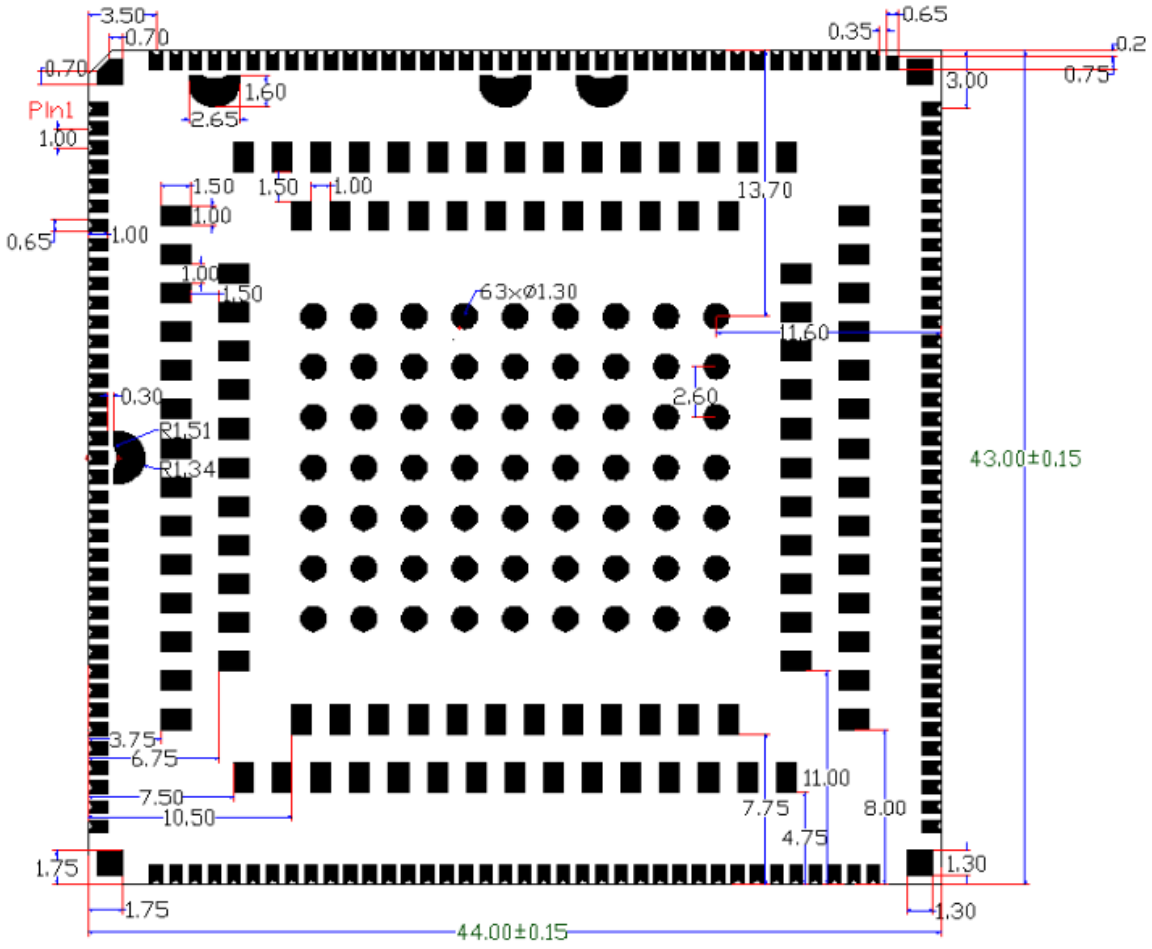


Figure 46: Module Bottom Dimensions (Top View)

8.2. Recommended Footprint

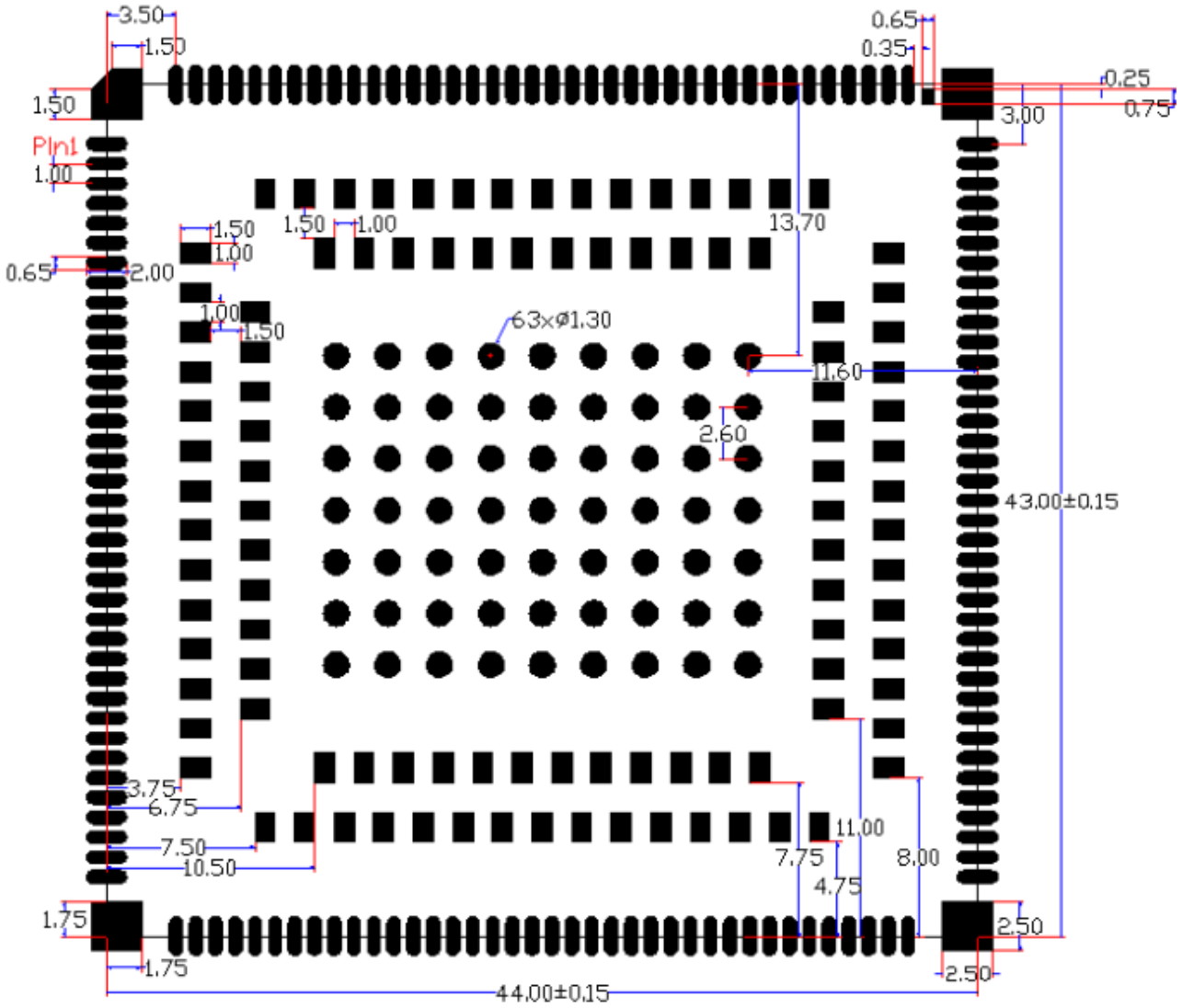


Figure 47: Recommended Footprint (Top View)

NOTES

1. For easy maintenance of the module, keep about 3mm between the module and other components on host PCB.
2. All RESERVED pins should be kept open and MUST NOT be connected to ground.

8.3. Top and Bottom View of the Module

Figure 48: Top View of the Module

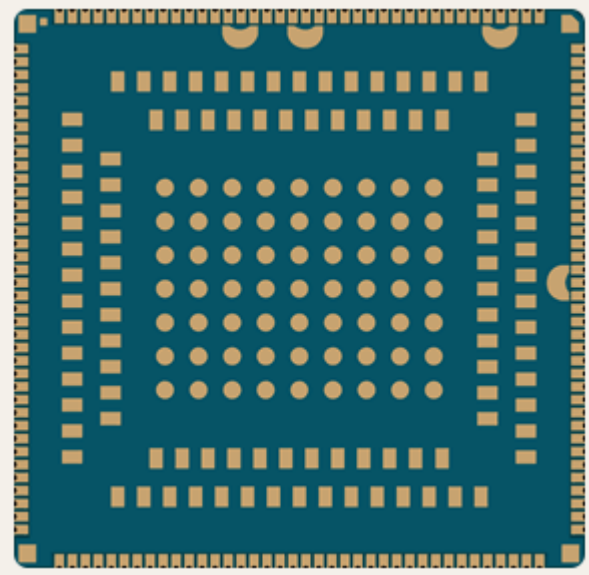


Figure 49: Bottom View of the Module

NOTE

These are renderings of SC66 module. For authentic dimension and appearance, please refer to the module that you receive from Quectel.

9 Storage, Manufacturing and Packaging

9.1. Storage

SC66 is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at <40ºC/90%RH.
2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
   - Mounted within 168 hours at the factory environment of ≤30ºC/60%RH.
   - Stored at <10%RH.
3. Devices require baking before mounting, if any circumstance below occurs.
   - When the ambient temperature is 23ºC±5ºC and the humidity indication card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%.
4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devic es before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/J EDECJ-STD-033* for baking procedure.

9.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18mm~0.20mm. It is recommended to slightly reduce the amount of solder paste for LGA pads, thus avoiding short-circuit. For more details, please refer to ***document [4]***.

It is suggested that the peak reflow temperature is 240~245ºC, and the absolute maximum reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

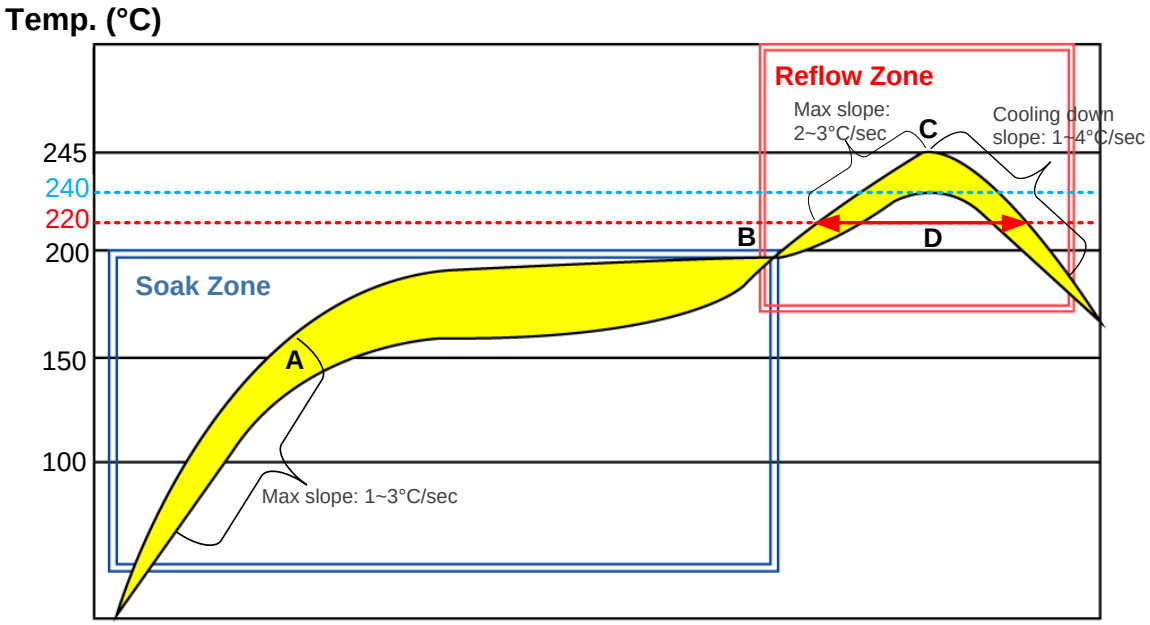


Figure 50: Recommended Reflow Soldering Thermal Profile

Table 62: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 to 120 sec

Reflow Zone	
Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	240°C ~ 245°C
Cooling down slope	1 to 4°C/sec
Reflow Cycle	
Max reflow cycle	1

9.3. Packaging

SC66 is packaged in tape and reel carriers. Each reel is 330mm in diameter and contains 200 modules. The following figures show the package details, measured in mm.

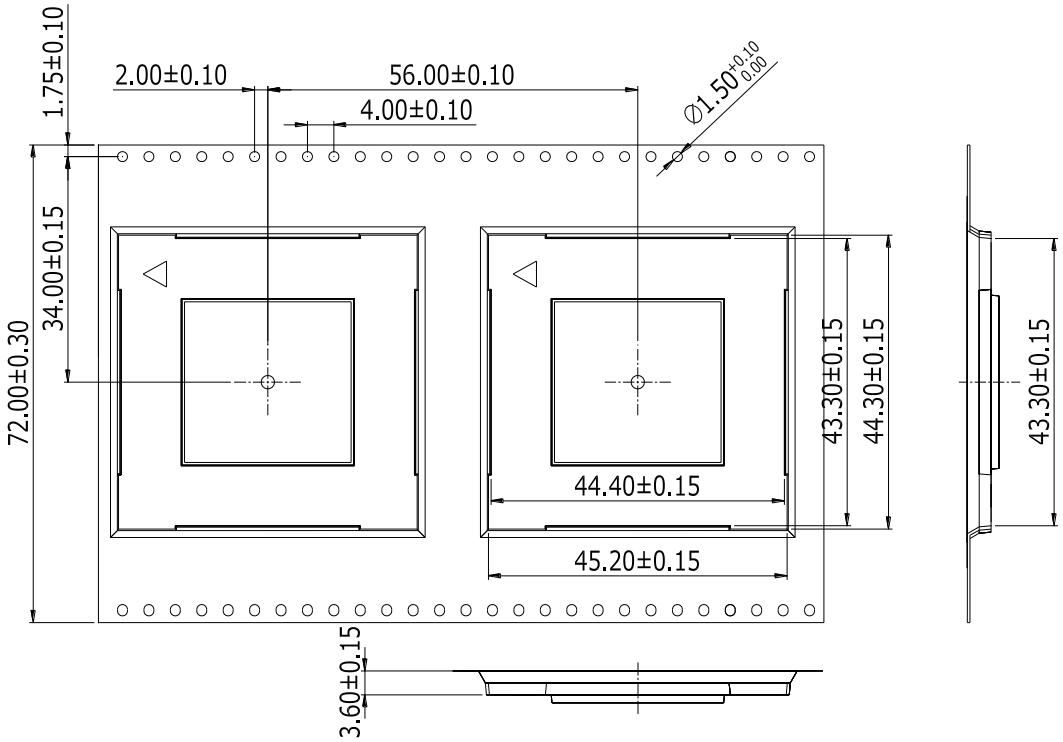


Figure 51: Tape Dimensions

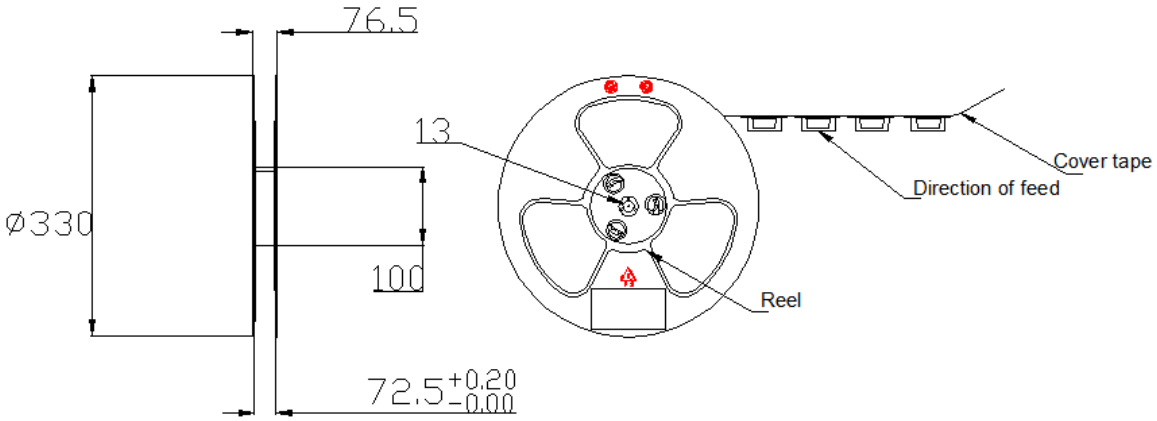


Figure 52: Reel Dimensions

Table 63: Reel Packaging

Model Name	MOQ for MP	Minimum Package: 200pcs	Minimum Package×4=800pcs
SC66	200	Size: 398mm × 383mm × 83mm N.W: 1.92kg G.W: 3.67kg	Size: 420mm × 350mm × 405mm N.W: 8.18kg G.W: 15.18kg

10 Appendix A References

Table 64: Related Documents

SN	Document Name	Remark
[1]	Quectel_Smart_EVB-G2_User_Guide	EVB User Guide for SC66
[2]	Quectel_SC66_GPIO_Configuration	GPIO Configuration of SC66
[3]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[4]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[5]	Quectel_SC66_Reference_Design	Reference Design for SC66

Table 65: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
bps	Bits per Second
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DRX	Discontinuous Reception
EFR	Enhanced Full Rate
EGSM	Extended GSM900 band (includes standard GSM900 band)
ESD	Electrostatic Discharge
FR	Full Rate

GMSK	Gaussian Minimum Shift Keying
GPS	Global Positioning System
GPU	Graphics Processing Unit
GSM	Global System for Mobile Communications
HR	Half Rate
HSDPA	High Speed Down Link Packet Access
HSPA	High Speed Packet Access
I/O	Input/Output
IQ	Inphase and Quadrature
LCD	Liquid Crystal Display
LCM	LCD Module
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LRA	Linear Resonant Actuator
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PMI	Power Management Interface
PMU	Power Management Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RH	Relative Humidity
RHCP	Right Hand Circularly Polarized

RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TE	Terminal Equipment
TX	Transmitting Direction
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_I	Voltage Input
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_O	Voltage Output
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

11 Appendix B GPRS Coding Schemes

Table 66: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

12 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 67: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA
14	4	4	NA

15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

13 Appendix D EDGE Modulation and Coding Schemes

Table 68: EDGE Modulation and Coding Schemes

Coding Schemes	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps