FMD2007/263
Dec. 18, 2007

TO: Digital Cube, Inc.

APPROVAL SPECIFICATIONS
OF
Wireless LAN Module

P/N : MBH7WLZ16-8890
D/N : FMD/03158

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FUJITSU MEDIA DEVICES LIMITED

MBH7WLZ16-8890 Specification

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TITLE	MBH7WLZ16-8890 Specification
DRAW NO.	Tech Bes No. FMD/03158
FUJITSU MEDIA DEVICES LIMITED	PAGE 1 / 25

1. Introduction

This document applies to the Wireless LAN module MBH7WLZ16-8890 for Digital Cube, Inc.

2. Features

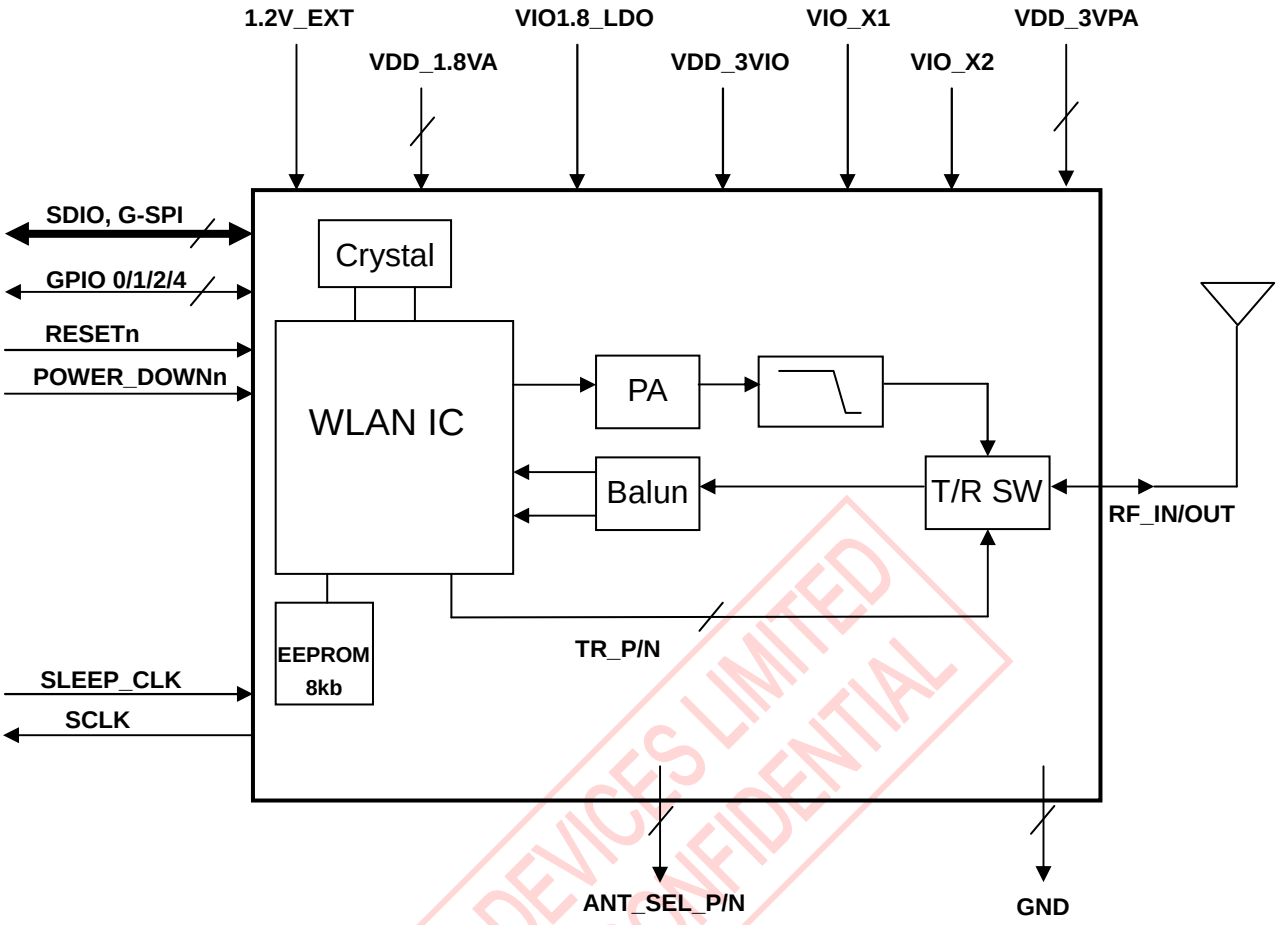
MBH7WLZ16-8890 is a microminiaturized Wireless LAN module conforming to the IEEE standard 802.11/ 802.11b/802.11g, and transmits and receives in the 2.4 GHz ISM band.
MBH7WLZ16-8890 has the following features:

- IEEE standard 802.11/802.11b/802.11g Compliant
- Frequency Range: 2400 – 2492 MHz (1 – 13 channel (IEEE802.11/11b/11g) ISM band)
- Modulation Technique: Direct Sequence Spread Spectrum (CCK, DQPSK, DBPSK)
  Orthogonal Frequency Division Multiplexing (64QAM, 16QAM, DQPSK, DBPSK)
- Transmission Rate: 1 Mbps, 2 Mbps (802.11), 5.5 Mbps, 11 Mbps (802.11b)
  6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps (802.11g)
- Host Interface: SDIO
  Generic SPI (G-SPI)
- Security: 64/128-bit WEP, WPA (TKIP), WPA2 (AES-CCMP)
- QoS (Quality of Service) support
- Surface mount, 60pin LGA type (Compatible with Pb-free solder processing)
- RoHS Compliant
- Miniaturized package: 8.5 x 8.5 x 1.2 mm
- Antenna port: Single Antenna port
- Built-in Crystal Oscillator
- Low power consumption

3. Part Number

Fujitsu Media Devices Limited Part Number is MBH7WLZ16-8890

4. Block Diagram



5. Pin Description and Power

5-1. Pin Description

Name	No.	I/O	Description
SPI_SDI/ SD_CMD	18	I/O	G-SPI mode: G-SPI Data Input SDIO 4-bit mode: Command/Response SDIO 1-bit mode: Command Line SDIO SPI mode: Data Input
SPI_CLK/ SD_CLK	19	I/O	G-SPI mode: G-SPI Clock Input SDIO 4-bit mode: Clock Input SDIO 1-bit mode: Clock Input SDIO SPI mode: Clock Input
SPI_SCSn/ SD_DAT0	17	I/O	G-SPI mode: G-SPI Chip Select Input (active low) SDIO 4-bit mode: Data Line Bit [0] SDIO 1-bit mode: Data Line SDIO SPI mode: Data Output
SPI_SDO/ SD_DAT1	16	I/O	G-SPI mode: G-SPI Data Output SDIO 4-bit mode: Data Line Bit [1] SDIO 1-bit mode: Interrupt SDIO SPI mode: Reserved
SPI_SINTn/ SD_DAT2	15	I/O	G-SPI mode: G-SPI Interrupt Output (active low) SDIO 4-bit mode: Data Line Bit [2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional) SDIO SPI mode: Reserved
SD_DAT3	14	I/O	SDIO 4-bit mode: Data Line Bit [3] SDIO 1-bit mode: Reserved SDIO SPI mode: Card Select (active low)
GPIO[0]/ SLEEPn	11	I/O	General Purpose Input/Output (Internal pull-up) These pins are asynchronous to internal clocks. Several of these pins can be selected to perform alternate functions such as an LED controller. When not used, these pins should be left floating. Notes: • GPIO[0]: SLEEPn. This pin drives low during power down sleep mode. • GPIO[1]: LED output (strap pin). Transmit power or receive ready LED. • GPIO[4]: WLAN MAC wake-up input / Interrupt input
GPIO[1]/ LED	21	I/O	
GPIO[2]	39	I/O	
GPIO[4]/ Module_wake_up	20	I/O	
WL_ACTIVE	40	O	Bluetooth WLAN Active 2-Wire BCA Mode: When high, WLAN is transmitting or receiving packets. 3-Wire BCA Mode: 0 = Bluetooth device allowed to transmit 1 = Bluetooth device not allowed to transmit This pin drives low when POWER_DOWNn is asserted. In WLAN Sleep mode, all I/O PADs are powered down. This pad must stay at a low state when in power down mode.
BT_PRIORITY	42	I	Bluetooth Priority 2-Wire BCA Mode: When high, Bluetooth is transmitting or receiving high priority packets. 3-Wire BCA Mode: When high, Bluetooth is requesting to transmit or receive packets.
BT_STATE	41	I	Bluetooth State 0 = normal priority, Rx 1 = high priority, Tx BT_STATE is used to input the Bluetooth priority and direction of traffic following the assertion of the BT_PRIORITY input.
BT_FREQ	43	I	4-Wire BCA Mode: Bluetooth Frequency Asserted (logic high) when the Bluetooth transceiver hops into the restricted channels defined by the coexistence mechanism. 2-Wire, 3-Wire BCA Mode: Tied to ground (GND)
ANT_SEL_P	37	O	Differential Antenna Select Positive Output Provides the antenna select positive control signal. Default value is 1. Also used as RF switch control for single Bluetooth/WLAN antenna configurations.

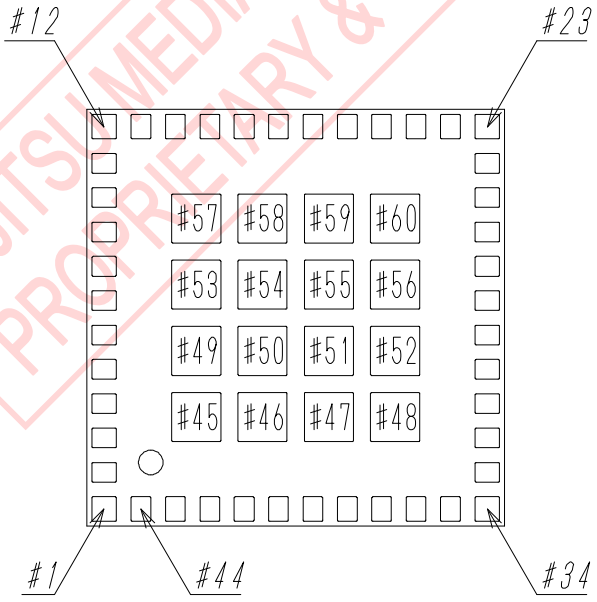
ANT_SEL_N	ANT_SEL_P	For antenna diversity	For single BT/WLAN antenna
0	0	---	---
0	1	Antenna 1	Bluetooth
1	0	Antenna 0	WLAN
1	1	---	---

Name	No.	I/O	Description
ANT_SEL_N	36	O	Differential Antenna Select Negative Output Provides the antenna select negative control signal. Default value is 0. Also used as RF switch control for single Bluetooth/WLAN antenna configurations.
RESETn	8	I	Reset (active low, Internal pull-up)
POWER_DOWNn	7	I	Full power down (active low, Internal pull-up) 0 = full power down mode 1 = normal mode Connect to power down pin of host or 1.8V.
SLEEP_CLK	9	I	Clock Input for External Sleep Clock NOTE: SLEEP_CLK is used by the WLAN and Bluetooth MAC. The input clock frequency is typically 32 kHz/32.768 kHz/3.2 kHz. The Bluetooth radio chip supply is 3.2 kHz. The WLAN requires 32 kHz.
SCLK	24	O	Serial Interface Clock (Internal pull-up) Serial interface clock output for EEPROM or power management device programming interface control.
RF_IN/OUT	3	RF	Antenna port, 50Ω
1.2V_EXT	22	Power	1.2V Digital Power Supply
VDD_1.8VA_1	5	Power	1.8V Analog Power Supply
VDD_1.8VA_2	6	Power	1.8V Analog Power Supply
VIO1.8_LDO	29	Power	1.8V Digital I/O and Internal Voltage Regulator Power Supply
VDD_3VIO	27	Power	3.0V Digital I/O Power Supply
VIO_X1	13	Power	1.8V/3.3V Host Supply
VIO_X2	26	Power	1.8V/3.3V Digital Power Supply
VDD_3VPA_1	32	Power	3.0V Power Supply for PA
VDD_3VPA_2	31	Power	3.0V Power Supply for PA
GND	1,2,4,10, 12,23,25,28, 30,33 - 35 38,44 - 60	Ground	Ground

ANT_SEL_N	ANT_SEL_P	For antenna diversity	For single BT/WLAN antenna
0	0	---	---
0	1	Antenna 1	Bluetooth
1	0	Antenna 0	WLAN
1	1	---	---

I/O Type:

I: Digital Input, O: Digital Output, I/O: Digital Input/Output



Pin Assignment (Bottom View)

5-2. Power

MBH7WLZ16-8890 requires the following supply voltages:

- 1.2V_EXT — 1.2V Digital Core Power Supply (1.2V Supply can be derived from the Internal Voltage Regulator.)
- VDD_1.8VA_1, VDD_1.8VA_2 — 1.8V Analog Power Supply
- VIO1.8_LDO — 1.8V Digital I/O and Internal Voltage Regulator Power Supply
- VIO_X1 — 1.8V/3.3V Host Power Supply
- VIO_X2 — 1.8V/3.3V Digital Power Supply
- VDD_3VIO — 3.0V Digital I/O Power Supply
- VDD_3VPA_1, VDD_3VPA_2 — 3.0V PA Power Supply

The following table lists the pins operating from each voltage supply.

No.	Name	No.	Name	No.	Name	No.	Name
VIO_X1		VIO_X2		VDD_3VIO		VIO1.8_LDO	
7	POWER_DOWNn	24	SCLK	36	ANT_SEL_N	40	WL_ACTIVE
8	RESETn			37	ANT_SEL_P	41	BT_STATE
9	SLEEP_CLK					42	BT_PRIORITY
11	GPIO[0]/SLEEPn					43	BT_FREQ
14	SD_DAT3						
15	SPI_SINTn/SD_DAT2						
16	SPI_SDO/SD_DAT1						
17	SPI_SCSn/SD_DAT0						
18	SPI_SDI/SD_CMD						
19	SPI_CLK/SD_CLK						
20	GPIO[4]/Module_wake_up						
21	GPIO[1]/LED						
39	GPIO[2]						

6. Electrical Characteristics

6-1. General Specification

Network Standard	IEEE standard 802.11/802.11b/802.11g Compliant
Interface	Secure Digital Input/Output (SDIO) Generic SPI (G-SPI)
Frequency Band	2400 ~ 2492 MHz (ISM band) (IEEE802.11b: Channel 1 ~ 13, IEEE802.11g: Channel 1 ~ 13)
Data Transfer Mode	Direct Sequence Spread Spectrum (DSSS) Orthogonal Frequency Division Multiplexing (OFDM)
Modulation Techniques	CCK (11 Mbps, 5.5 Mbps), DQPSK (2 Mbps), DBPSK (1 Mbps) OFDM-64QAM (54 Mbps, 48 Mbps), OFDM-16QAM (36 Mbps, 24 Mbps) OFDM-DQPSK (18 Mbps, 12 Mbps), OFDM-DBPSK (9 Mbps, 6 Mbps)
Media Access Protocol	CSMA/CA (Carrier Sense Multiple Access with Collision Avoidance)
Access Method	Ad-Hoc mode, Infrastructure mode

6-2. Absolute Maximum Rating

Symbol	Parameter	Min	Typ	Max	Unit
1.2V_EXT	Power Supply Voltage with respect to GND	---	1.2	1.35	V
VDD_1.8VA_1, VDD_1.8VA_2	Power Supply Voltage with respect to GND	---	1.8	2.3	V
VIO1.8_LDO	Power Supply Voltage with respect to GND	---	1.8	2.3	V
VDD_3VIO	Power Supply Voltage with respect to GND	---	3.0	3.5	V
VIO_X1	Power Supply Voltage with respect to GND	---	1.8	2.3	V
		---	3.3	4.2	V
VIO_X2	Power Supply Voltage with respect to GND	---	1.8	2.3	V
		---	3.3	4.2	V
VDD_3VPA_1, VDD_3VPA_2	Power Supply Voltage with respect to GND	---	3.3	5.0	V
$T_{STORAGE}$	Storage Temperature	-40	+25	+105	℃

6-3. Recommendable Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
1.2V_EXT	1.2V digital power supply	1.08	1.2	1.32	V
VDD_1.8VA_1, VDD_1.8VA_2	1.8V analog I/O power supply	1.7	1.8	1.9	V
VIO1.8_LDO	1.8V internal voltage regulator power supply	1.62	1.8	1.98	V
VDD_3VIO	3.0V digital I/O power supply	2.95	3.0	3.4	V
VIO_X1	Host interface digital I/O power supply	1.62	1.8	1.98	V
		2.97	3.3	3.63	V
VIO_X2	1.8V digital I/O power supply	1.62	1.8	1.98	V
		2.97	3.3	3.63	V
VDD_3VPA_1, VDD_3VPA_2	3.0V PA power supply	2.95	3.0	3.6	V
T_A	Ambient operating temperature	-20	+25	+70	℃

6-4. DC Electricals – Digital 3V Pads (VDD_3VIO)

Symbol	Parameter	Min	Typ	Max	Unit
V_{30}	Power supply voltage (VDD_3VIO)	2.95	3.0	3.4	V
V_{IH}	Input high voltage	2.0	---	V_{30}+0.3	V
V_{IL}	Input low voltage	-0.3	---	0.6	V
V_{HYS}	Input hysteresis	250	---	---	mV
V_{OH}	Output high voltage	2.3	---	---	V
V_{OL}	Output low voltage	---	---	0.4	V

6-5. DC Electricals – Digital 1.8V/3V Pads (VIO_X1, VIO_X2)

Symbol	Parameter	Mode	Condition	Min	Typ	Max	Unit
V_{18}	Power supply voltage (VIO_X1, VIO_X2)	1.8V	---	1.62	1.8	1.98	V
V_{33}	Power supply voltage (VIO_X1, VIO_X2)	3.3V	---	2.97	3.3	3.63	V
V_{IH}	Input high voltage	1.8V	---	1.2	---	V_{18}+0.3	V
		3.3V	---	2.0	---	V_{33}+0.3	V
V_{IL}	Input low voltage	1.8V	---	-0.3	---	0.6	V
		3.3V	---	-0.3	---	1	
V_{HYS}	Input hysteresis	1.8V	---	250	---	---	mV
		3.3V	---	300	---	---	mV
V_{OH}	Output high voltage	1.8V	SR[1] = Slew Rate[2] **SR I_{OH}(max)** 3 16 mA 2 16 mA 1 5 mA 0 5 mA	1.22	---	---	V
		3.3V	SR = Slew Rate **SR I_{OH}(max)** 3 16.5 mA 2 16.5 mA 1 5.5 mA 0 5.5 mA	2.57	---	---	V
V_{OL}	Output low voltage	1.8V	SR = Slew Rate[3] **SR I_{OL}(max)** 3 23 mA 2 15.5 mA 1 7.5 mA 0 7.5 mA	---	---	0.4	V
		3.3V	SR = Slew Rate **SR I_{OL}(max)** 3 23.5 mA 2 15.5 mA 1 7.5 mA 0 7.5 mA	---	---	0.4	V
I_pullup[4]	---	---	---	16	22	29	µA
I_pulldown	---	---	---	12	23	33	µA
I_pullup_weak	---	---	---	---	---	10	µA
I_pulldown_weak	---	---	---	---	---	10	µA

1. Slew rate that controls the output drive strength and rise/fall time of the pad.
2. I_{OH} is the maximum current draw to maintain a minimum V_{OH} level.
3. I_{OL} is the maximum sink current to maintain a maximum V_{OL} level.
4. There are two types of pull-up/pull-down pads—regular and weak. Each pad type (regular and weak) has different internal resistor values.

6-6. Power Supply Configurations

For flexibility, MBH7WLZ16-8890 integrates an internal voltage regulator. The 1.2V_EXT supply can be derived from this regulator.
The following table lists the connections of the VIO1.8_LDO and 1.2V_EXT power supplies in various applications.

Configuration	VIO1.8_LDO	1.2V_EXT
Internal voltage regulator with/without Bluetooth coexistence interface	Connected	Not Connected
External 1.2V supply with/without Bluetooth coexistence interface	Connected	Connected

6-7. Power on Reset Sequence

Figure 6-1 shows the Power on Reset (POR) Sequence of MBH7WLZ16-8890.

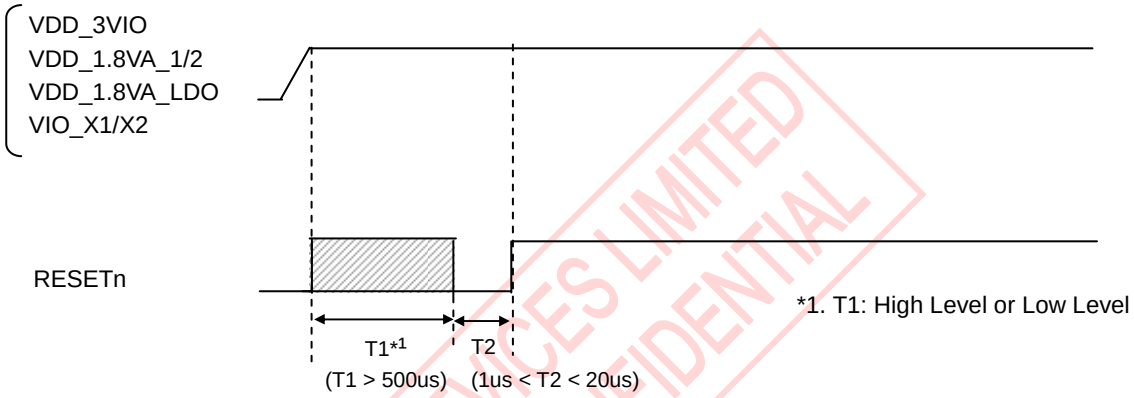


Figure 6-1 Power on Reset Sequence

6-8. Power Management

The following table lists the state of the functional pins when in power down mode.

No.	Tri-State (Floating)	No.	Output Low	No.	Output High
9	SLEEP_CLK	11	GPIO[0]/SLEEPn	37	ANT_SEL_P
14	SD_DAT3	24	SCLK		
15	SPI_SINTn/SD_DAT2	36	ANT_SEL_N		
16	SPI_SDO/SD_DAT1	39	GPIO[2]		
17	SPI_SCSn/SD_DAT0	40	WL_ACTIVE		
18	SPI_SDI/SD_CMD				
19	SPI_CLK/SD_CLK				
20	GPIO[4]/Module_wake_up				
21	GPIO[1]/LED				
41	BT_STATE				
42	BT_PRIORITY				
43	BT_FREQ				

6-9. Reset Configuration

MBH7WLZ16-8890 is reset to its default operating state under the following conditions:

- Power on Reset
- Software/Firmware reset

6-9-1. Internal Reset

MBH7WLZ16-8890 is reset and the internal CPU begins the boot sequence when any of the following internal reset events occurs:

- Internal CPU issues a software reset
- Host driver issues a soft reset
- Watchdog timer expires (used for debug purpose only)

6-9-2. External Reset

MBH7WLZ16-8890 is reset and the internal CPU begins the boot sequence when the RESETn input pin transitions from low to high.

6-9-3. Calibration

MBH7WLZ16-8890 performs calibration when the device is powered up. In addition, calibration is also performed under the following operating conditions:

- Exiting receive mode
- Exiting transmit mode
- Change of channel frequency

6-10. RF Specification*[1]

Items		Condition	Min	Typ	Max	Unit
Transmit power levels	Channel 1-13	54 Mbps (64QAM) 48 Mbps (64QAM)	-	12.0	-	dBm
		36 Mbps (16QAM) 24 Mbps (16QAM) 18 Mbps (DQPSK) 12 Mbps (DQPSK) 9 Mbps (DBPSK) 6 Mbps (DBPSK)	-	15.0	-	dBm
		11 Mbps (CCK) 5.5Mbps (CCK) 2 Mbps (DQPSK) 1 Mbps (DBPSK)	-	16.0	-	dBm
	Channel 14	11 Mbps (CCK) 5.5Mbps (CCK) 2 Mbps (DQPSK) 1 Mbps (DBPSK)	-	8.0	-	dBm
802.11b Transmit spectrum mask	1st Side Lobe	1 Mbps (DBPSK)	-	-	-30	dBr
	2nd Side Lobe		-	-	-50	dBr
802.11g Transmit spectrum mask	11 MHz offset	6 Mbps (DBPSK)	-	-	-20	dBr
	20 MHz offset		-	-	-28	dBr
	30 MHz offset		-	-	-40	dBr
Transmit center frequency tolerance		54 Mbps (64QAM)	-25	-	25	ppm
Symbol clock frequency tolerance		54 Mbps (64QAM)	-25	-	25	ppm
Transmit power-on ramp		11 Mbps (CCK)	-	-	2	µs
Transmit power-down ramp		11 Mbps (CCK)	-	-	2	µs
RF carrier suppression		2 Mbps (DQPSK)	15	-	-	dB
EVM (Peak)		11 Mbps (CCK)	-	10	35	%
		1 Mbps (DBPSK)	-	8	35	%
EVM (RMS)		54 Mbps (64QAM)	-	-31	-25	dB
		6 Mbps (DBPSK)	-	-28	-5	dB
Receiver minimum input level sensitivity		54 Mbps (64QAM)	-	-74	-65	dBm
		6 Mbps (DBPSK)	-	-90	-82	dBm
		11 Mbps (CCK)	-	-89	-76	dBm
		1 Mbps (DBPSK)	-	-92	-85	dBm
Receiver maximum input level		54 Mbps (64QAM)	-20	-	-	dBm
		11 Mbps (CCK)	-10	-	-	dBm
Receiver adjacent channel rejection		54 Mbps (64QAM)	-1	-	-	dB
		11 Mbps (CCK)	35	-	-	dB

*1) Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

7. Host Interface

MBH7WLZ16-8890 connects several host interface bus units to the internal bus of the device. The connection of each host interface bus unit to the internal bus is multiplexed with the other host interface bus units. MBH7WLZ16-8890 allows only one host interface unit to be active at a time.
MBH7WLZ16-8890 supports the following host interfaces:

- SDIO interface
- G-SPI interface

7-1. SDIO Interface

MBH7WLZ16-8890 supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the WLAN device. The SDIO interface contains interface circuitry between an external SDIO bus and the internal shared bus.
MBH7WLZ16-8890 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in MBH7WLZ16-8890 through the use of BARs and a DMA engine.
The SDIO device interface main features include:

- Internal memory used for CIS
- Supports SPI, 1-bit SDIO, and 4-bit SDIO transfer modes at the full clock range of 0 to 50 MHz
- Special Interrupt register for information exchange
- Allows module to interrupt host

The SDIO interface pins are powered from the VIO_X1 voltage supply.

7-1-1. SDIO Command List

All mandatory SDIO commands are supported for both SDIO and SPI modes. SDIO mode commands are shown in Table 7-1. SPI mode commands are shown in Table 7-2.

Table 7-1 SDIO Mode, SDIO Commands

Command	Command Name	Description
CMD0	GO_IDLE_STATE	Used to change from SDIO to SPI mode
CMD3	SEND_RELATIVE_ADDR	SDIO Host asks for RCA
CMD5	IO_SEND_OP_COND	SDIO Host asks for and sets operation voltage
CMD7	SELECT/DESELECT_CARD	Sets SDIO target device to command state or back to standby
CMD15	GO_INACTIVE_STATE	Sets SDIO target device to inactive state
CMD52	IO_RW_DIRECT	Used to read/write host register and CIS table
CMD53	IO_RW_EXTENDED	Used to read/write data from/to SQU memory

Table 7-2 SPI Mode, SDIO Commands

Command	Command Name	Description
CMD0	GO_IDLE_STATE	Used to change from SDIO to SPI mode
CMD5	IO_SEND_OP_COND	Used in initialization state
CMD52	IO_RW_DIRECT	Used to read/write host register and CIS table
CMD53	IO_RW_EXTENDED	Used to read/write data from/to SQU memory
CMD58	CRC_ON_OFF	SPI only. Enable/disable CRC

7-1-2. Power-Up Initialization

The power-up transaction sequences for SDIO and SPI modes are as follows:

7-1-2-1. SDIO Mode Power-Up Transaction Sequence

(1) CMD5 (arg = 0)
(2) SDIO Card response with OCR
(3) CMD5 from host to set operation voltage using OCR
(4) SDIO Card response with IORDY = 1 and MP = 0 (not SD memory, not combo card)
(5) CMD3 and CMD7 to set in one active mode
(6) CMD15 to put the card inactive

7-1-2-2. SPI Mode Power-Up Transaction Sequence

(1) CMD0 + CS = LOW
(2) CMD5 (arg = 0)
(3) SDIO Card response with OCR
(4) CMD5 from host to set operation voltage using OCR
(5) CMD15 to put the card inactive

7-1-3. Operation Sequence

Table 7-3 lists the registers used to program the operation sequence. See the SDIO Registers section of the separate Host Interface Registers document for register programming information.

Table 7-3 SDIO Registers

Register	Offset
Host Interrupt	0x107
Card Status	0x120

Operation transaction sequences are as follows:

7-1-3-1. SDIO Host Reads CIS Table Sequence

(1) Check Card Status, Offset 0x120[2]. It is set by Card after CIS table is initialized.
(2) HOST reads CIS Table using Function 0 address 8030_807F and function 1 address 8080_80FF.

7-1-3-2. SDIO Host Downloads Packet

(1) Card sets Card Status, Offset 0x120[0].
(2) Host Polls Dnld_Card_Rdy and IO_Ready.
(3) Host starts CMD53 block mode using function 1 with IO port address. CMD53 write clears Dnld_Card_Rdy.
(4) Host sends the data in terms of predefined blocks. If BUSY, host delays the next block.
(5) After CMD53 write completes, an interrupt CardInt is sent to firmware.
(6) Firmware checks Host Interrupt Status, Offset 0x107[2] and Host Interrupt Status, Offset 0x107[0] registers. If Dnld_CRC_Err = 1, this packet has CRC error. If Dnld_Restart = 1, firmware ignores this packet.
(7) Back to the first step.

7-1-3-3. SDIO Host Uploads Packet

(1) Card sets Card Status, Offset 0x120[1].
(2) Upld_Card_Rdy triggers an interrupt to SDIO HOST in the interrupt period.
(3) SDIO HOST read to clear INT or write 0 to clear the interrupt.
(4) SDIO HOST checks Upld_Card_Rdy and IO_Ready.
(5) HOST starts CMD53 read using function 1 with IO address with infinite block number or defined block number. CMD53 clears Upld_Card_Rdy bit.
(6) After Host receives all data, HOST writes Abort using CMD52.
(7) This terminate read operation. Card gets an interrupt with abort and with packet read, is complete.
(8) Firmware reads interrupt, clears interrupt.
(9) Firmware reads Host Interrupt Status, Offset 0x107[1]. If it is set by HOST, Firmware prepares to reissue this packet.
(10) Back to the first step.

The SDIO HOST checks IO_READY before starting a new CMD53. The SDIO target device can take a new SDIO HOST command only after the SDIO target device internal state machine is set back to IO_READY state. Otherwise, the new CMD53 is ignored.

7-1-4. SDIO Timing

SDIO Timing specifications are shown in the followings.

Table 7-4 SDIO Timing Data

Symbol	Items	Condition	Min	Typ	Max	Unit
fpp	CLK Frequency	Normal	0	-	25	MHz
		High Speed	0	-	50	MHz
TWL	CLK Low Time	Normal	10	-	-	ns
		High Speed	7	-	-	ns
TWH	CLK High Time	Normal	10	-	-	ns
		High Speed	7	-	-	ns
TISU	Input Setup Time	Normal	5	-	-	ns
		High Speed	6	-	-	
TIH	Input Hold Time	Normal	5	-	-	ns
		High Speed	2	-	-	
TODLY	Output Delay Time	-	0	-	14	ns
TOH	Output Hold Time	High Speed	2.5	-	-	ns

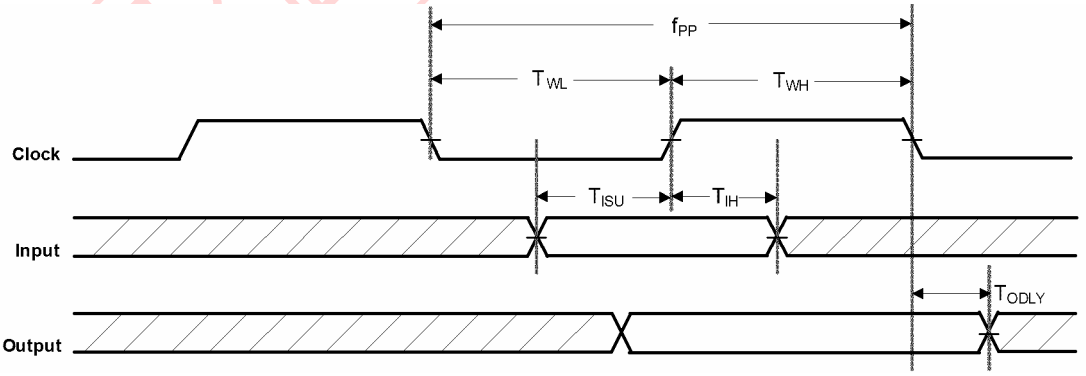


Figure 7-1 SDIO Timing Diagram (Normal mode)

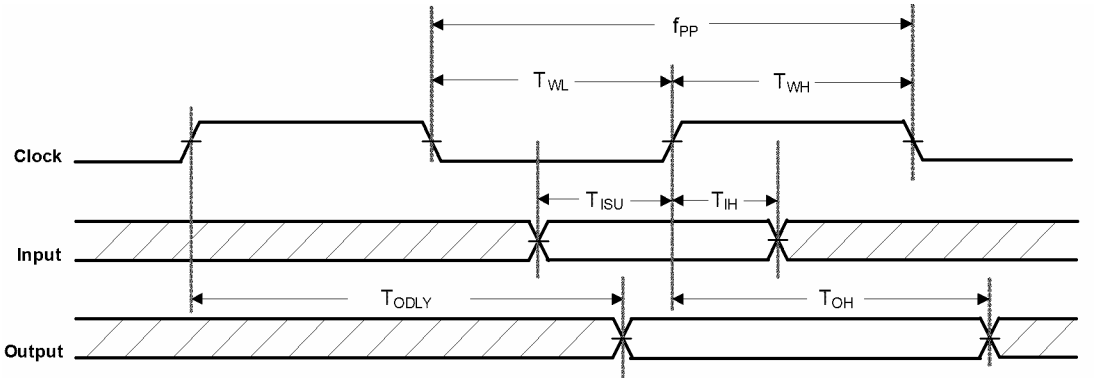


Figure 7-2 SDIO Timing Diagram (High speed mode)

Note: The SDIO-SPI CS signal timing is identical to all other SDIO inputs.

7-2. G-SPI Interface

MBH7WLZ16-8890 supports a generic, half-duplex, DMA-assisted SPI host interface (G-SPI) that allows a host controller using a generic SPI bus protocol to access the WLAN device. The G-SPI interface contains interface circuitry between an external SPI bus and the internal shared bus.
MBH7WLZ16-8890 acts as the device on the SPI bus. The host unit can access the G-SPI registers directly and can access shared memory in MBH7WLZ16-8890 through the use of BARs and a DMA engine.
The SPI unit supports generic SPI interface protocols as detailed in the following sections. The design is capable of 50MHz operation. The interface supports the following functionally.

- SPI unit bus device operation.
- SPI unit register read / write.
- Interrupt generation to internal CPU.
- Interrupt generation to the SPI unit host.
- DMA to internal memories
- Wake interrupt to the Power Management Unit

MBH7WLZ16-8890 G-SPI interface pins are powered from the VIO_X1 voltage supply.

7-2-1. G-SPI Interface Functional Description

The G-SPI supports a variety of simple address/data protocols over a standard SPI physical bus. The protocols supported are differentiated by the number of address bits and data ordering.
Each transaction is initiated by assertion of the active low signal SCSn. Following the assertion of SCSn, the SDI input is latched with every positive edge of SCLK. When data is output, it is clocked out with the negative edge of SCLK. The clock input SCLK is low at the start and completion of a transaction.

7-2-1-1. Transaction Delays

The first block of data to be transferred is from host to the device. This block of data contains an address and read/write control. The MSB of the address is low for read operations and high for write operations.

7-2-1-1-1. Write Transaction Delay

For write transactions, the data phase of a transaction immediately follows the address phase of the transaction. There is no need to extend the low time of the clock between address and data or for the host to clock any dummy cycles.

7-2-1-1-2. Read Transaction Delay

There is a delay required between the end of the address phase on the bus and the start of the data phase of the transaction. This delay is shown as TDRR (time delay read register) and TDRP (time delay read port). This delay represents the time delay required for the device to prepare valid data to return to the host.
This delay can be created in two different ways.
First, the read transaction delay is created by the host clocking a known number of dummy clock cycles to the device. The number of dummy clock cycles is specified in the Delay Read Register. There are two parameters in this parameter:

- Register read access
- Port read access

During the data phase of a transaction, the host continues to provide clock pulses and either drives data on the SDI input or read data from the SDO output.

7-2-1-2. Data Transfer

The host always accesses configuration registers in the G-SPI unit. To access internal memory space, some registers are defined as Port registers. When Port registers are accessed, the device reads or writes from internal memory space using the corresponding Base Address Register (BAR) and DMA engine.
Every transfer between host and device is a burst transfer (single address followed by multiple data). A transfer is terminated by the host after reading or writing the desired amount of data by de-asserting the SCSn input.

7-2-1-2-1. Port Register Access

When the host system reads Port Registers, there is no limit to the burst length (other than the limit imposed by the valid address range of the internal bus). When the host system writes to Port Registers, the only condition on burst length is that the length be a multiple number of DWORDS.
Port Registers (I/O Port, Command Port, Data Port) are used to access internal 32-bit memory space and are always accessed on 32-bit boundaries. Each of these port registers has a corresponding BAR for reads and writes (acting as a pointer to the starting physical address location). Internal memory is also accessed only on 32-bit boundaries. This is accomplished by programming the corresponding BAR with 32-bit aligned values. During these accesses, the lower 16 bits are always presented on the bus first.

7-2-1-2-1-1. Port Register Write Data

Write data to a Port Register is packed into sequential 32-bit memory locations starting at the location of the corresponding BAR. When reading from the Data and Command Ports of the device, the DMA engine continues to fill the FIFO whenever there is room for eight DWORDs (32-bits) of data. When writing data to the device, the de-assertion of SCSn input causes a flush to the write FIFO.

7-2-1-2-1-2. Port Register Read Data

When reading data from the I/O Port of the device, it is selectable whether the DMA engine performs a single read or burst reads. Burst reads are treated like Data and Command Port reads. Single reads cause the DMA engine to perform a single DWORD access on the internal bus. A single read transaction must be terminated following the first or second 16-bit block of returned data.

7-2-1-2-2. Configuration Register Access

When the host system accesses registers other than the Port Registers, the burst length must be limited to one 16-bit data transfer, or two 16-bit data transfers if the address is on a DWORD boundary. When a unit on the internal bus accesses G-SPI interface registers, the access must be a single DWORD access or smaller.
G-SPI interface registers, with the exception of Port Registers, can be read from or written to on 16-bit boundaries. Transactions can be terminated after a single 16-bit word is read or written.

7-2-1-3. G-SPI Clock Frequency

The G-SPI clock frequency must not be greater than 2.5 times the internal bus clock frequency.

7-2-2. G-SPI Timing

G-SPI Timing specifications are shown in the followings.

Table 7-5 G-SPI Timing Data

Symbol	Parameter	Min	Typ	Max	Unit
TSCLK	Clock Period	20	---	---	ns
TWH	Clock High	5	---	---	ns
TWL	Clock Low	9	---	---	ns
TWR	Clock Rise Time	---	---	1	ns
TWF	Clock Fall Time	---	---	1	ns
TH	SDI Hold Time	2.5	---	---	ns
TSU	SDI Setup Time	2.5	---	---	ns
TV	SDIO Hold Time	5	---	---	ns
TCSS	SCSn Fall to Clock	5	---	---	ns
TCSH	Clock to SCSn Rise	0	---	---	ns
TCRF	SCSn Rise to SCSn Fall	400	---	---	ns

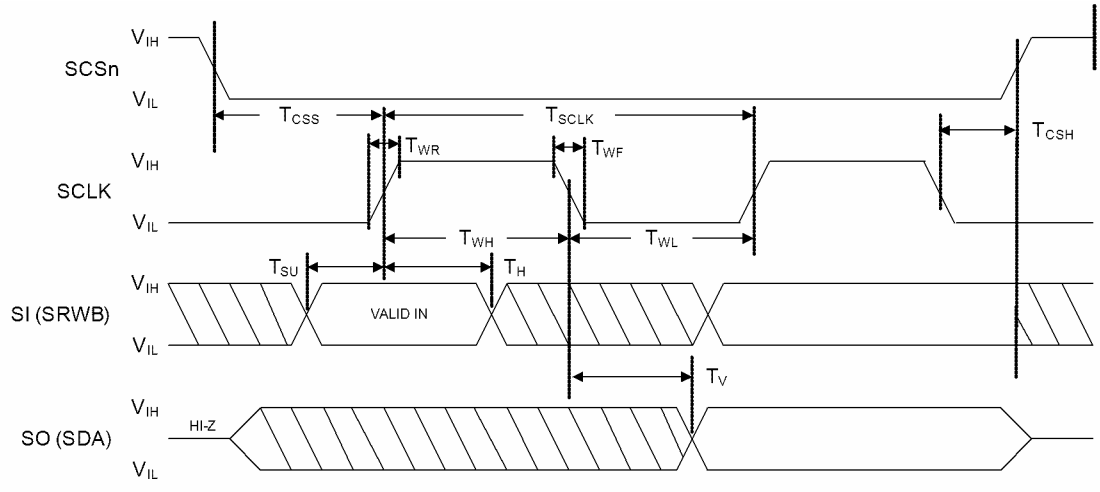


Figure 7-3 G-SPI Transaction Timing

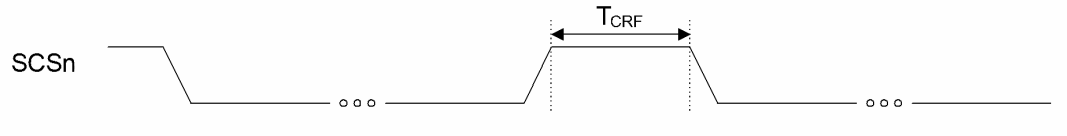
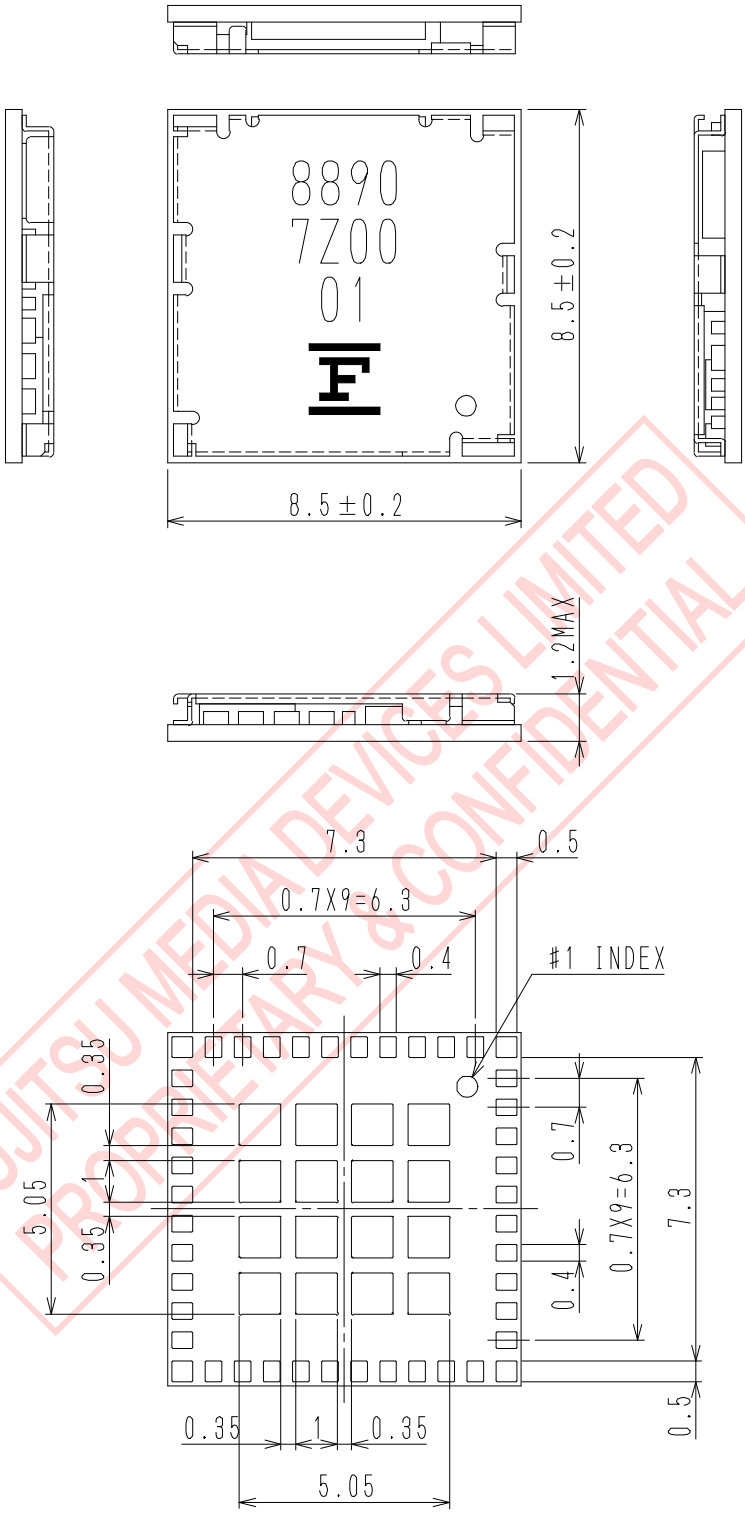


Figure 7-4 G-SPI Inter-Transaction Timing

8. Mechanical Characteristics

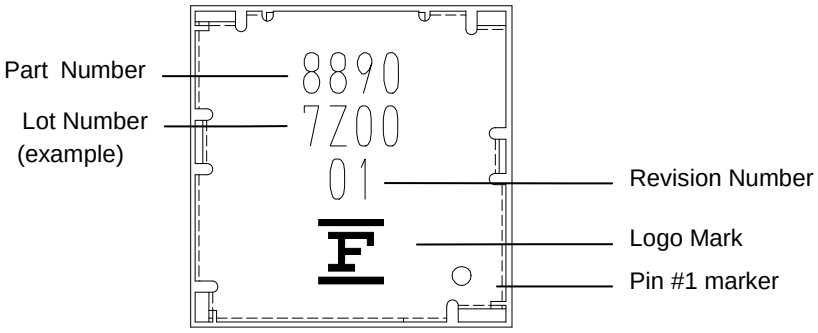
8-1. Appearance and Dimensions



Unit: mm

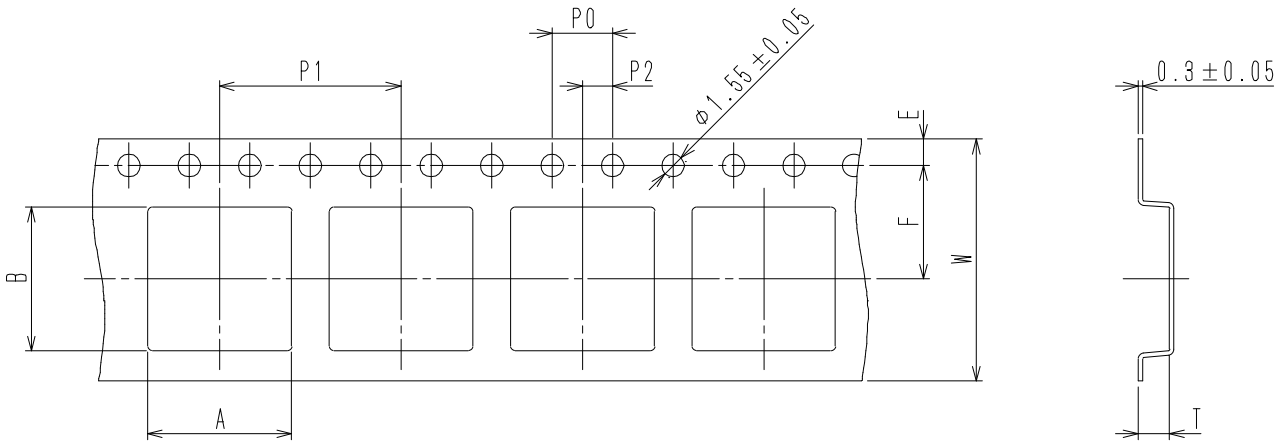
						TITLE	MBH7WLZ16-8890 Specification
						DRAW NO.	Tech Bes No. FMD/03158
EDIT	DATE	DESIG.	CHECK	DESCRIPTION		FUJITSU MEDIA DEVICES LIMITED	PAGE 19 / 25
DESIG.			CHECK		APPR.		

8-2. Marking



9. Shipment Packing Specification

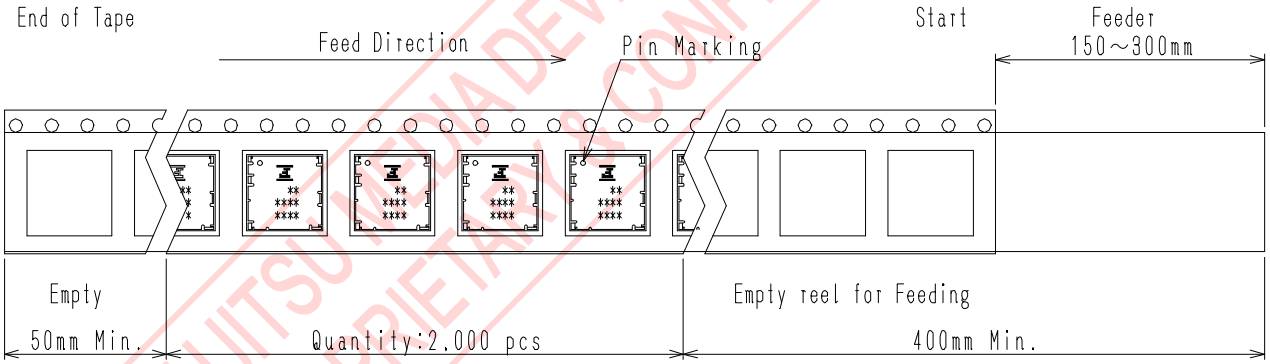
9-1. Carrier Tape Appearance and Dimensions



	A	B	W	F	E	P0	P1	P2	T
Dimensions	9.5	9.5	16.0	7.5	1.75	4.0	12.0	2.0	2.1
Tolerance	+/-0.1	+/-0.1	+/-0.3	+/-0.1	+/-0.1	+/-0.1	+/-0.1	+/-0.1	+/-0.1

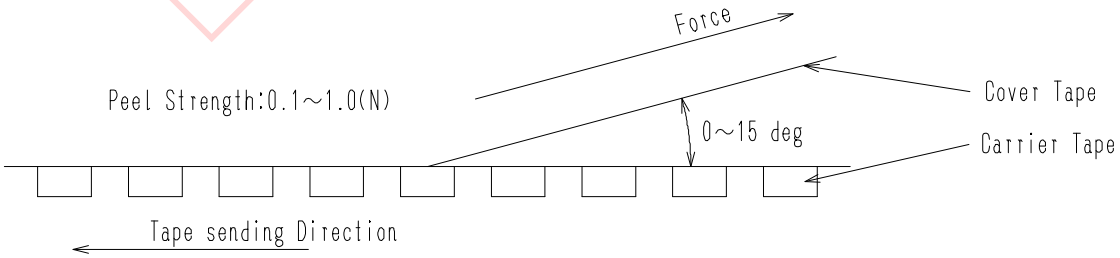
(unit:mm)

9-2. Taping Configuration



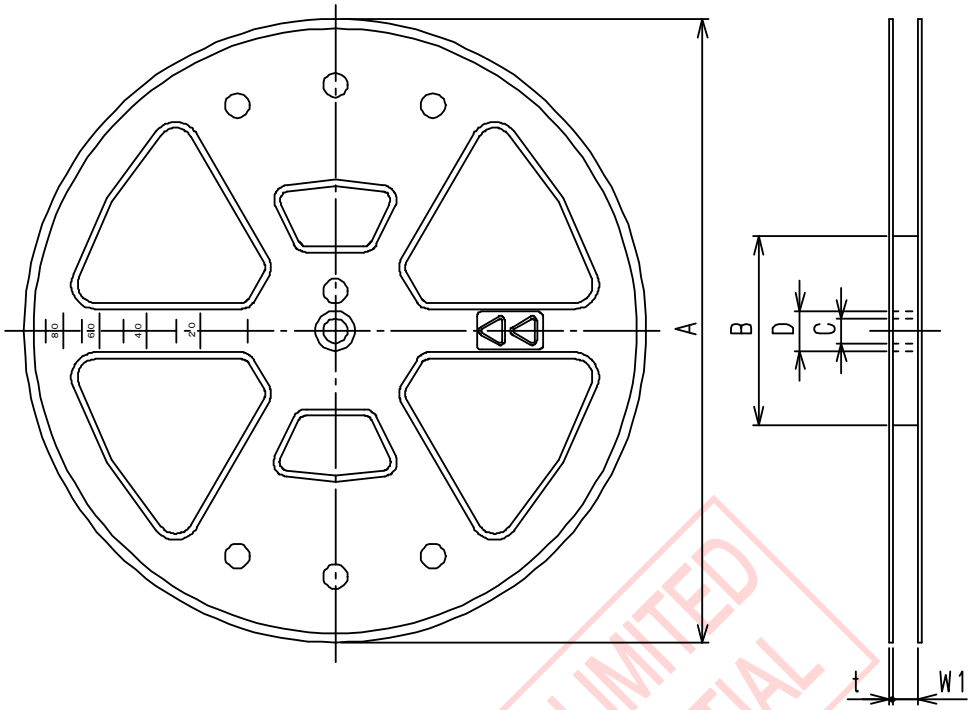
(unit:mm)

9-3. Tape Reel Strength



9-4. Reel Configuration and Bar Code Label Specification

9-4-1. Reel Configuration

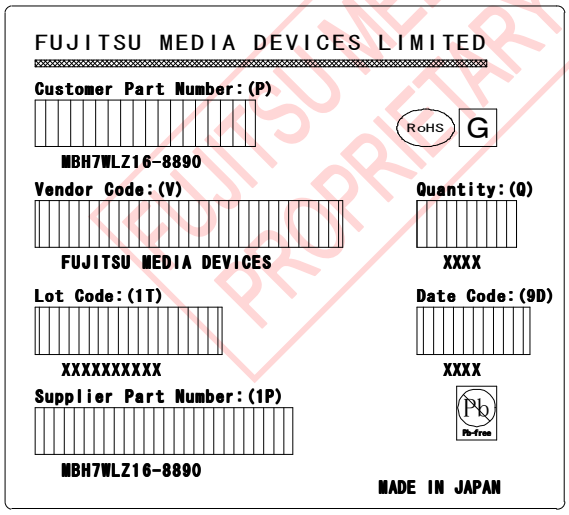


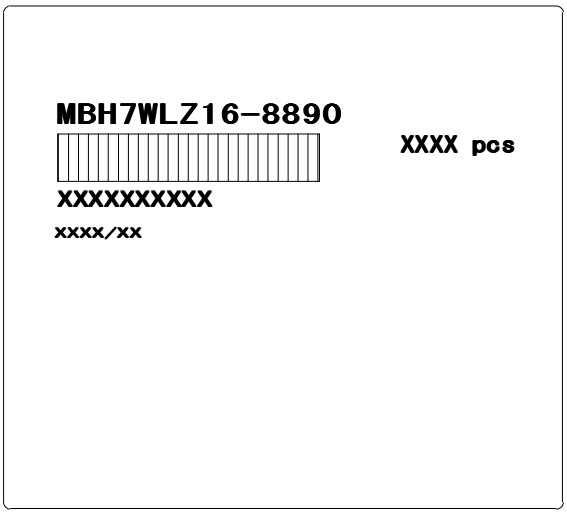
* Label indications P/N, Quantity and Lot.Number

	A	B	C	D	W1	T
Dimensions	330.0	80.0	13.0	21.0	17.4	2.0
Tolerance	+/-2.0	+/-1.0	+/-0.2	+/-0.8	+/-1.0	+/-1.0

(unit:mm)

9-4-2. Bar Code Label Specification





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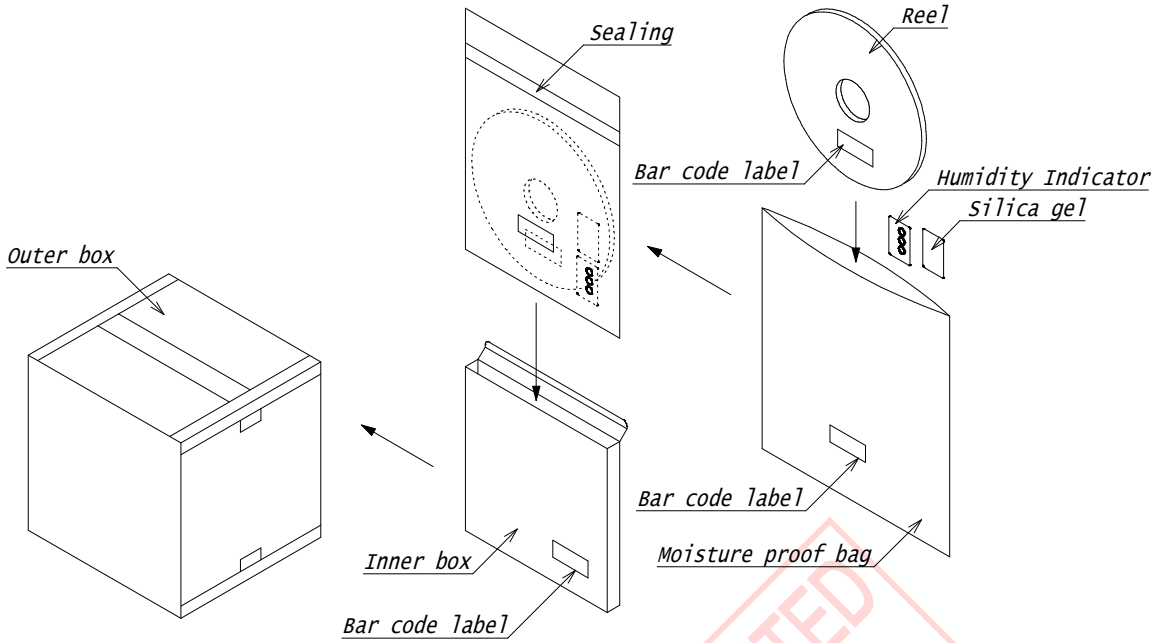
DESIG.			CHECK				APPR.					

TITLE	MBH7WLZ16-8890 Specification
DRAW NO.	Tech Bes No. FMD/03158
FUJITSU MEDIA DEVICES LIMITED	PAGE 22 / 25

9-5. Packing Specification



Carrier tape	Polystyrene+Styrenebutadiene
Caver tape	Polyester
Reel	Polystyrene+Carbon
Humidity Indicator	Paper
Moisture proof bag	PET/Al/PE 3Layer bag
Inner box	cardboard
Outer box	cardboard

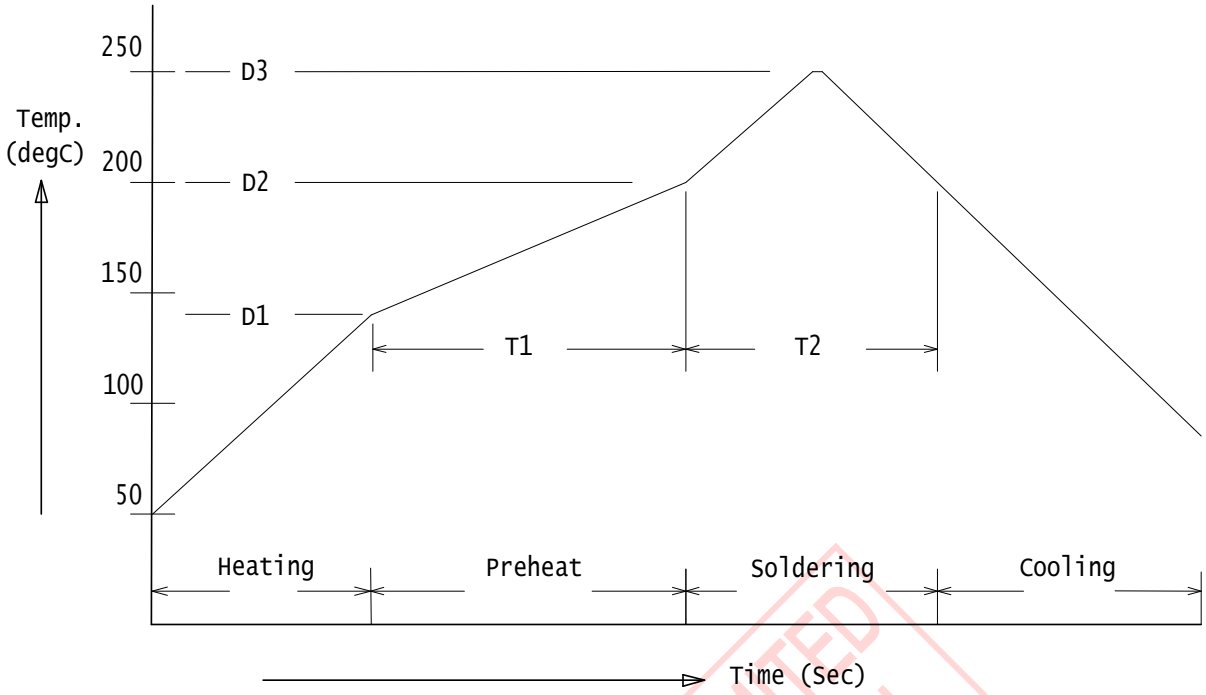
10. Moisture Sensitivity Level

IPC/JEDEC Standard J-STD-020D: Level 3

In case of keeping except above condition, be sure to apply baking.

Baking Method: Ta = 60 ℃, over 24 h

11. Recommended Reflow Profile



Note: * Reflow soldering is recommended two times maximum.
* If your soldering conditions are different from our recommendation, consult with us.

No	Item	Temperature (℃)	Time (sec)
1	Pre-heat	D1: 140 ~ D2: 200	T1: 60 ~ 120
2	Soldering	D2: >= 200	T2: 80 max
3	Peak-Temp.	D3: 250℃ max	

Figure 11-1 Reflow-Profile

- Soldering Iron Conditions
  (1) Temperature: 350 ℃ max
  (2) Duration: 4 sec max (1 part)
  (3) Capacity: 30 W max

- Cleaning Conditions
  (1) Solvent
  I.P.A.
  (2) Method-Temperature-Duration
  Permeation: 40 ℃ max, 5 min max

12. Other Notice

(1) Change of Specification
When needed, we will change the specifications of this product based on an agreement with purchaser.

(2) Disposal Information
Regarding disposal of this product, please consult with the professionals.

(3) Supply After Discontinuance of Purchaser's Equipment
When the purchaser discontinue the production of equipment in which this product is in use, the supply of this product after the discontinuance will be mutually discussed and agreed between the purchaser and Fujitsu Media Devices.

(4) High Safety
This product is designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but is not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite). The purchaser shall not use this product for the above-mentioned uses. If the purchaser's equipment is likely to be used for the above-mentioned uses, please consult with our sales representative before use. Fujitsu Media Devices shall not be liable against the purchaser and/or any third party for any claims or damages arising in connection with the above-mentioned uses of this product.

13. Revision History

Revision No.	Date	Description
01	18-Dec-2007	First release