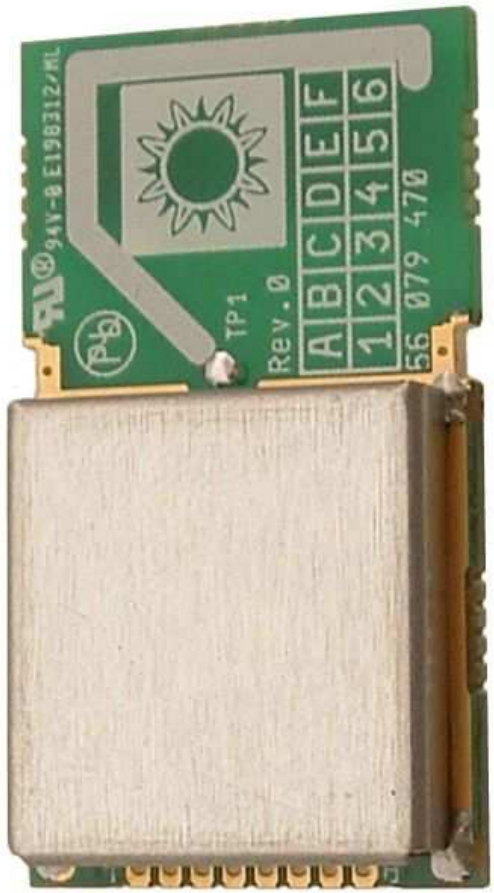
User manual
Transceiver module TXRX01



Contents

1 GENERAL

TXRX01 is a 2.4GHz Data Transceiver for short distance communications. It contains all components necessary to establish a two way communication with other modules of this make and model.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. this device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1. l'appareil ne doit pas produire de brouillage, et
2. l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

As with all RF-based communication devices, the operation range is affected by the given environmental conditions. No minimum range can be specified.

Precaution

- This module was designed to operate within ATLAS MTS developed machines only.
- This module is not to be used outside of this environment.
- This part must be handled as an "ELECTROSTATIC SENSITIVE DEVICE"
- This module may only be implemented by properly trained, authorized personnel.
- This module must only be operated in conjunction with a Host CPU, running an ATLAS approved firmware. This firmware must guarantee that the bandwith limits of the 2.4GHz ISM are not violated. It must be observed that, depending on configured bitrates, the max. and min. allowed operating frequency will vary.
- Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

2 SYSTEM INTEGRATION

The objective was to make the integration into the overall system as flexible as possible. Therefore, the footprint of the module was designed in a SMD style. It is recommended, that the connection to the Carrier board should be made by hand-soldering.

The TXRX01 module can be controlled by any microcontroller. You can operate and configure the module through a Serial Peripheral Interface (SPI). The register map, which is accessible through the SPI, contains all configuration registers in the module and is accessible in all operation modes of the chip.

The embedded baseband protocol engine (Enhanced ShockBurst™) is based on packet communication and supports various modes from manual operation to advanced autonomous protocol operation. Internal FIFOs ensure a smooth data flow between the radio front end and the system's MCU. Enhanced Shock-Burst™ reduces system cost by handling all the high speed link layer operations.

The radio front end uses GFSK modulation. It has user configurable parameters like frequency channel, output power and air data rate.
Internal voltage regulators ensure a high Power Supply Rejection Ratio (PSRR) and a wide power supply range.

3 PIN ASSIGNMENT

The TXRX01 consists of 8 connectors which includes the power supply and SPI interface.

Table 1: Pin assignment

Pin	Function	Type	Description
1	VDD	Power	3.3 V DC
2	VSS	Power	Ground (0V)
3	CE	Digital Input	Enable Activates RX or TX mode
4	/CS	Digital Input	SPI Chip Select
5	SCK	Digital Input	SPI Clock
6	MOSI	Digital Input	SPI Slave Data Input
7	MISO	Digital Output	SPI Slave Data Output, with tri-state option
8	IRQ	Digital Output	Maskable interrupt pin. Active low

4 RF CONSIDERATIONS

On module TXRX01 STR (Part number 56 079 470), the system antenna is designed as a stripline on the PCB. In order to obtain maximum operational range, coverage of the antenna by RF-attenuating or shielding materials should be avoided.

The module TXRX01 UFL (Part number 56 079 471) provides an U.FL connector instead of the stripline antenna. Except for the antenna-connector, the module is identical to TXRX01 STR. The technical data are the same. As external antenna the antenna 56 079 475 should be used only!

5 OPERATION

5.1 OPERATIONAL MODES

You can configure the TXRX01 module in power down, standby, RX or TX mode. This section describes these modes in detail.

5.2 STATE DIAGRAM

The state diagram in Figure 1 shows the operating modes and how they function. There are three types of distinct states highlighted in the state diagram:

- Recommended operating mode: is a recommended state used during normal operation.
- Possible operating mode: is a possible operating state, but is not used during normal operation.
- Transition state: is a time limited state used during start up of the oscillator and settling of the PLL.

When the VDD reaches 1.9V or higher, the TXRX01 module enters the Power on reset state where it remains in reset until entering the Power Down mode.

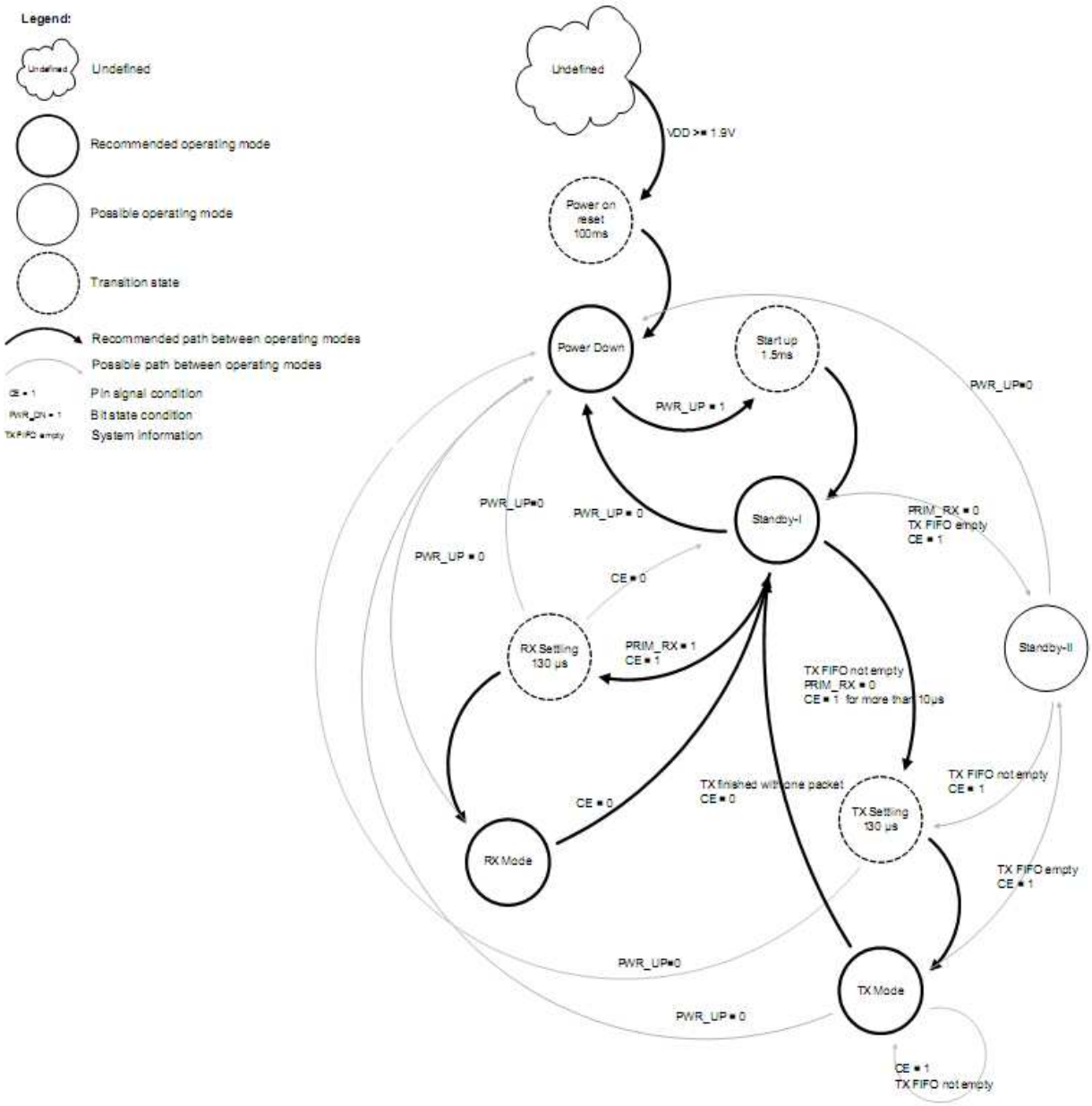


Figure 1: State diagram

5.3 POWER DOWN MODE

In power down mode the TXRX01 module is disabled using minimal current consumption. All register values available are maintained and the SPI is kept active, enabling change of configuration and the uploading/downloading of data registers.
Power down mode is entered by setting the PWR_UP bit in the CONFIG register low.

5.4 STANDBY MODES

5.4.1 Standby-I mode

By setting the PWR_UP bit in the CONFIG register to 1, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start up times. In this mode only part of the crystal oscillator is active. Change to active modes only happens if CE is set high and when CE is set low, the TXRX01 module returns to standby-I mode from both the TX and RX modes.

5.4.2 Standby-II mode

In standby-II mode extra clock buffers are active and more current is used compared to standby-I mode. The TXRX01 module enters standby-II mode if CE is held high on a PTX device with an empty TX FIFO. If a new packet is uploaded to the TX FIFO, the PLL immediately starts and the packet is transmitted after the normal PLL settling delay (130µs).
Register values are maintained and the SPI can be activated during both standby modes.

5.5 RX MODE

The RX mode is an active mode where the TXRX01 module is used as a receiver. To enter this mode, the TXRX01 module must have the PWR_UP bit, PRIM_RX bit and the CE pin set high.
In RX mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the baseband protocol engine. The baseband protocol engine constantly searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFOs. If the RX FIFOs are full, the received packet is discarded. The TXRX01 module remains in RX mode until the MCU configures it to standby-I mode or power down mode. However, if the automatic protocol features (Enhanced ShockBurst™) in the baseband protocol engine are enabled, the TXRX01 module can enter other modes in order to execute the protocol.
In RX mode a Received Power Detector (RPD) signal is available. The RPD is a signal that is set high when a RF signal higher than -64 dBm is detected inside the receiving frequency channel. The internal RPD signal is filtered before presented to the RPD register. The RF signal must be present for at least 40µs before the RPD is set high.

5.6 TX MODE

The TX mode is an active mode for transmitting packets. To enter this mode, the TXRX01 module must have the PWR_UP bit set high, PRIM_RX bit set low, a payload in the TX FIFO and a high pulse on the CE for more than 10µs.
The TXRX01 module stays in TX mode until it finishes transmitting a packet. If CE = 0, TXRX01 module returns to standby-I mode. If CE = 1, the status of the TX FIFO determines the next action. If the TX FIFO is not empty the TXRX01 module remains in TX mode and transmits the next packet. If the TX FIFO is empty the TXRX01 module goes into standby-II mode. The TXRX01 module transmitter PLL operates in open loop when in TX mode. It is important never to keep the TXRX01 module in TX mode for more than 4ms at a time. If the Enhanced ShockBurst™ features are enabled, TXRX01 module is never in TX mode longer than 4ms.

5.7 OPERATIONAL MODES CONFIGURATION

The following table describes how to configure the operational modes.

Table 2: Operational modes

Mode	PWR_UP register	PRIM_RX register	CE input pin	FIFO state
RX mode	1	1	1	-
TX mode	1	0	1	Data in TX FIFOs. Will empty all levels in TX FIFOs (a)
TX mode	1	0	Min. 10µs high pulse	Data in TX FIFOs.Will empty one level in TX FIFOs (b)
Standby-II	1	0	1	TX FIFO empty.
Standby-I	1	-	0	No ongoing packet transmission.
Power Down	0	-	-	-

(a) If CE is held high all TX FIFOs are emptied and all necessary ACK and possible retransmits are carried out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when the CE is still high, TXRX01 module enters standby-II mode. In this mode the transmission of a packet is started as soon as the CSN is set high after an upload (UL) of a packet to TX FIFO.

(b) This operating mode pulses the CE high for at least 10µs. This allows one packet to be transmitted. This is the normal operating mode. After the packet is transmitted, the TXRX01 module enters standby-I mode.

5.8 DATA AND CONTROL INTERFACE

The data and control interface gives you access to all the features in the TXRX01 module. The data and control interface consists of the following six digital signals:

- IRQ (this signal is active low and controlled by three maskable interrupt sources)
- CE (this signal is active high and used to activate the chip in RX or TX mode)
- CSN (SPI signal)
- SCK (SPI signal)
- MOSI (SPI signal)
- MISO (SPI signal)

Using 1 byte SPI commands, you can activate the TXRX01 module data FIFOs or the register map during all modes of operation.

5.8.1 Features

- Special SPI commands for quick access to the most frequently used features
- 0-10Mbps 4-wire SPI
- 8 bit command set
- Easily configurable register map
- Full three level FIFO for both TX and RX direction

5.8.2 Functional description

The SPI is a standard SPI with a maximum data rate of 10Mbps.

5.8.3 SPI operation

The module provides a set of registers which control all settings and data flow. It is advisable that the firmware should read-back the contents of the channel registers, in order to avoid switching to erroneous frequencies.

5.8.3.1 SPI Commands

The SPI commands are shown in Table 19. Every new command must be started by a high to low transition on CSN.

The STATUS register is serially shifted out on the MISO pin simultaneously to the SPI command word shifting to the MOSI pin.
The serial shifting SPI commands is in the following format:
Command word: MSBit to LSBit (one byte)
Data bytes: LSByte to MSByte, MSBit in each byte first

Table 3: SPI commands

Command name	Command word (binary)	# Data bytes	Operation
R_REGISTER	000A AAAA	1 to 5 LSByte first	Read command and status registers. AAAAA = 5 bit Register Map Address
W_REGISTER	001A AAAA	1 to 5 LSByte first	Write command and status registers. AAAAA = 5 bit Register Map Address Executable in power down or standby modes only.
R_RX_PAYLOAD	0110 0001	1 to 32 LSByte first	Read RX-payload: 1 – 32 bytes. A read operation always starts at byte 0. Payload is deleted from FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32 LSByte first	Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0 used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode. Should not be executed during transmission of acknowledge, that is, acknowledge package will not be completed.
REUSE_TX_PL	1110 0011	0	Used for a PTX device. Reuse last transmitted payload. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX payload reuse must not be activated or deactivated during package transmission.
R_RX_PL_WID (a)	0110 0000	1	Read RX payload width for the top R_RX_PAYLOAD in the RX FIFO.
W_ACK_PAYLOAD (a)	1010 1PPP	1 to 32 LSByte first	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled using first in - first out principle. Write payload: 1– 32 bytes. A write operation always starts at byte 0.
W_TX_PAYLOAD_NO ACK (a)	1011 0000	1 to 32 LSByte first	Used in TX mode. Disables AUTOACK on this specific packet.
NOP	1111 1111	0	No Operation. Might be used to read the STATUS register

(a) The bits in the FEATURE register have to be set.

The W_REGISTER and R_REGISTER commands operate on single or multi-byte registers. When accessing multi-byte registers read or write to the MSBit of LSByte first. You can terminate the writing before all bytes in a multi-byte register are written, leaving the unwritten MSByte(s) unchanged. For example, the LSByte of RX_ADDR_P0 can be modified by writing only one byte to the RX_ADDR_P0 register. The content of the status register is always read to MISO after a high to low transition on CSN.
Note: The 3 bit pipe information in the STATUS register is updated during the IRQ pin high to low transition. The pipe information is unreliable if the STATUS register is read during an IRQ pin high to low transition.

5.8.4 Data FIFO

The data FIFOs store transmitted payloads (TX FIFO) or received payloads that are ready to be clocked out (RX FIFO). The FIFOs are accessible in both PTX mode and PRX mode.

The following FIFOs are present in TXRX01 module:

- TX three level, 32 byte FIFO

- RX three level, 32 byte FIFO

Both FIFOs have a controller and are accessible through the SPI by using dedicated SPI commands. A TX FIFO in PRX can store payloads for ACK packets to three different PTX devices. If the TX FIFO contains more than one payload to a pipe, payloads are handled using the first in - first out principle. The TX FIFO in a PRX is blocked if all pending payloads are addressed to pipes where the link to the PTX is lost. In this case, the MCU can flush the TX FIFO using the FLUSH_TX command.
The RX FIFO in PRX can contain payloads from up to three different PTX devices and a TX FIFO in PTX can have up to three payloads stored.

You can write to the TX FIFO using these three commands; W_TX_PAYLOAD and W_TX_PAYLOAD_NO_ACK in PTX mode and W_ACK_PAYLOAD in PRX mode. All three commands provide access to the TX_PLD register (see Table 27. on page 60. for details of this register).
The RX FIFO can be read by the command R_RX_PAYLOAD in PTX and PRX mode. This command provides access to the RX_PLD register.
The payload in TX FIFO in a PTX is not removed if the MAX_RT IRQ is asserted.

You can read if the TX and RX FIFO are full or empty in the FIFO_STATUS register.

5.8.5 Register map

Table 4: Register map

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
0	CONFIG				Configuration Register
	Reserved	7	0	R/W	Only '0' allowed
	MASK_RX_DR	6	0	R/W	Mask interrupt caused by RX_DR 1: Interrupt not reflected on the **IRQ** pin 0: Reflect RX_DR as active low interrupt on the **IRQ** pin
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS 1: Interrupt not reflected on the **IRQ** pin 0: Reflect TX_DS as active low interrupt on the **IRQ** pin
	MASK_MAX_RT	4	0	R/W	Mask interrupt caused by MAX_RT 1: Interrupt not reflected on the **IRQ** pin 0: Reflect MAX_RT as active low interrupt on the **IRQ** pin
	EN_CRC	3	1	R/W	Enable CRC. Forced high if one of the bits in the EN_AA is high
	CRCO	2	0	R/W	CRC encoding scheme '0' - 1 byte '1' – 2 bytes
	PWR_UP	1	0	R/W	1: POWER UP, 0: POWER DOWN
	PRIM_RX	0	0	R/W	RX/TX control 1: PRX, 0: PTX
1	EN_AA				Enable 'Auto Acknowledgment' Function
	Reserved	7:6	0	R/W	Only '00' allowed
	ENAA_P5	5	1	R/W	Enable auto acknowledgement data pipe 5
	ENAA_P4	4	1	R/W	Enable auto acknowledgement data pipe 4
	ENAA_P3	3	1	R/W	Enable auto acknowledgement data pipe 3
	ENAA_P2	2	1	R/W	Enable auto acknowledgement data pipe 2

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
	ENAA_P1	1	1	R/W	Enable auto acknowledgement data pipe 1
	ENAA_P0	0	1	R/W	Enable auto acknowledgement data pipe 0
2	EN_RXADDR				Enabled RX Addresses
	Reserved	7:6	0	R/W	Only '00' allowed
	ERX_P5	5	0	R/W	Enable data pipe 5.
	ERX_P4	4	0	R/W	Enable data pipe 4.
	ERX_P3	3	0	R/W	Enable data pipe 3.
	ERX_P2	2	0	R/W	Enable data pipe 2.
	ERX_P1	1	1	R/W	Enable data pipe 1.
	ERX_P0	0	1	R/W	Enable data pipe 0.
3	SETUP_AW				Setup of Address Widths (common for all data pipes)
	Reserved	7:2	0	R/W	Only '000000' allowed
	AW	1:0	11	R/W	RX/TX Address field width '00' - Illegal '01' - 3 bytes '10' - 4 bytes '11' – 5 bytes LSByte is used if address width is below 5 bytes
4	SETUP_RETR				Setup of Automatic Retransmission
	ARD (a	7:4	0	R/W	Auto Retransmit Delay ‘0000’ – Wait 250µS ‘0001’ – Wait 500µS ‘0010’ – Wait 750µS …….. ‘1111’ – Wait 4000µS (Delay defined from end of transmission to start of next transmission) (b
	ARC	3:0	11	R/W	Auto Retransmit Count ‘0000’ –Re-Transmit disabled ‘0001’ – Up to 1 Re-Transmit on fail of AA …… ‘1111’ – Up to 15 Re-Transmit on fail of AA
5	RF_CH				RF Channel
	Reserved	7	0	R/W	Only '0' allowed
	RF_CH	6:0	10	R/W	Sets the frequency channel TXRX01 module operates on **Attention** To avoid violation of FCC or IC regulations, the allowed range for this register is limited to 2 – 80 (2.402 - 2.480GHz).
6	RF_SETUP				RF Setup Register
	CONT_WAVE	7	0	R/W	Enables continuous carrier transmit when high.
	Reserved	6	0	R/W	Only '0' allowed
	RF_DR_LOW	5	0	R/W	Set RF Data Rate to 250kbps. See RF_DR_HIGH for encoding.
	PLL_LOCK	4	0	R/W	Force PLL lock signal. Only used in test

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
	RF_DR_HIGH	3	1	R/W	Select between the high speed data rates. This bit is don't care if RF_DR_LOW is set. Encoding: [RF_DR_LOW, RF_DR_HIGH]: '00' – 1Mbps '01' – 2Mbps '10' – 250kbps '11' – Reserved
	RF_PWR	2:1	11	R/W	Set RF output power in TX mode '00' – -18dBm '01' – -12dBm '10' – -6dBm '11' – 0dBm
	Obsolete	0			Don't care
7	STATUS				Status Register (In parallel to the SPI command word applied on the **MOSI** pin, the STATUS register is shifted serially out on the **MISO** pin)
	Reserved	7	0	R/W	Only '0' allowed
	RX_DR	6	0	R/W	Data Ready RX FIFO interrupt. Asserted when new data arrives RX FIFO (c. Write 1 to clear bit.
	TX_DS	5	0	R/W	Data Sent TX FIFO interrupt. Asserted when packet transmitted on TX. If AUTO_ACK is activated, this bit is set high only when ACK is received. Write 1 to clear bit.
	MAX_RT	4	0	R/W	Maximum number of TX retransmits interrupt Write 1 to clear bit. If MAX_RT is asserted it must be cleared to enable further communication.
	RX_P_NO	3:1	111	R	Data pipe number for the payload available for reading from RX_FIFO 000-101: Data Pipe Number 110: Not Used 111: RX FIFO Empty
	TX_FULL	0	0	R	TX FIFO full flag. 1: TX FIFO full. 0: Available locations in TX FIFO.
8	OBSERVE_TX				Transmit observe register
	PLOS_CNT	7:4	0	R	Count lost packets. The counter is overflow protected to 15, and discontinues at max until reset. The counter is reset by writing to RF_CH.
	ARC_CNT	3:0	0	R	Count retransmitted packets. The counter is reset when transmission of a new packet starts.
9	RPD				
	Reserved	7:1	0	R	
	RPD	0	0	R	Received Power Detector.
0A	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	Receive address data pipe 0. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)
0B	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	Receive address data pipe 1. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
0C	RX_ADDR_P2	7:0	0xC3	R/W	Receive address data pipe 2. Only LSB. MSBytes are equal to RX_ADDR_P1[39:8]
0D	RX_ADDR_P3	7:0	0xC4	R/W	Receive address data pipe 3. Only LSB. MSBytes are equal to RX_ADDR_P1[39:8]
0E	RX_ADDR_P4	7:0	0xC5	R/W	Receive address data pipe 4. Only LSB. MSBytes are equal to RX_ADDR_P1[39:8]
0F	RX_ADDR_P5	7:0	0xC6	R/W	Receive address data pipe 5. Only LSB. MSBytes are equal to RX_ADDR_P1[39:8]
10	TX_ADDR	39:0	0xE7E7E 7E7E7	R/W	Transmit address. Used for a PTX device only. (LSByte is written first) Set RX_ADDR_P0 equal to this address to handle automatic acknowledge if this is a PTX device with Enhanced ShockBurst™ enabled.
11	RX_PW_P0				
	Reserved	7:6	0	R/W	Only '00' allowed
	RX_PW_P0	5:0	0	R/W	Number of bytes in RX payload in data pipe 0 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
12	RX_PW_P1				
	Reserved	7:6	0	R/W	Only '00' allowed
	RX_PW_P1	5:0	0	R/W	Number of bytes in RX payload in data pipe 1 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
13	RX_PW_P2				
	Reserved	7:6	0	R/W	Only '00' allowed
	RX_PW_P2	5:0	0	R/W	Number of bytes in RX payload in data pipe 2 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
14	RX_PW_P3				
	Reserved	7:6	0	R/W	Only '00' allowed
	RX_PW_P3	5:0	0	R/W	Number of bytes in RX payload in data pipe 3 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
15	RX_PW_P4				
	Reserved	7:6	0	R/W	Only '00' allowed

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
	RX_PW_P4	5:0	0	R/W	Number of bytes in RX payload in data pipe 4 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
16	RX_PW_P5				
	Reserved	7:6	0	R/W	Only '00' allowed
	RX_PW_P5	5:0	0	R/W	Number of bytes in RX payload in data pipe 5 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
17	FIFO_STATUS				FIFO Status Register
	Reserved	7	0	R/W	Only '0' allowed
	TX_REUSE	6	0	R	Used for a PTX device Pulse the rfce high for at least 10µs to Reuse last transmitted payload. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX_REUSE is set by the SPI command REUSE_TX_PL, and is reset by the SPI commands W_TX_PAYLOAD or FLUSH TX
	TX_FULL	5	0	R	TX FIFO full flag. 1: TX FIFO full. 0: Available locations in TX FIFO.
	TX_EMPTY	4	1	R	TX FIFO empty flag. 1: TX FIFO empty. 0: Data in TX FIFO.
	Reserved	3:2	0	R/W	Only '00' allowed
	RX_FULL	1	0	R	RX FIFO full flag. 1: RX FIFO full. 0: Available locations in RX FIFO.
	RX_EMPTY	0	1	R	RX FIFO empty flag. 1: RX FIFO empty. 0: Data in RX FIFO.
N/A	ACK_PLD	255:0	X	W	Written by separate SPI command ACK packet payload to data pipe number PPP given in SPI command. Used in RX mode only. Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled first in first out.
N/A	TX_PLD	255:0	X	W	Written by separate SPI command TX data payload register 1 - 32 bytes. This register is implemented as a FIFO with three levels. Used in TX mode only.
N/A	RX_PLD	255:0	X	R	Read by separate SPI command. RX data payload register. 1 - 32 bytes. This register is implemented as a FIFO with three levels. All RX channels share the same FIFO.

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
1C	DYNPD				Enable dynamic payload length
	Reserved	7:6	0	R/W	Only '00' allowed
	DPL_P5	5	0	R/W	Enable dynamic payload length data pipe 5. (Requires EN_DPL and ENAA_P5)
	DPL_P4	4	0	R/W	Enable dynamic payload length data pipe 4. (Requires EN_DPL and ENAA_P4)
	DPL_P3	3	0	R/W	Enable dynamic payload length data pipe 3. (Requires EN_DPL and ENAA_P3)
	DPL_P2	2	0	R/W	Enable dynamic payload length data pipe 2. (Requires EN_DPL and ENAA_P2)
	DPL_P1	1	0	R/W	Enable dynamic payload length data pipe 1. (Requires EN_DPL and ENAA_P1)
	DPL_P0	0	0	R/W	Enable dynamic payload length data pipe 0. (Requires EN_DPL and ENAA_P0)
1D	FEATURE			R/W	Feature Register
	Reserved	7:3	0	R/W	Only '00000' allowed
	EN_DPL	2	0	R/W	Enables Dynamic Payload Length
	EN_ACK_PAY (d	1	0	R/W	Enables Payload with ACK
	EN_DYN_ACK	0	0	R/W	Enables the W_TX_PAYLOAD_NOACK command

(a Please take care when setting this parameter. If the ACK payload is more than 15 byte in 2Mbps mode the ARD must be 500µS or more, if the ACK payload is more than 5byte in 1Mbps mode the ARD must be 500µS or more. In 250kbps mode (even when the payload is not in ACK) the ARD must be 500µS or more.

(b This is the time the PTX is waiting for an ACK packet before a retransmit is made. The PTX is in RX mode for a minimum of 250µS, but it stays in RX mode to the end of the packet if that is longer than 250µS. Then it goes to standby-I mode for the rest of the specified ARD. After the ARD it goes to TX mode and then retransmits the packet.

(c The RX_DR IRQ is asserted by a new packet arrival event. The procedure for handling this interrupt should be: 1) read payload through SPI, 2) clear RX_DR IRQ, 3) read FIFO_STATUS to check if there are more payloads available in RX FIFO, 4) if there are more data in RX FIFO, repeat from step 1).

(d If ACK packet payload is activated, ACK packets have dynamic payload lengths and the Dynamic Payload Length feature should be enabled for pipe 0 on the PTX and PRX. This is to ensure that they receive the ACK packets with payloads. If the ACK payload is more than 15 byte in 2Mbps mode the ARD must be 500µS or more, and if the ACK payload is more than 5 byte in 1Mbps mode the ARD must be 500µS or more. In 250kbps mode (even when the payload is not in ACK) the ARD must be 500µS or more.

5.8.6 Interrupt

The TXRX01 module has an active low interrupt (IRQ) pin. The IRQ pin is activated when TX_DS IRQ, RX_DR IRQ or MAX_RT IRQ are set high by the state machine in the STATUS register. The IRQ pin resets when MCU writes '1' to the IRQ source bit in the STATUS register. The IRQ mask in the CONFIG register is used to select the IRQ sources that are allowed to assert the IRQ pin. By setting one of the MASK bits high, the corresponding IRQ source is disabled. By default all IRQ sources are enabled.

Note: The 3 bit pipe information in the STATUS register is updated during the IRQ pin high to low transition. The pipe information is unreliable if the STATUS register is read during an IRQ pin high to low transition.

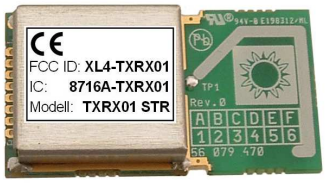
6 LABEL AND LABEL LOCATION INFO

The transceiver module TXRX01 must be labelled with its FCC ID and IC number.

6.1 MODULE TXRX01 STR

CE
FCC ID: **XL4-TXRX01**
IC: **8716A-TXRX01**
Modell: **TXRX01 STR**

Label for TXRX01 STR module (1,8 cm * 2,9 cm)



If the label is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module.

Contains

FCC ID: XL4-TXRX01
IC: 8716A-TXRX01
Modell: TXRX01 STR

Exterior label TXRX01 STR (3 cm * 4,1 cm)

6.2 MODULE TXRX01 UFL

CE
FCC ID: **XL4-TXRX01**
IC: **8716A-TXRX01**
Modell: **TXRX01 UFL**

Label for TXRX01 UFL module (1,8 cm * 2,9 cm)

If the label is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module.

Contains

FCC ID: XL4-TXRX01
IC: 8716A-TXRX01
Modell: TXRX01 UFL

Exterior label TXRX01 UFL (3 cm * 4,1 cm)

7 POWER SUPPLY

This module is designed to operate at an internal voltage of 3.3VDC max. This is provided by the use of a LDO voltage regulator with a typical dropout voltage of 150mV, allowing Lithium batteries with a nominal output of >= 3.5V to be used. The absolute maximum input voltage is 4VDC.

8 INPUT CURRENT

The input current is mode dependent and reaches a peak of 12 mA while transmitting and 14 mA while receiving, both at 2 Megabits per second.
In Standby mode, the supply current does not exceed 400uA.
In Sleep mode, the supply current is below 1uA.

All data are specified at Vdd = +3.3VDC.

9 TECHNICAL DATA

Power supply:	Umin = 3.0 V DC
	Unom = 3.3 V DC
	Umax = 4.0 V DC
Input voltage	-0.3 V - 5.25 V
Output voltage	VSS to VDD
Total Power Dissipation (TA=85℃)	60 mW
Operating Temperature	-40 +85 ℃
Storage Temperature	-40 +125 ℃
Frequency band:	2.4GHz ISM (2.402 - 2.480GHz)
Channel band with:	max 2MHz in 2 Mbps mode
Radio channels:	79
Modulation:	GFSK
Radio data rate:	max 2 Mbps
Transmission power:	max. 0 dBm
Lowest internal clock frequency:	16.000 MHz
SPI speed:	up to 10 Mbps
Antenna type	
TXRX01 STR:	Integral
TXRX01 UFL:	external (ID 56079475)