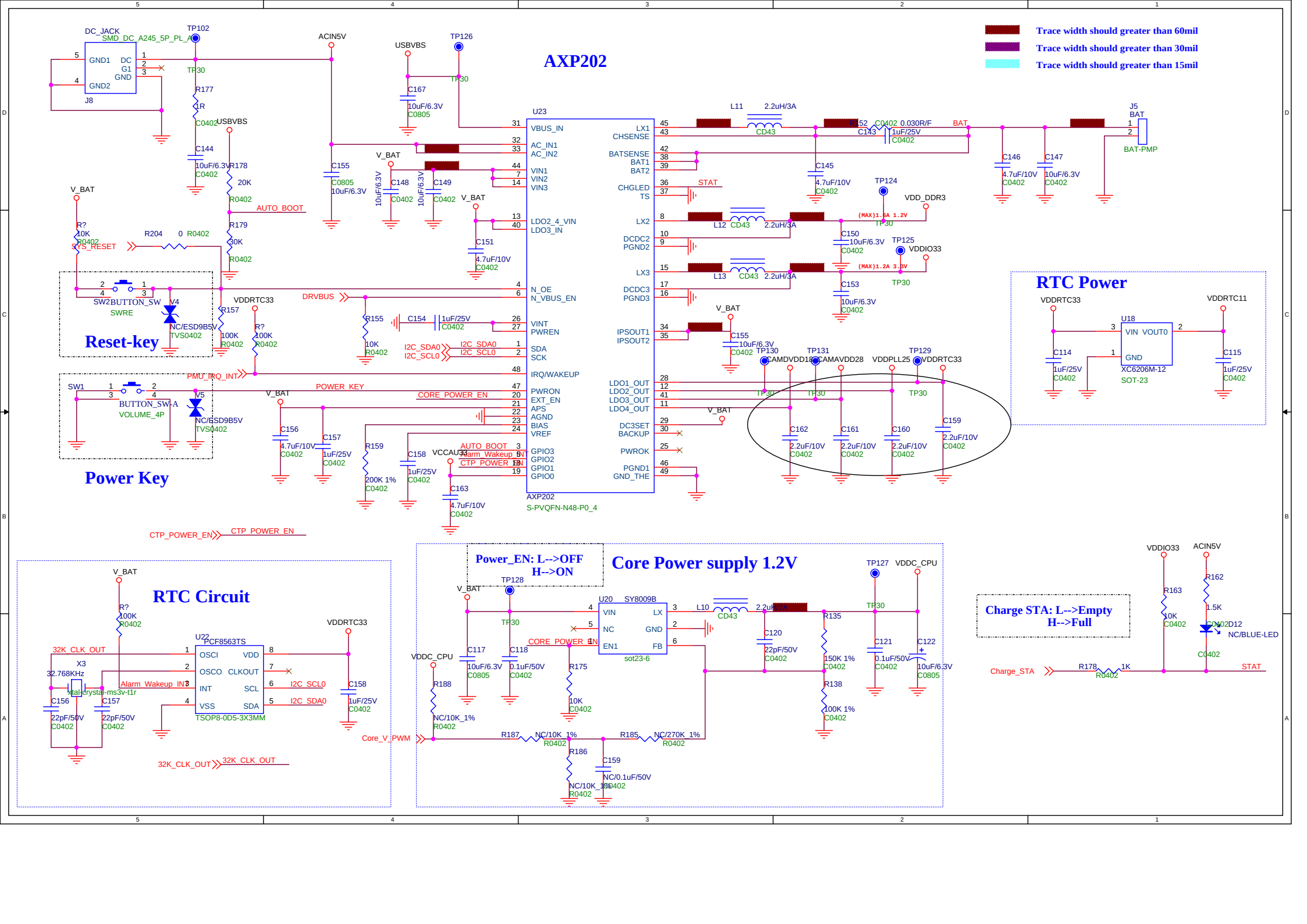
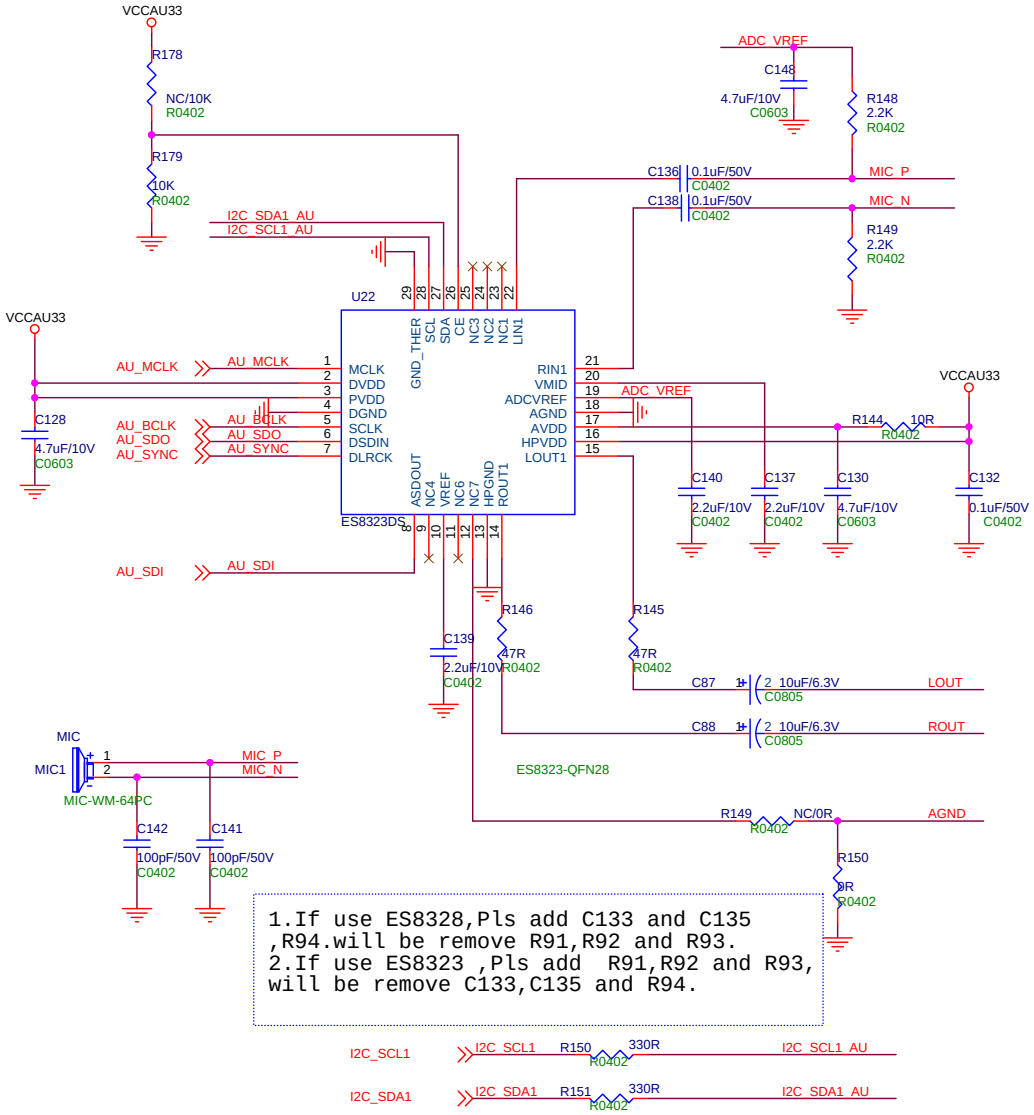

AXP202
Trace width should greater than 60mil
Trace width should greater than 30mil
Trace width should greater than 15mil
DC_JACK
SMD_DC_A245_5P_PL_A
J8
TP102
TP30
R177
1R
C0402
C144
10uF/6.3V
C0402
USBVBS
ACIN5V
TP126
C167
10uF/6.3V
C0805
C155
C0805
10uF/6.3V
V_BAT
C148
C0402
C149
C0402
R178
20K
R0402
AUTO_BOOT
R179
30K
R0402
R204
0 R0402
SYS_RESET
R?
10K
R0402
SW2
BUTTON_SW
SWRE
V4
NC/ESD9B5V
TVS0402
Reset-key
VDDRTC33
R157
100K
R0402
R?
100K
R0402
DRVBUS
R155
10K
R0402
C154
1uF/25V
C0402
I2C_SDA0
I2C_SCL0
PMU_IRQ_INT
SW1
BUTTON_SW-A
VOLUME_4P
V5
NC/ESD9B5V
TVS0402
Power Key
POWER_KEY
CORE_POWER_EN
AUTO_BOOT
Alarm_Wakeup_IN
CTP_POWER_EN
C156
4.7uF/10V
C0402
C157
1uF/25V
C0402
R159
200K 1%
C0402
C158
1uF/25V
C0402
VCCAU33
C163
4.7uF/10V
C0402
U23
VBUS_IN
AC_IN1
AC_IN2
VIN1
VIN2
VIN3
LDO2_4_VIN
LDO3_IN
N_OE
N_VBUS_EN
VINT
PWREN
SDA
SCK
IRQ/WAKEUP
PWRON
EXT_EN
APS
AGND
BIAS
VREF
GPIO3
GPIO2
GPIO1
GPIO0
LX1
CHSENSE
BATSENSE
BAT1
BAT2
CHGLED
TS
LX2
DCDC2
PGND2
LX3
DCDC3
PGND3
IPSOUT1
IPSOUT2
LDO1_OUT
LDO2_OUT
LDO3_OUT
LDO4_OUT
DC3SET
BACKUP
PWROK
PGND1
GND_THE
AXP202
S-PVQFN-N48-P0_4
L11
2.2uH/3A
CD43
R152
C0402
0.030R/F
C143
1uF/25V
C0402
BAT
J5
BAT
BAT-PMP
C145
4.7uF/10V
C0402
C146
4.7uF/10V
C0402
C147
10uF/6.3V
C0402
STAT
TP124
VDD_DDR3
L12
CD43
2.2uH/3A
(MAX)1.6A 1.2V
TP30
C150
10uF/6.3V
C0402
TP125
VDDIO33
L13
CD43
2.2uH/3A
(MAX)1.2A 3.3V
TP30
C153
10uF/6.3V
C0402
C151
4.7uF/10V
C0402
C155
10uF/6.3V
C0402
TP130
CAMDVDD18
TP131
CAMAVDD28
TP129
VDDPLL25
VDDRTC33
TP30
TP30
TP30
C162
2.2uF/10V
C0402
C161
2.2uF/10V
C0402
C160
2.2uF/10V
C0402
C159
2.2uF/10V
C0402
RTC Power
VDDRTC33
U18
VIN VOUT0
GND
XC6206M-12
SOT-23
VDDRTC11
C114
1uF/25V
C0402
C115
1uF/25V
C0402
RTC Circuit
R?
100K
R0402
U22
PCF8563TS
OSCI
OSCO
INT
VSS
VDD
CLKOUT
SCL
SDA
TSOP8-0D5-3X3MM
32K_CLK_OUT
X3
32.768KHz
Xtal-crystal-ms3v-t1r
C156
22pF/50V
C0402
C157
22pF/50V
C0402
VDDRTC33
C158
1uF/25V
C0402
I2C_SCL0
I2C_SDA0
Alarm_Wakeup_IN
32K_CLK_OUT
Power_EN: L-->OFF
H-->ON
Core Power supply 1.2V
TP128
U20
SY8009B
VIN
NC
EN1
LX
GND
FB
sot23-6
L10
CD43
2.2uH/3A
TP127
VDDC_CPU
TP30
C117
10uF/6.3V
C0805
C118
0.1uF/50V
C0402
R175
10K
C0402
R188
NC/10K_1%
R0402
C120
22pF/50V
C0402
R135
150K 1%
C0402
R138
100K 1%
C0402
C121
0.1uF/50V
C0402
C122
10uF/6.3V
C0805
Core_V_PWM
R187
NC/10K_1%
R0402
R185
NC/270K_1%
R0402
R186
NC/10K_1%
R0402
C159
NC/0.1uF/50V
C0402
Charge STA: L-->Empty
H-->Full
VDDIO33
ACIN5V
R163
10K
C0402
R162
1.5K
C0402
D12
NC/BLUE-LED
Charge_STA
R178
1K
R0402
STAT

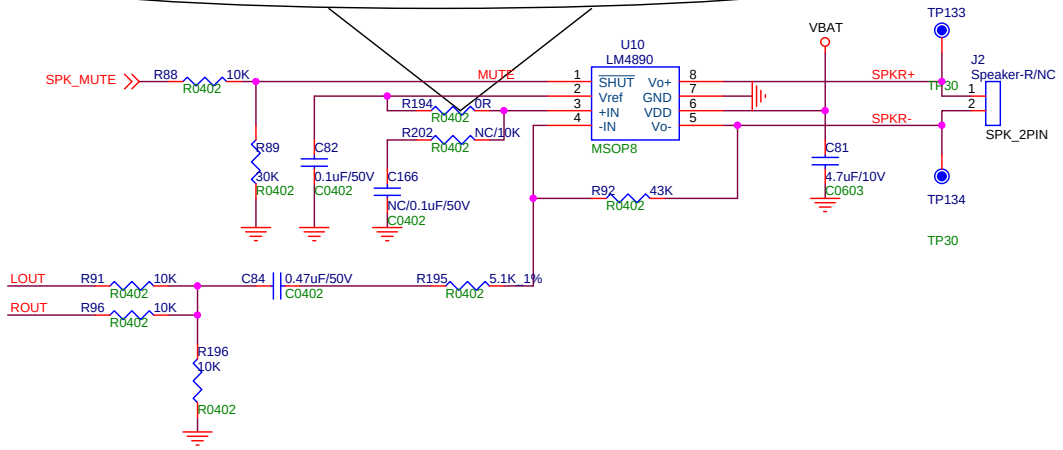
Audio codec ES8323



1.If use ES8328,Pls add C133 and C135 ,R94.will be remove R91,R92 and R93.
2.If use ES8323 ,Pls add R91,R92 and R93, will be remove C133,C135 and R94.

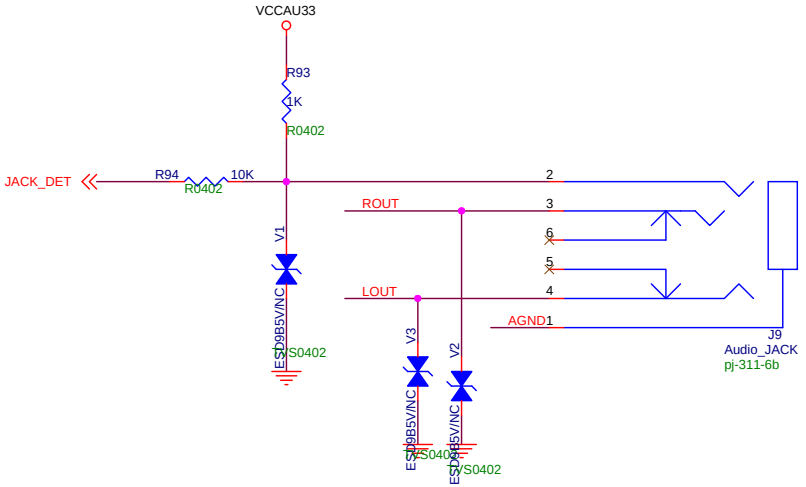
Amplifier

If use LM4890,pls change R194 Value for 0, other value Pls reference amplifier application

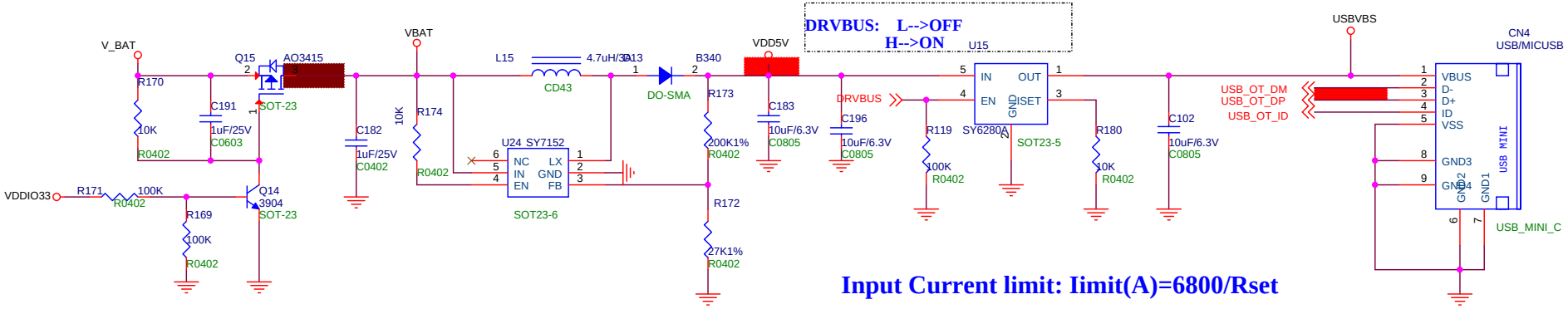


Speaker

EarPhone



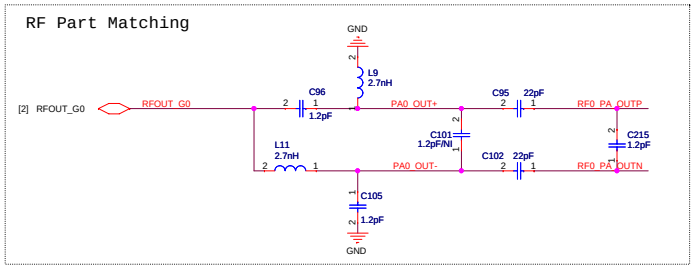
OTG/HOST/Charger

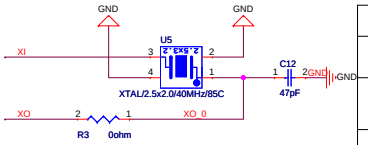


Input Current limit: Iimit(A)=6800/Rset

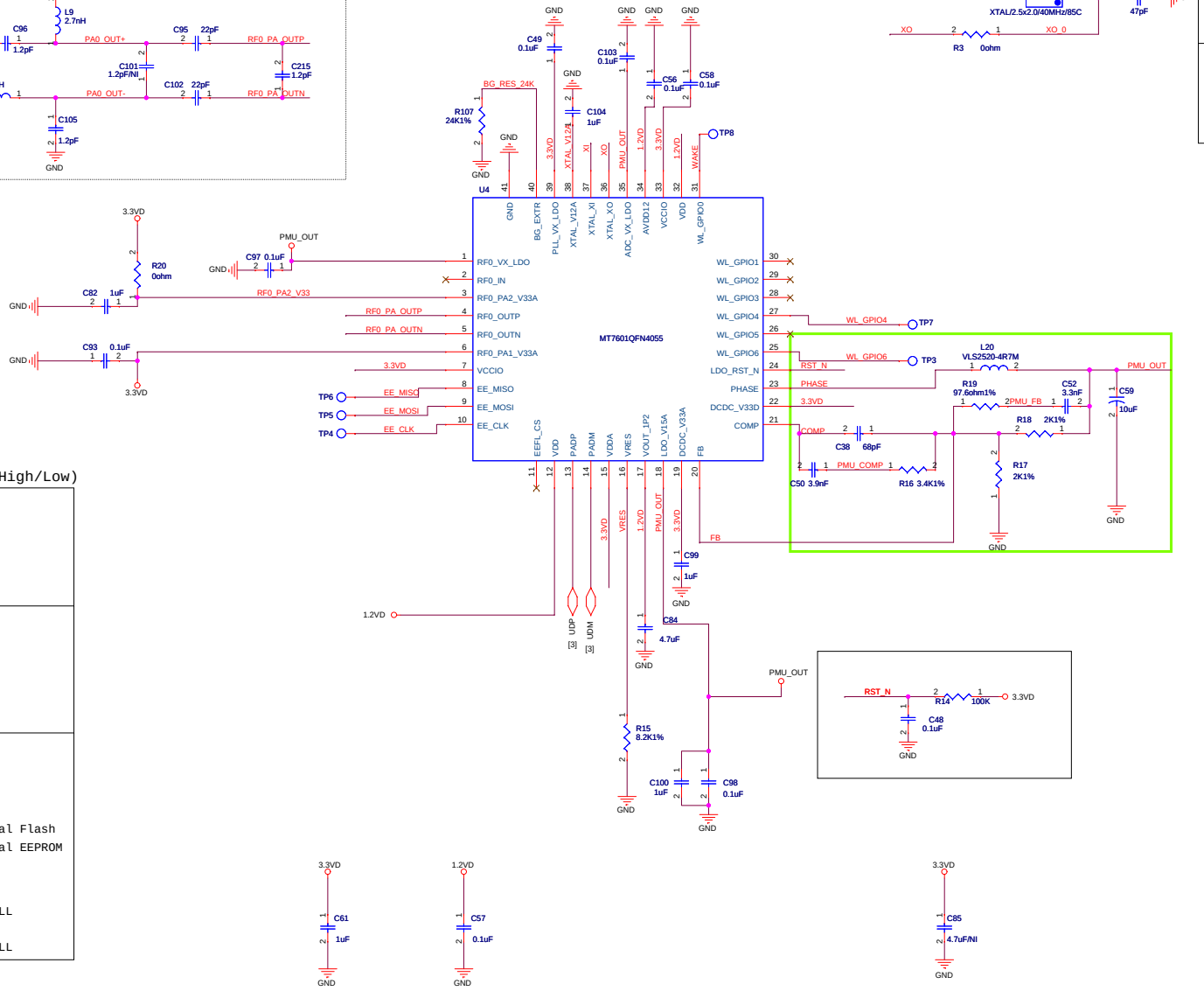
Trace width should greater than 70mil

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Saturday, October 27, 2012	Sheet 1 of 1	





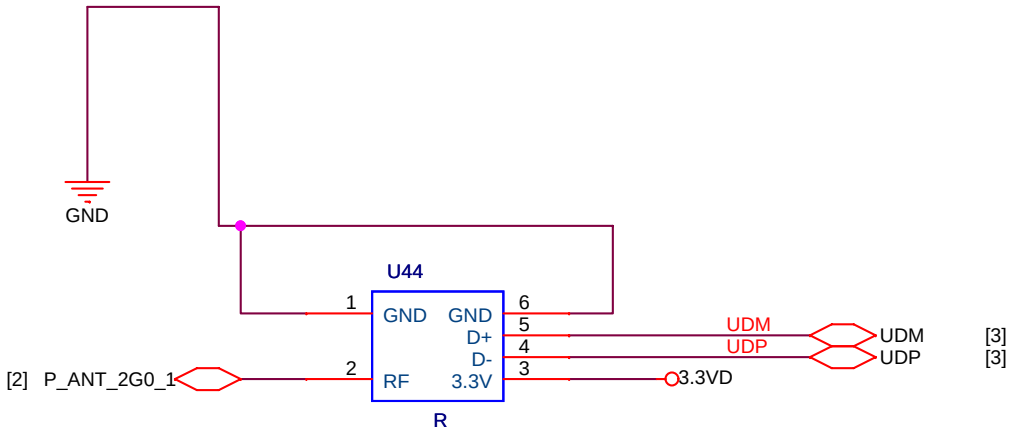
1. Using PMU and Translate 1.5V	
	PLL_LDO 3.3V Input
R8 0 ohm NI R7 0 ohm ON	LDO_V15A 1.5V Input
C38 30pF,C50 1.5nF R16 8.2K,R19 100 ohm C52 3.3nF,R18 2K L20 4.7uH, C59 10uF R17 2K	ON PMU 10uF Setting PMU_OUT = 1.5V



Boot Strapping (Internal Pull High/Low)

EE_MISO	0 : 40MHz Xtal 1 : 20MHz Xtal
WL_GPIO4	0 : E-fuse 1 : EEPROM
WL_GPIO6 EE_CLK EE_MOSI	PCI-E Mode 000:Normal Boot from RAM USB Mode 001:Normal Boot from ROM 010:Normal Boot from Serial Flash 011:Normal Boot from Serial EEPROM 100:SPI mode Boot from RAM 101: Scan mode + bypass PLL 110: Test mode 111: Test mode + bypass PLL

Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, October 27, 2012	Sheet 1 of 1	



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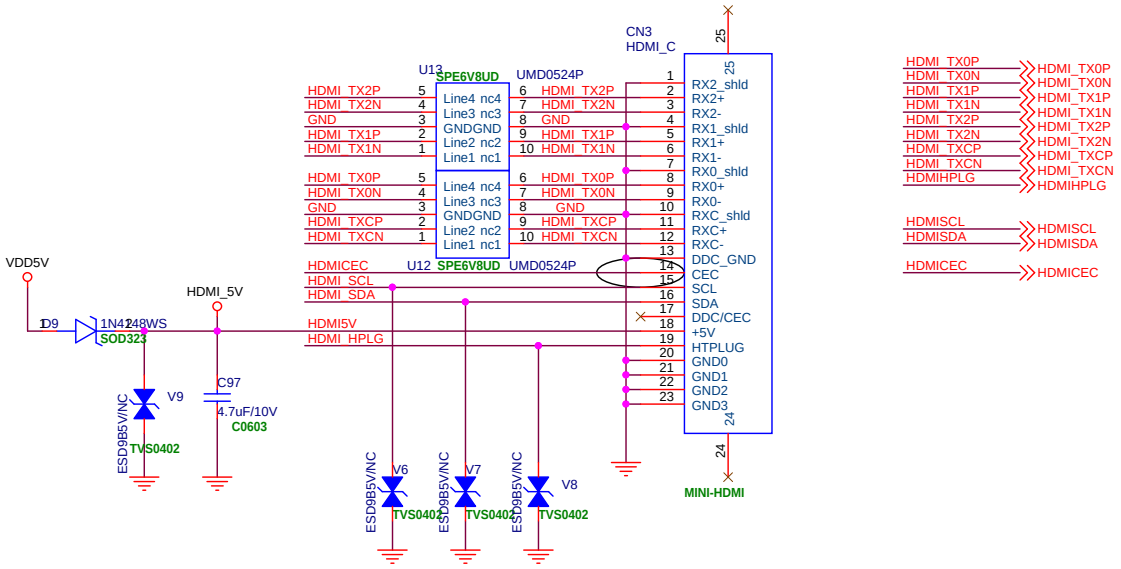
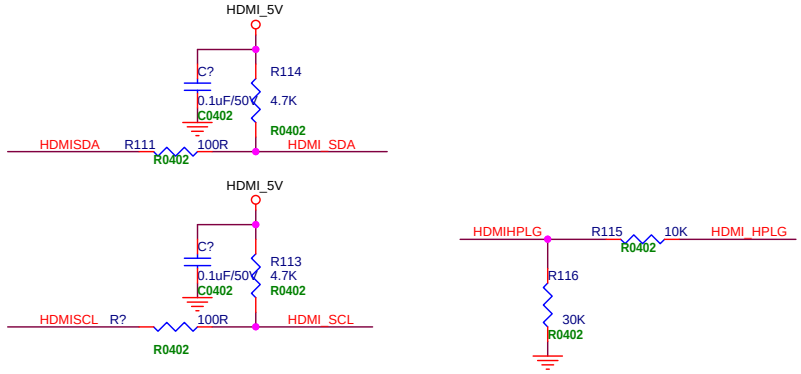
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, November 02, 2012	Sheet 1 of 1	

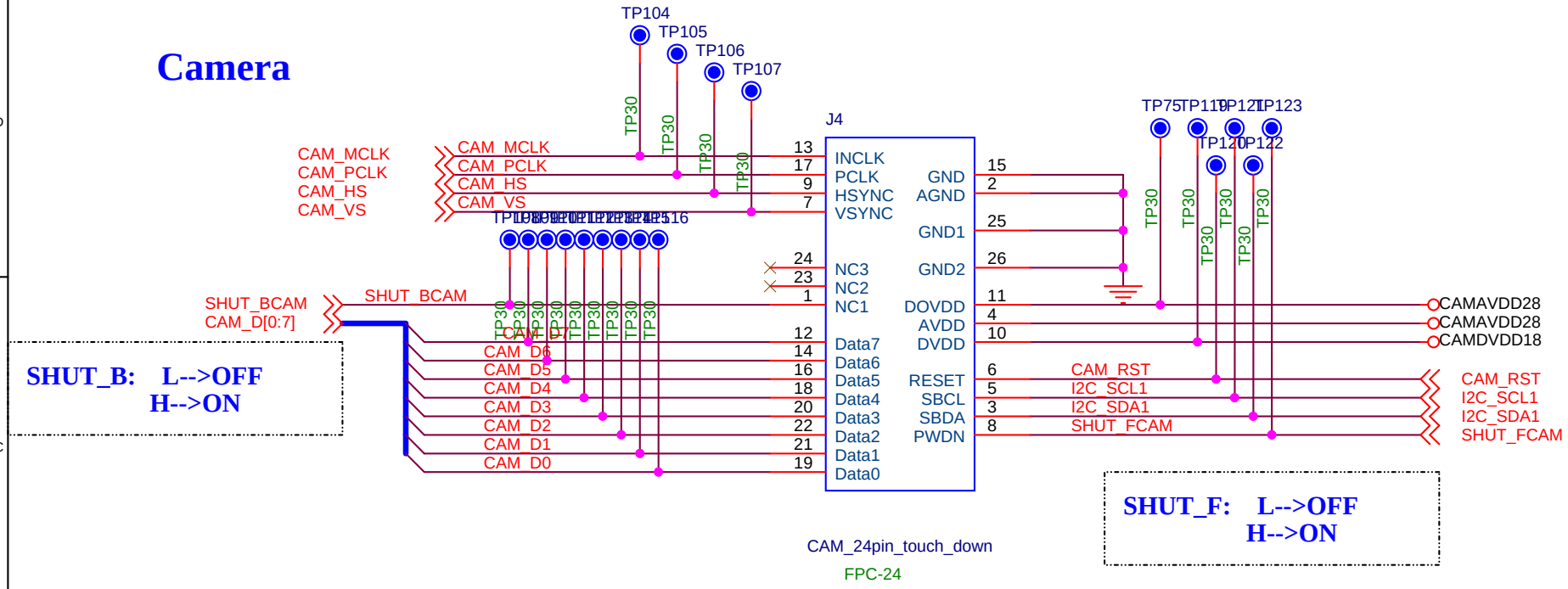
HDMI Connector



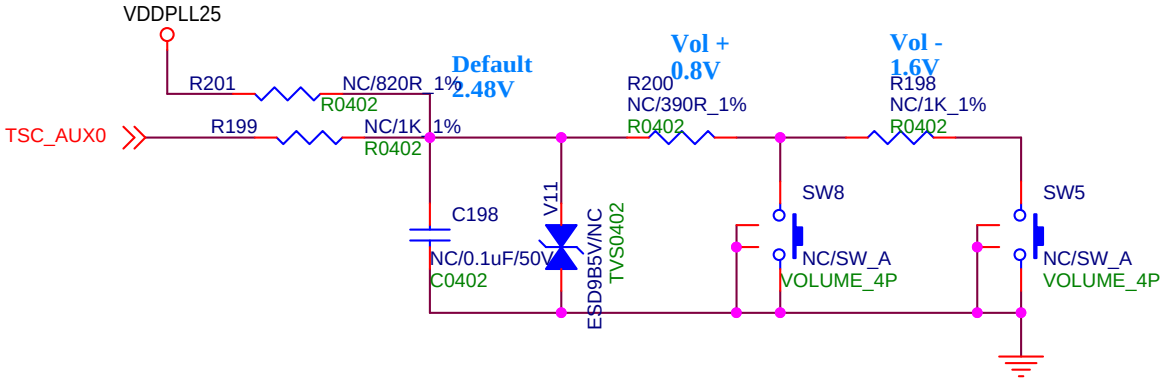
HDMI Level Shifter

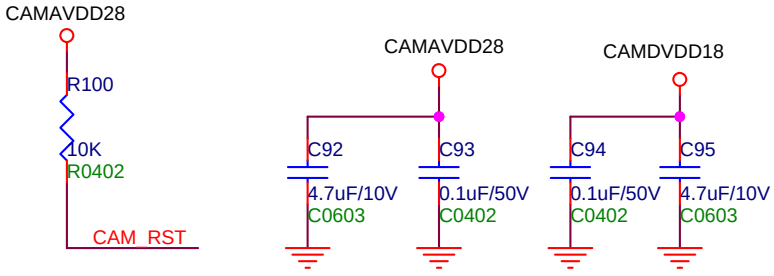


Camera

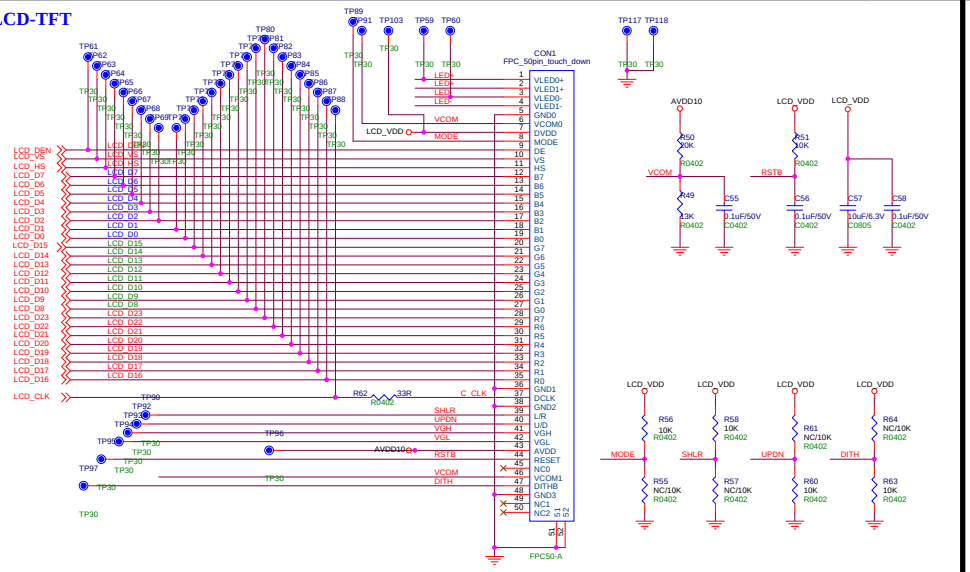


Function Keys

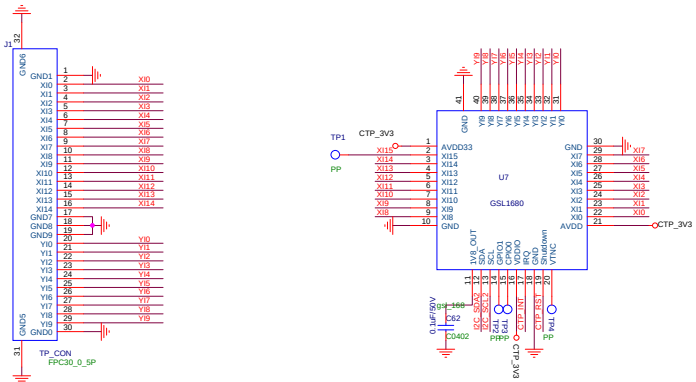


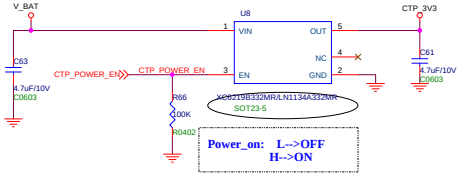


LCD-TFT

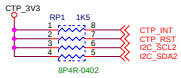


CTP

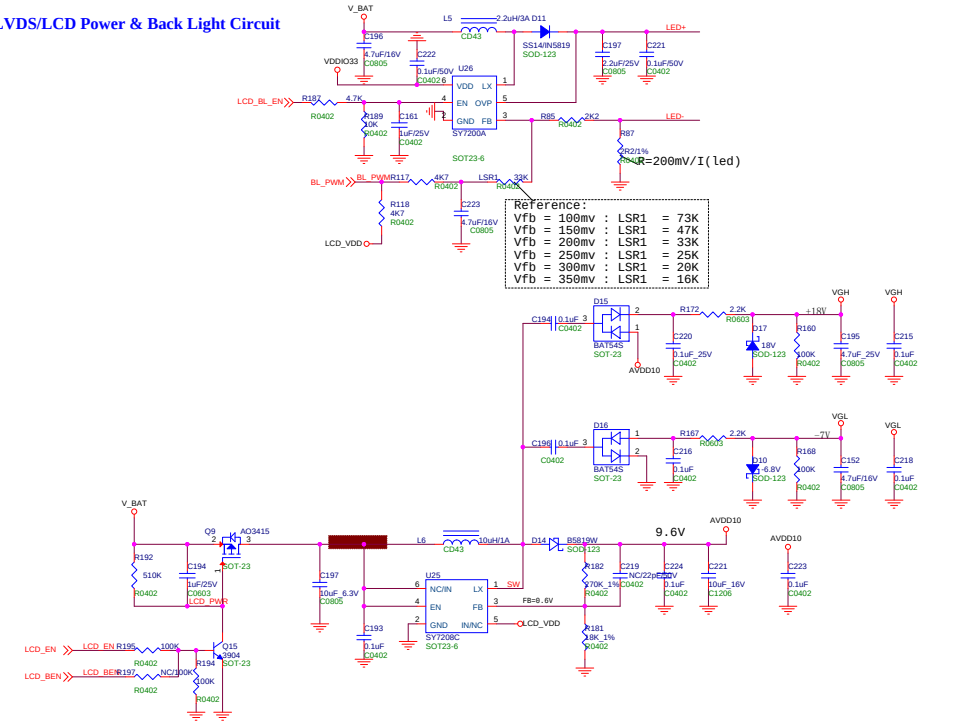




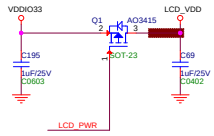
Pull High Circuit



LVDS/LCD Power & Back Light Circuit

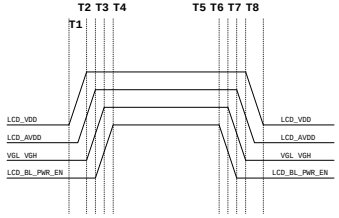


LCD Power



LCD_Power_EN: L-->ON
H-->OFF

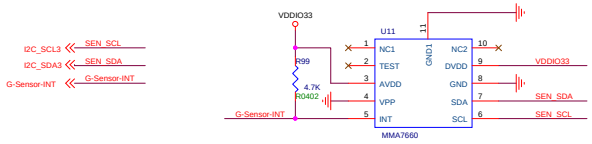
LCD Power on /off sequence



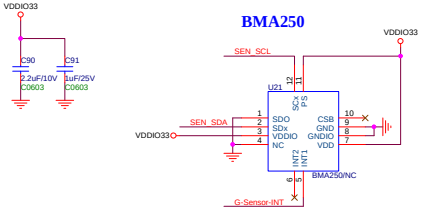
Item	Min	Typ	Max	Unit
T1	0	--	--	ms
T2	10	--	--	ms
T3	20	--	--	ms
T4	20	--	--	ms
T5	10	--	--	ms
T6	20	--	--	ms
T7	10	--	--	ms
T8	0	--	--	ms

G_sensor

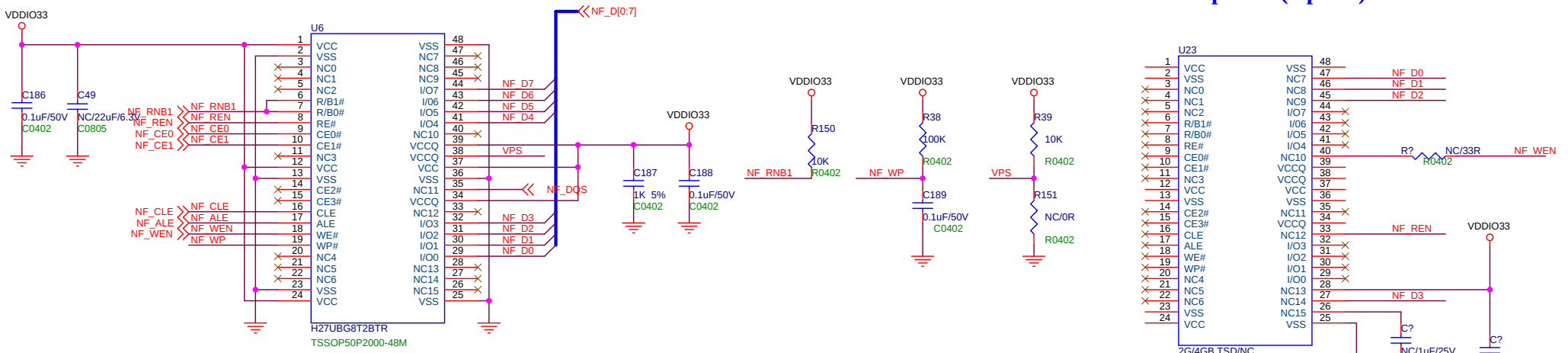
MMA7660



BMA250

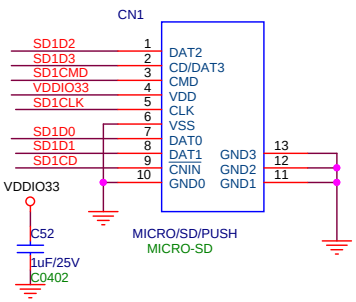


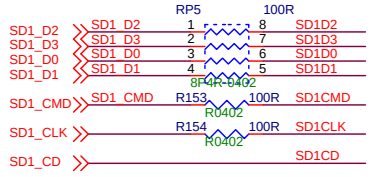
NAND Flash memory



TSD Component(Option)

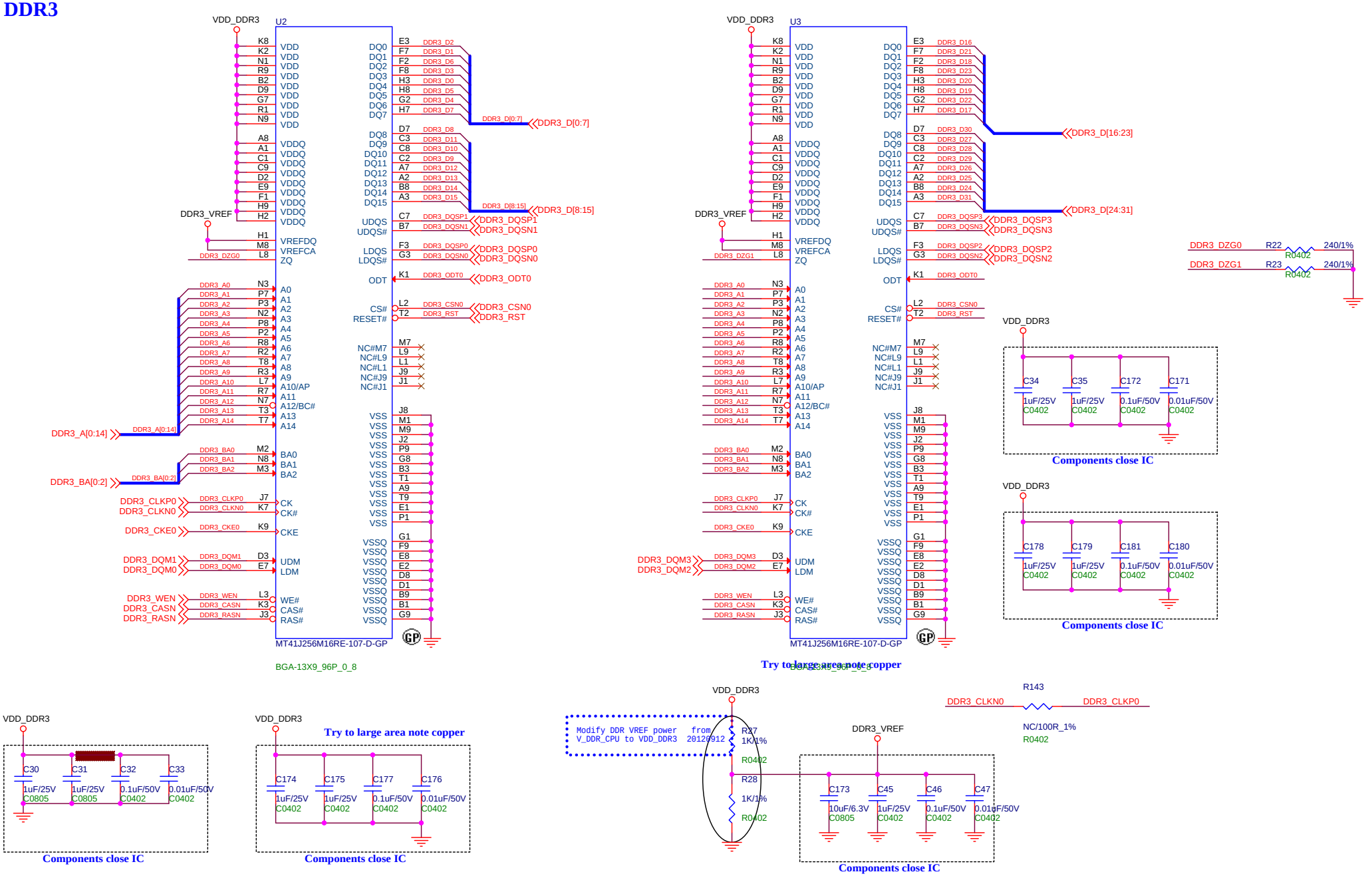
TF Card



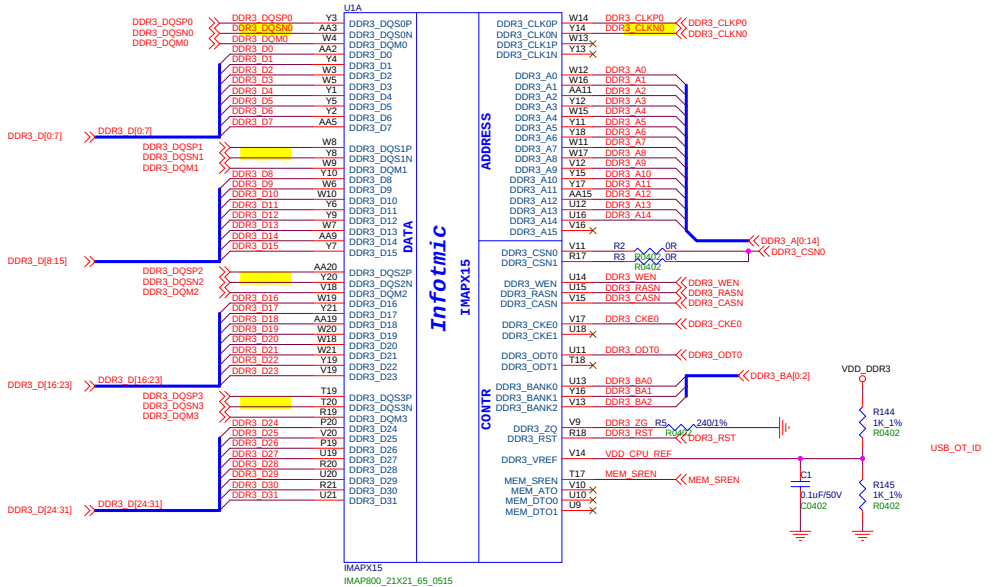


For SD Card interface, all signals should keep the equal trace length within 500mil.

DDR3

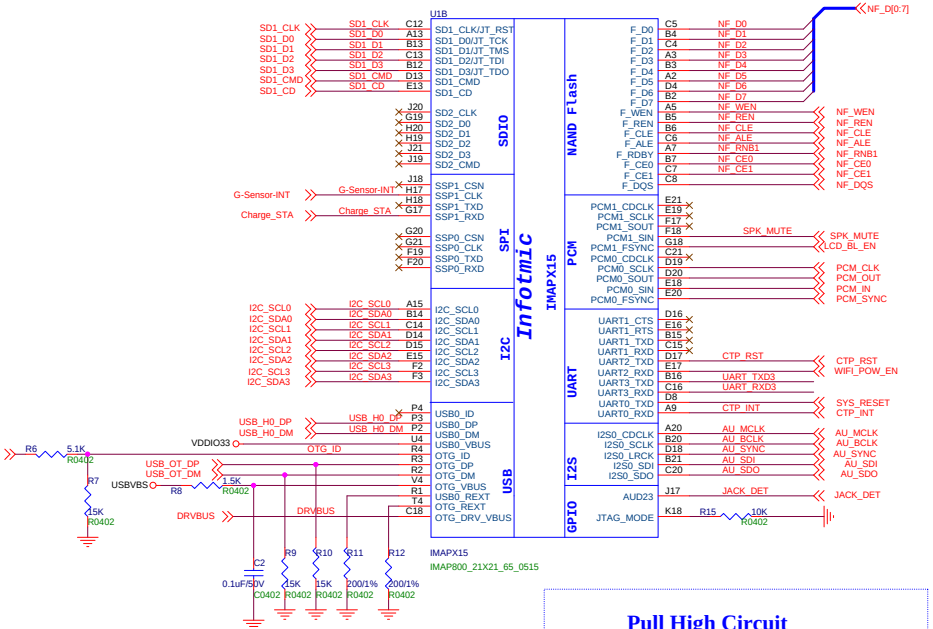

VDD_DDR3
U2
DDR3_VREF
DDR3_A[0:14]
DDR3_BA[0:2]
DDR3_CLKP0
DDR3_CLKN0
DDR3_CKE0
DDR3_DQM1
DDR3_DQM0
DDR3_WEN
DDR3_CASN
DDR3_RASN
DDR3_D[0:7]
DDR3_D[8:15]
DDR3_DQSP1
DDR3_DQSN1
DDR3_DQSP0
DDR3_DQSN0
DDR3_ODT0
DDR3_CSN0
DDR3_RST
MT41J256M16RE-107-D-GP
BGA-13X9_96P_0_8
U3
DDR3_D[16:23]
DDR3_D[24:31]
DDR3_DQSP3
DDR3_DQSN3
DDR3_DQSP2
DDR3_DQSN2
DDR3_DZG0
DDR3_DZG1
R22
R23
R0402
240/1%
Components close IC
C34
C35
C172
C171
C178
C179
C181
C180
1uF/25V
0.1uF/50V
0.01uF/50V
C0402
Try to large area note copper
C30
C31
C32
C33
C0805
C174
C175
C177
C176
Modify DDR VREF power from V_DDR_CPU to VDD_DDR3
20120912
R27
R28
1K/1%
R143
DDR3_CLKN0
DDR3_CLKP0
NC/100R_1%
C173
C45
C46
C47
10uF/6.3V

DDR3 Interface

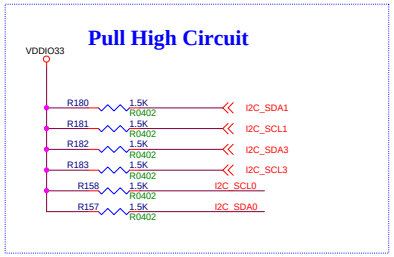


Difference line impedance for 100R

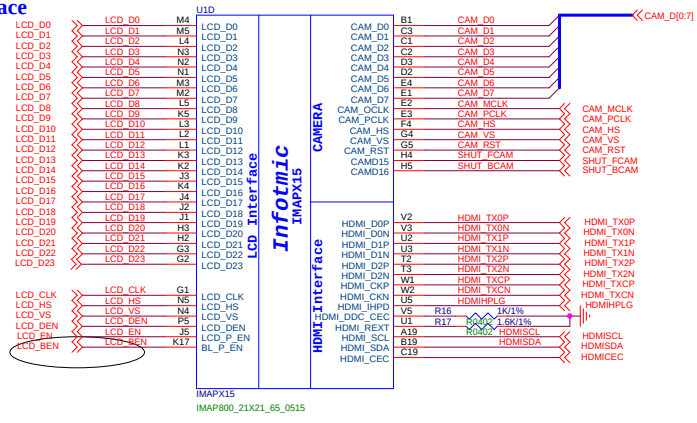
SDIO/UART/I2C/I2S/USB/SPI/NAND Interface



Pull High Circuit



LCD/HDMI/CAMERA Interface



Different LCD Display will have different application please Ref LCD signal connection

Processor	LCD Controller	Processor	LCD Controller	Processor	LCD Controller
LCD_0	blue data 0	LCD_8	Green data 0	LCD_16	Red data 0
LCD_1	blue data 1	LCD_9	Green data 1	LCD_17	Red data 1
LCD_2	blue data 2	LCD_10	Green data 2	LCD_18	Red data 2
LCD_3	blue data 3	LCD_11	Green data 3	LCD_19	Red data 3
LCD_4	blue data 4	LCD_12	Green data 4	LCD_20	Red data 4
LCD_5	blue data 5	LCD_13	Green data 5	LCD_21	Red data 5
LCD_6	blue data 6	LCD_14	Green data 6	LCD_22	Red data 6
LCD_7	blue data 7	LCD_15	Green data 7	LCD_23	Red data 7

DDR3 Memory Layout Rules

Address and Command Signals Routing Rules:

1.Trace Total length 2.5 to 4.5 inches
2.Trace width=5mils
3.Trace space=12 to 15mils
4.Impedance= target 50 Ohm
5.Trace space to other signal groups = 20 to 25 mils
6.length=±20 mils of Length Matching

Control Signals Routing Rules

1.Trace Total length 2.5 to 6.0 inches
2.Trace width=5mils
3.Trace space=12 to 15mils
4.Impedance= target 50 Ohm
5.Trace space to other signal groups = 20 to 25 mils
6.length=±20 mils of Length Matching

Data Group Signals Routing Rules:

1.Trace Total length 2.5 to 4.5 inches
2.Trace width=8mils
3.Trace space=12 mils minimum
4.Impedance= target 50 Ohm
5.Trace space to other signal groups = 12 mils
6.length=±20 mils of Length Matching

DQS Differential Strobe Signals Routing Rules:

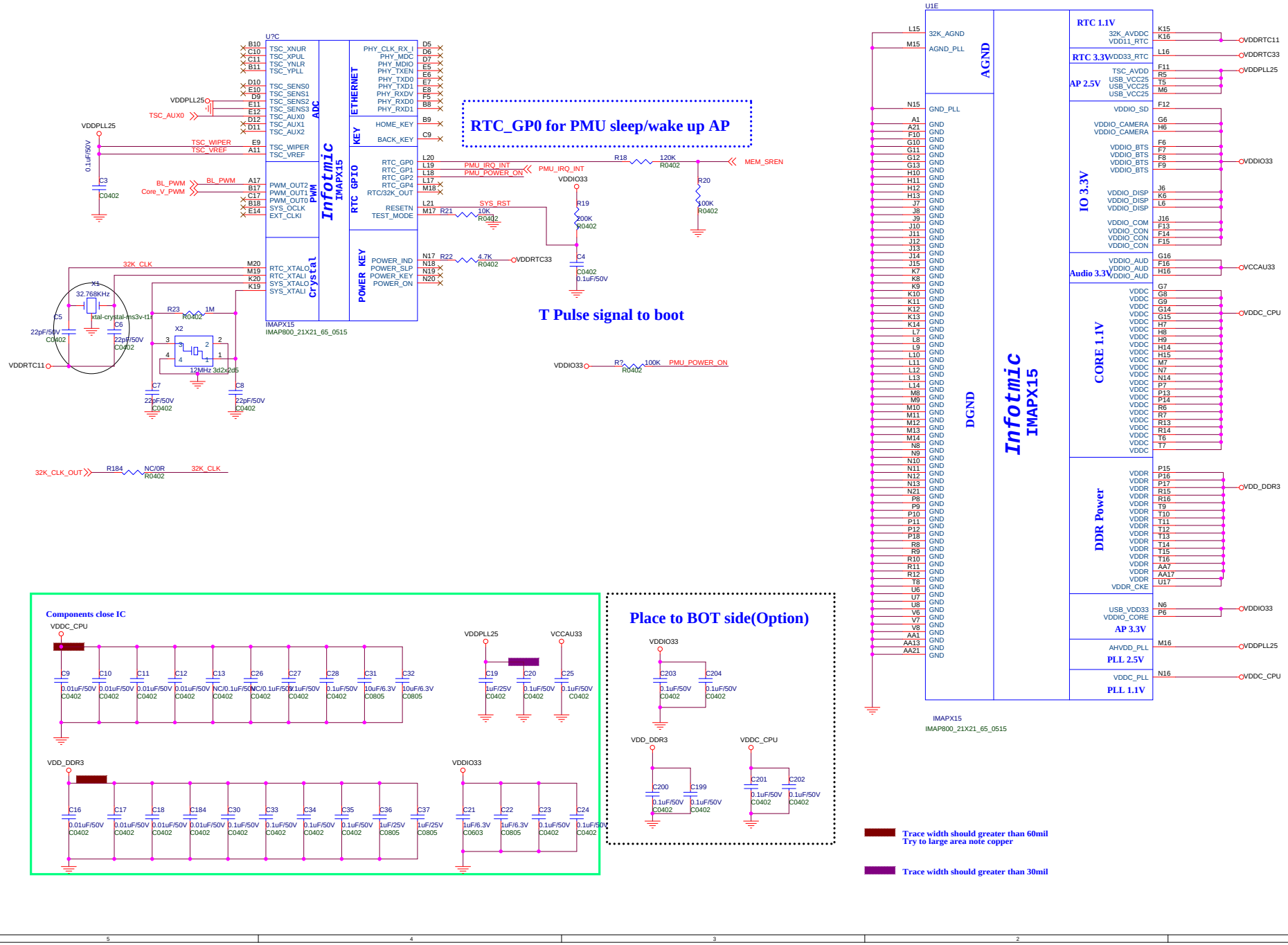
1.Trace Total length 2.5 to 4.5 inches
2.Trace width=8mils
3.Trace space=4 mils minimum
4.Impedance= target 100 Ohm
5.Trace space to other signal groups = 15 mils
6.length=±20 mils of Length Matching

Clock Signals Routing Rules:

1.Trace Total length 1.9 to 5.0 inches
2.Trace width=8mils
3.Trace space=5 mils
4.Impedance= target 100 Ohm
5.Trace space to other signal groups = 20 mils
6.length=±10 mils Length Matching

Note: More detailed description please reference DDR3 Layout Guide

Difference line impedance for 100R


U?C
Infotmic
IMAPX15
ADC
PWM
Crystal
ETHERNET
KEY
RTC GP1O
POWER KEY
TSC_XNUR
TSC_XPUL
TSC_YNLR
TSC_YPLL
TSC_SENS0
TSC_SENS1
TSC_SENS2
TSC_SENS3
TSC_AUX0
TSC_AUX1
TSC_AUX2
TSC_WIPER
TSC_VREF
PWM_OUT2
PWM_OUT1
PWM_OUT0
SYS_OCLK
EXT_CLKI
RTC_XTALO
RTC_XTALI
SYS_XTALO
SYS_XTALI
PHY_CLK_RX_I
PHY_MDC
PHY_MDIO
PHY_TXEN
PHY_TXD0
PHY_TXD1
PHY_RXDV
PHY_RXD0
PHY_RXD1
HOME_KEY
BACK_KEY
RTC_GP0
RTC_GP1
RTC_GP2
RTC_GP4
RTC/32K_OUT
RESETN
TEST_MODE
POWER_IND
POWER_SLP
POWER_KEY
POWER_ON
IMAPX15
IMAP800_21X21_65_0515
VDDPLL25
TSC_AUX0
TSC_WIPER
TSC_VREF
BL_PWM
Core_V_PWM
32K_CLK
VDDRTC11
32K_CLK_OUT
PMU_IRQ_INT
PMU_POWER_ON
SYS_RST
MEM_SREN
VDDIO33
VDDRTC33
RTC_GP0 for PMU sleep/wake up AP
T Pulse signal to boot
Components close IC
VDDC_CPU
VDD_DDR3
VCCAU33
Place to BOT side(Option)
U1E
AGND
DGND
GND
32K_AGND
AGND_PLL
GND_PLL
RTC 1.1V
RTC 3.3V
AP 2.5V
IO 3.3V
Audio 3.3V
CORE 1.1V
DDR Power
AP 3.3V
PLL 2.5V
PLL 1.1V
Trace width should greater than 60mil
Try to large area note copper
Trace width should greater than 30mil