AP6255

Data Sheet

Revision

Revision	Date	Description	Revised By
1.0	2015/04/09	- Preliminary	Gary
1.1	2015/04/26	- Add GPIO pin definition	Gary
1.2	2016/06/20	- Modify BT Specification	Richard
1.3	2016/08/30	- Modify Dimensions	Richard
1.4	2017/02/06	- Modify BT output power spec	Richard
1.5	2017/05/11	- Modify 5GHz channel list	Richard
1.6	2017/08/04	- Modify Recommended Reflow Profile	Richard
1.7	2017/08/14	- Modify WLAN Specification	Richard
1.8	2017/08/21	- Modify WLAN Specification	Ali
1.9	2017/11/23	- Modify WLAN RX Specification	Richard
2.0	2018/04/18	- Modify Security Items	Richard
2.1	2018/10/24	- Modify Operating temperature	Richard
2.2	2018/10/30	- Add PCM Timing	Eason
2.3	2018/12/17	- Modify Pin definition	Richard
2.4	2019/04/02	- Modify Pin definition	Richard
2.5	2019/04/30	- Modify BT digital modulator	Richard

Contents

1. Introduction

1.1 Overview

AP6255 is a fully Wi-Fi and Bluetooth functionalities module with seamless roaming capabilities and advance security, also it could interact with different vendors' 802.11a/b/g/n/ac 1x1 Access Points with SISO standard and can accomplish up to speed of 433.3Mbps with single stream in 802.11ac to connect the wireless LAN. Furthermore AP6255 included SDIO interface for Wi-Fi, UART/ PCM interface for Bluetooth.

In addition, this compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for tablet, OTT box and portable devices.

1.2 Product Features

- Lead Free design which is compliant with ROHS requirements.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Single-stream spatial multiplexing up to 433.3 Mbps data rate.
- 20, 40, 80 MHz channels with optional SGI (256 QAM modulation)
- Supports 1antenna with one for WLAN & Bluetooth shared port. Also, shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.
    - Supports standard SDIO v3.0, compatible with SDIO v2.0 HOST interfaces.

- BT host digital interface:
    - HCI UART (up to 4 Mbps)
    - PCM for audio data
- Complies with Bluetooth Core Specification Version 4.2 with provisions for supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.

A simplified block diagram of the module is depicted in the figure above.

2. General Specification

2.1 General Specification

Model Name	AP6255
Product Description	1Tx/1Rx 802.11 ac/a/b/g/n Wi-Fi + BT 4.2 Module
Dimension	L x W: 12 x 12(Typ.)mm、H : 1.65 (Max.) mm
WiFi Interface	SDIO V3.0/ 2.0
BT Interface	UART / PCM
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 125°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -20 °C to +75 °C and 3.2V < VBAT < 3.8V without derating performance.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	5	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.9	V

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage.

Symbol	Condition	Minimum ESD Rating	Unit
ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	1	kV
ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	250	V

2.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.2	3.3	4.8	V
VDDIO	1.6	1.8 / 3.3	3.8	V

VBAT current consumption 1A (Peak), when VBAT = 3.3V

The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	Min.	Max.	Unit
VIL/VIH	0.35×VDDIO	0.65×VDDIO	V
VOL/VOH output@2mA	0.4	VDDIO-0.4	V
For VDDIO=3.3V	**Min.**	**Max.**	**Unit**
VIL/VIH	0.80	2	V
VOL/VOH output@2mA	0.4	VDDIO-0.4	V

3. Wi-Fi RF Specification

3.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

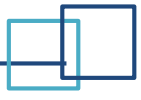
Feature	Description
WLAN Standard	IEEE 802.11b/g/n/ac, WiFi compliant
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)
Number of Channels	2.4GHz：Ch1 ~ Ch13
Modulation	802.11b : DQPSK, DBPSK, CCK 802.11g/n : 64-QAM,16-QAM, QPSK, BPSK
Output Power	802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM ≤ -9dB 802.11b /1Mbps : 18 dBm ± 1.5 dB @ EVM ≤ -9dB
	802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB 802.11g /6Mbps : 17 dBm ± 1.5 dB @ EVM ≤ -5dB
	802.11n@20MHz /MCS7 : 14 dBm ± 1.5 dB @ EVM ≤ -27dB 802.11n@20MHz /MCS0 : 16 dBm ± 1.5 dB @ EVM ≤ -5dB
Receive Sensitivity (11b) @8% PER	- 1Mbps PER @ -96 dBm, +/- 2dB
	- 2Mbps PER @ -90 dBm, +/- 2dB
	- 5.5Mbps PER @ -88 dBm, +/- 2dB
	- 11Mbps PER @ -87 dBm, +/- 2dB
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -90 dBm, +/- 2dB
	- 9Mbps PER @ -88 dBm, +/- 2dB
	- 12Mbps PER @ -87 dBm, +/- 2dB
	- 18Mbps PER @ -85 dBm, +/- 2dB
	- 24Mbps PER @ -83 dBm, +/- 2dB
	- 36Mbps PER @ -80 dBm, +/- 2dB
	- 48Mbps PER @ -76 dBm, +/- 2dB
	- 54Mbps PER @ -74 dBm, +/- 2dB
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -89 dBm, +/- 2dB
	- MCS=1 PER @ -85 dBm, +/- 2dB
	- MCS=2 PER @ -84 dBm, +/- 2dB
	- MCS=3 PER @ -80 dBm, +/- 2dB
	- MCS=4 PER @ -77 dBm, +/- 2dB
	- MCS=5 PER @ -75 dBm, +/- 2dB

	- MCS=6 PER @ -72 dBm, +/- 2dB
	- MCS=7 PER @ -71 dBm, +/- 2dB
Maximum Input Level	802.11b : -10dBm
	802.11g/n : -20dBm
Antenna Reference	Small antennas with 0~2 dBi peak gain

3.2 5GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature	Description
WLAN Standard	IEEE 802.11a/b/g/n/ac, Wi-Fi compliant
Frequency Range	5.18 GHz ~ 5.845 GHz (5.0 GHz ISM Band)
Number of Channels	5.0GHz：Please see the table[1]
Modulation	802.11a/n : 64-QAM,16-QAM, QPSK, BPSK 802.11ac : 256-QAM, 64-QAM,16-QAM, QPSK, BPSK
Output Power	802.11a /54Mbps : 14 dBm ± 1.5 dB @ EVM ≤ -25dB 802.11a /6Mbps : 14 dBm ± 1.5 dB @ EVM ≤ -5dB
	802.11n /MCS7 : 13 dBm ± 1.5 dB @ EVM ≤ -27dB 802.11n /MCS0 : 14 dBm ± 1.5 dB @ EVM ≤ -5dB
	802.11ac/MCS8 : 12 dBm ± 1.5 dB @ EVM ≤ -30dB 802.11ac/MCS0 : 14 dBm ± 1.5 dB @ EVM ≤ -5dB
	802.11ac/MCS9 : 10 dBm ± 1.5 dB @ EVM ≤ -32dB 802.11ac/MCS0 : 12 dBm ± 1.5 dB @ EVM ≤ -5dB
Receive Sensitivity (11a, 20MHz) @10% PER	- 6Mbps PER @ -91 dBm, +/- 2dB
	- 9Mbps PER @ -89 dBm, +/- 2dB
	- 12Mbps PER @ -88 dBm, +/- 2dB
	- 18Mbps PER @ -86 dBm, +/- 2dB
	- 24Mbps PER @ -82 dBm, +/- 2dB
	- 36Mbps PER @ -79 dBm, +/- 2dB
	- 48Mbps PER @ -74 dBm, +/- 2dB
	- 54Mbps PER @ -73 dBm, +/- 2dB
(11n,20MHz) @10% PERReceive Sensitivity	- MCS=0 PER @ -90 dBm, +/- 2dB
	- MCS=1 PER @ -88 dBm, +/- 2dB
	- MCS=2 PER @ -85 dBm, +/- 2dB
	- MCS=3 PER @ -82 dBm, +/- 2dB
	- MCS=4 PER @ -78 dBm, +/- 2dB
	- MCS=5 PER @ -74 dBm, +/- 2dB
	- MCS=6 PER @ -72 dBm, +/- 2dB
	- MCS=7 PER @ -71 dBm, +/- 2dB
(11n,40MHz) @10% PERReceive Sensitivity	- MCS=0 PER @ -88 dBm, +/- 2dB
	- MCS=1 PER @ -85 dBm, +/- 2dB
	- MCS=2 PER @ -83 dBm, +/- 2dB



	- MCS=3 PER @ -79 dBm, +/- 2dB
	- MCS=4 PER @ -76 dBm, +/- 2dB
	- MCS=5 PER @ -71 dBm, +/- 2dB
	- MCS=6 PER @ -70 dBm, +/- 2dB
	- MCS=7 PER @ -68 dBm, +/- 2dB
Receive Sensitivity (11ac,20MHz) @10% PER	- MCS=0 PER @ -89 dBm, +/- 2dB
	- MCS=1 PER @ -87 dBm, +/- 2dB
	- MCS=2 PER @ -84 dBm, +/- 2dB
	- MCS=3 PER @ -81 dBm, +/- 2dB
	- MCS=4 PER @ -77 dBm, +/- 2dB
	- MCS=5 PER @ -73 dBm, +/- 2dB
	- MCS=6 PER @ -71 dBm, +/- 2dB
	- MCS=7 PER @ -70 dBm, +/- 2dB
	- MCS=8 PER @ -66 dBm, +/- 2dB
Receive Sensitivity (11ac,40MHz) @10% PER	- MCS=0 PER @ -87 dBm, +/- 2dB
	- MCS=1 PER @ -83 dBm, +/- 2dB
	- MCS=2 PER @ -81 dBm, +/- 2dB
	- MCS=3 PER @ -78 dBm, +/- 2dB
	- MCS=4 PER @ -75 dBm, +/- 2dB
	- MCS=5 PER @ -70 dBm, +/- 2dB
	- MCS=6 PER @ -68 dBm, +/- 2dB
	- MCS=7 PER @ -66 dBm, +/- 2dB
	- MCS=8 PER @ -64 dBm, +/- 2dB
	- MCS=9 PER @ -63 dBm, +/- 2dB
Receive Sensitivity (11ac,80MHz) @10% PER	- MCS=0 PER @ -83 dBm, +/- 2dB
	- MCS=1 PER @ -80 dBm, +/- 2dB
	- MCS=2 PER @ -78 dBm, +/- 2dB
	- MCS=3 PER @ -74 dBm, +/- 2dB
	- MCS=4 PER @ -71 dBm, +/- 2dB
	- MCS=5 PER @ -69 dBm, +/- 2dB
	- MCS=6 PER @ -65 dBm, +/- 2dB
	- MCS=7 PER @ -63 dBm, +/- 2dB
	- MCS=8 PER @ -60 dBm, +/- 2dB
	- MCS=9 PER @ -59 dBm, +/- 2dB
Maximum Input Level	802.11a/n : -20dBm

	802.11ac : -30dBm
Antenna Reference	Small antennas with 0~2 dBi peak gain

4. Bluetooth Specification

4.1 Bluetooth Specificatio

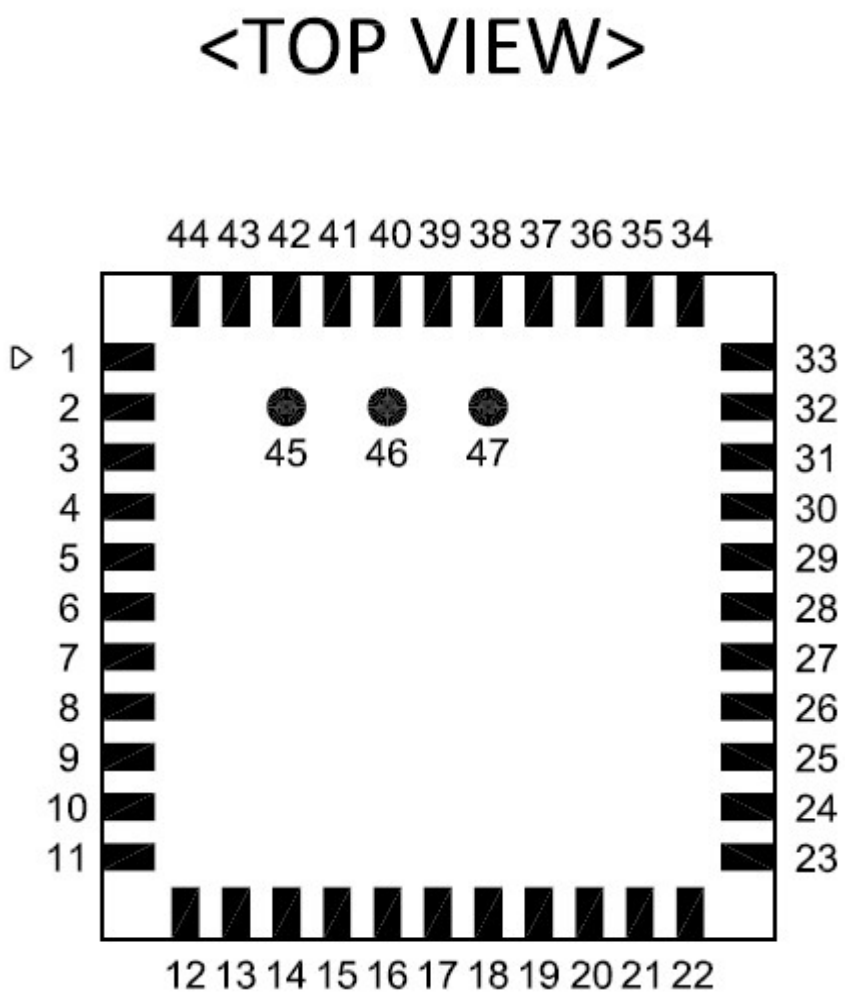
4.2 Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature	**Description**		
General Specification			
Bluetooth Standard	Bluetooth V4.2 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	GFSK, π/4-DQPSK, 8-DPSK		
RF Specification			
	Min.	**Typical.**	**Max.**
Output Power[1]		7	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for 8-DPSK (3Mbps)		-80 dBm	
Maximum Input Level	GFSK (1Mbps) :-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8-DPSK (3Mbps) :-20dBm		

Note*：The Bluetooth output power is able to be configured by firmware (hcd file).

5. Pin Definition

5.1 Pin Outline



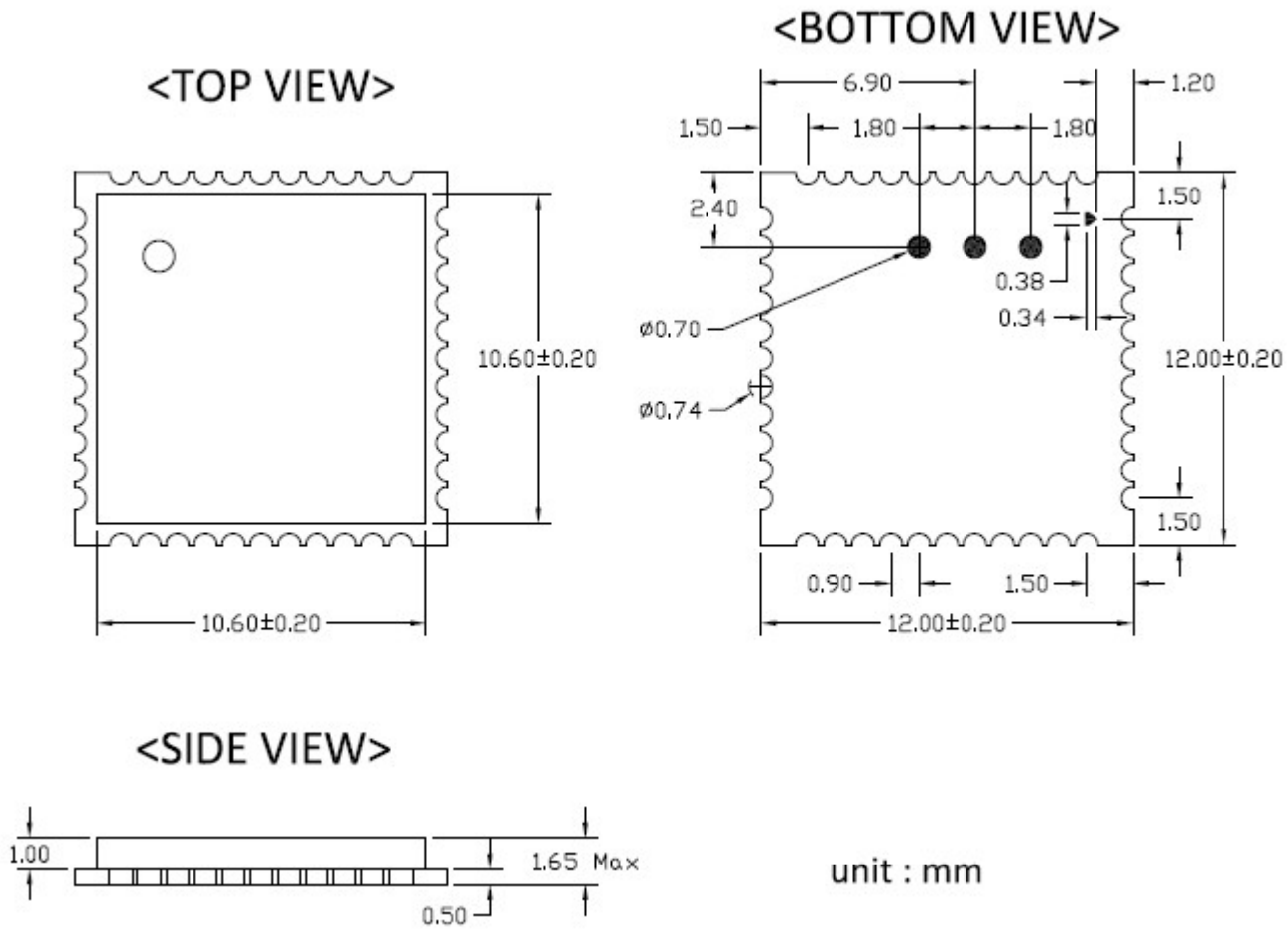
5.2 Pin Assignment

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	NC	—	Floating (Don't connected to ground)
5	NC	—	Floating (Don't connected to ground)
6	BT_WAKE	I	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
8	NC	—	Floating (Don't connected to ground)
9	VBAT	P	Main power voltage source input
10	XTAL_IN	I	Crystal input
11	XTAL_OUT	O	Crystal output
12	WL_REG_ON	I	Power up/down internal regulators used by WiFi section
13	WL_HOST_WAKE	O	WLAN to wake-up HOST
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line 3
16	SDIO_DATA_CMD	I/O	SDIO command line
17	SDIO_DATA_CLK	I/O	SDIO clock line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	VIN_LDO_OUT	P	Internal Buck voltage generation pin
22	VDDIO	P	I/O Voltage supply input
23	VIN_LDO	P	Internal Buck voltage generation pin
24	LPO	I	External Low Power Clock input (32.768KHz)
25	PCM_OUT	O	PCM Data output
26	PCM_CLK	I/O	PCM clock
27	PCM_IN	I	PCM data input
28	PCM_SYNC	I/O	PCM sync signal
29	SDIO_VSEL	I	SDIO mode selection pin 1：When VDDIO = 1.8V , 0：When VDDIO = 3.3V
30	NC	—	Floating (Don't connected to ground)
31	GND	—	Ground connections

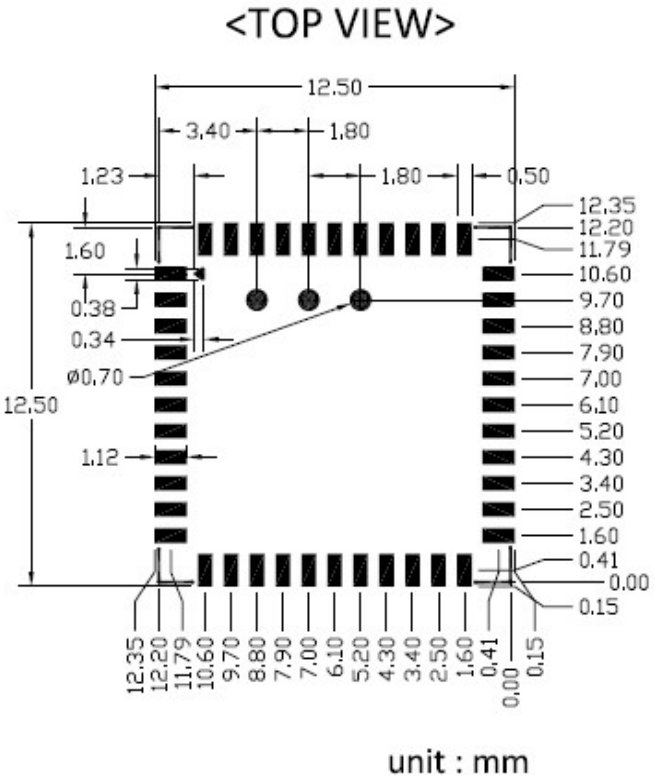
32	NC	—	Floating (Don't connected to ground)
33	GND	—	Ground connections
34	BT_REG_ON	I	Power up/down internal regulators used by BT section
35	NC	—	Floating (Don't connected to ground)
36	GND	—	Ground connections
37	GPIO_6	I/O	GPIO configuration pin
38	GPIO_3	I/O	GPIO configuration pin
39	GPIO_5	I/O	GPIO configuration pin
40	GPIO_2	I/O	GPIO configuration pin
41	UART_RTS_N	O	Bluetooth UART interface
42	UART_TXD	O	Bluetooth UART interface
43	UART_RXD	I	Bluetooth UART interface
44	UART_CTS_N	I	Bluetooth UART interface
45	TP1(NC)	—	Floating (Don't connected to ground)
46	TP2(NC)	—	Floating (Don't connected to ground)
47	TP3(NC)	—	Floating (Don't connected to ground)

6. Dimensions

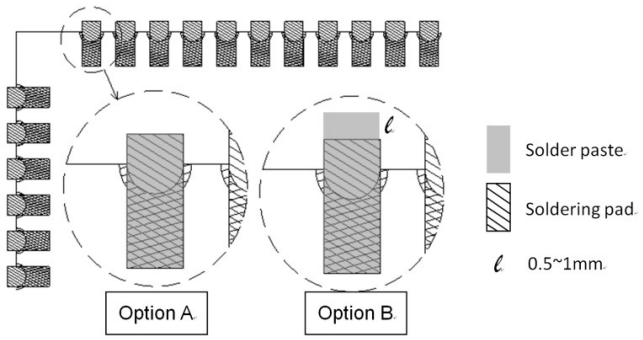
6.1 Module Dimensions



6.2 Recommended Footprint



- Solder paste layer design is generally the same as recommended footprint.
  (錫膏層設計通常建議和焊墊尺寸相同)
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial.
  In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner.
  (如果模組吃錫品質考量側面爬錫，如何優化鋼網開孔設計以調整適當的錫膏量是非常重要的。尤其鋼網的厚度大約是 0.1mm 或更薄時，可考慮局部加厚鋼網的設計。).



7. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7Vio - Vio	V

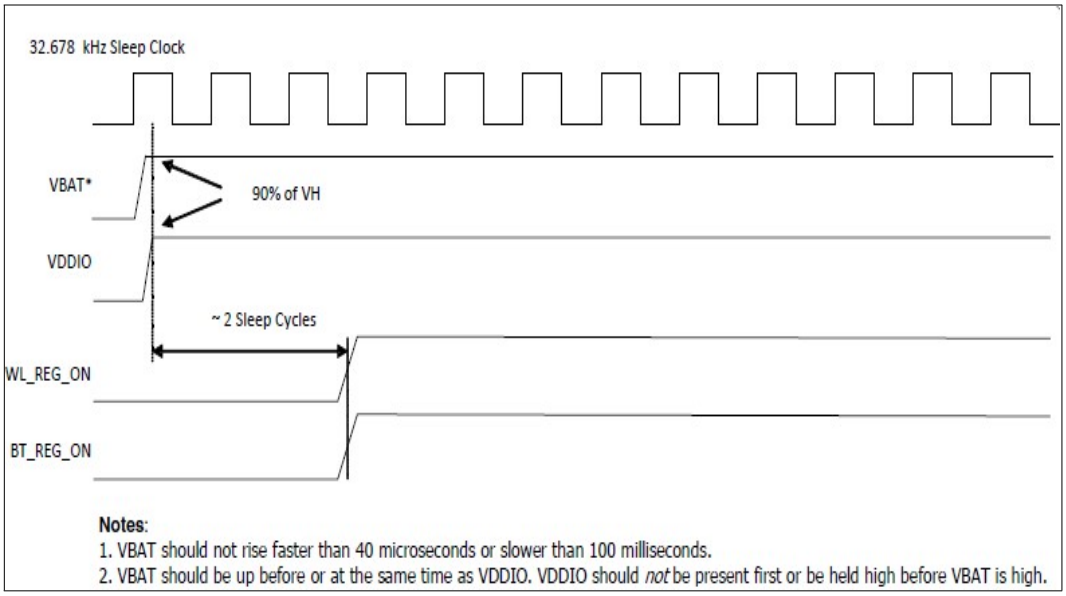
Input signal amplitude follow VDDIO (1.8V or 3.3V)

8. Host Interface Timing Diagram

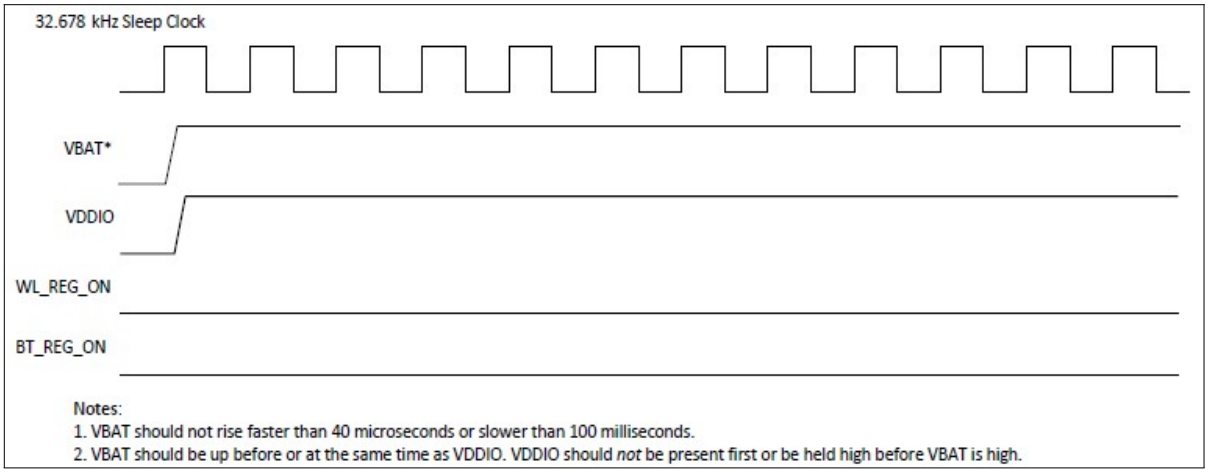
8.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.
Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

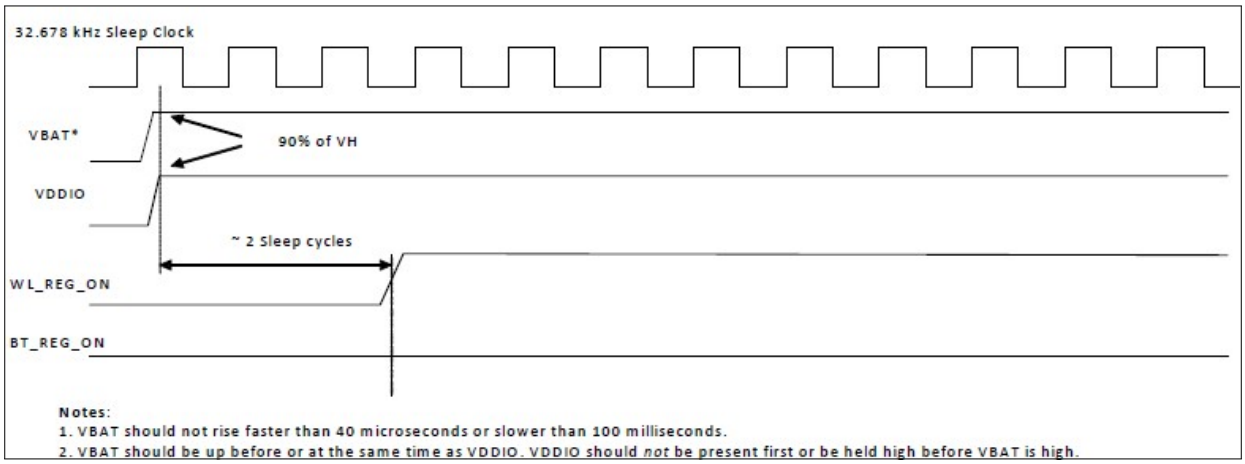
- WL_REG_ON: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- BT_REG_ON: Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



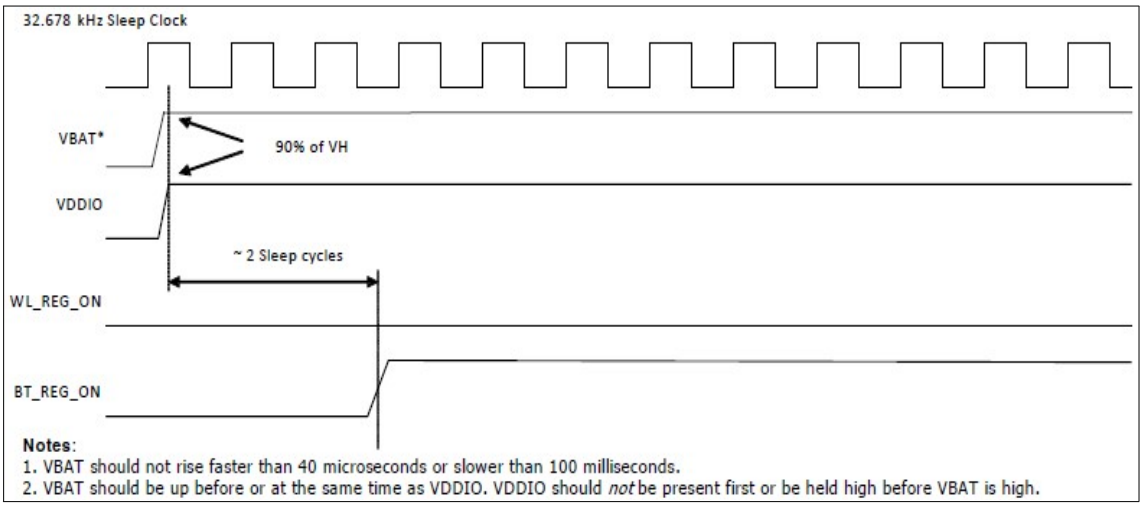
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF



WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

8.2 SDIO Interface Description

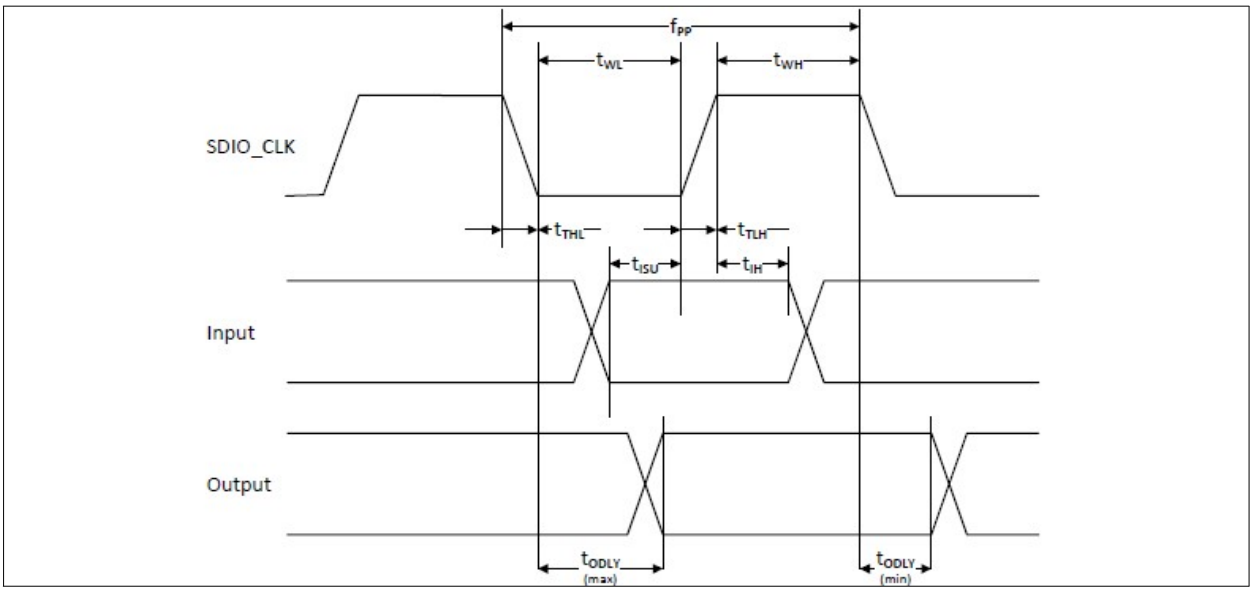
The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50(100 Mbps),SDR104(208MHz) and DDR50(50MHz, dual rates) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- Function 0 Standard SDIO function (Max Block Size / Byte Count = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max Block Size / Byte Count = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max Block Size/Byte Count=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

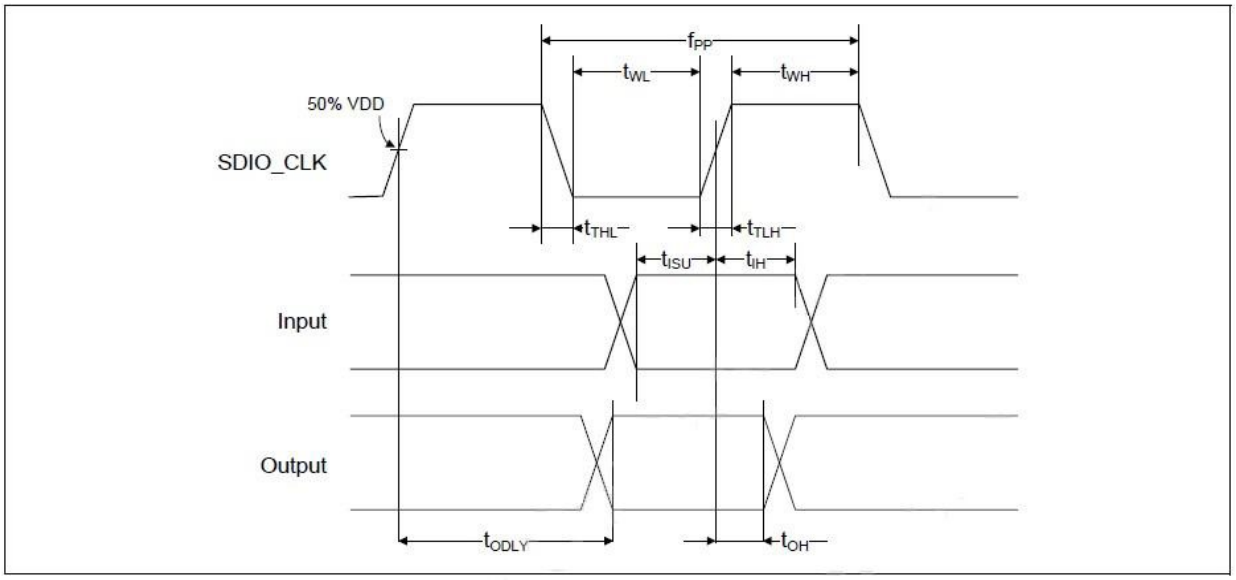
SDIO Default Mode Timing Diagram



Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

SDIO High Speed Mode Timing Diagram

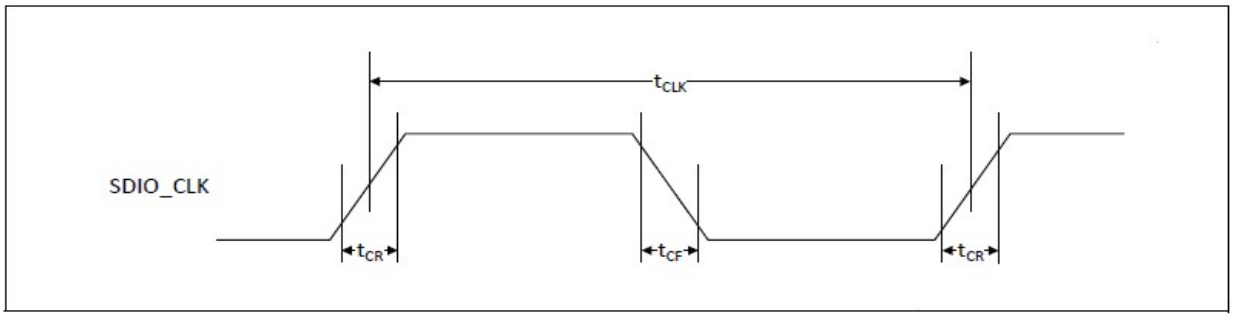


Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40 pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

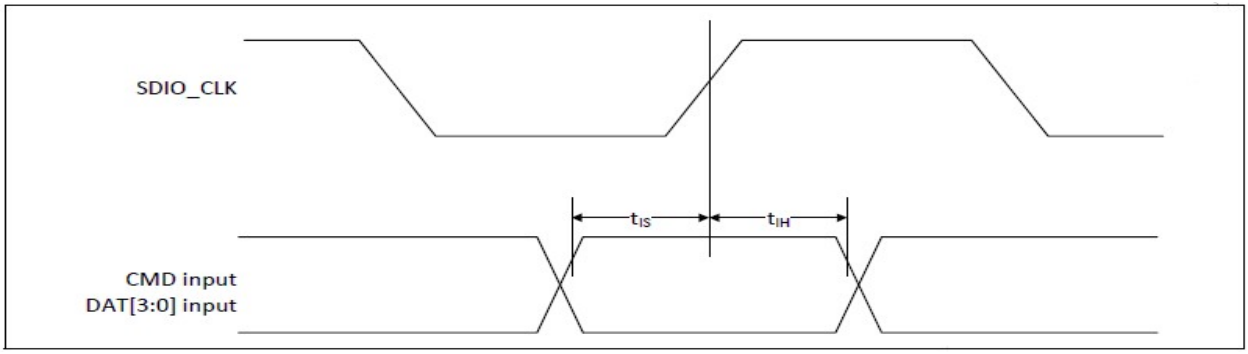
SDIO Bus Timing Specifications in SDR Modes

Clock timing (SDR Modes)



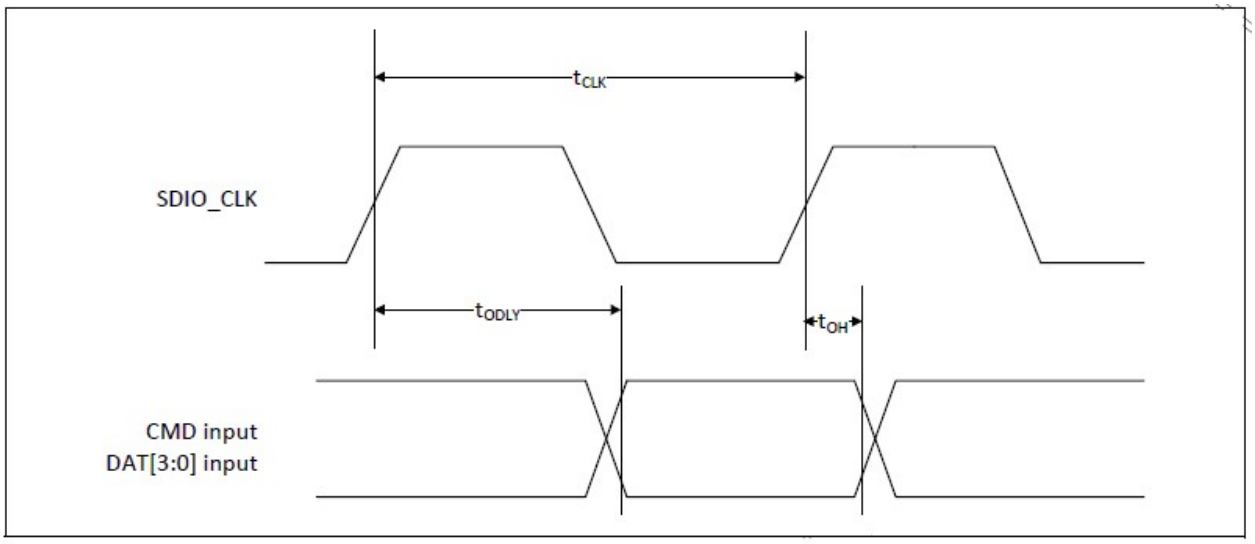
Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @208 MHz, C_{CARD} = 10 pF
Clock duty	–	30	70	%	–

SDIO Bus Input timing (SDR Modes)



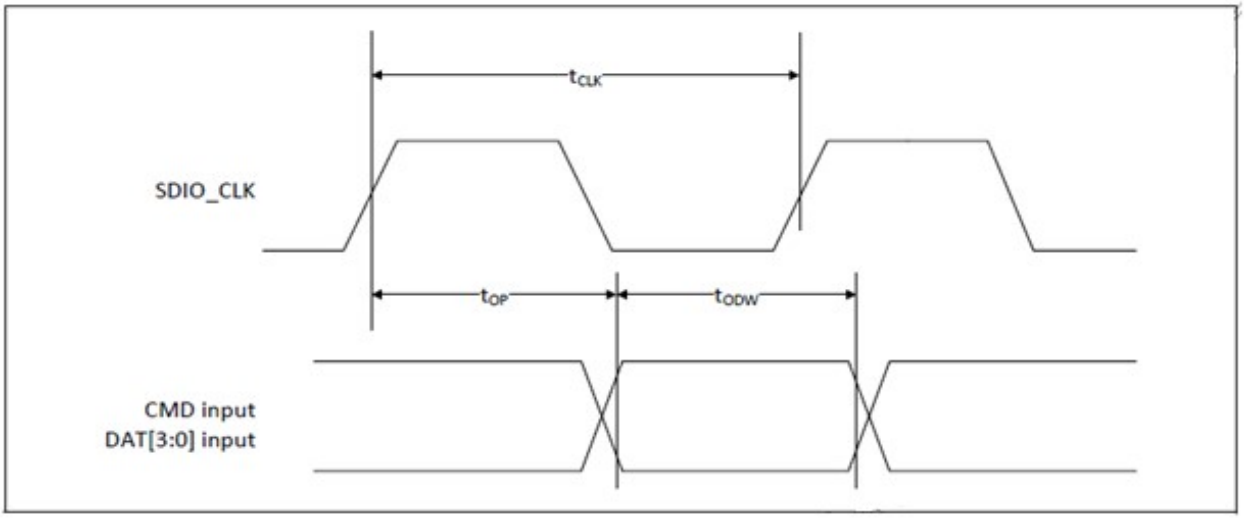
Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

SDIO Bus output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	t_{CLK} ≥ 10 ns C_L = 30 pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	t_{CLK} ≥ 20 ns C_L = 40 pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) C_L = 15 pF

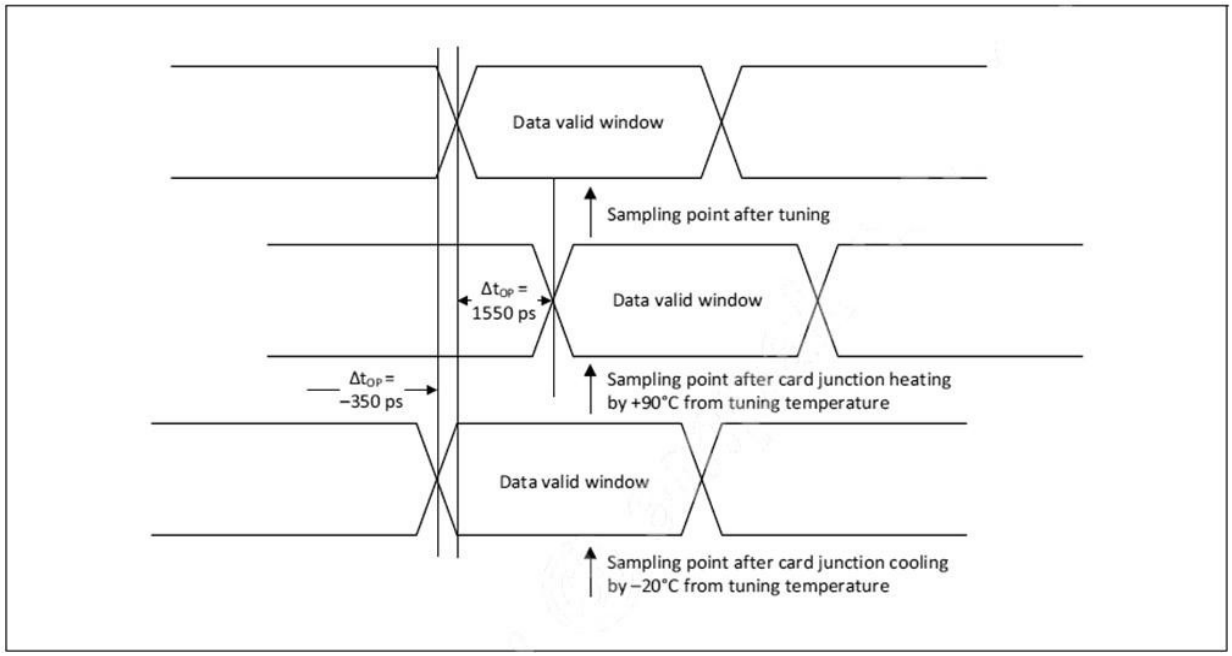
Card output timing (SDR Modes 100MHz to 208MHz)



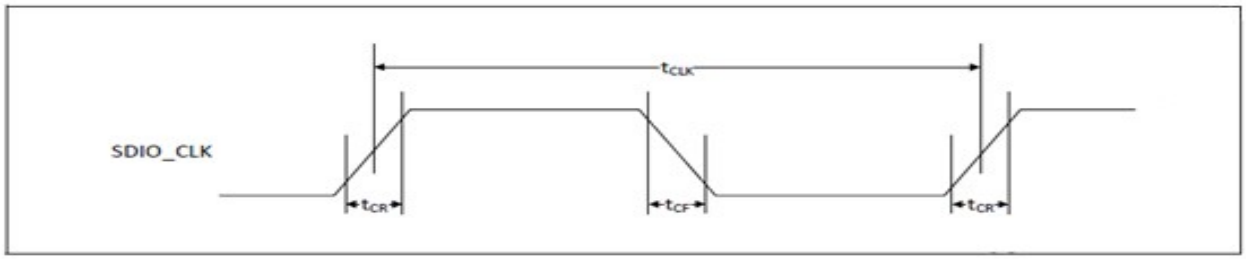
Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	–350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	t_{ODW}=2.88 ns @208 MHz

- Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation
- Δt_{OP} = –350 ps for junction temperature of Δt_{OP} = –20 degrees during operation
- Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = –20 to +125 degrees during operation

Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)

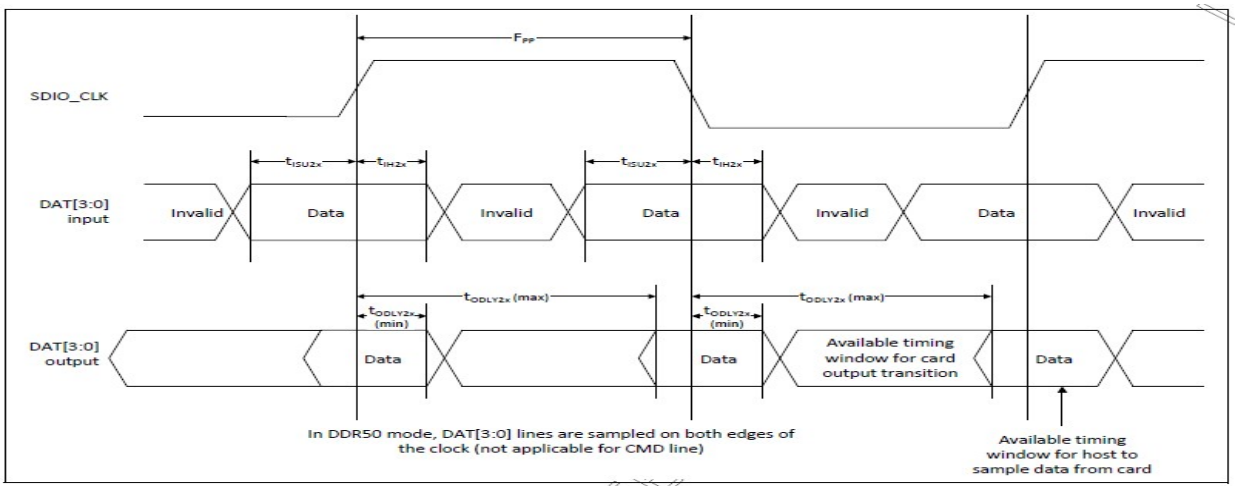


SDIO Bus Timing Specifications in DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	20	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × tCLK	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty	–	45	55	%	–

Data Timing



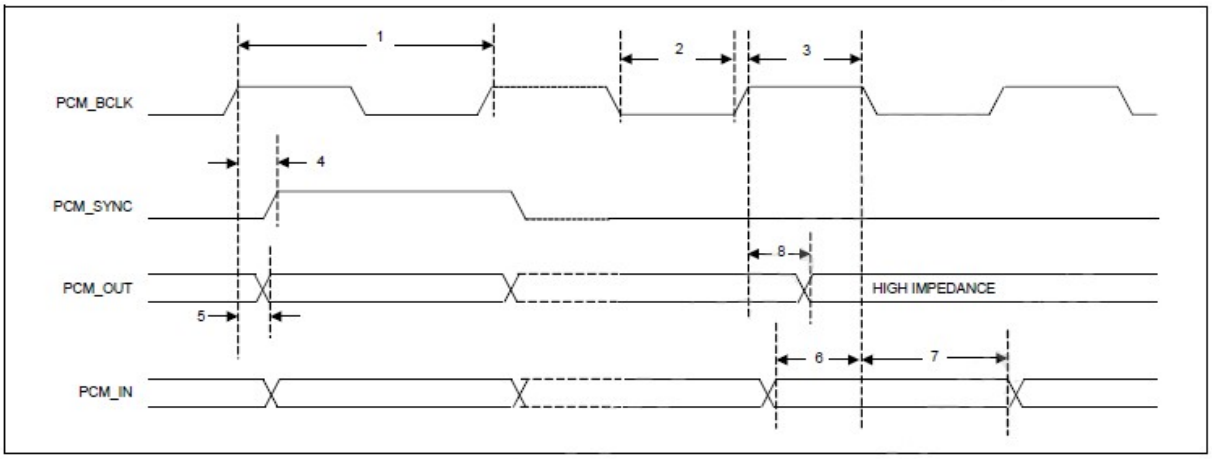
Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30 pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	C_{CARD} < 25 pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)

8.3 PCM Interface Description

The PCM Interface on the BCM43456 can connect to linear PCM Codec devices in master or slave mode. In master mode, the BCM43456 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM43456.The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Short Frame Sync, Master Modem

PCM Timing Diagram (Short Frame Sync, Master Mode)

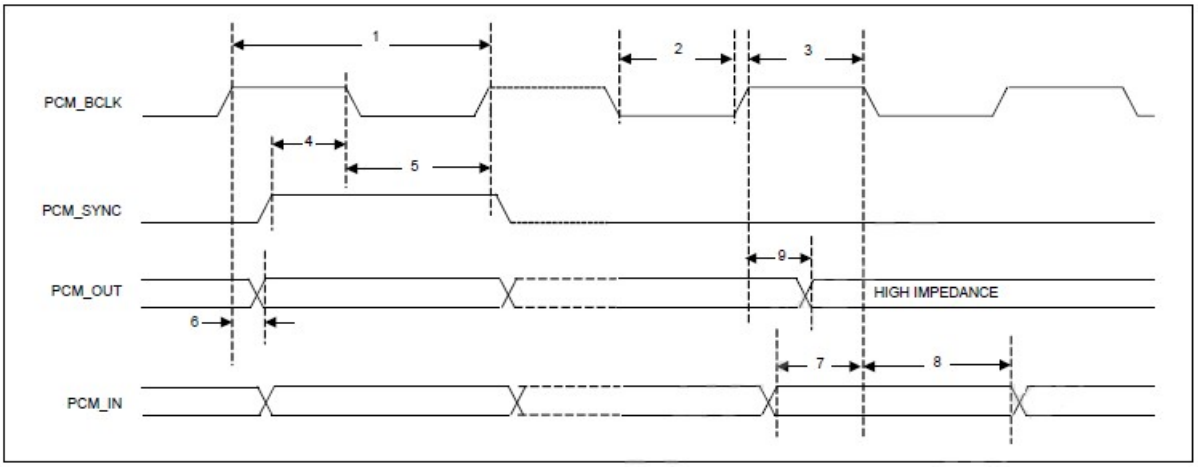


PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)

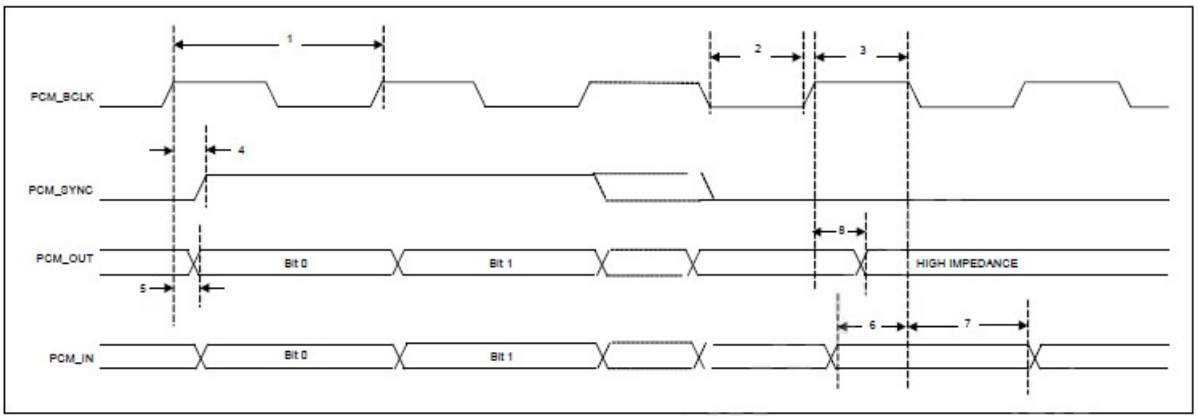


PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)

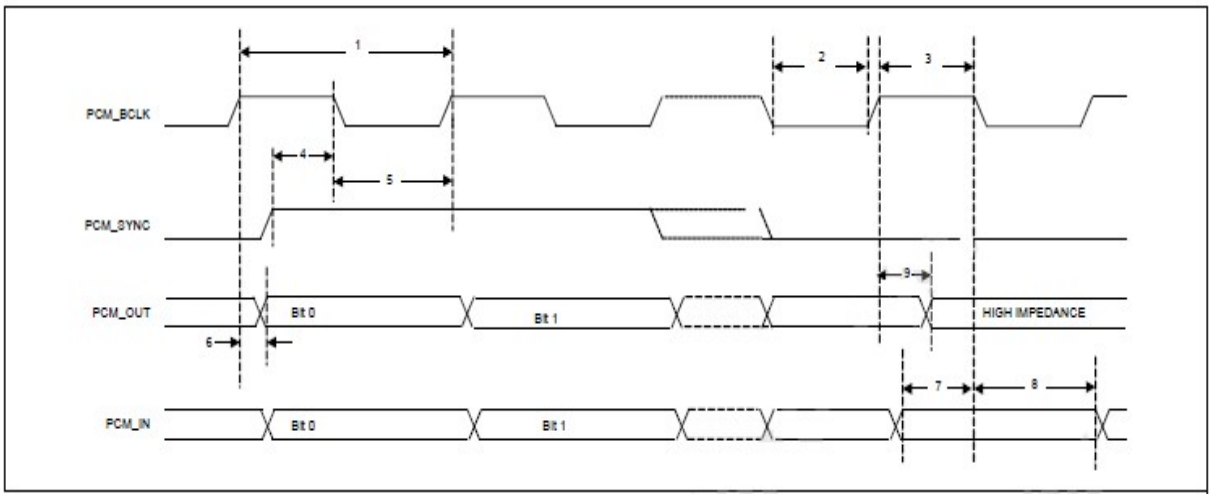


PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)

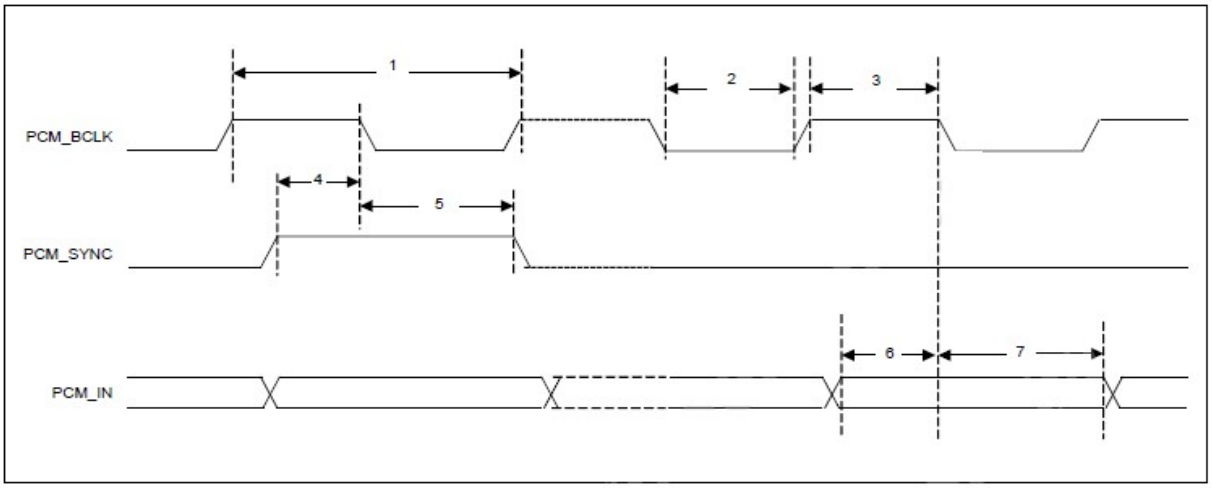


PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

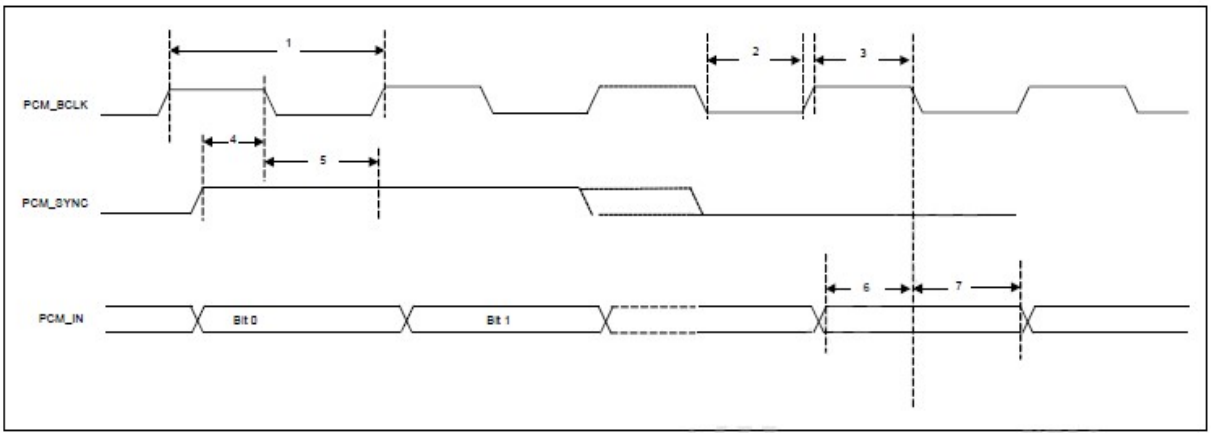


PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)



PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

8.4 UART Interface Description

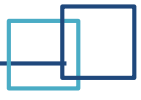
The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The BCM43456 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

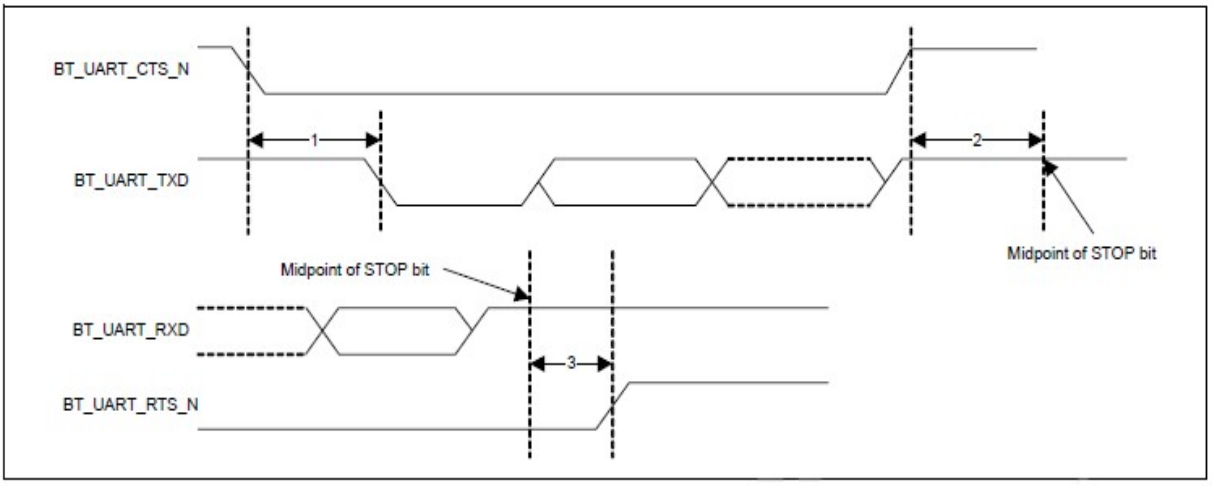
Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The BCM43456 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.



Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

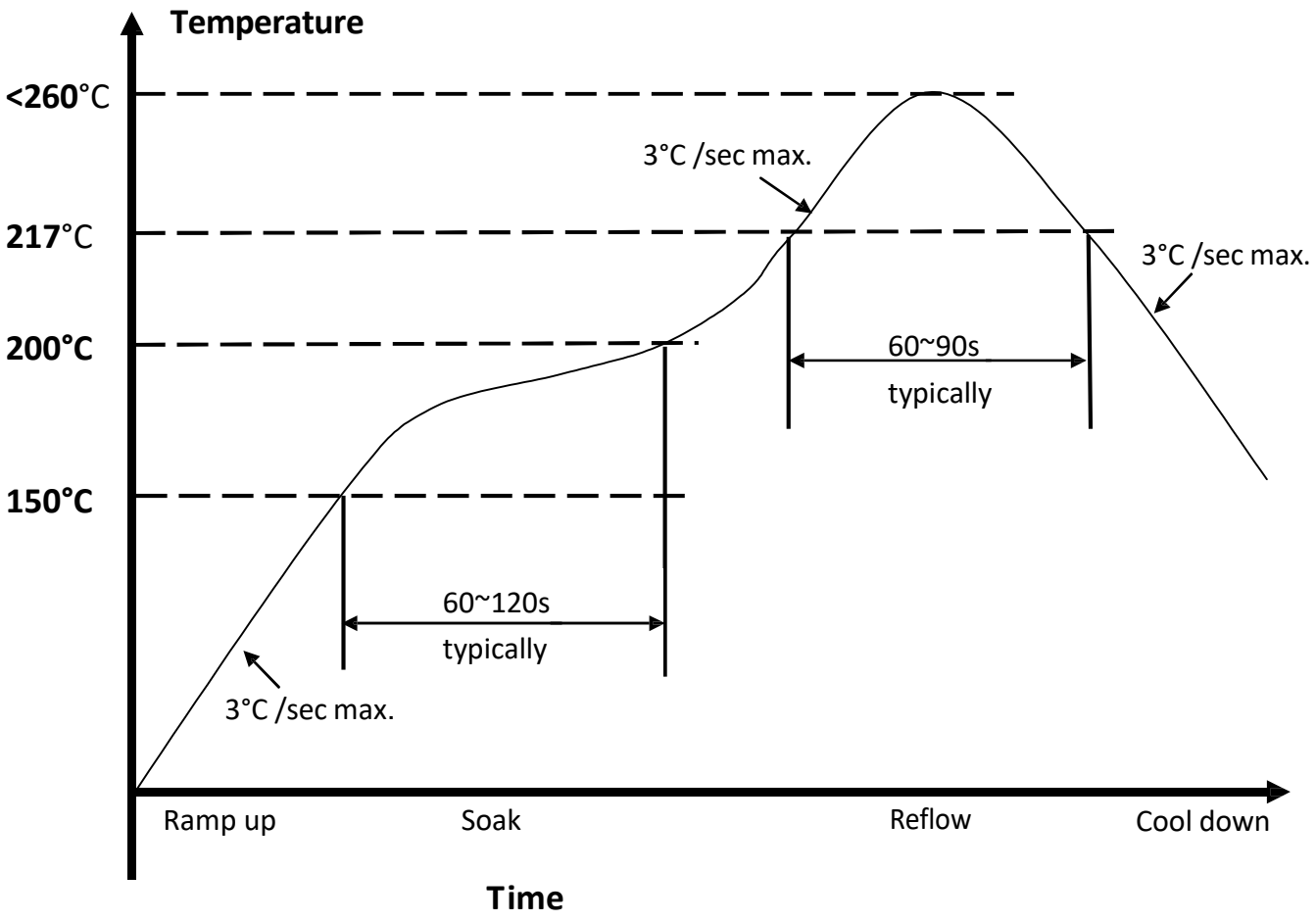
UART Timing



UART Timing Specifications

Ref	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

9. Recommended Reflow Profile



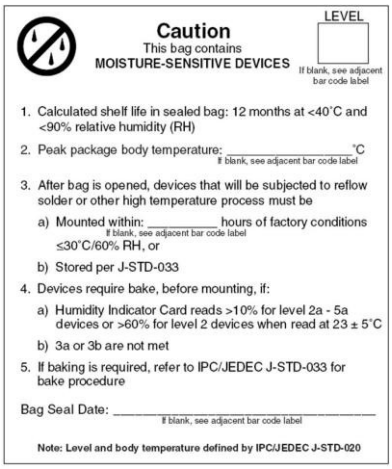
1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C
3. Cycle of Reflow : 2 times max.
4. Adding Nitrogen (N2) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component.

10. Package Information

10.1 Label

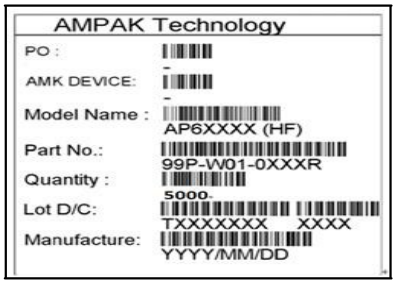
Label A→ Anti-static and humidity notice

Label B→ MSL caution / Storage Condition

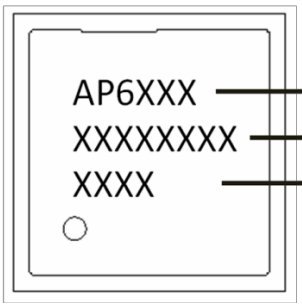


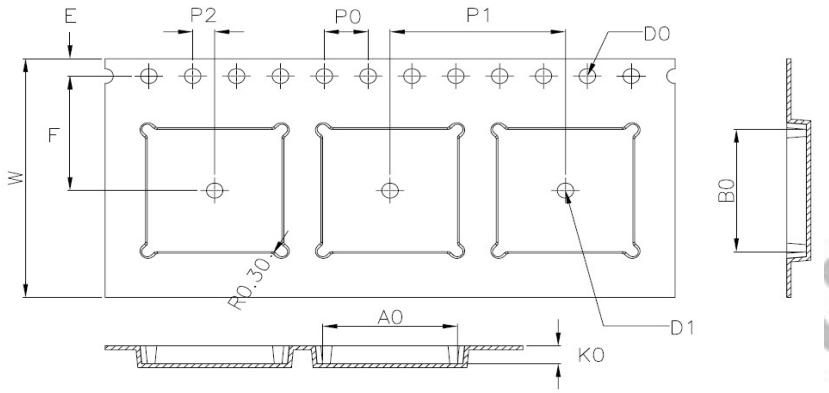
Label C→ Inner box label .

Label D→ Carton box label .



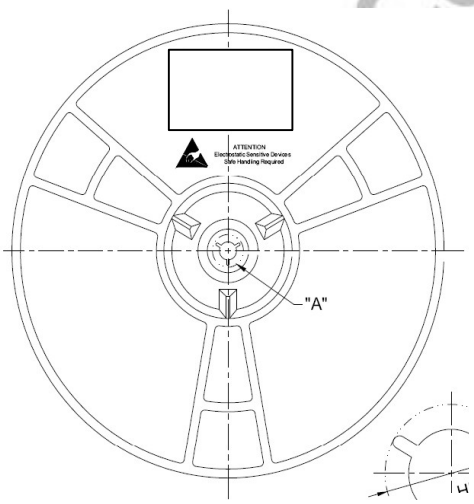
10.2 Dimension

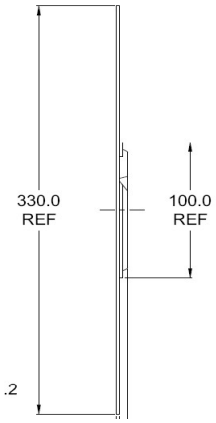


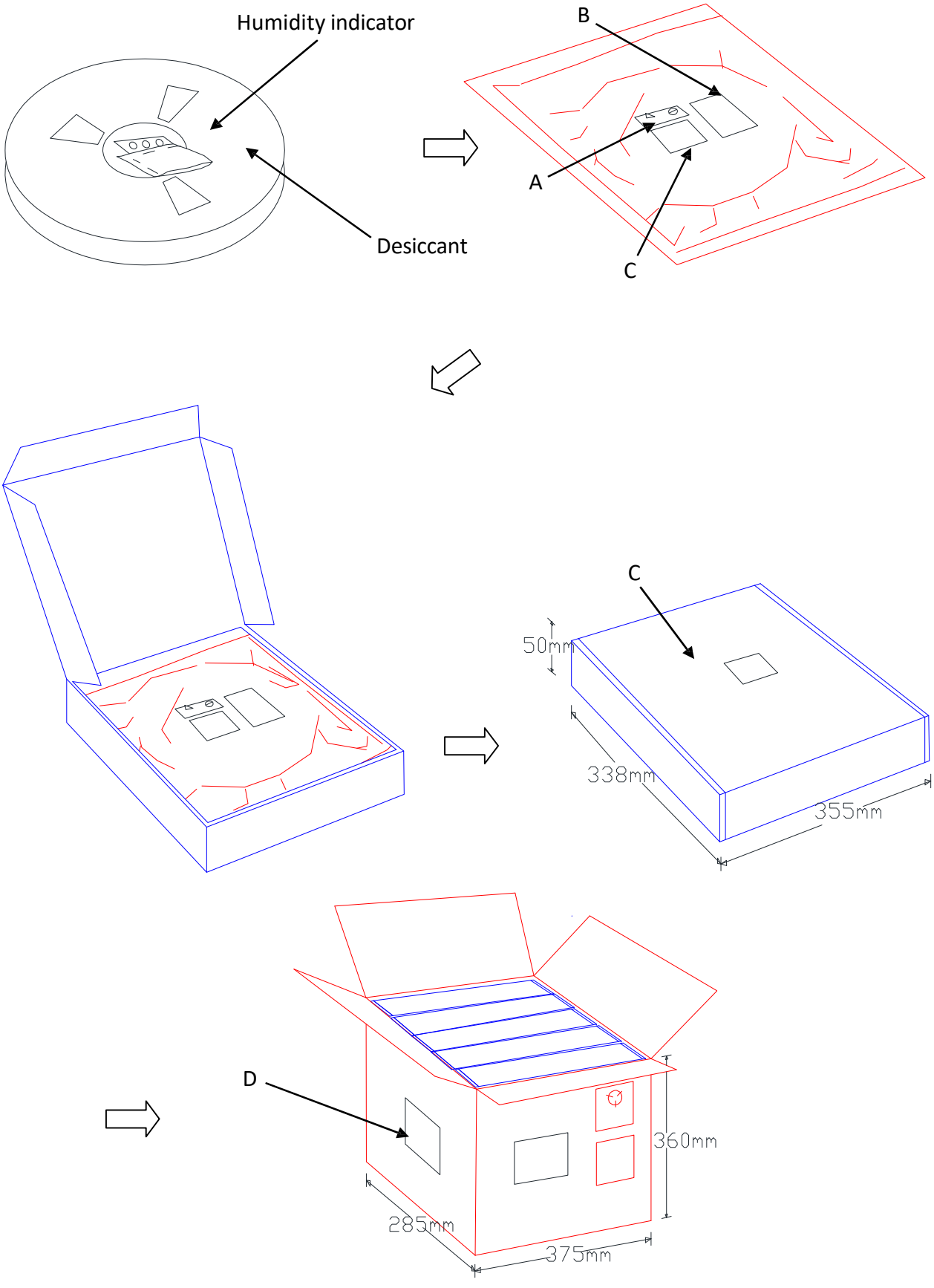


W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 +0.10 −0.00
D1	ø1.50MIN

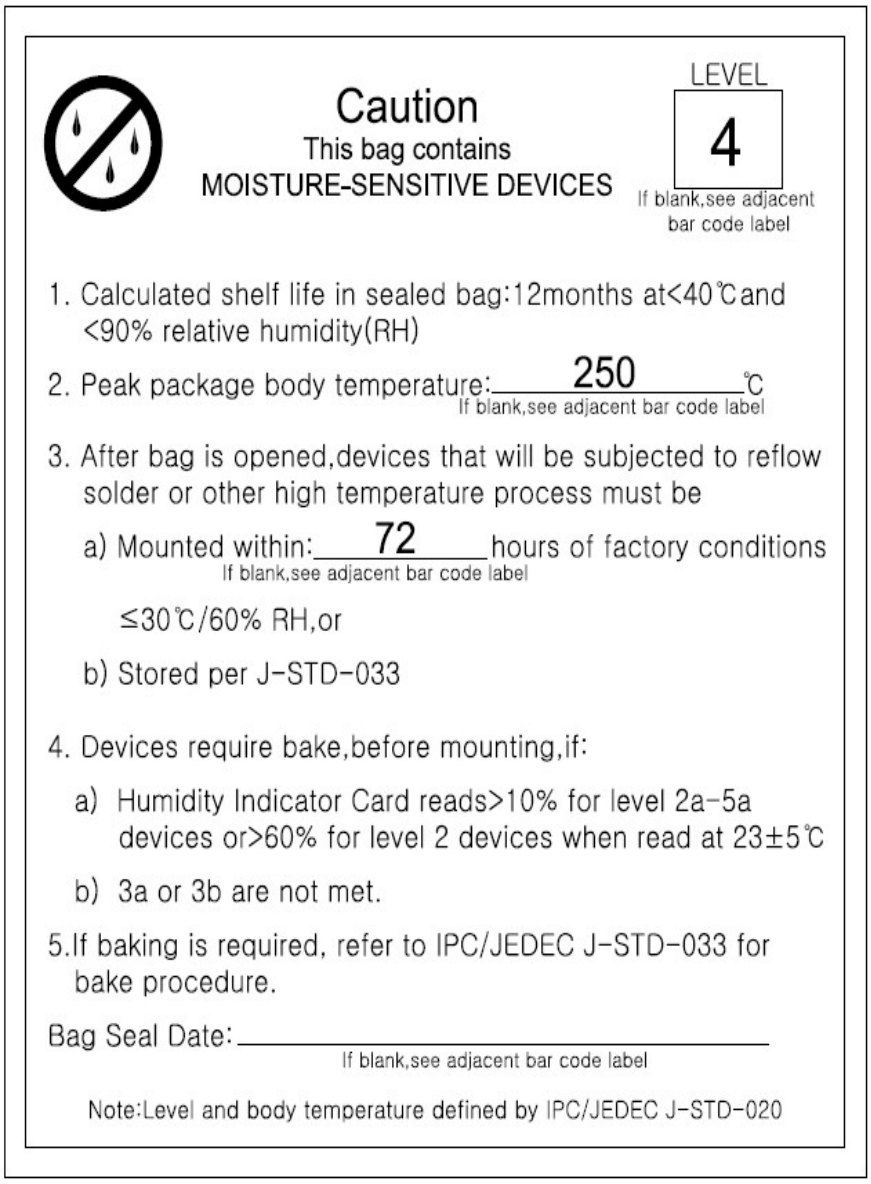
1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material: Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness: 0.30±0.05mm.
6. Component load per 13”reel : 1500 PCS






Humidity indicator
Desiccant
B
A
C
C
50mm
338mm
355mm
D
360mm
285mm
375mm

10.3 MSL Level / Storage Condition



Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL 4
If blank,see adjacent bar code label

1. Calculated shelf life in sealed bag:12months at<40℃and <90% relative humidity(RH)
2. Peak package body temperature: 250 ℃
   If blank,see adjacent bar code label
3. After bag is opened,devices that will be subjected to reflow solder or other high temperature process must be
   a) Mounted within: 72 hours of factory conditions
      If blank,see adjacent bar code label
      ≤30℃/60% RH,or
   b) Stored per J-STD-033
4. Devices require bake,before mounting,if:
   a) Humidity Indicator Card reads>10% for level 2a-5a devices or>60% for level 2 devices when read at 23±5℃
   b) 3a or 3b are not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

Bag Seal Date: _____
If blank,see adjacent bar code label

Note:Level and body temperature defined by IPC/JEDEC J-STD-020

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

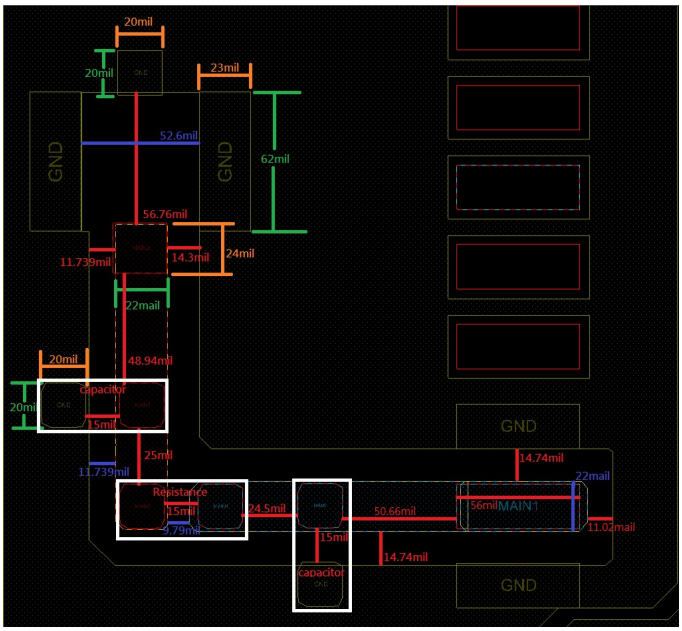
FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This device and its antenna(s) must not be co-located or operating in conjunction with any other antenna or transmitter.

For product available in the USA/Canada market, only channel 1~11 can be operated. Selection of other channels is not possible.
This device is restricted to indoor use.

Trace antenna designs:



IMPORTANT NOTE:
FCC Radiation Exposure Statement:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled

environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This module is intended for OEM integrators under the following conditions:
1. This module is certified pursuant to two Part 15 rules sections(15.407, 15.247).

2. This module has been approved to operate with the antenna types listed below, with the maximum permissible gain indicated.

Frequency Band	Antenna Type	Model Number	Gain(dBi)
2400-2483.5MHz	PCB Antenna	A9703688-D	1.39
5150-5850MHz	PCB Antenna	A9703688-D	3.34

3. Label and compliance information

Label of the end product:

The host product must be labeled in a visible area with the following " Contains FCC ID: XHM-AP6255D42".
The end product shall bear the following 15.19 statement: This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
If the labelling area is considered too small and therefore it is impractical (smaller than the palm of the hand) to display the compliance statement, then the statement may be placed in the user manual or product packaging.

4. Information on test modes and additional testing requirements

This module is restricted to integration into hosts for indoor use only.
This module has been approved under stand-alone configuration.
OEM integrator has be limited the operation channels in channel 1-11 for 2.4GHz band.
The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations.
The information on how to configure test modes for host product evaluation for different operational conditions for a stand-alone modular transmitter in a host, , versus with multiple, simultaneously transmitting modules or other transmitters in a host can be found at KDB Publication 996369 D04.

5. Additional testing, Part 15 Subpart B disclaimer

Appropriate measurements (e.g. 15 B compliance) and if applicable additional equipment authorizations (e.g. SDoC) of the host product to be addressed by the integrator/manufacturer.
This module is only FCC authorized for the specific rule parts 15.247, 15.407 listed on the grant, and the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host product as being Part 15 Subpart B compliant.

6. The user manual of the end product should include:

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons.
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This device is restricted to indoor use.
The antenna(s) used for this transmitter must not transmit simultaneously with any other antenna or transmitter.

Professional installation

Section 15.204(b) states that an approved "transmission system" must always be marketed as a complete system including the antenna.

Note, Supplier's Declaration of Conformity §2.1077(a)(3)
Name: FLYTECH TECHNOLOGY CO.,LTD.
Address: 271 East Brokaw Road, San Jose, CA 95112, U.S.A.
Telephone number or Internet contact: http://www.flytech.com/contact_location.php