5G Module, M3100

User Manual

Contents

1

Introduction

Introduction

This document defines the M3100 module and describes its air interface and hardware interface which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of M3100 module. Associated with application note and user guide, customers can use M3100 module to design and set up mobile applications easily.

2

Product Concept

General Description
Key Features

General Description

M3100 module is a 5G/LTE-FDD/LTE-TDD/WCDMA wireless communication module with receive diversity, which provides data connectivity on 5G (sub-6 GHz), LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, and WCDMA networks.

Customers can choose a dedicated type based on the region or operator. The following table shows the frequency bands of M3100 module.

Table 1. Frequency Bands of M3100 Module

Mode	Band
5G (Sub-6)	n2/n14/n25/n28/n30/n41/n48/n66/n71/n77/n78
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B20/B25/B26/B28/B29/B30/B66/B71
LTE-TDD	B38/B39/B40/B41/B48
WCDMA	B1/B2/B4/B5/B8
GNSS[1)]	GPS/GLONASS

NOTE
1)GNSS function is optional.

Key Features

The following table describes the detailed features of M3100 module.

Table 2.Key Features of M3100 Module

Feature	Details
Power Supply	Supply voltage : 3.6V ~ 4.2V Typical supply voltage : 3.8V
Transmit Power	Class 3 for WCDMA bands Class 3 for LTE bands Class 2 for LTE B41 band Class 3 for 5GNR bands Class 2 for 5GNR n77 band

5GNR Features	Support Rel17 5G NR Support sub6 SA and NSA operation mode Support 256 QAM uplink/downlink in sub6 GHz Support downlink 4x4 MIMO
LTE Features	Support up to CA Cat 19 FDD and TDD Support uplink QPSK , 16-QAM and 64-QAM modulation Support downlink QPSK, 16-QAM, 64-QAM, 256-QAM modulation Support 1.4MHz to 20MHz (5×CA) RF bandwidth Support 4x4MIMO in DL direction
WCDMA Features	Support 3GPP R9 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA Support QPSK, 16-QAM and 64-QAM modulation
USB Interface	One eUSB 2.0 and one SS USB 3.1 Gen 2
Qualcomm Universal peripheral engine (QUP)	The QUP module provides up to 9 serial interfaces, also known as serial engines (SE) for SPI, UART, and I2C
PCIe Interface	Three PCIe interfaces: 1. Interface 0: one lane PCIe Gen 4 or two lanes PCIe Gen 3 2. Interface 1: two lanes PCIe Gen 3 3. Interface 2: one lane PCIe Gen 3
Antenna interfaces	Including antenna(ANT0), antenna (ANT1), MIMO PRx antenna(ANT2), MIMO DRx antenna(ANT3)
Physical Characteristics	Size : 44.0mm x 60.0mm x 3.0mm Weight : TBD
Temperature Range	Operation temperature range: -30°C ~ +75°C Storage temperature range: -40°C~ +95°C

3

Application Interface

General Description
Pin Assignment
Pin Description
Operating Modes
Power Supply
PCIe Interface

General Description

M3100 module is equipped with (80-pin x 2, 40-pin x 1) BtoB connector that can be connected to cellular application platform.
Sub-interfaces included in these pins are described in detail in the following chapters:

- Power supply
- USIM interface
- eUSB 2.0/3.1 interface
- UART interface
- I2C interface
- SPI interface
- PCIe 3.0 interface
- I2S, PCM interface
- Charger IC control interface
- THERM interface
- GPIO's control interface

Pin Assignment

The following figure shows the pin assignment of M3100 module

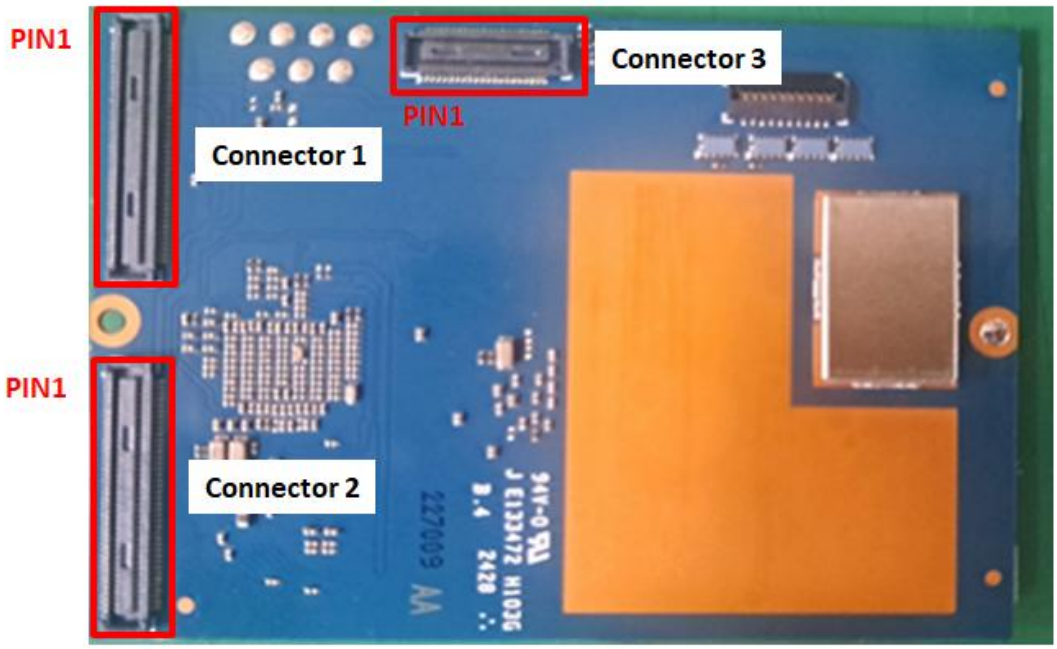


Figure 2. Pin Assignment (Bottom View)

B to B connector 1			
Pin name	Pin No.		Pin name
VREG_S7_0P9	1	2	VREG_S7_0P9
VREG_S7_0P9	3	4	VREG_S7_0P9
VREG_S7_0P9	5	6	VREG_S7_0P9
VPH_PWR_3P8	7	8	VPH_PWR_3P8
VPH_PWR_3P8	9	10	VPH_PWR_3P8
VPH_PWR_3P8	11	12	VPH_PWR_3P8
VPH_PWR_3P8	13	14	VPH_PWR_3P8
VREG_S4_1P9	15	16	VREG_L15_1P2
VREG_S4_1P9	17	18	VREG_L6_1P8
VREG_S4_1P9	19	20	VREG_L6_1P8
VREG_S2_1P2	21	22	VREG_DBB1_3P3
VREG_S2_1P2	23	24	VREG_DBB1_3P3
VREG_S2_1P2	25	26	VREG_1P2_SYS
VREG_1P8_SYS	27	28	VREG_1P2_SYS
VREG_1P8_SYS	29	30	VREG_L11_1P8
VREG_L1_1P2	31	32	SLIC_INT_N
VREG_L1_1P2	33	34	QEP_PWR_EN
VREG_L5_1P8	35	36	UIM2_PRESENT
VREG_L5_1P8	37	38	UIM2_DATA
VREG_L10_3P1	39	40	UIM2_CLK
VREG_L10_3P1	41	42	UIM2_RESET
PM7550B_SYS_OK_PON_N	43	44	VREG_L13_1P8
FORCE_USB_BOOT_PM7550B	45	46	AQR_MDC
FAST_BOOT	47	48	AQR_MDIO
PM7550B_PHY_ON	49	50	TOUCH_RESET
GND	51	52	BUTTON_LEFT
QEP_RESET_N	53	54	AMBIENT_THERM
PPS_ETH_PHY	55	56	GND
QEP_MDC	57	58	SDX75_USXGMII0_TX_M
QEP_MDIO	59	60	SDX75_USXGMII0_TX_P
QEP_INT_N	61	62	GND
WLAN_FEM_SEL0	63	64	SDX75_USXGMII0_RX_M
WLAN_FEM_SEL1	65	66	SDX75_USXGMII0_RX_P
GND	67	68	GND
SDX75_SGMII1_TX_M	69	70	SENSOR_I2C_SDA
SDX75_SGMII1_TX_P	71	72	SENSOR_I2C_SCL
GND	73	74	DIV_ANT_SEL0
SDX75_SGMII1_RX_M	75	76	DIV_ANT_SEL1
SDX75_SGMII1_RX_P	77	78	SLIC_RST_N
GND	79	80	GND

B to B connector 2			
Pin name	Pin No.		Pin name
GND	1	2	GND
USB_SS_TX_P	3	4	PCIE0_WCN_REFCLK_P
USB_SS_TX_M	5	6	PCIE0_WCN_REFCLK_M
GND	7	8	GND
USB_SS_RX_P	9	10	PCIE0_WCN_RX0_P
USB_SS_RX_M	11	12	PCIE0_WCN_RX0_M
GND	13	14	GND
USB_HS_EDP	15	16	PCIE0_WCN_TX0_P
USB_HS_EDM	17	18	PCIE0_WCN_TX0_M
GND	19	20	GND
DBG_UART_TX	21	22	PCIE0_WCN_RX1_P
DBG_UART_RX	23	24	PCIE0_WCN_RX1_M
STATUS_LED_ON	25	26	GND
ALSP_INT	27	28	PCIE0_WCN_TX1_P
BUTTON_MENU	29	30	PCIE0_WCN_TX1_M
BUTTON_RIGHT	31	32	GND
I2C_SDA	33	34	PCIE0_RST_N
I2C_SCL	35	36	PCIE0_WAKE_N
GND	37	38	PCIE0_CLK_REQ_N
KPD_PWR_N	39	40	PMX_UIM1_RESET
FACTORY_RESIN_N	41	42	PMX_UIM1_CLK
PM_FAULT_N	43	44	PMX_UIM1_DATA
BT_SEC_I2S_D1	45	46	WCN_HOST_SOL
BT_SEC_I2S_SCK	47	48	WCN_DEV_SOL
BT_SEC_I2S_D0	49	50	WCN_SW_CTRL_WLAN
BT_SEC_I2S_WS	51	52	BT_UART_CTS_N
BT_UART_TXD	53	54	BT_UART_RFR_N
BT_UART_RXD	55	56	PA_MUTING
WCN_BT_EN	57	58	WCN_LAA_RX
WLAN_EN	59	60	UIM2_LS_EN
WCN_AS_EN	61	62	SENSOR_MISO
WLAN_LTE_COXM_TXD	63	64	SENSOR_MOSI
WLAN_LTE_COXM_RXD	65	66	SENSOR_CLK
ANT_SEL0	67	68	SENSOR_CS_N
ANT_SEL1	69	70	UIM1_PRESENT
WCN_SW_CTRL	71	72	GND
GND	73	74	SLEEP_CLK
SPMI_CLK	75	76	GND
SPMI_DATA	77	78	RFCLK1
GND	79	80	GND

B to B connector 3			
Pin name	Pin No.		Pin name
WK_5G_WLAN_DIS	1	2	GND
WK_6G_PWR_EN	3	4	PCIE1_REFCLK_P
DEBUG_UART_TX	5	6	PCIE1_REFCLK_M
DEBUG_UART_RX	7	8	GND
GND	9	10	PCIE1_RX0_P
N46_B46_SP2T	11	12	PCIE1_RX0_M
WK_5G_PWR_EN	13	14	GND
SFP_PWR_EN	15	16	PCIE1_TX0_P
GND	17	18	PCIE1_TX0_M
RFFE0_DATA	19	20	GND
RFFE0_CLK	21	22	PCIE1_RX1_P
GND	23	24	PCIE1_RX1_M
PCIE2_REFCLK_P	25	26	GND
PCIE2_REFCLK_M	27	28	PCIE0_TX1_P
GND	29	30	PCIE0_TX1_M
PCIE2_TX_P	31	32	GND
PCIE2_TX_M	33	34	RFFE1_DATA
GND	35	36	RFFE1_CLK
PCIE2_RX_P	37	38	GND
PCIE2_RX_M	39	40	SDX_PCIE1_RESET_N

Pin Description

The following tables show the pin definition and description of M3100 module.

Table 3 : I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
OD	Open Drain
PI	Power Input
PO	Power Output

Table 4 : Pin Description

Connector 1			
Pin Name	**Pin No.**	**I/O**	**Description**
VREG_S7_0P9	1~6	PO	SMPS switch node
VPH_PWR_3P8	7 ~ 14	PO	Main power input
VREG_S4_1P9	15,17,19	PO	SMPS switch node
VREG_S2_1P2	21,23,25	PO	SMPS switch node
VREG_1P8_SYS	27,29	PO	LDO regulated output
VREG_L1_1P2	31,33	PO	LDO regulated output
VREG_L5_1P8	35,37	PO	LDO regulated output
VREG_L10_3P1	39,41	PO	LDO regulated output
VREG_L15_1P2	16	PO	LDO regulated output
VREG_L6_1P8	18,20	PO	LDO regulated output
VREG_DBB1_3P3	22,24	PI	DBB1 input
VREG_1P2_SYS	26,28	PO	LDO regulated output
VREG_L11_1P8	30	PO	LDO regulated output
PM7550B_SYS_OK_PON_N	43	IO	PM7550B Charger_SYS_OK__N
FORCE_USB_BOOT_PM7550B	45	IO	FORCED_USB_BOOT

FAST_BOOT	47	IO	Configurable I/O
PM7550B_PHY_ON	49	IO	PM7550B PHY ON
QEP_RESET_N	53	IO	Configurable I/O
PPS_ETH_PHY	55	IO	Configurable I/O
QEP_MDC	57	IO	Configurable I/O
QEP_MDIO	59	IO	Configurable I/O
QEP_INT_N	61	IO	Configurable I/O
WLAN_FEM_SEL0	63	IO	Configurable I/O
WLAN_FEM_SEL1	65	IO	Configurable I/O
SDX75_SGMII1_TX_M	69	AO	USXGMII interface 1 serial data Tx - minus
SDX75_SGMII1_TX_P	71	AO	USXGMII interface 1 serial data Tx - plus
SDX75_SGMII1_RX_M	75	AI	USXGMII interface 1 serial data Rx - minus
SDX75_SGMII1_RX_P	77	AI	USXGMII interface 1 serial data Rx - plus
SLIC_INT_N	32	IO	Configurable I/O
QEP_PWR_EN	34	IO	Configurable I/O
UIM2_PRESENT	36	IO	UIM2 presence detection
UIM2_DATA	38	IO	UIM2 data
UIM2_CLK	40	IO	UIM2 clock
UIM2_RESET	42	IO	UIM2 reset
VREG_L13_1P8	44	PO	LDO regulated output
AQR_MDC	46	IO	MDIO interface clock signal
AQR_MDIO	48	IO	MDIO interface data signal
TOUCH_RESET	50	IO	Configurable I/O
BUTTON_LEFT	52	IO	Configurable I/O
AMBIENT_THERM	54	AI	Analog multiplexer (AMUX) input
SDX75_USXGMII0_TX_M	58	AO	USXGMII interface 0 serial data Tx - minus
SDX75_USXGMII0_TX_P	60	AO	USXGMII interface 0 serial data Tx - plus
SDX75_USXGMII0_RX_M	64	AI	USXGMII interface 0 serial data Rx - minus
SDX75_USXGMII0_RX_P	66	AI	USXGMII interface 0 serial data Rx - plus
SENSOR_I2C_SDA	70	IO	BLSP I2C data
SENSOR_I2C_SCL	72	IO	BLSP I2C clock
DIV_ANT_SEL0	74	IO	Configurable I/O
DIV_ANT_SEL1	76	IO	Configurable I/O

SLIC_RST_N	78	IO	Configurable I/O
GND	51,56,62,67, 68,73,79,80		Ground

Connector 2			
Pin Name	**Pin No.**	**I/O**	**Description**
USB_SS_TX_P	3	AI, AO	USB super-speed transmit - plus
USB_SS_TX_M	5	AI, AO	USB super-speed transmit - minus
USB_SS_RX_P	9	AI, AO	USB super-speed receive - plus
USB_SS_RX_M	11	AI, AO	USB super-speed receive - minus
USB_HS_EDP	15	AI, AO	EUSB port - plus
USB_HS_EDM	17	AI, AO	EUSB port - minus
DBG_UART_TX	21	IO	BLSP UART transmit data
DBG_UART_RX	23	IO	BLSP UART receive data
STATUS_LED_ON	25	IO	Configurable I/O
ALSP_INT	27	IO	Configurable I/O
BUTTON_MENU	29	IO	Configurable I/O
BUTTON_RIGHT	31	IO	Configurable I/O
I2C_SDA	33	IO	BLSP I2C data
I2C_SCL	35	IO	BLSP I2C clock
KPD_PWR_N	39	DI	Module PWR ON key (low active)
FACTORY_RESIN_N	41	DI	Factory reset (low active)
PM_FAULT_N	43	IO	PMIC pault signal
BT_SEC_I2S_D1	45	IO	Secondary I2S data 1 - for BT
BT_SEC_I2S_SCK	47	IO	Secondary I2S clock - for BT
BT_SEC_I2S_D0	49	IO	Secondary I2S data 0 - for BT
BT_SEC_I2S_WS	51	IO	Secondary I2S word select - for BT
BT_UART_TXD	53	IO	BLSP UART transmit data
BT_UART_RXD	55	IO	BLSP UART receive data
WCN_BT_EN	57	IO	Configurable I/O
WLAN_EN	59	IO	Configurable I/O
WCN_AS_EN	61	IO	Configurable I/O
WLAN_LTE_COXM_TXD	63	IO	Configurable I/O

WLAN_LTE_COXM_RXD	65	IO	Configurable I/O
ANT_SEL0	67	IO	Configurable I/O
ANT_SEL1	69	IO	Configurable I/O
WCN_SW_CTRL	71	IO	Configurable I/O
SPMI_CLK	75	DI, DO	Slave and PBUS interface for PMICs – clock
SPMI_DATA	77	DI, DO	Slave and PBUS interface for PMICs – data
PCIE0_WCN_REFCLK_P	4	AO	PCIe 0 Gen 3 reference clock - plus
PCIE0_WCN_REFCLK_M	6	AO	PCIe 0 Gen 3 reference clock - minus
PCIE0_WCN_RX0_P	10	AI	PCIe 0 Gen 3 receive 0 - plus
PCIE0_WCN_RX0_M	12	AI	PCIe 0 Gen 3 receive 0 - minus
PCIE0_WCN_TX0_P	16	AO	PCIe 0 Gen 3 transmit 0 - plus
PCIE0_WCN_TX0_M	18	AO	PCIe 0 Gen 3 transmit 0 - minus
PCIE0_WCN_RX1_P	22	AI	PCIe 0 Gen 3 receive 1 - plus
PCIE0_WCN_RX1_M	24	AI	PCIe 0 Gen 3 receive 1 - minus
PCIE0_WCN_TX1_P	28	AO	PCIe 0 Gen 3 transmit 1 - plus
PCIE0_WCN_TX1_M	30	AO	PCIe 0 Gen 3 transmit 1 - minus
PCIE0_RST_N	34	IO	PCIe0 reset signal
PCIE0_WAKE_N	36	IO	PCIe0 wake up signal
PCIE0_CLK_REQ_N	38	IO	PCIE0 clock request
PMX_UIM1_RESET	40	IO	UIM1 reset
PMX_UIM1_CLK	42	IO	UIM1 clock
PMX_UIM1_DATA	44	IO	UIM1 data
WCN_HOST_SOL	46	IO	Configurable I/O
WCN_DEV_SOL	48	IO	Configurable I/O
WCN_SW_CTRL_WLAN	50	IO	Configurable I/O
BT_UART_CTS_N	52	IO	BLSP UART CTS
BT_UART_RFR_N	54	IO	BLSP UART RFR
PA_MUTING	56	IO	Configurable I/O
WCN_LAA_RX	58	IO	Configurable I/O
UIM2_LS_EN	60	DI	UIM2_LS_EN
SENSOR_MISO	62	IO	Configurable I/O
SENSOR_MOSI	64	IO	Configurable I/O
SENSOR_CLK	66	IO	Configurable I/O

SENSOR_CS_N	68	IO	Configurable I/O
UIM1_PRESENT	70	IO	UIM1 presence detection
SLEEP_CLK	74	DI	Sleep clock
RFCLK1	78	DI	76.8 MHz RF clock
GND	1,2,7,8,13,14, 19,20,26,32, 37,72,73,76, 79,80		Ground

Connector 3			
Pin Name	**Pin No.**	**I/O**	**Description**
WK_5G_WLAN_DIS	1	IO	Configurable I/O
WK_6G_PWR_EN	3	IO	Configurable I/O
DEBUG_UART_TX	5	IO	BLSP UART transmit data
DEBUG_UART_RX	7	IO	BLSP UART receive data
N46_B46_SP2T	11	IO	Configurable I/O
WK_5G_PWR_EN	13	IO	Configurable I/O
SFP_PWR_EN	15	IO	Configurable I/O
RFFE0_DATA	19	IO	RF front end interface data
RFFE0_CLK	21	IO	RF front end interface clock
PCIE2_REFCLK_P	25	AO	PCIe 2 Gen 3 reference clock - plus
PCIE2_REFCLK_M	27	AO	PCIe 2 Gen 3 reference clock - minus
PCIE2_TX_P	31	AO	PCIe 2 Gen 3 transmit - plus
PCIE2_TX_M	33	AO	PCIe 2 Gen 3 transmit - minus
PCIE2_RX_P	37	AI	PCIe 2 Gen 3 receive - plus
PCIE2_RX_M	39	AI	PCIe 2 Gen 3 receive - minus
PCIE1_REFCLK_P	4	AO	PCIe 1 Gen 3 reference clock - plus
PCIE1_REFCLK_M	6	AO	PCIe 1 Gen 3 reference clock - minus
PCIE1_RX0_P	10	AI	PCIe 1 Gen 3 receive 0 - plus
PCIE1_RX0_M	12	AI	PCIe 1 Gen 3 receive 0 - minus
PCIE1_TX0_P	16	AO	PCIe 1 Gen 3 transmit 0 - plus
PCIE1_TX0_M	18	AO	PCIe 1 Gen 3 transmit 1 - minus
PCIE1_RX1_P	22	AI	PCIe 1 Gen 3 receive 1 - plus

PCIE1_RX1_M	24	AI	PCIe 1 Gen 3 receive 1 - minus
PCIE0_TX1_P	28	AO	PCIe 1 Gen 3 transmit 1 - plus
PCIE0_TX1_M	30	AO	PCIe 1 Gen 3 transmit 1 - minus
RFFE1_DATA	34	IO	RF front end interface data
RFFE1_CLK	36	IO	RF front end interface clock
SDX_PCIE1_RESET_N	40	IO	PCIe1 reset signal
GND	2,8,9,14,17, 20,23,26,29, 32,35,38		Ground

Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 5 :Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Airplane Mode	In this mode, RF function will be invalid and Application Processor sleep state.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interfaces are not accessible.	

- Airplane mode

When the module enters into airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following ways.

Software(TBD)

AT+CFUN command provides the choice of the functionality level through setting <fun> into 0, 1 or 4.

AT+CFUN=0: Minimum functionality mode; both (U)SIM and RF functions are disabled.
AT+CFUN=1: Full functionality mode (by default).
AT+CFUN=4: Airplane mode. RF function is disabled.

Power Supply

- Power supply pins

M3100 provides eleven VPH_PWR pins dedicated to connect with the external power supply.

The following table shows the details of VBAT pins and ground pins

Table 6 : VPH_PWR and GND Pins

Pin name	Pin No. (CON 1)	Description	Min	Typ	Max	Unit
VPH_PWR	7 ~ 14	Power supply for module's main power	3.5	3.8	4.2	V
GND	1, 2, 37, 38, 51, 52, 68, 77, 78	Ground	-	0	-	

- Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure the input voltage will neverdrop below 3.3V. The following figure shows the voltage drop during Tx power in 3G,4G and 5G networks.

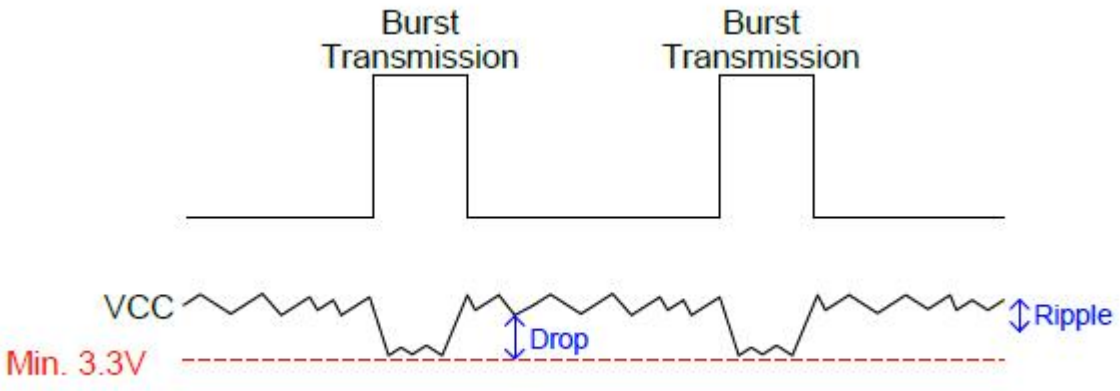


Figure 3: Power Supply Limits during Tx Power

- Reference Design for Power Supply

: TBD

PCIe Interface

M3100 includes one PCIe interface which are compliant with PCI Express Specification Revision3.0, 4.0. The key features of the PCIe interface are shown below:

- PCI Express Specification Revision 3.0& 4.0 compliance
- Data rate at 8Gbps per lane
- Can be used to connect to an external Ethernet IC (MAC and PHY) or WLAN IC.

Table 11: Pin Definition of the PCIe Interface

Pin Name	Pin No.	Description	DC Characteristics
PCIE0_WCN_REFCLK_P	4	PCIe 0 Gen 3 reference clock - plus	Compliant with PCIe Gen 3.0 & 4.0 standard specifications. Require differential impedance of 85Ω.
PCIE0_WCN_REFCLK_M	6	PCIe 0 Gen 3 reference clock - minus	
PCIE0_WCN_RX0_P	10	PCIe 0 Gen 3 receive 0 - plus	
PCIE0_WCN_RX0_M	12	PCIe 0 Gen 3 receive 0 - minus	
PCIE0_WCN_TX0_P	16	PCIe 0 Gen 3 transmit 0 - plus	
PCIE0_WCN_TX0_M	18	PCIe 0 Gen 3 transmit 0 - minus	
PCIE0_WCN_RX1_P	22	PCIe 0 Gen 3 receive 1 - plus	
PCIE0_WCN_RX1_M	24	PCIe 0 Gen 3 receive 1 - minus	
PCIE0_WCN_TX1_P	28	PCIe 0 Gen 3 transmit 1 - plus	
PCIE0_WCN_TX1_M	30	PCIe 0 Gen 3 transmit 1 - minus	
PCIE0_RST_N	34	PCIe0 reset signal	
PCIE0_WAKE_N	36	PCIe0 wake up signal	
PCIE0_CLK_REQ_N	38	PCIE0 clock request	

In order to enhance the reliability and availability in applications, please follow the criteria below in thePCIe interface circuit design:

A. Keep PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, and19.2MHz clock signals.
B. A capacitance should be added in series on Tx/Rx traces to remove any DC bias.
C. Keep the maximum trace length less than 300mm.
D. The length difference of Tx or Rx differential pairs should be less than 0.7mm for PCIe routing traces.
E. The differential impedance of PCIe data trace should be 85Ω±10%.
F. Separate the SS-USB data pairs (Tx, Rx) and PCIe data pairs (Tx, Rx) from each other as far aspossible. If SS_USB and PCIe data pairs must cross on adjacent layers, please keep crossings atright angles to minimize unbalanced (asymmetric) coupling.
G. PCIe data traces must not be routed under components or crossing other traces.

4

Antenna Interfaces

Antenna Connector Definition
Operating Frequency

Antenna Connector Definition

The pin definition of antennas interfaces are shown below.

Table 12. Connector Definition of the RF Antenna

Con. Name	Description	Comment
ANT0	MHB TRx0, LB DRx, UHB Tx1/DRx	50Ω impedance
ANT1	LB TRx0, UHB TRx0, MHB Tx1/DRx	50Ω impedance
ANT2	MHB/UHB MIMO PRx antenna	50Ω impedance
ANT3	MHB/UHB MIMO DRx antenna	50Ω impedance
ANT7	GNSS antenna interface	50Ω impedance

Operating Frequency

Table 13.Module Operating Frequency

Band	Transmit	Receive	Unit
WCDMA B1	1920~1980	2110~2170	MHz
WCDMA B2	1850~1910	1930~1990	MHz
WCDMA B4	1710~1755	2110~2155	MHz
WCDMA B5	824~849	869~894	MHz
WCDMA B8	880~915	925~960	MHz
LTE B1	1920~1980	2110~2170	MHz
LTE B2	1850~1910	1930~1990	MHz
LTE B3	1710~1785	1805~1880	MHz
LTE B4	1710~1755	2110~2155	MHz
LTE B5	824~849	869~894	MHz
LTE B7	2500~2570	2620~2690	MHz
LTE B8	880~915	925~960	MHz
LTE B12	699~716	729~746	MHz
LTE B13	777~787	746~756	MHz
LTE B14	788~798	758~768	MHz
LTE B20	832~862	791~821	MHz
LTE B25	1850~1915	1930~1995	MHz
LTE B26	814~849	859~984	MHz
LTE B28	703~748	758~803	MHz
LTE B29	N/A	717~728	MHz
LTE B30	2305~2315	2350~2360	MHz
LTE B38	2570~2620	2570~2620	MHz
LTE B39	1880~1920	1880~1920	MHz
LTE B40	2300~2400	2300~2400	MHz

LTE B41	2496~2690	2496~2690	MHz
LTE B48	3550~3700	3550~3700	MHz
LTE B66	1710~1780	2110~2200	MHz
LTE B71	663~698	617~652	MHz
5GNR n2	1850~1910	1930~1990	MHz
5GNR n5	824~849	869~894	MHz
5GNR n14	788~798	758~768	MHz
5GNR n25	1850~1915	1930~1995	MHz
5GNR n28	703~748	758~803	MHz
5GNR n30	2305~2315	2350~2360	MHz
5GNR n41	2496~2690	2496~2690	MHz
5GNR n48	3550~3700	3550~3700	MHz
5GNR n66	1710~1780	2110~2200	MHz
5GNR n71	663~698	617~652	MHz
5GNR n77	3450~3550, 3700~3980	3450~3550, 3700~3980	MHz
5GNR n78	3450~3550	3450~3550	MHz

5

Electrical, Reliability and Radio Characteristics

Absolute Maximum Ratings
Operation and Storage Temperatures
RF Receiving Sensitivity

Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 14: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VPH_PWR	TBD	TBD	V
Peak Current of VPH_PWR	TBD	TBD	A
Voltage at Digital Pins	TBD	TBD	V
Voltage at ADC	TBD	TBD	V

Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 15.Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range	-30	+25	+75	ºC
Storage Temperature Range	-40		+95	ºC

RF Receiving Sensitivity

The following tables show conducted RF receiving sensitivity of M3100 module.

Table 16. M3100 Module Conducted RF Receiving Sensitivity

Band	Primary	Diversity	3GPP (SIMO)
WCDMA B1	TBD	TBD	-106.7dBm
WCDMA B2	TBD	TBD	-104.7dBm
WCDMA B4	TBD	TBD	-106.7dBm
WCDMA B5	TBD	TBD	-104.7dBm
WCDMA B8	TBD	TBD	-103.7dBm
LTE B1(10MHz)	TBD	TBD	-97.0dBm
LTE B2(10MHz)	TBD	TBD	-95.0dBm
LTE B3(10MHz)	TBD	TBD	-94.0dBm
LTE B4(10MHz)	TBD	TBD	-97.0dBm
LTE B5(10MHz)	TBD	TBD	-95.0dBm
LTE B7(10MHz)	TBD	TBD	-95.0dBm
LTE B8(10MHz)	TBD	TBD	-94.0dBm
LTE B12(10MHz)	TBD	TBD	-94.0dBm
LTE B13(10MHz)	TBD	TBD	-94.0dBm
LTE B14(10MHz)	TBD	TBD	-94.0dBm
LTE B20(10MHz)	TBD	TBD	-94.0dBm
LTE B25(10MHz)	TBD	TBD	-93.5dBm
LTE B26(10MHz)	TBD	TBD	-94.5dBm
LTE B28(10MHz)	TBD	TBD	-95.5dBm
LTE B30(10MHz)	TBD	TBD	-96.0dBm
LTE B38(10MHz)	TBD	TBD	-97.0dBm
LTE B39(10MHz)	TBD	TBD	-97.0dBm

LTE B40(10MHz)	TBD	TBD	-97.0dBm
LTE B41(10MHz)	TBD	TBD	-95.0dBm
LTE B48(10MHz)	TBD	TBD	-96.0dBm
LTE B66(10MHz)	TBD	TBD	-96.5dBm
LTE B71(10MHz)	TBD	TBD	-94.2dBm
5GNR n2(20MHz)(SCS:15KHz)	TBD	TBD	-91.8dBm
5GNR n5(20MHz)(SCS:15KHz)	TBD	TBD	-86.8dBm
5GNR n14(10MHz)(SCS:15KHz)	TBD	TBD	-93.8dBm
5GNR n25(20MHz)(SCS:15KHz)	TBD	TBD	-90.3dBm
5GNR n28(20MHz)(SCS:15KHz)	TBD	TBD	-90.8dBm
5GNR n30(10MHz)(SCS:15KHz)	TBD	TBD	-95.8dBm
5GNR n41(20MHz)(SCS:30KHz)	TBD	TBD	-92.0dBm
5GNR n48(20MHz)(SCS:30KHz)	TBD	TBD	-92.9dBm
5GNR n66(20MHz)(SCS:15KHz)	TBD	TBD	-93.3dBm
5GNR n71(20MHz)(SCS:15KHz)	TBD	TBD	-86.0dBm
5GNR n77(20MHz)(SCS:30KHz)	TBD	TBD	-92.4dBm
5GNR n78(20MHz)(SCS:30KHz)	TBD	TBD	-92.9dBm

6

Mechanical Dimensions

Mechanical Dimensions of Module
Design Effect Drawings of the Module

Mechanical Dimensions of Module

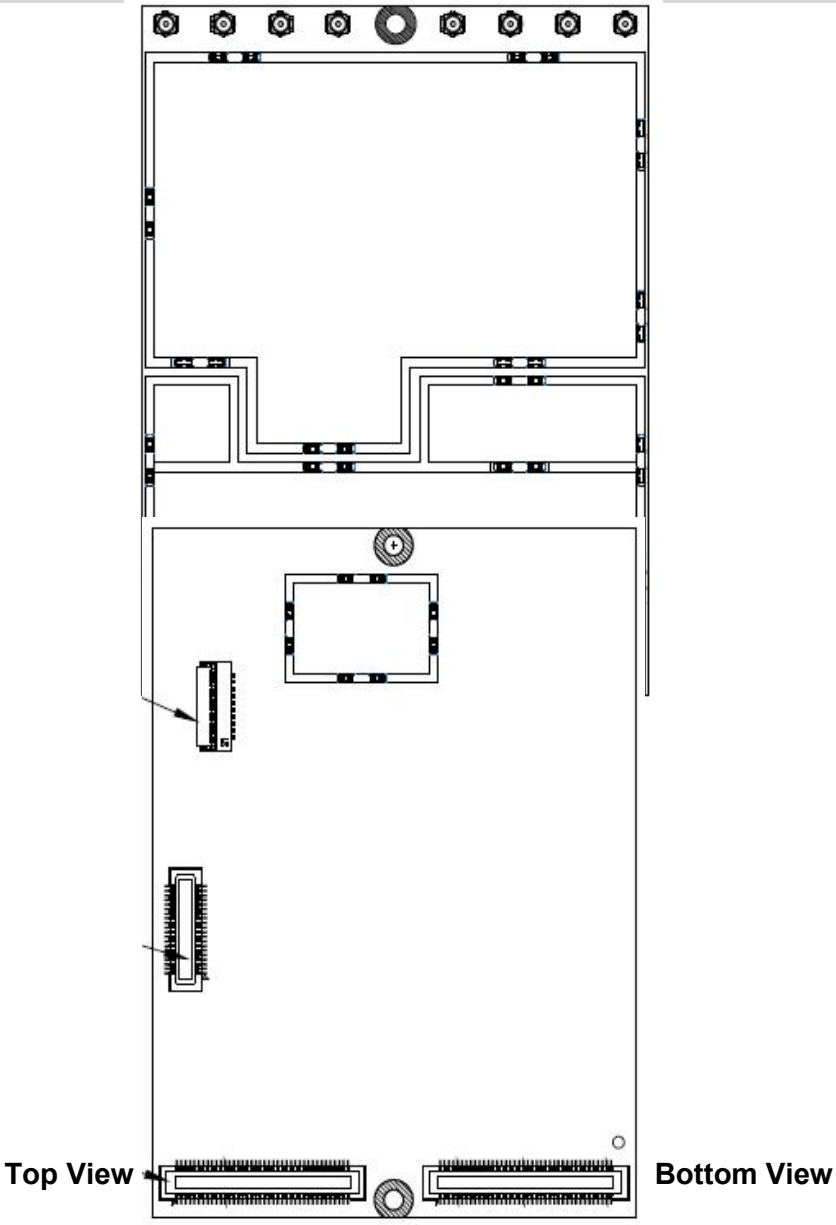
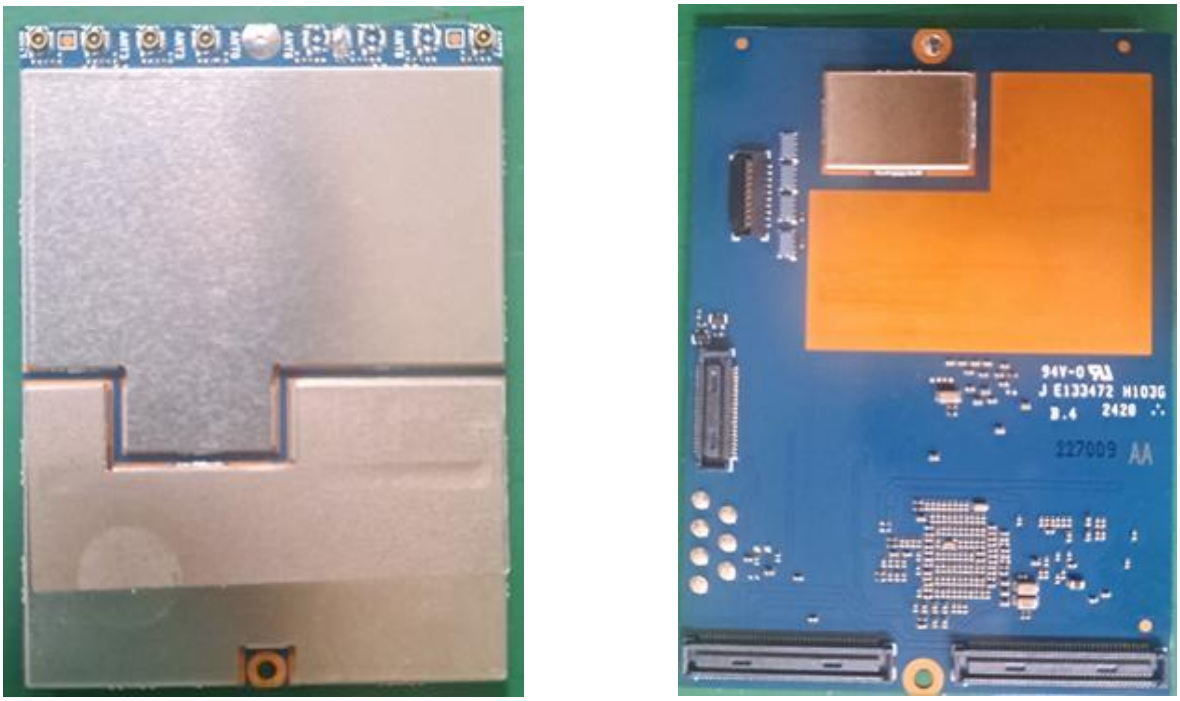


Figure 9. Module Top and Bottom Dimensions

Design Effect Drawings of the Module



Top View

Bottom View

Figure 10. Top & Bottom View of the Module

7

Regulatory Information

Regulatory Statements

Regulatory Statements

FCC Equipment Authorization ID: XHG-M3100

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
   The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

List of applicable FCC rules

This module has been tested for compliance to FCC Part 15
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Summarize the specific operational use conditions

The module is tested for standalone mobile RF exposure use condition. Any other usage conditions such as co-location with other transmitter(s) or being used in a portable condition will need a separate reassessment through a class II permissive change application or new certification.

RF exposure considerations

This equipment complies with FCC mobile radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

Antennas

The following antennas have been certified for use with this module; antennas of the same type with equal or lower gain may also be used with this module. The antenna must be installed such that 20 cm can be maintained between the antenna and users.

Antenna Type(PIFA)	WCDMA B2 0.51dBi; WCDMA B4 -0.71dBi; WCDMA B5 0.89dBi; LTE B2(25) 1.15dBi; LTE B4(66) 1.39dBi; LTE B5(26) 0.89dBi; LTE B7 4.03dBi; LTE B12 4.06dBi; LTE B13 0.19dBi; LTE B14 0.74dBi; LTE B30 2.45dBi; LTE B38 3.4dBi; LTE B40 2.85dBi; LTE B41 4.03dBi; LTE B48 1.21dBi; LTE B71 3.38dBi; 5G NR n2(25) 1.15dBi; 5G NR n5 0.89dBi; 5G NR n14 0.74dBi; 5G NR n30 2.45dBi; 5G NR n41 4.03dBi; 5G NR n48 1.21dBi; 5G NR n66 1.39dBi; 5G NR n71 3.38dBi; 5G NR n77 2.77dBi; 5G NR n78 2.77dBi;
Antenna connector	INTENNA
Antenna Manufacturer	SUNNYWAY

Label and compliance information
The final end product must be labeled in a visible area with the following: “Contains FCC ID: XHG-M3100”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

Information on test modes and additional testing requirements
This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) or portable use will require a separate class II permissive change re-evaluation or new certification.

Additional testing, Part 15 Subpart B disclaimer
This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rule requirements if applicable.
As long as all conditions above are met, further transmitter test will not be required.
However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE:
In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User
The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual

OEM/Host manufacturer responsibilities
OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and EMF essential requirements of the FCC rules. This module must not be incorporated into any other device or system without retesting for compliance as multi-radio and combined equipment