5G Module, M2500

User Manual

Contents

1

Introduction

Introduction

This document defines the M2500 module and describes its air interface and hardware interface which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of M2500 module. Associated with application note and user guide, customers can use M2500 module to design and set up mobile applications easily.

2

Product Concept

General Description
Key Features
Functional Diagram

General Description

M2500 module is a 5G/LTE-FDD/LTE-TDD/WCDMA wireless communication module with receive diversity, which provides data connectivity on 5G (sub-6 GHz), LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, and WCDMA networks.

Customers can choose a dedicated type based on the region or operator. The following table shows the frequency bands of M2500 module.

Table 1. Frequency Bands of M2500 Module

Mode	Band
5G (Sub-6)	n25/n41/n48/n66/n71/n77
LTE-FDD	B2/B4/B5/B12/B25/B26/B66/B71
LTE-TDD	B41/B48
WCDMA	B2/B4/B5
GNSS[1)]	GPS/GLONASS

NOTE
1)GNSS function is optional.

Key Features

The following table describes the detailed features of M2500 module.

Table 2.Key Features of M2500 Module

Feature	Details
Power Supply	Supply voltage : 3.6V ~ 4.2V Typical supply voltage : 3.8V
Transmit Power	Class 3 for WCDMA bands Class 3 for LTE bands Class 2 for LTE B41 band Class 3 for 5GNR bands Class 2 for 5GNR n77 band

5GNR Features	Support Rel16 5G NR Support sub6 SA and NSA operation mode Support 256 QAM uplink/downlink in sub6 GHz Support downlink 4x4 MIMO
LTE Features	Support up to CA Cat 19 FDD and TDD Support uplink QPSK , 16-QAM and 64-QAM modulation Support downlink QPSK, 16-QAM, 64-QAM, 256-QAM modulation Support 1.4MHz to 20MHz (5×CA) RF bandwidth Support 4x4MIMO in DL direction
WCDMA Features	Support 3GPP R9 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA Support QPSK, 16-QAM and 64-QAM modulation
USB Interface	One : HS USB 2.0 or SS USB 3.1 Gen2
UART Interface	four instances (each 4-bit wide) up to 4 MHz
PCIe Interface	One: Gen 3, 2 lanes; or Gen 4, 1 lane
Antenna interfaces	Including main antenna(ANT0), Rx-diversity antenna (ANT2), MIMO PRx antenna(ANT1), MIMO DRx antenna(ANT3)andUHB main antenna (ANT4)
Physical Characteristics	Size : 40.0mm x 60.0mm x 3.0mm Weight : TBD
Temperature Range	Operation temperature range: -30°C ~ +75°C Storage temperature range: -40°C~ +95°C

Functional Diagram

The following figure shows a block diagram of M2500 and illustrates the major functional parts

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interfaces

Figure 1. Functional Diagram

3

Application Interface

General Description
Pin Assignment
Pin Description
Operating Modes
Power Supply
Power on/off Scenarios
Reset the Module
UIM Interface
USB Interface

General Description

M2500 module is equipped with (86-pin x 2) BtoB connector that can be connected to cellular application platform.
Sub-interfaces included in these pins are described in detail in the following chapters:

- Power supply
- USIM interface
- USB 2.0/3.1 interface
- UART interface
- I2C interface
- SPI interface
- PCIe 3.0 interface
- PCM interface
- Charger IC control interface
- THERM interface
- GPIO's control interface

Pin Assignment

The following figure shows the pin assignment of M2500 module

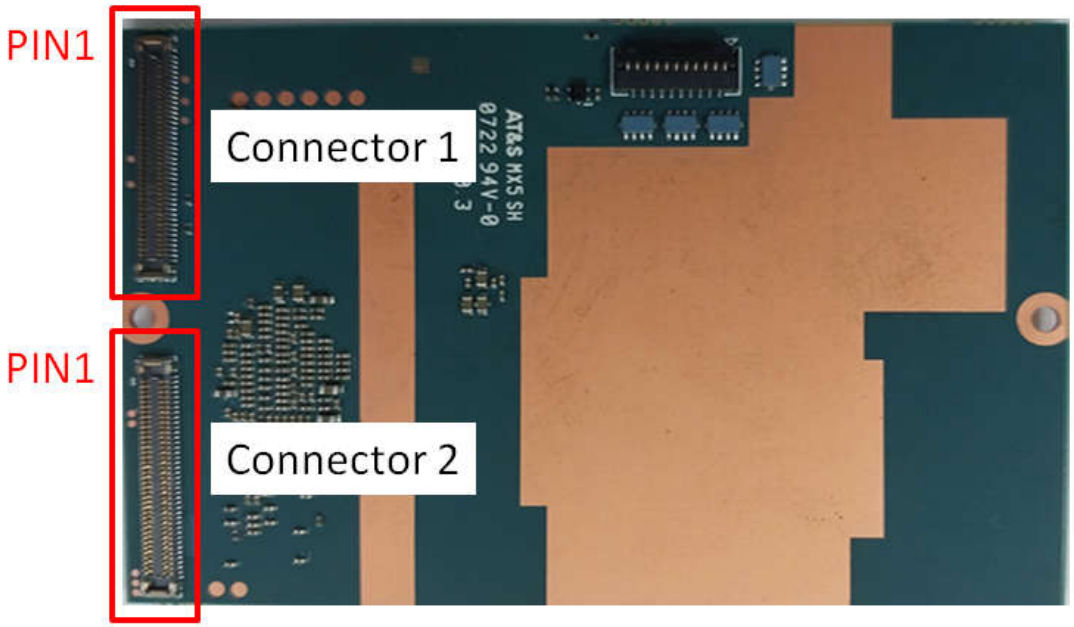

Figure 2. Pin Assignment (Bottom View)

B to B connector 1				B to B connector 2			
Pin name	Pin No.		Pin name	Pin name	Pin No.		Pin name
GND	1	2	GND	GND	1	2	GND
VREG_S7_0P95	3	4	VREG_S7_0P95	USB_SS_TX_P	3	4	SDX_PCIE_REFCLK_P
VREG_S7_0P95	5	6	VREG_S7_0P95	USB_SS_TX_M	5	6	SDX_PCIE_REFCLK_M
VREG_S4_1P9	7	8	VREG_S4_1P9	GND	7	8	GND
VREG_S4_1P9	9	10	VREG_S4_1P9	USB_SS_RX_P	9	10	SWITCH_PCIE0_US_RX0_P
VPH_PWR	11	12	VPH_PWR	USB_SS_RX_M	11	12	SWITCH_PCIE0_US_RX0_M
VPH_PWR	13	14	VPH_PWR	GND	13	14	GND
VPH_PWR	15	16	VPH_PWR	USB_HS_DP	15	16	SWITCH_PCIE1_US_RX1_P
VPH_PWR	17	18	VPH_PWR	USB_HS_DM	17	18	SWITCH_PCIE1_US_RX1_M
VPH_PWR	19	20	VPH_PWR	SDX_UIM2_DETECT	19	20	GND
VPH_PWR	21	22	VPH_PWR	SDX_UIM2_DATA	21	22	SDX_PCIE0_US_RX0_P
VREG_L6_1P8	23	24	VREG_L6_1P8	SDX_UIM2_CLK	23	24	SDX_PCIE0_US_RX0_M
VREG_L6_1P8	25	26	VREG_L6_1P8	SDX_UIM2_RESET_N	25	26	GND
VREG_L11_1P8	27	28	VREG_L11_1P8	SPI_MOSI	27	28	SDX_PCIE1_US_RX1_P
VREG_L13_1P8	29	30	VREG_L13_1P8	SPI_MISO	29	30	SDX_PCIE1_US_RX1_M
VREG_L10_3P1	31	32	VREG_L10_3P1	SPI_CLK	31	32	GND
VREG_S2_1P3	33	34	VREG_S2_1P3	SPI_CS_N	33	34	SDX_UIM1_RESET_N
VREG_S2_1P3	35	36	VREG_S2_1P3	DBG_UART_TX	35	36	SDX_UIM1_CLK
GND	37	38	GND	DBG_UART_RX	37	38	SDX_UIM1_DATA
KPD_PWR_N	39	40	WLAN_EN	GND	39	40	SDX_UIM1_DETECT
PWR_KEY_DET	41	42	PCIE_WLAN_WAKE2_N	I2C_SDA	41	42	I2C_SCL_MIRB
CABLE_PWR_N	43	44	WL_PA_MUTING	I2C_SCL	43	44	I2C_SDA_MIRB
GPIO_62	45	46	SDX_TO_WL_CTI	PCM_SYNC	45	46	PM_FAULT_N
RESIN_N	47	48	WL_TO_SDX_CTI	PCM_DIN	47	48	GPIO_100
USB_VBUS	49	50	DNI	PCM_DOUT	49	50	I2C_SDA
GND	51	52	GND	PCM_CLK	51	52	I2C_SCL
BATT_ID	53	54	SLIC_INT_N	SDC_CMD	53	54	VREG_1P8_SYS
FORCED_USB_BOOT	55	56	SLIC_RESET_N	SDC_CLK	55	56	VBUS_DET
FAST_BOOT	57	58	ANT_SEL0	SDC_DATA_0	57	58	GPIO_63
CHG_INT_N	59	60	ANT_SEL1	SDC_DATA_1	59	60	FACTORY_RESIN_N
CHG_INOK_B	61	62	DIV_ANT_SEL0	SDC_DATA_2	61	62	SDX_COEX_UART_TX
CHG_SHUT_DOWN	63	64	DIV_ANT_SEL1	SDC_DATA_3	63	64	SDX_COEX_UART_RX
PWR_BAT_LED	65	66	WL_SW_CTRL	SDC1_PWR_EN	65	66	AMBIENT_THERM
BUTTON_LEFT	67	68	GND	SDC1_DET	67	68	SKIN_THERM1
BUTTON_MENU	69	70	NTN_PWR_EN	ZIG_SDX_ISP_ENT	69	70	SKIN_THERM2
BUTTON_RIGHT	71	72	SGMII_VREG_PX_EN	ZIG_SDX_ISP_TX	71	72	SLEEP_CLK
SPMI_CLK	73	74	PCIE_SDX_CLKREQA_N	ZIG_SDX_ISP_RX	73	74	GND
SPMI_DATA	75	76	NTN_PCIE_A_RESET_N	ZIG_SDX_RSTIN	75	76	RF_CLK3
GND	77	78	GND	GND	77	78	GND

Pin Description

The following tables show the pin definition and description of M2500 module.

Table 3 : I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
OD	Open Drain
PI	Power Input
PO	Power Output

Table 4 : Pin Description

Connector 1			
Pin Name	**Pin No.**	**I/O**	**Description**
VREG_S7_0P95	3 ~ 6	PO	S7 SMPS switch node
VREG_S4_1P9	7 ~ 10	PO	S4 SMPS switch node
VPH_PWR	11~ 22	PI	Main power input
VREG_L6_1P8	23 ~ 26	PO	L6 LDO regulated output
VREG_L11_1P8	27, 28	PO	L11 LDO regulated output
VREG_L13_1P8	29. 30	PO	L13 LDO regulated output
VREG_L10_3P1	31, 32	PO	L10 LDO regulated output
VREG_S2_1P3	33 ~ 36	PO	S2 SMPS switch node
GND	1, 2, 37, 38, 51, 52, 68, 77, 78		Ground
KPD_PWR_N	39	DI	Module PWR ON key (low active)
PWR_KEY_DET	41	IO	Configurable I/O
CABLE_PWR_N	43	IO	PM7250B Charger_SYS_OK__N
GPIO_62	45	IO	Configurable I/O
RESIN_N	47	DI	AP HW reset

USB_VBUS	49	PI	USB_VBUS TP
BATT_ID	53	IO	BATT_ID
FORCED_USB_BOOT	55	IO	FORCED_USB_BOOT
FAST_BOOT	57	IO	Configurable I/O
CHG_INT_N	59	IO	Configurable I/O
CHG_INOK_B	61	IO	Configurable I/O
CHG_SHUT_DOWN	63	IO	Configurable I/O
PWR_BAT_LED	65	IO	Configurable I/O
BUTTON_LEFT	67	IO	Configurable I/O
BUTTON_MENU	69	IO	Configurable I/O
BUTTON_RIGHT	71	IO	Configurable I/O
SPMI_CLK	73	DI,DO	SPMI interface
SPMI_DATA	75	DI,DO	SPMI interface
DNI	40	IO	Configurable I/O
DNI	42	IO	Configurable I/O
DNI	44	IO	Configurable I/O
DNI	46	IO	Configurable I/O
DNI	48	IO	Configurable I/O
DNI	50	IO	Configurable I/O
SLIC_INT_N	54	IO	Configurable I/O
SLIC_RESET_N	56	IO	Configurable I/O
ANT_SEL0	58	IO	RF front end interface data
ANT_SEL1	60	IO	RF front end interface data
DIV_ANT_SEL0	62	IO	RF front end interface data
DIV_ANT_SEL1	64	IO	RF front end interface data
DNI	66	IO	Configurable I/O
NTN_PWR_EN	70	IO	Configurable I/O
SGMII_VREG_PX_EN	72	IO	Generic RF controller bit
PCIE_SDX_CLKREQA_N	74	IO	PCIe clock request
NTN_PCIE_A_RESET_N	76	IO	PCIe reset

Connector 2			
Pin Name	**Pin No.**	**I/O**	**Description**
USB_SS_TX_P	3	AO	USB super-speed transmit – plus
USB_SS_TX_M	5	AO	USB super-speed transmit – minus
USB_SS_RX_P	9	AI	USB super-speed receive – plus

USB_SS_RX_M	11	AI	USB super-speed receive – minus
USB_HS_DP	15	AI, AO	USB high-speed data – positive
USB_HS_DM	17	AI, AO	USB high-speed data – negative
SDX_UIM2_DETECT	19	IO	UIM2 presence detection
SDX_UIM2_DATA	21	IO	UIM2 data
SDX_UIM2_CLK	23	IO	UIM2 CLK
SDX_UIM2_RESET_N	25	IO	UIM2 reset
SPI_MOSI	27	IO	BLSP SPI master out, slave in
SPI_MISO	29	IO	BLSP SPI master in, slave out
SPI_CLK	31	IO	BLSP SPI clock
SPI_CS_N	33	IO	BLSP SPI chip select
DBG_UART_TX	35	IO	BLSP UART transmit data
DBG_UART_RX	37	IO	BLSP UART receive data
I2C_SDA	41	IO	BLSP I2C data
I2C_SCL	43	IO	BLSP I2C clock
PCM_SYNC	45	IO	Primary audio interface MI2S word select
PCM_DIN	47	IO	Primary audio interface MI2S data
PCM_DOUT	49	IO	Primary audio interface MI2S data
PCM_CLK	51	IO	Primary audio interface MI2S clock
SDC_CMD	53	IO	Secure digital controller 1 command
SDC_CLK	55	IO	Secure digital controller 1 clock
SDC_DATA_0	57	IO	Secure digital controller 1 data bit 0
SDC_DATA_1	59	IO	Secure digital controller 1 data bit 1
SDC_DATA_2	61	IO	Secure digital controller 1 data bit 2
SDC_DATA_3	63	IO	Secure digital controller 1 data bit 3
SDC1_PWR_EN	65	IO	Configurable I/O
SDC1_DET	67	IO	Configurable I/O
ZIG_SDX_ISP_ENT	69	IO	Configurable I/O
ZIG_SDX_ISP_TX	71	IO	Configurable I/O
ZIG_SDX_ISP_RX	73	IO	Configurable I/O
ZIG_SDX_RSTIN	75	IO	Configurable I/O
SDX_PCIE_REFCLK_P	4	AI, AO	PCIe Gen 3/4 reference clock – plus
SDX_PCIE_REFCLK_M	6	AI, AO	PCIe Gen 3/4 reference clock – minus
SWITCH_PCIE0_US_RX0_P	10	AO	PCIe Gen 3/4 transmit – plus
SWITCH_PCIE0_US_RX0_M	12	AO	PCIe Gen 3/4 transmit – minus
SWITCH_PCIE1_US_RX1_P	16	AO	PCIe Gen 3 transmit – plus

SWITCH_PCIE1_US_RX1_M	18	AO	PCIe Gen 3 transmit – minus
SDX_PCIE0_US_RX0_P	22	AI	PCIe Gen 3/4 receive – plus
SDX_PCIE0_US_RX0_M	24	AI	PCIe Gen 3/4 receive – minus
SDX_PCIE1_US_RX1_P	28	AI	PCIe Gen 3 receive – plus
SDX_PCIE1_US_RX1_M	30	AI	PCIe Gen 3 receive – minus
SDX_UIM1_RESET_N	34	IO	UIM1 reset
SDX_UIM1_CLK	36	IO	UIM1 clock
SDX_UIM1_DATA	38	IO	UIM1 data
SDX_UIM1_DETECT	40	IO	UIM1 presence detection
I2C_SCL_MIRB	42	IO	Configurable I/O
I2C_SDA_MIRB	44	IO	Configurable I/O
PM_FAULT_N	46	DI, DO	PMIC fault signal that initiates shutdown
GPIO_100	48	IO	Configurable I/O
I2C_SDA	50	IO	Configurable I/O
I2C_SCL	52	IO	Configurable I/O
VREG_1P8_SYS	54	PI	System 1.8 V I/O output
VBUS_DET	56	DI	USB VBUS detection
GPIO_63	58	IO	Configurable I/O
FACTORY_RESIN_N	60	IO	Configurable I/O
SDX_COEX_UART_TX	62	IO	Configurable I/O
SDX_COEX_UART_RX	64	IO	Configurable I/O
AMBIENT_THERM	66	AI	Analog multiplexer (AMUX) input 4
SKIN_THERM1	68	AI	Analog multiplexer (AMUX) input 6
SKIN_THERM2	70	IO	Configurable I/O
SLEEP_CLK	72	DI	Sleep clock
RF_CLK3	76	AI, AO	76.8 MHz RF clock
GND	1, 2, 7, 8, 13, 14, 20, 26, 32, 39, 74, 77, 78		Ground

Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 5 :Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Airplane Mode	In this mode, RF function will be invalid and Application Processor sleep state.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interfaces are not accessible.	

- Airplane mode

When the module enters into airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following ways.

Software(TBD)

AT+CFUN command provides the choice of the functionality level through setting <fun> into 0, 1 or 4.

AT+CFUN=0: Minimum functionality mode; both (U)SIM and RF functions are disabled.

AT+CFUN=1: Full functionality mode (by default).

AT+CFUN=4: Airplane mode. RF function is disabled.

Power Supply

- Power supply pins

M2500 provides eleven VPH_PWR pins dedicated to connect with the external power supply.

The following table shows the details of VBAT pins and ground pins

Table 6 : VPH_PWR and GND Pins

Pin name	Pin No. (CON 1)	Description	Min	Typ	Max	Unit
VPH_PWR	11~ 22	Power supply for module's main power	3.3	3.8	4.2	V
GND	1, 2, 37, 38, 51, 52, 68, 77, 78	Ground	-	0	-	

- Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure the input voltage will neverdrop below 3.3V. The following figure shows the voltage drop during Tx power in 3G,4G and 5G networks.

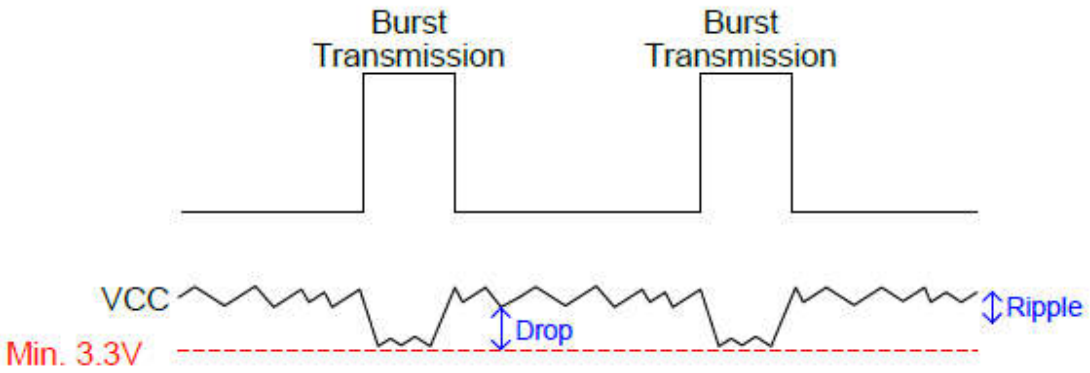

Figure 3: Power Supply Limits during Tx Power

- Reference Design for Power Supply

: TBD

PCIe Interface

M2500 includes one PCIe interface which are compliant with PCI Express Specification Revision3.0, 4.0. The key features of the PCIe interface are shown below:

- PCI Express Specification Revision 3.0& 4.0 compliance
- Data rate at 8Gbps per lane
- Can be used to connect to an external Ethernet IC (MAC and PHY) or WLAN IC.

Table 11: Pin Definition of the PCIe Interface

Pin Name	Pin No.	Description	DC Characteristics
SDX_PCIE_REFCLK_P	4	PCIe Gen 3/4 reference clock – plus	Compliant with PCIe Gen 3.0 & 4.0 standard specifications. Require differential impedance of 85Ω.
SDX_PCIE_REFCLK_M	6	PCIe Gen 3/4 reference clock – minus	
SWITCH_PCIE0_US_RX0_P	10	PCIe Gen 3/4 transmit – plus	
SWITCH_PCIE0_US_RX0_M	12	PCIe Gen 3/4 transmit – minus	
SWITCH_PCIE1_US_RX1_P	16	PCIe Gen 3 transmit – plus	
SWITCH_PCIE1_US_RX1_M	18	PCIe Gen 3 transmit – minus	
SDX_PCIE0_US_RX0_P	22	PCIe Gen 3/4 receive – plus	
SDX_PCIE0_US_RX0_M	24	PCIe Gen 3/4 receive – minus	
SDX_PCIE1_US_RX1_P	28	PCIe Gen 3 receive – plus	
SDX_PCIE1_US_RX1_M	30	PCIe Gen 3 receive – minus	
PCIE_WLAN_WAKE2_N	42	PCIe wake-up	
PCIE_SDX_CLKREQA_N	74	PCIe clock request	
NTN_PCIE_A_RESET_N	76	PCIe reset	

In order to enhance the reliability and availability in applications, please follow the criteria below in thePCIe interface circuit design:

A. Keep PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, and19.2MHz clock signals.
B. A capacitance should be added in series on Tx/Rx traces to remove any DC bias.
C. Keep the maximum trace length less than 300mm.
D. The length difference of Tx or Rx differential pairs should be less than 0.7mm for PCIe routing traces.
E. The differential impedance of PCIe data trace should be 85Ω±10%.
F. Separate the SS-USB data pairs (Tx, Rx) and PCIe data pairs (Tx, Rx) from each other as far aspossible. If SS_USB and PCIe data pairs must cross on adjacent layers, please keep crossings atright angles to minimize unbalanced (asymmetric) coupling.
G. PCIe data traces must not be routed under components or crossing other traces.

4

Antenna Interfaces

Antenna Connector Definition
Operating Frequency
Reference Design of RF Antenna Interface

Antenna Connector Definition

The pin definition of antennas interfaces are shown below.

Table 12. Connector Definition of the RF Antenna

Con. Name	Description	Comment
ANT0	Main antenna, support Tx and Rx	50Ωimpedance
ANT1	MIMO PRx antenna	50Ωimpedance
ANT2	DRx antenna, support MB Tx1	50Ωimpedance
ANT3	MIMO DRx antenna, support n41 Tx0	50Ωimpedance
ANT4	UHB main antenna, support Tx and Rx	50Ωimpedance
ANT5	GNSS antenna interface	50Ωimpedance

Operating Frequency

Table 13.Module Operating Frequency

Band	Transmit	Receive	Unit
WCDMA B2	1850~1910	1930~1990	MHz
WCDMA B4	1710~1755	2110~2155	MHz
WCDMA B5	824~849	869~894	MHz
LTE B2	1850~1910	1930~1990	MHz
LTE B4	1710~1755	2110~2155	MHz
LTE B5	824~849	869~894	MHz
LTE B12	699~716	729~746	MHz
LTE B25	1850~1915	1930~1995	MHz
LTE B26	814~849	859~984	MHz
LTE B41	2496~2690	2496~2690	MHz
LTE B48	3550~3700	3550~3700	MHz
LTE B66	1710~1780	2110~2200	MHz
LTE B71	663~698	617~652	MHz
5GNR n25	1850~1915	1930~1995	MHz
5GNR n41	2496~2690	2496~2690	MHz
5GNR n48	3550~3700	3550~3700	MHz
5GNR n66	1710~1780	2110~2200	MHz
5GNR n71	663~698	617~652	MHz
5GNR n77	3450~3550, 3700~3980	3450~3550, 3700~3980	MHz

5

Electrical, Reliability and Radio Characteristics

Absolute Maximum Ratings
Operation and Storage Temperatures
RF Receiving Sensitivity

Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 14: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VPH_PWR	TBD	TBD	V
Peak Current of VPH_PWR	TBD	TBD	A
Voltage at Digital Pins	TBD	TBD	V
Voltage at ADC	TBD	TBD	V

Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 15.Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range	-30	+25	+75	°C
Storage Temperature Range	-40		+95	°C

RF Receiving Sensitivity

The following tables show conducted RF receiving sensitivity of M2500 module.

Table 16. M2500 Module Conducted RF Receiving Sensitivity

Band	Primary	Diversity	3GPP (SIMO)
WCDMA B2	TBD	TBD	-104.7dBm
WCDMA B4	TBD	TBD	-106.7dBm
WCDMA B5	TBD	TBD	-104.7dBm
LTE B2(10MHz)	TBD	TBD	-95.0dBm
LTE B4(10MHz)	TBD	TBD	-97.0dBm
LTE B5(10MHz)	TBD	TBD	-95.0dBm
LTE B12(10MHz)	TBD	TBD	-94.0dBm
LTE B25(10MHz)	TBD	TBD	-93.5dBm
LTE B26(10MHz)	TBD	TBD	-94.5dBm
LTE B41(10MHz)	TBD	TBD	-95.0dBm
LTE B48(10MHz)	TBD	TBD	-96.0dBm
LTE B66(10MHz)	TBD	TBD	-96.5dBm
LTE B71(10MHz)	TBD	TBD	-94.2dBm
5GNR n25(20MHz)(SCS:15KHz)	TBD	TBD	-90.3dBm
5GNR n41(20MHz)(SCS:30KHz)	TBD	TBD	-92.0dBm
5GNR n48(20MHz)(SCS:30KHz)	TBD	TBD	-92.9dBm
5GNR n66(20MHz)(SCS:15KHz)	TBD	TBD	-93.3dBm
5GNR n71(20MHz)(SCS:15KHz)	TBD	TBD	-86.0dBm
5GNR n77(20MHz)(SCS:30KHz)	TBD	TBD	-92.4dBm

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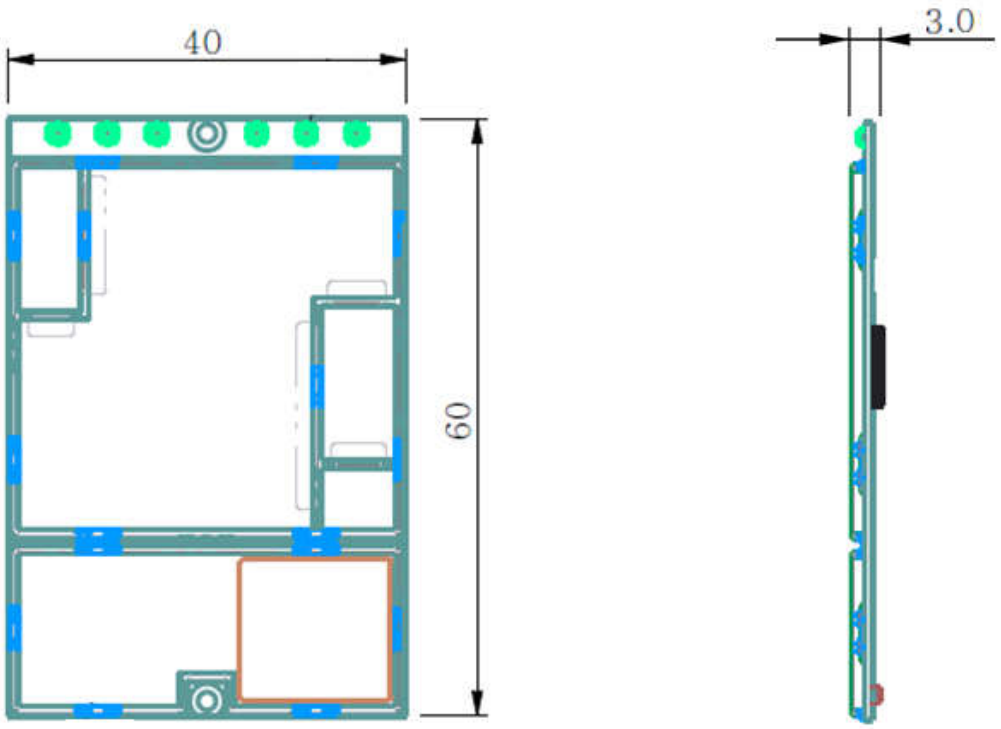
Mechanical Dimensions

Mechanical Dimensions of Module
Design Effect Drawings of the Module
Antenna Trace Layout

Mechanical Dimensions of Module



Top View **Side View**

Figure 9. Module Top and Side Dimensions

Design Effect Drawings of the Module

Figure 10. Top View of the Module

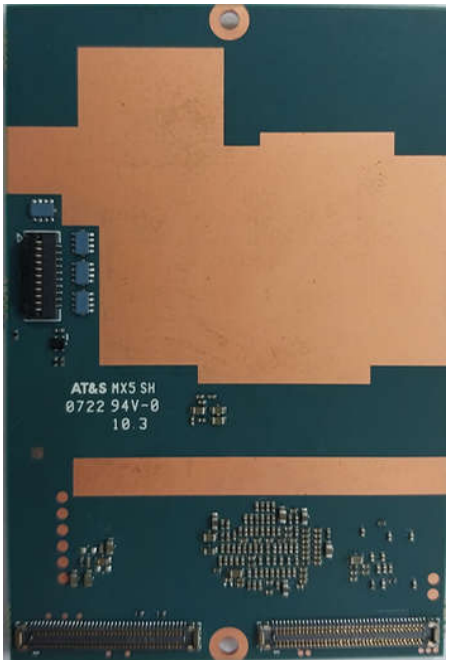


Figure 11.Bottom View of the Module

Antenna Trace Layout

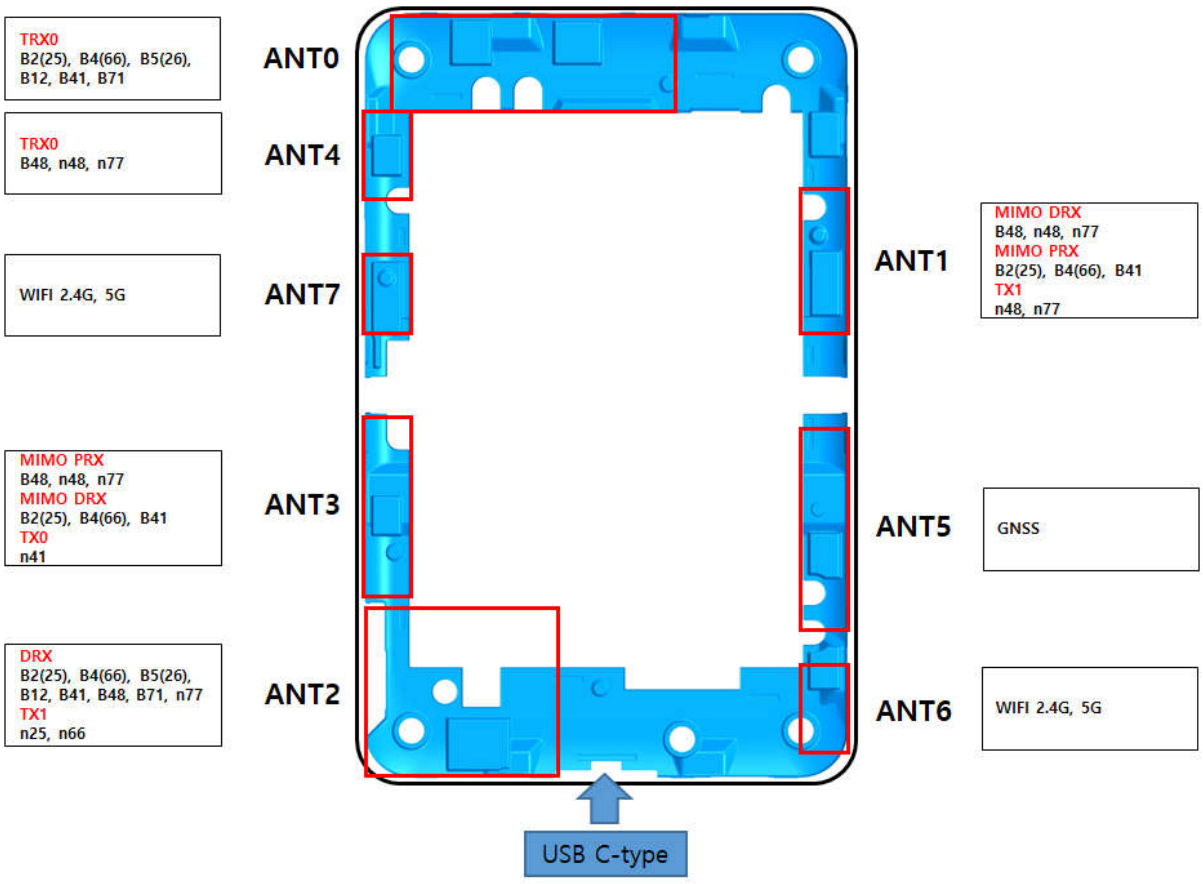


Figure 12.Antenna Trace Layout

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Regulatory Information

Regulatory Statements

Regulatory Statements

FCC Equipment Authorization ID: XHG-M2500

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
   The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily removed. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XHG-M2500”
The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1)The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.
(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna Type	PIFA
Bands	Gain(dBi)
5G NR n25	-1.54
5G NR n41	-2.18
5G NR n48	-1.71
5G NR n66	-1.19
5G NR n71	-2.75
5G NR n77	-1.49

Antenna Type	PIFA
Bands	Gain(dBi)
WCDMA B2	-1.66
WCDMA B4	-1.56
WCDMA B5	-0.66
LTE B2(25)	-1.66
LTE B4(66)	-1.56
LTE B5(26)	-0.66
LTE B12	-1.43
LTE B41	-2.99
LTE B48	-1.71
LTE B71	-2.75

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User
The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules
This module has been tested and found to comply with part 22, part 24, part 27, part 90, and 96 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)
1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cmbetween the radiator & your body.