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1 Introduction

The **MB1.Q** PCB (**Media Board 1st Generation**) is a high-performance multimedia board mainly used in PX products.

This document holds the technical description concerning the **MB1.Q** PCB.

2 different assembly variants of the MB1 board are available:

1. Fully assembled
2. Only the radar part is assembled (for more details see the chapter 6 Variants)

1.1 Scope

The MB1 board implements the following main parts and functions:

- Multimedia 28pin
 - Main board power supply
 - MIPI CSI → 2x data channels + 1x clock channel
 - I2C
 - I2S
 - GPIOs
- Power Supply
 - 1x LDO
 - 1x DC/DC
- Optical Camera
 - Power supply (specific power-ON sequence)
 - MIPI CSI → 2x data channels + 1x clock channel
 - I2C
- I2C Switch
- Ambient Light Sensor
- Audio
 - 2x Speakers
 - 1x Digital microphone
- Radar
- 128 Kbit EEPROM
- User Interface
 - 1x Green LED
- uC
- SWD (programming interface for the uC)

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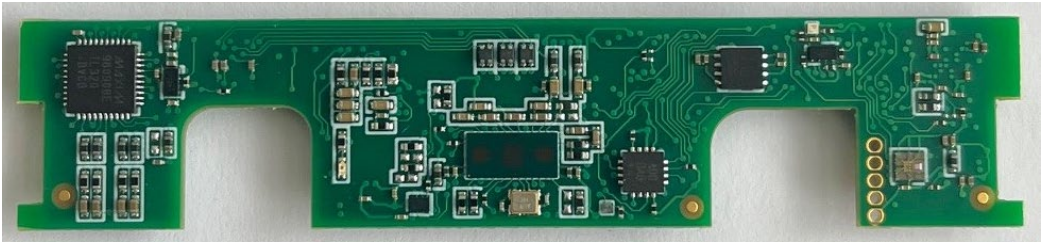
1.2 PCBA

1.2.1 PMB

MB1 Top



MB1 Bottom

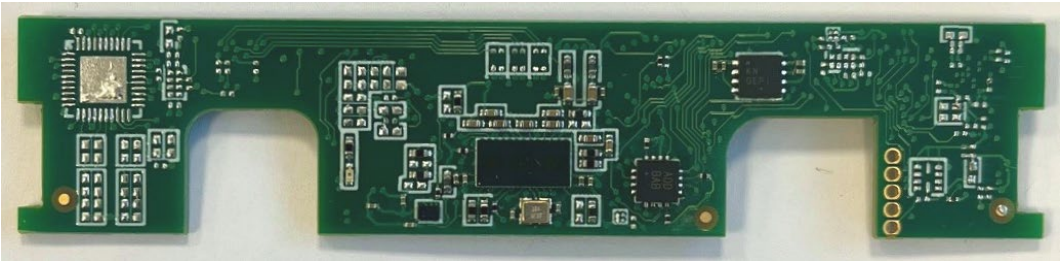


1.2.2 PMBL

MB11 Top



MB11 Bottom



1.3 Definitions, Acronyms and Abbreviations

	Description
I2C	Inter-Integrated Circuit
I2S	Integrated Interchip Sound
GPIO	General Purpose Input Output
SWD	Serial Wire Debug
LED	Light Emitting Diode
MMIC	Microwave Monolithic Integrated Circuits
VCO	Voltage Controlled Oscillator
PLL	Phase Locked Loop
RF	Radio Frequency
CSI	Camera Serial Interface
MIPI	Mobile Industry Processor Interface
CMOS	Complementary Metal-Oxide Semiconductor
EEPROM	Electrically Erasable Programmable Read-Only Memory
LDO	Low Drop Out
uC	Microcontroller
CPU	Central Processing Unit
FPU	Floating Point Unit
ART	Adaptive Real Time
DSP	Digital Signal Processing
MPU	Memory Protection Unit
ESD	Electrostatic Discharge
UV	Ultra-Violet
IR	Infra-Red
~	Low Active Signal

1.4 References

REF [1]	S50100040 (Schematics MB1.Q)
REF [2]	PORT 1 mini Optical Camera – Technical Specifications Q41910733
REF [3]	https://ams.com/
REF [4]	https://www.maximintegrated.com/
REF [5]	https://www.infineon.com/
REF [6]	http://www.st.com/

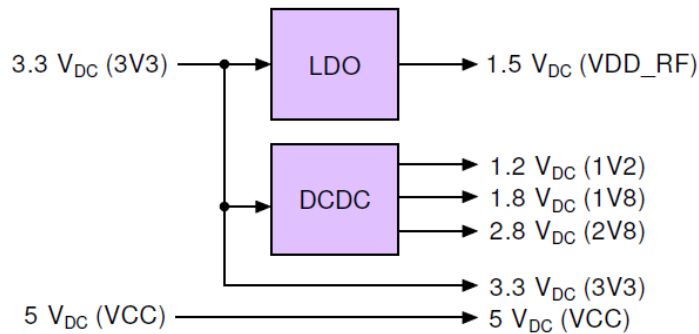
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2 General board implementation

2.1 Power supply

The MB1 main power supply is $+3.3 V_{DC} \pm 3\%$ and $+5 V_{DC} \pm 3\%$ and it comes directly from the Multimedia 28pin connector (see chapter 3.1 Multimedia 28pin).

On board the power supply is structured as follows:



The 1V8 power supply it is enabled with 14 ms delay (it is a request of the Optical Camera). This is implemented with the DCDC regulator MAX17270 (R+C delay on the enable pin of the 1V8).

The board power supplies are generated from the main power supply and are represented in the following table:

Board Power Supplies				
PWR In	PWR Out	I _{max} Out	Name	Regulator Typ.
3V3 3.3 V _{DC}	1.5 V _{DC}	300 mA	VDD_RF	LDO: NCV8164 Schindler Id. Nr. 561351
3V3 3.3 V _{DC}	1.2 V _{DC}	1.1 A	1V2	DCDC: MAX17270 Schindler Id. Nr. 561286
	1.8 V _{DC}	1.1 A	1V8	
	2.8 V _{DC}	0.6 A	2V8	

2.2 Reset

The board reset is controlled/managed directly from the host CPU connected to the Multimedia 28pin connector and the trigger point is the on board uC.

The reset of the following blocks is controlled/managed directly from the on board uC:

Block	Signal name	uC GPIO
Radar	uC_RADAR_RESET	PA1
Audio codec	AUDIO_RESET~	PC8

Note: The audio codec can be also reset through the I2C I/O Expander with the Output 6.

For more details regarding the connections and the signals see the REF [1] document and the chapter 3 Connectors.

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2.3 Optical Camera

The following Optical Camera is supported by the MB1 board:

Schindler Id. Nr.	Type	Main features	Note
59910733	See REF [2] 	- Image Sensor: Sony IMX219 - Resolution: 8 MP (3280 x 2464) - CMOS Size: 1/4 Inch - Aperture (F): 2.0 - Focal Length: 2.96 mm - FOV (View Angle): 77.6° - Distortion: < 1% - Focusing Range: 20 cm ~ Infinity - Interface: MIPI + I2C (control signals) - Dimensions - Lens: 6.50 x 6.50 x 4.9 mm - Module: 80 x 9 mm	REF [2]

The MIPI CSI interface is directly connected to the Multimedia 28pin connector. The control signals of the Optical Camera (I2C interface) are connected to the Multimedia 28pin connector through a voltage level translator (from 3.3 V_{DC} to 1.8 V_{DC}).

During the power-up of the Optical Camera the 1V8 power supply must be enabled ONLY when the 1V2 and the 2V8 power supplies are stable. A delay of 10 ms must be considered. This power-up sequence is done by the MAX17270 DC/DC regulator.

For more details regarding the connections and the signals see the REF [1] document and the chapter 3 Connectors.

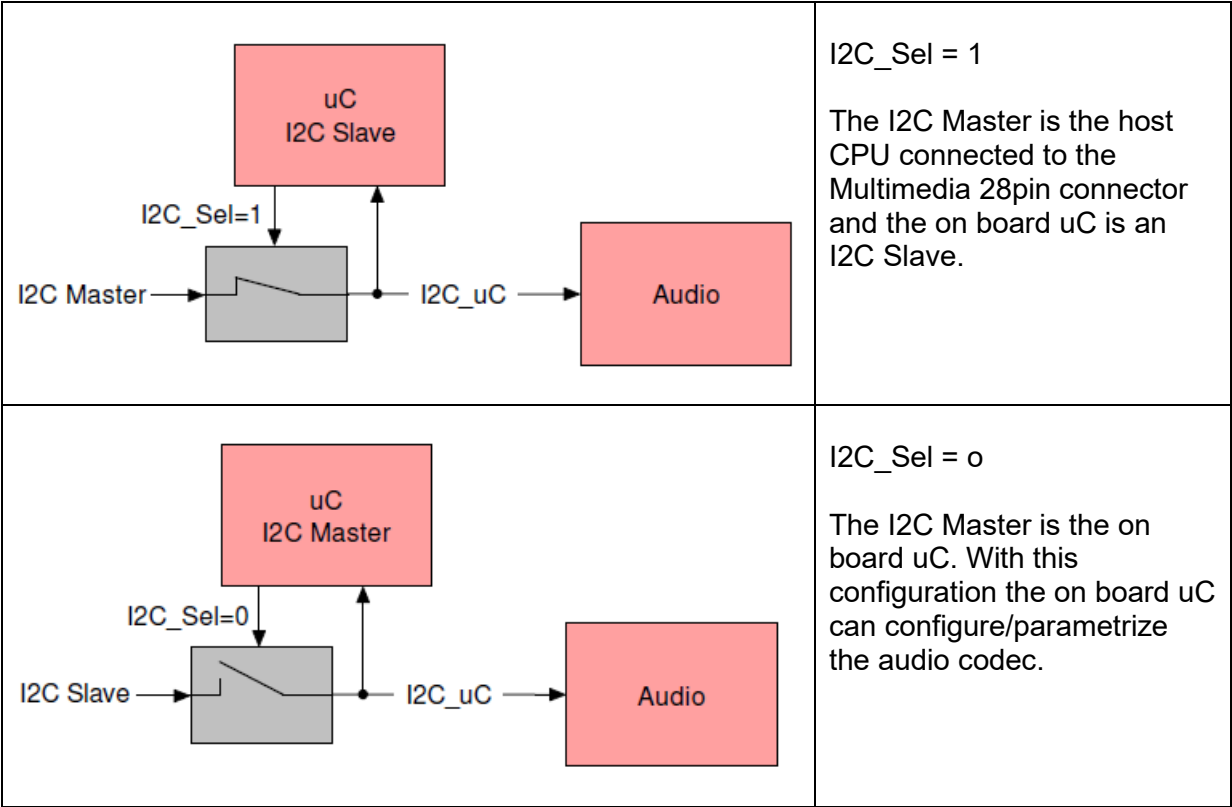
2.4 I2C Switch

A digital switch on the I2C lines is present on board. The switch is directly managed by the uC through the following pin:

Block	Signal name	uC GPIO
I2C Switch	I2C_SEL	PE7

The functionality of the I2C switch is represent in the table below:

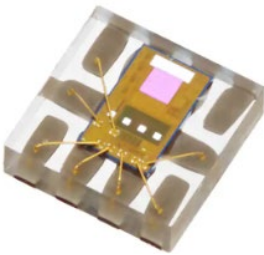
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For more details regarding the connections and the signals see the REF [1] document and the chapter 3 Connectors.

2.5 Ambient Light Sensor

The following Ambient Light Sensor is present on board:

Schindler Id. Nr.	Type	Main features	Note
561349	AMS <i>TSL2540</i> 	• very-high sensitivity light-to-digital converter • Single device integrated optical solution ○ 2.0mm x 2.0mm x 0.5mm ○ Power management features ○ I2C fast mode interface compatible • Accurate ambient light sensing ○ Photopic ambient light sense (ALS) ○ UV / IR blocking filter ○ Programmable gain and integration time • Power supply: 1.8 V • Case: 10-QFN, 2 x 2 mm	REF [3]

For more details regarding the connections and the signals see the REF [1] document and the chapter 3 Connectors.

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2.6 Audio

The audio block is composed as follow and is managed directly from the codec represented in the table below:

- 2x Speaker
- 1x Digital microphone

Schindler Id. Nr.	Type	Main features	Note
561387	MAXIM <i>MAX98090</i>	• 102 dB DR Stereo DAC to HP (8 kHz < F_s < 96 kHz) • 3.6 mW Stereo Playback Power Consumption • 99 dB DR Stereo ADC (8 kHz < F_s < 96 kHz) • 4.2 mW Stereo Record Power Consumption • Stereo PDM Digital Microphone Input • Master Clock Frequencies from 256 x F_s to 60 MHz • I2S/LJ/RJ/TDM Digital Audio Interface • FlexSound Technology Signal Processing • Stereo Low EMI Class D Speaker Amplifiers ○ 3.2 W/Channel (RL = 4 Ω, SPKR_VDD = 5 V) ○ 1.8 W/Channel (RL = 8 Ω, SPKL_VDD = 5 V) • Stereo DirectDrive Class H Headphone Amplifier Jack Detection and Identification • Differential Receiver Amplifier/Stereo Line Output • Extensive Click-and-Pop Reduction Circuitry • RF Immune Analog Inputs and Outputs • Programmable Microphone Bias • I2C Control Interface with Two Address Options • Case: 40-TQFN, 5 x 5 mm	REF [4]

The audio codec can be controlled through the on board uC or through the host CPU connected to the Multimedia 28pin connector. An additional interrupt line of the chip is connected to the on board uC as follow:

Block	Signal name	uC GPIO
Audio codec	AUDIO_IRQ~	PD1

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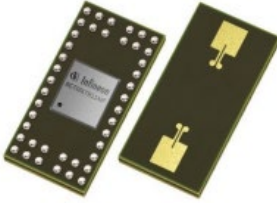
The audio codec can be reset is 2 different ways (more details in the chapter 2.3 Reset):

- Through the I2C I/O Expander
- Through the on board uC

For more details regarding the connections and the signals see the REF [1] document and the chapter 3 Connectors.

2.7 Radar

The following Radar is present on board:

Schindler Id. Nr.	Type	Main features	Note
561350	Infineon BGT60LTR11AIP 	• 60 GHz transceiver MMIC with one transmitter and one receiver unit • Antennas in package (AIP) 6.7 × 3.3 × 0.56 mm³ • Pulsed Doppler mode of operation for low power consumption • Autonomous mode ○ Integrated detector for motion and direction of movement ○ Direct output of motion detection signal ○ 15 configurable thresholds for target detection range ○ 16 configurations for detection status hold time ○ 4 configurable operating frequencies ○ 4 configurable pulse repetition rates • High performance enabled from Infineon's BiCMOS technology ○ Fully integrated low phase noise VCO and PLL ○ Medium power amplifier with configurable output power and integrated power detector ○ Low noise variable gain baseband amplifiers ○ Fully ESD protected device • Power supply: 1.5 V • Case: PG-UF2BGA-42 6.7 x 3.3 mm	REF [5]

For more details regarding the connections and the signals see the REF [1] document and the chapter 3 Connectors.

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2.8 EEPROM

The following EEPROM is present on board:

Schindler Id. Nr.	Type	Main features	Note
561260	ST Microelectronics <i>M24128-DFMC6TG</i>	- Compatible with all I2C bus modes: 1 MHz 400 kHz 100 kHz - Memory array: 128 Kbit (16 Kbyte) of EEPROM - Page size: 64 bytes - Additional Write lockable page (M24128-D order code) - Single supply voltage and high speed: 1 MHz clock from 1.7 V to 5.5 V - Write: - Byte Write within 5 ms - Page Write within 5 ms - Operating temperature range: - From -40 °C up to +85 °C - Random and sequential Read modes - Write protect of the whole memory array - Enhanced ESD/Latch-Up protection - More than 4 million Write cycles - More than 200-years data retention - Case: 8-UFDFPN, 2 x 3 mm	REF [6]

For more details regarding the connections and the signals see the REF [1] document and the chapter 3 Connectors.

2.9 User Interface

The user interface is composed from a single green LED connected directly to the I2C I/O Expander like the following table:

LED Color	Signal name	I2C I/O Expander GPIO
Green	STS_LED	Output 7

For more details regarding the connections and the signals see the REF [1] document and the chapter 3 Connectors.

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2.10 uC

The following uC is present on board:

Schindler Id. Nr.	Type	Main features	Note
561348	ST Microelectronics <i>STM32F446</i>	- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, ART accelerator, full set of DSP instructions and MPU - Op. Freq. up to 180 MHz - Internal memories 512 Kbytes of Flash memory 128 Kbytes of SRAM - Power supply: 3.3 V - Case: 81-WLCSP, 3.7 x 3.8 mm	REF [6]

Here below more in detail the uC characteristics:

System	Chrom-ART Accelerator™	
Power supply 1.2 V internal regulator POR/PDR/PVD	ART Accelerator™	
Xtal oscillators 32 kHz + 4 ~26 MHz	180 MHz Arm® Cortex®-M4 CPU	Connectivity
Internal RC oscillators 32 kHz + 16 MHz	Floating Point Unit (FPU)	4x SPI (3x with I²S)
PLL	Nested Vector Interrupt Controller (NVIC)	Camera interface
Clock control	JTAG/SW debug	4x I²C
RTC/AWU	Embedded Trace Macrocell (ETM)	2x CAN 2.0B
1x SysTick timer	Memory Protection Unit (MPU)	1x USB 2.0 OTG FS/HS
2x watchdogs (independent and window)	Multi-AHB bus matrix	1x USB 2.0 OTG FS
50/63/81/114 I/Os	16-channel DMA	1x SDMMC
Cyclic Redundancy Check (CRC)		4x USART + 2 UART LIN, smartcard, IrDA, modem control
96-bit unique ID		2x SAI (Serial Audio Interface)
Voltage scaling		HDMI CEC
		SPDIF input x4
Control	True random number generator (RNG)	Analog
2x 16-bit motor-control PWM synchronized AC timer	Up to 512-Kbyte Flash memory	2-channel 2x 12-bit DAC
10x 16-bit timers 2x 32-bit timers	128-Kbyte SRAM	Up to 3x 12-bit ADC 2.4 MSPS
	External memory interface W/SDRAM support	Up to 24 channels 7.2 MSPS
	80-byte + 4-Kbyte backup data	Temperature sensor
	512 OTP bytes	
	Dual Quad SPI	

For more details regarding the connections and the signals see the REF [1] document and the chapter 3 Connectors.

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3 Connectors

3.1 Multimedia 28pin

Connector Type: SMD FFC/FPC conn., 28 poles, 0.5 mm, Top Contact, Id. Nr. 561082
Silkscreen: -

Pin	Sig. Name	Max U	Tol.	Max I	Typ.	Description
1	EXT_RESET_uC	3.3 V _{DC}	±3%	5 mA	I	uC Reset
2	ALS_INT~	3.3 V _{DC}	±3%	5 mA	O	ALS Interrupt
3, 4, 14, 19, 22, 25, 28	GND	0 V _{DC}	-	-	PWR	Ground
5	MOTION_DET_uC	3.3 V _{DC}	±3%	5 mA	O	uC Motion Detection
6, 7	N. C.	-	-	-	-	Not connected
8	I2S_BCLK	3.3 V _{DC}	±3%	5 mA	I	I2S Bit Clock
9	I2S_DIN	3.3 V _{DC}	±3%	5 mA	I	I2S Data Input
10	I2S_DOUT	3.3 V _{DC}	±3%	5 mA	O	I2S Data Output
11	I2S_LRCLK	3.3 V _{DC}	±3%	5 mA	I	I2S Left Right Clock
12, 17	5V	5 V _{DC}	±3%	200 mA	PWR	Main power supply
13, 18	3V3	3.3 V _{DC}	±3%	200 mA	PWR	Main power supply
15	I2C_SDA	3.3 V _{DC}	±3%	5 mA	I/O	I2C Data
16	I2C_SCL	3.3 V _{DC}	±3%	5 mA	O	I2C Clock
20	MIPI_CSI_CLK_P	3.3 V _{DC}	±3%	5 mA	O	MIPI CSI CLK+
21	MIPI_CSI_CLK_N	3.3 V _{DC}	±3%	5 mA	O	MIPI CSI CLK-
23	MIPI_CSI_D1_P	3.3 V _{DC}	±3%	5 mA	O	MIPI CSI D1+
24	MIPI_CSI_D1_N	3.3 V _{DC}	±3%	5 mA	O	MIPI CSI D1-
26	MIPI_CSI_D0_P	3.3 V _{DC}	±3%	5 mA	O	MIPI CSI D0+
27	MIPI_CSI_D0_N	3.3 V _{DC}	±3%	5 mA	O	MIPI CSI D0-

3.2 Speaker

Connector Type: SMD 4 poles crimp conn., right angle, 1.20 mm, Id. Nr. 561354
Silkscreen: -

Pin	Sig. Name	Max U	Tol.	Max I	Typ.	Description
1	SPKR+	±5 V _{DC}	±5%	200 mA	-	Speaker Non Inverting Output Right channel
2	SPKR-				-	Speaker Inverting Output Right channel
3	SPKL+	±5 V _{DC}	±5%	200 mA	-	Speaker Non Inverting Output Left channel
4	SPKL-				-	Speaker Inverting Output Left channel

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3.3 Microphone

Connector Type: SMD FFC/FPC conn., 4 poles, 0.5 mm, Bottom Contact, Id. Nr. 561352
Silkscreen: -

Pin	Sig. Name	Max U	Tol.	Max I	Typ.	Description
1	1V8	1.8 V _{DC}	±3%	10 mA	PWR	Power supply
2	GND	0 V _{DC}	-	-	PWR	Ground
3	DIG_MIC_CLK	1.8 V _{DC}	±3%	5 mA	O	Digital microphone Clock
4	DIG_MIC_DATA	1.8 V _{DC}	±3%	5 mA	I	Digital microphone Data

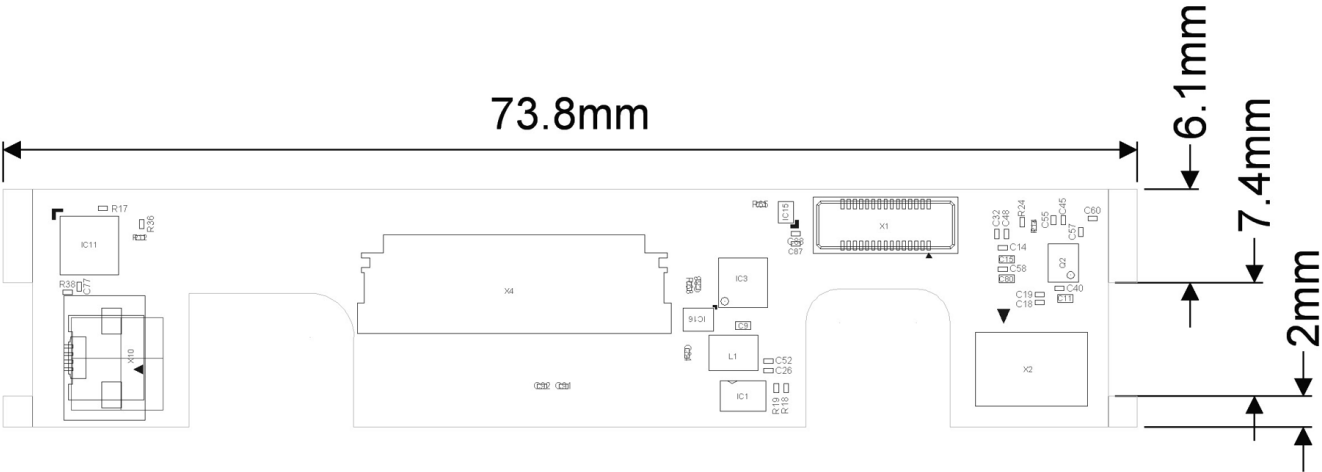
3.4 Optical Camera

Connector Type: SMD 2x15 poles HRS board conn., 0.4 mm, Id. Nr. 561287
Silkscreen: -

Pin	Sig. Name	Max U	Tol.	Max I	Typ.	Description
1, 2, 11, 13, 14, 17, 18	N. C.	-	-	-	-	Not connected
3, 5	1V8	1.8 V _{DC}	±3%	20 mA	PWR	Power supply Optical Camera
4	1V2	1.2 V _{DC}	±3%	20 mA	PWR	Power supply Optical Camera
6, 8, 9, 12, 15, 16, 19, 22, 25, 28	GND	0 V _{DC}	-	-	PWR	Ground
7	24M_CLK	3.3 V _{DC}	±3%	5 mA	O	24 MHz Clock
10	2V8	2.8 V _{DC}	±3%	20 mA	PWR	Power supply Optical Camera
20	MIPI_CSI_D1_N	3.3 V _{DC}	±3%	5 mA	I	MIPI CSI D1-
21	MIPI_CSI_D1_P	3.3 V _{DC}	±3%	5 mA	I	MIPI CSI D1+
23	MIPI_CSI_D0_N	3.3 V _{DC}	±3%	5 mA	I	MIPI CSI D0-
24	MIPI_CSI_D0_P	3.3 V _{DC}	±3%	5 mA	I	MIPI CSI D0+
26	MIPI_CSI_CLK_N	3.3 V _{DC}	±3%	5 mA	I	MIPI CSI CLK-
27	MIPI_CSI_CLK_P	3.3 V _{DC}	±3%	5 mA	I	MIPI CSI CLK+
29	I2C_SCL	1.8 V _{DC}	±3%	5 mA	O	I2C Clock. Voltage level 1.8 V _{DC}
30	I2C_SDA	1.8 V _{DC}	±3%	5 mA	I/O	I2C Data. Voltage level 1.8 V _{DC}

4 Mechanics

PCB Size	See mechanical drawing
PCB thickness	1.6 mm
Component height	Top side = 2 mm Bottom side = 2 mm
Weight	10 g



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5 Certifications

- a) User Information acc. to FCC15.21:
Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
- b) Part 15 Statement acc. to FCC 15.19:
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause interference.
(2) This device must accept any interference, including interference that may cause undesired operation.
- c) Statement acc. to RSS GEN Issue 5:
This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:
(1) This device may not cause interference.
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil contient des émetteurs / récepteurs exemptés de licence conformes aux RSS (RSS) d'Innovation, Sciences et Développement économique Canada. Le fonctionnement est soumis aux deux conditions suivantes:

- (1) Cet appareil ne doit pas causer d'interférences.
(2) Cet appareil doit accepter toutes les interférences, y compris celles susceptibles de provoquer un fonctionnement indésirable de l'appareil.

The end device is compliant with the following Standards:

- ICES-003 Issue 7 (2020)
- FCC CFR 47 Part 15 Subpart B

5.1 Compliance Procedure of Host device

The final host device, into which this modular approved transmitter is finally integrated has to comply itself to the appropriate technical requirements (typically §15.107 AC Powerline Conducted Limits when connected to the public AC Power lines and §15.109 Radiated Emission Limits for an Unintentional Radiator) and apply applicable FCC Equipment Authorization Procedures (SDoC or Certification).

Host devices marketed to Canada are typically subject to ICES-003 Information Technology Equipment (including Digital Apparatus) and the SDoC procedure.

This modular approved transmitter is tested and certified as stand-alone device under FCC §15.255 "Operation within the band 57-71 GHz" and ISSED RSS-210 Annex J: Devices operating in the band 57-71 GHz. When the module is integrated into a final host device, the integrator must repeat the Fundamental (EIRP) and Out-of-Band Emission measurements of one operating channel to assure compliance with the FCC/ISED requirements of the radar module when operating inside the host device.

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If the host device contains any additional transmitter, then simultaneous transmission compliance measurements are required to assure that the device complies with the FCC / ISSED requirements having all transmitters operational (FCC Multi-transmitter Policy). This also applies when multiple certified RF Modules are integrated and operational in addition to this radar module. RF Exposure to be addressed for the entire device.
Restrictions as defined in FCC §15.255 (a) & (b) and RSS-210 Annex J (J.2) apply.

5.2 Certification label

5.2.1 PMB label

Model: PMB
FCC ID: XFIPMB
IC: 9114A-PMB

Note: A QR/bar code with data related to the production (production date, production batch, Schindler ID number, ...) could be added on the label.

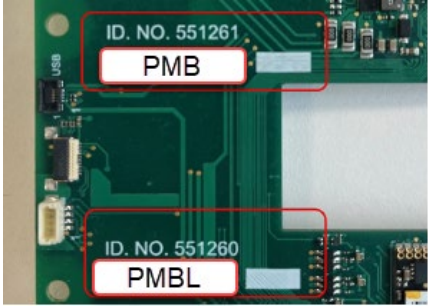


HVIN: PMB
PMN: PMB or PMBL (see chapter 6 Variants)

Remarks:

Product label on the board: The label will be applied on the PMB after the assembly and the tests of it. The PMB will never be supplied standalone, but always in an end device. The end device will be assembled and tested in the Schindler factory. The end device will be then shipped to the end customer that does not open it anymore.

PMB/PMBL identification: On the blank board of the PMB there will be 2 different Id. Nr. (PMB and PMBL) that can be crossed (2 empty squares will be present) during the production. In addition, you clearly see the 2 different assembly. See example below of another Schindler board.

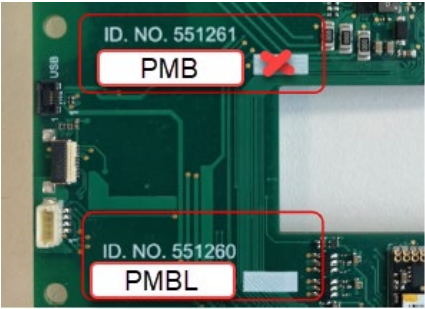
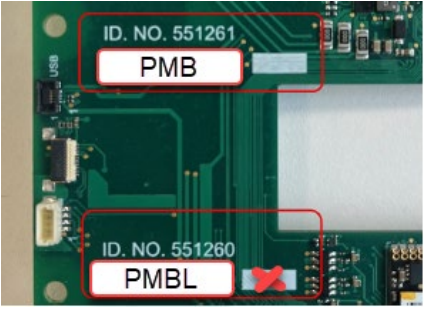
	PMB Schindler Ident Number: 551261 PMBL Schindler Ident Number: 551260
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	When in production a PMB is produced the empty square related to it will be crossed.
	When in production a PMBL is produced the empty square related to it will be crossed.

5.2.2 End device label

Here below an example of the end device label.

**Device Name**
Schindler

Power supply
PoE IN: 48V⁺ / 210mA / 10W



This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) this device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.


CAN ICES-3 (B)/NMB-3(B)

Contains
☐ FCC ID: XPYANNAB1 IC ID: 8595A-ANNAB1
☐ FCC ID: WP5TWN4F25 IC ID: 7948A-TWN4F25
☐ FCC ID: XFIPMB IC ID: 9114A-PMB

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6 Variants

2 different assembly variants of the MB1 board are available:

- 3. Fully assembled
 - PMN: PMB
- 4. Only the radar part is assembled
 - PMN: PMBL

For more details regarding the MB1 parts see the REF [1] document.

7 Sale

The PMB will never be sold standalone to a customer, but always in an end device.
The end device will be assembled and tested in the Schindler factory.
The end device will be then shipped to the end customer that does not open it anymore.

All the technical documents (including the integration instruction of the PMB) are internal confidential manufacturing documents.

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