

Voltage Rails

+VDC	Primary DC system power supply (6V-9.5V)
+VBATTERY	Battery Power supply (6-8.4V)
+VCC_CORE	Core Voltage for CPU
+V1.05S	1.05V for Calistoga & ICH7M core / FSB VTT
+V1.8	1.8V power rail for DDR2
+V0.9S	0.9V DDR2 Termination voltage
+V3.3AL	3.3V always on power rail
+V5AL	5V for ICH7-M's VCC5 Refsus
+V3.3S	3.3V main power rail
+V5S	5V main power rail
+V2.5S	2.5V power rail for 945GMS

Board stack up description

PCB Layers	Trace Impedence:55ohm +/-15%
Top(Signal1)	
Ground 1	
Signal2	
Signal3	
Power	
Signal4	
Ground 2	
Bottom(Signal5)	

USB Table

USB Port#	Function Description
0	
1	
2	
3	
4	
5	
6	
7	

I2C SMB Address

Device	Address	Hex	Master
Clock Generator	1101 001x	D2	ICH7-M
SO-DIMMO	1010 000x	A0	ICH7-M
CPU Thermal Sensor	1001 100x	98	KBC
Smart Battery	0001 011x	16	KBC
PCIE Slot	TBD	TBD	ICH7-M

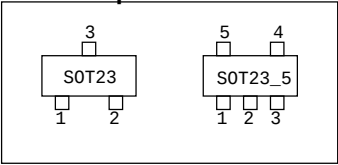
Power States

Signal	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*	+V*S	Clock
S0 (Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (STM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (STD)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SoftOff)	LOW	LOW	LOW	ON	OFF	OFF	OFF

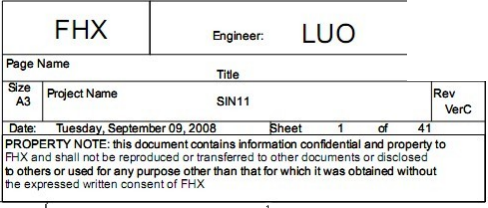
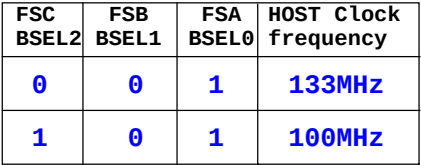
Wake up Events

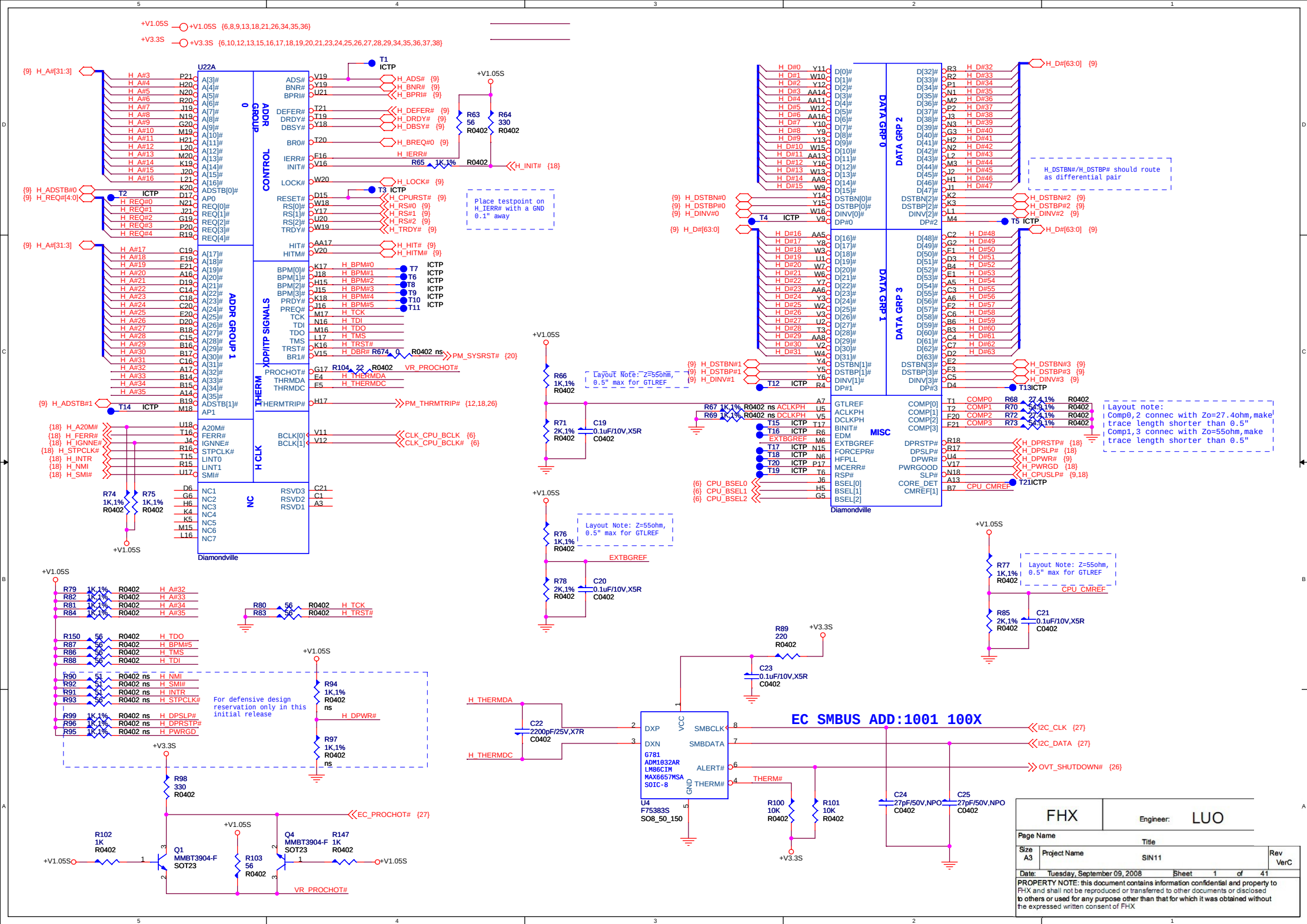
LID switch from EC
Power switch from EC

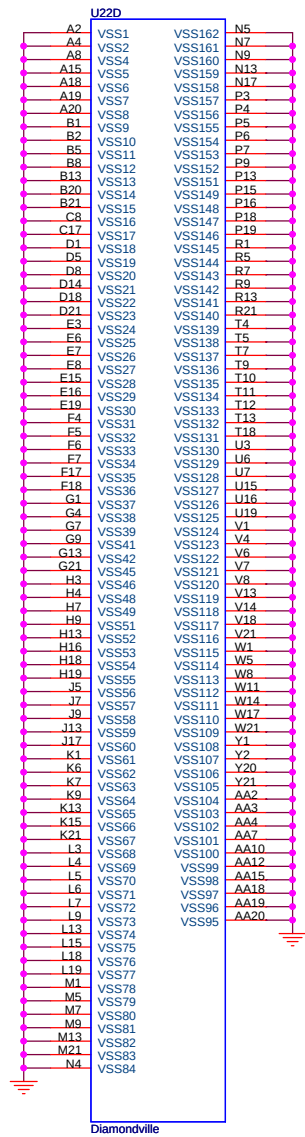
PCB Footprints



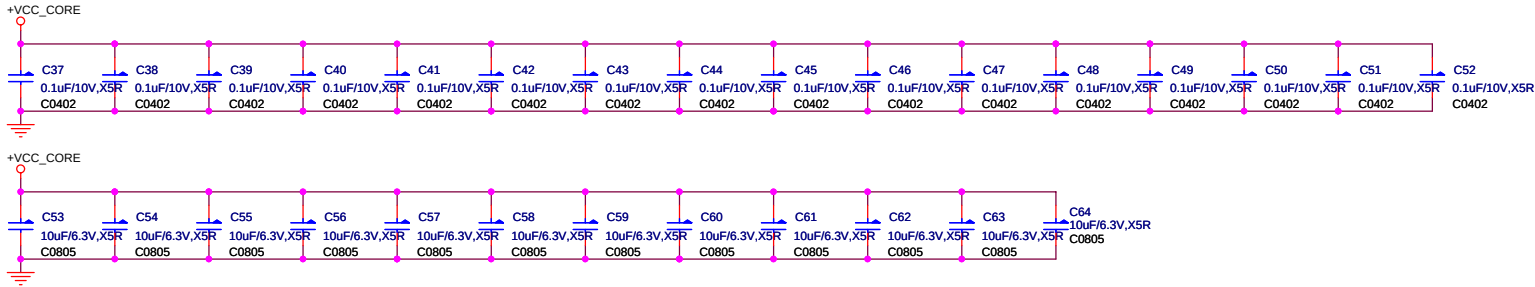
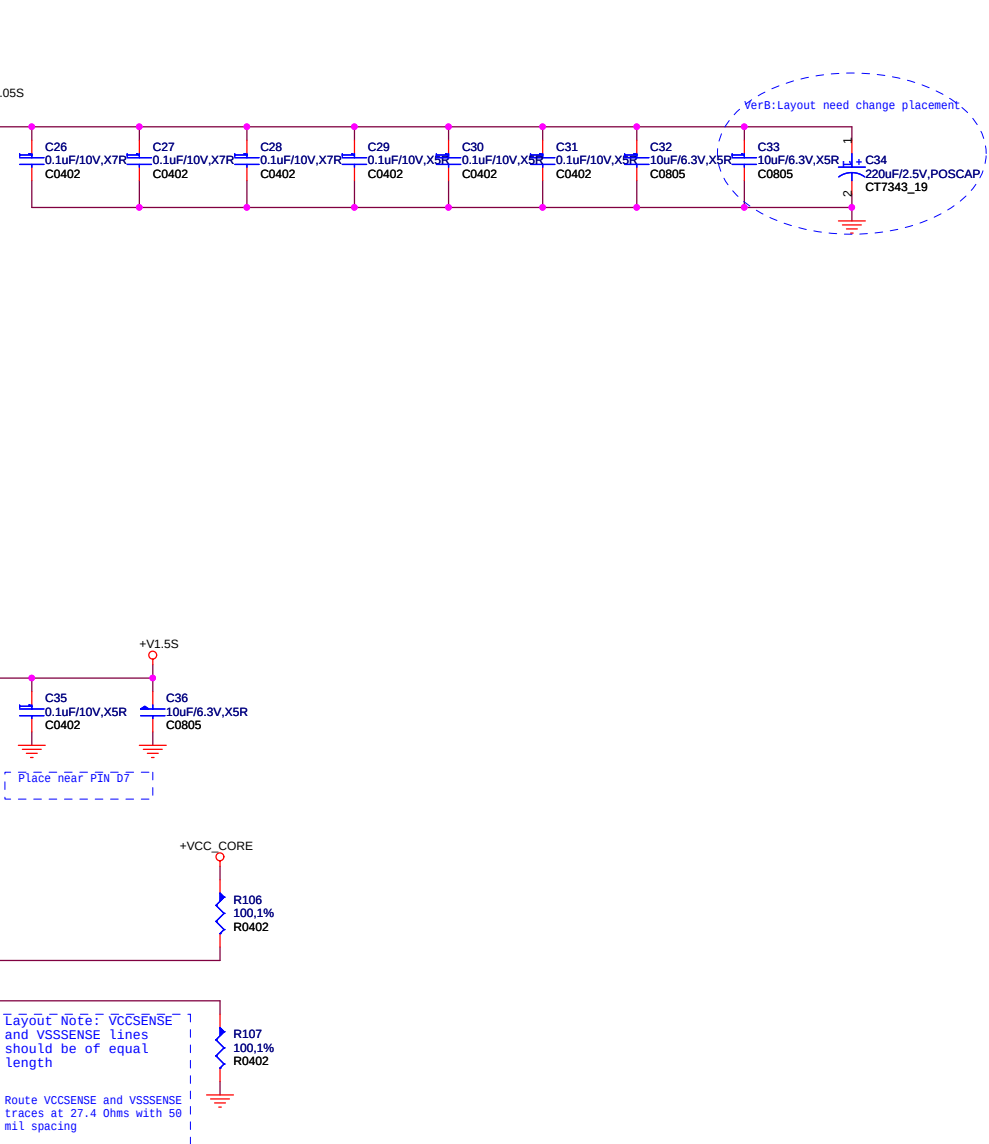
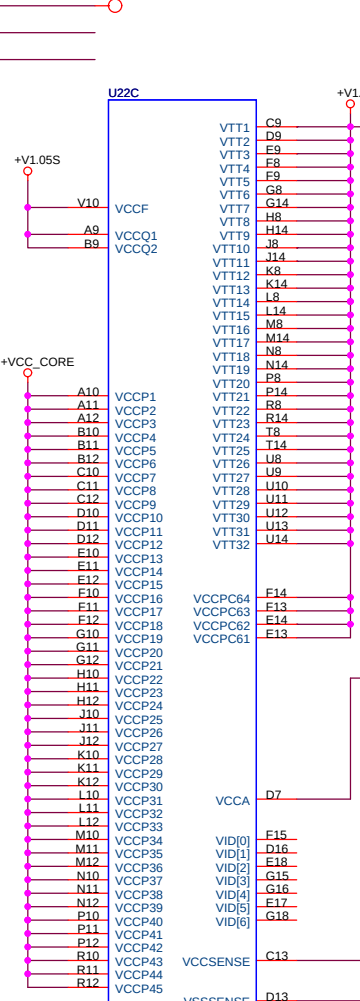
ns: Component marked "ns" is not stuff



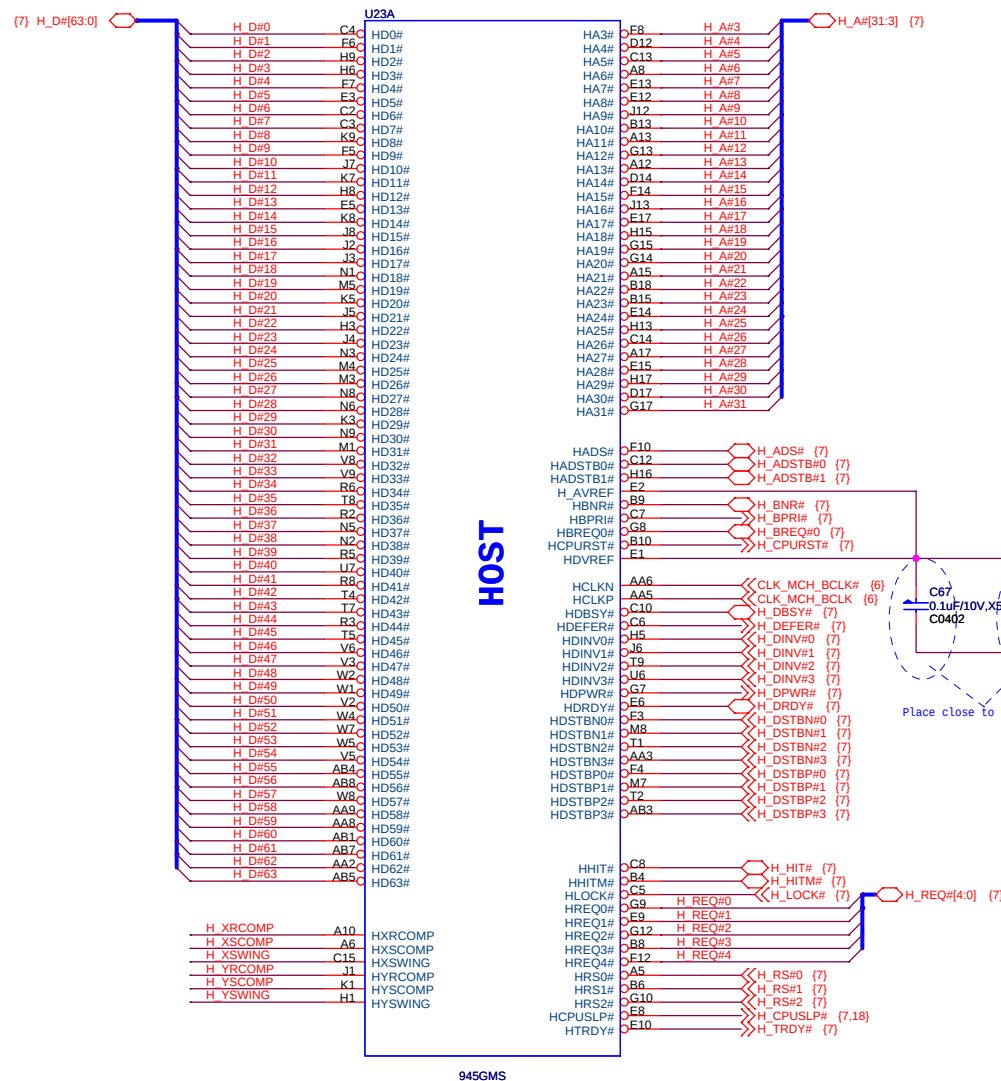
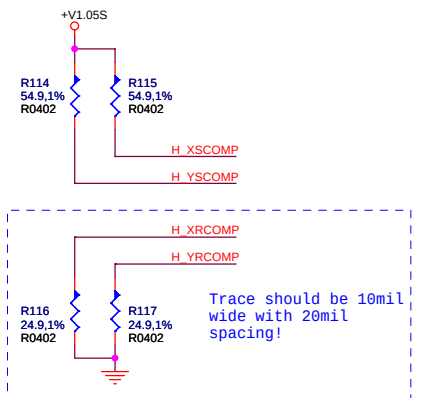




+VCC_CORE (35,38)
+V1.5S (10,13,21,23,34,35,36)
+V1.05S (6,7,9,13,18,21,26,34,35,36)



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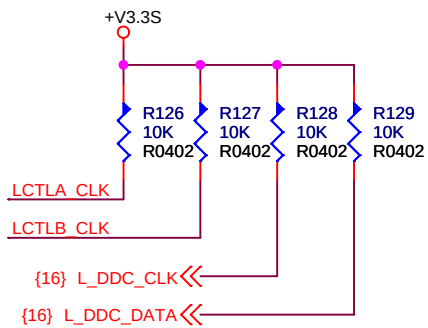
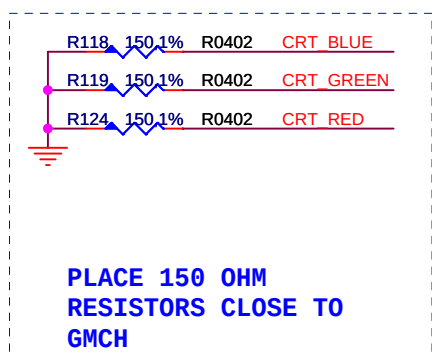
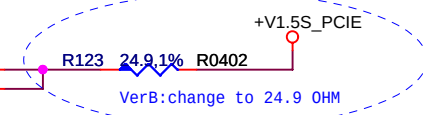
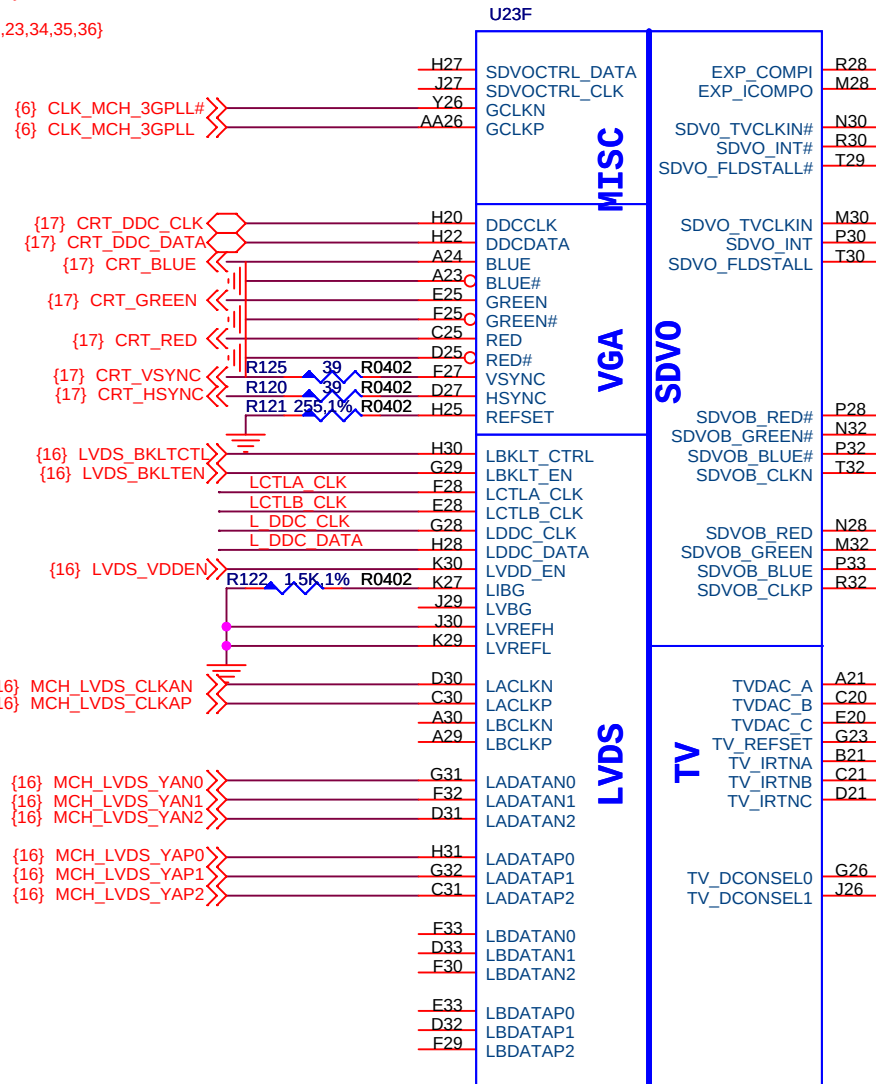


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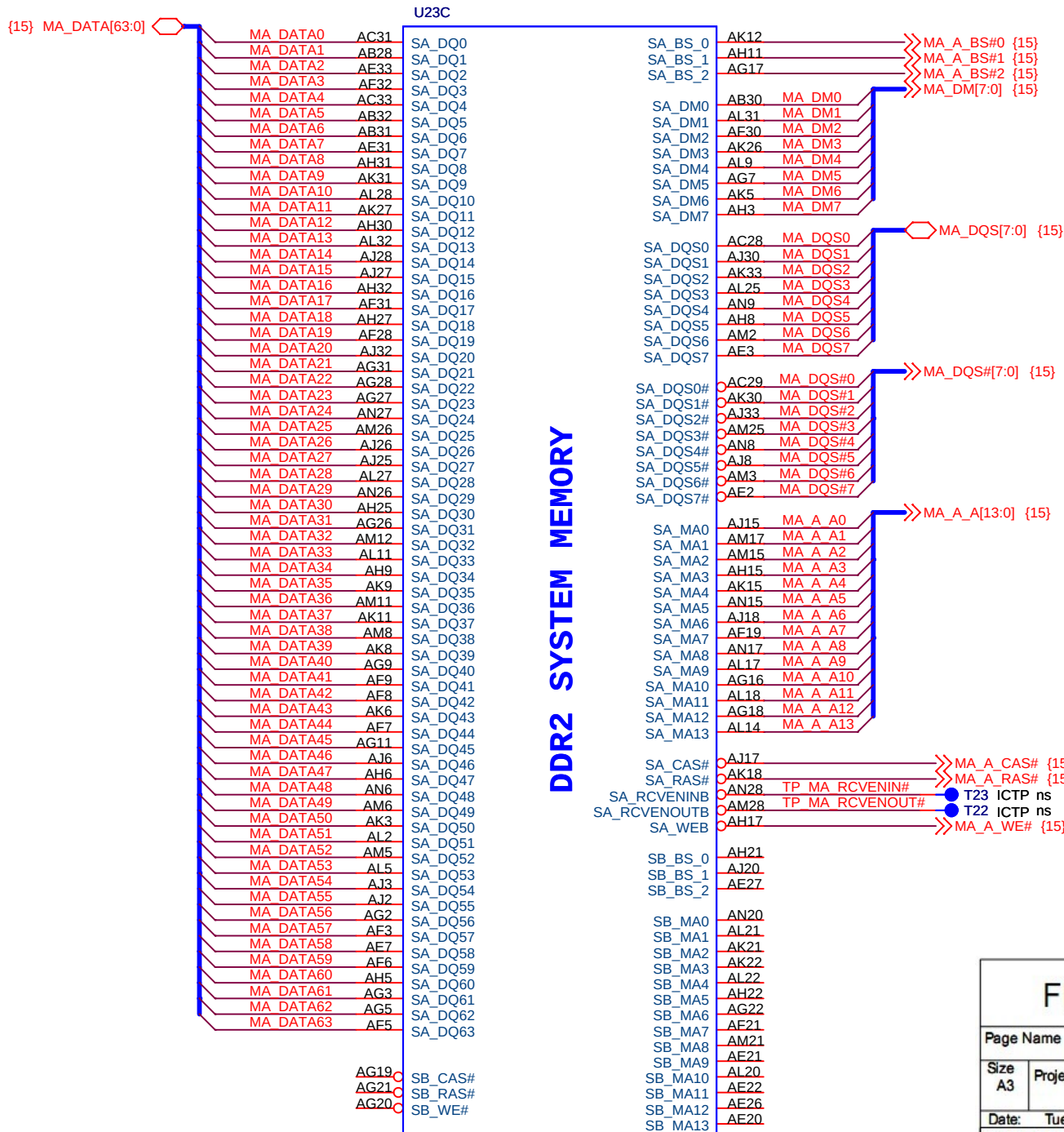
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+V1.5S_PCIE {13}

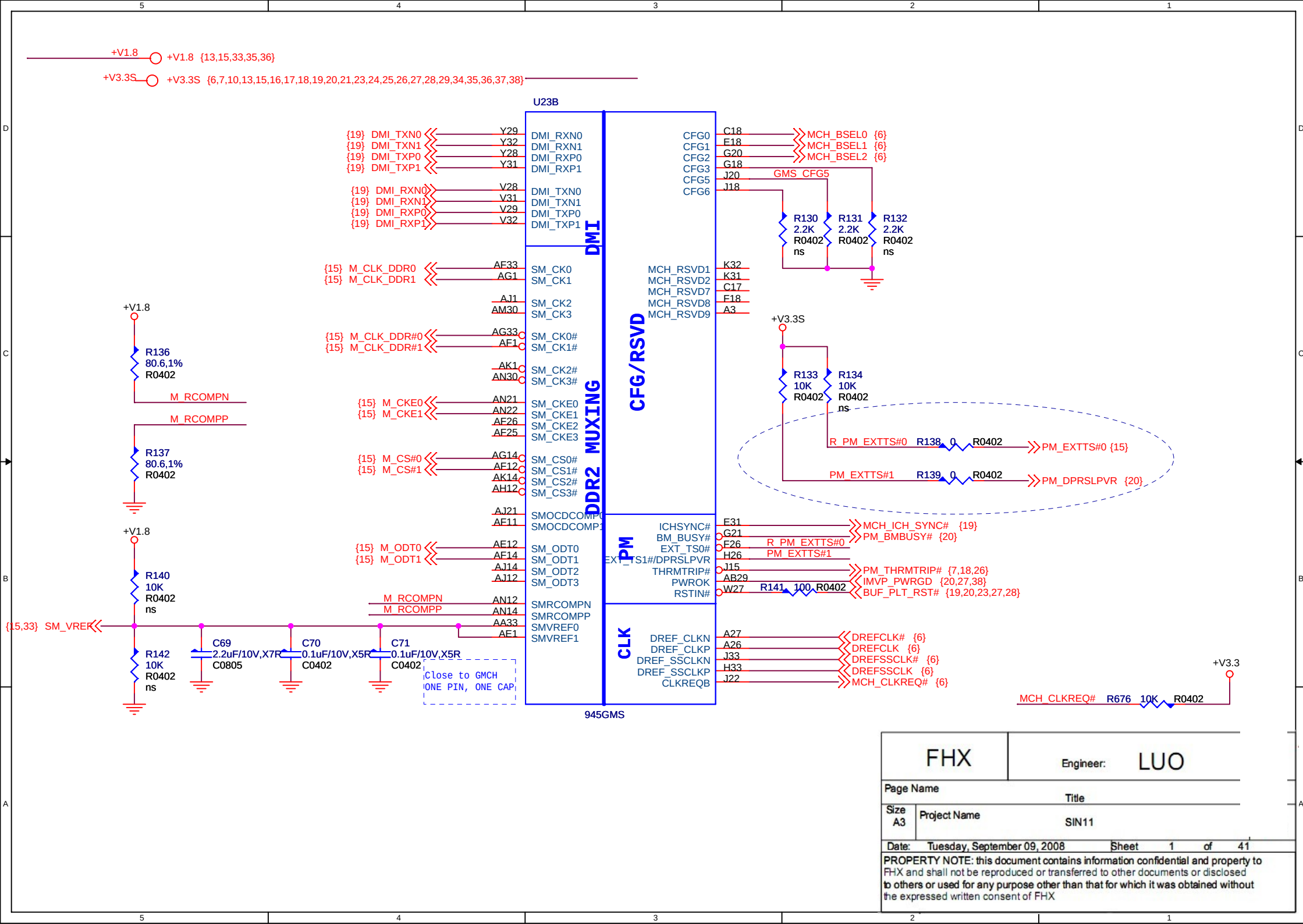
+V1.5S {8,13,21,23,34,35,36}

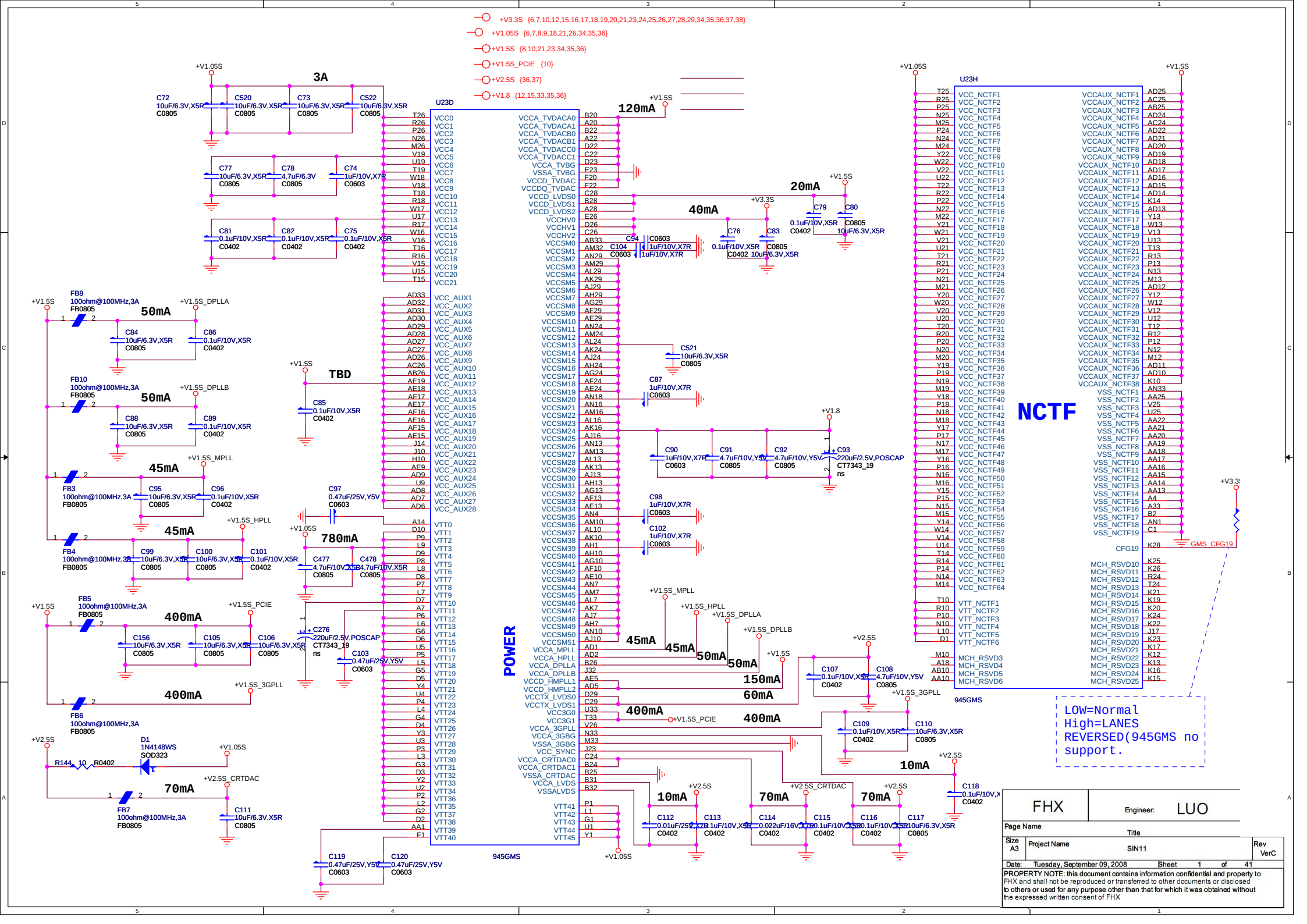


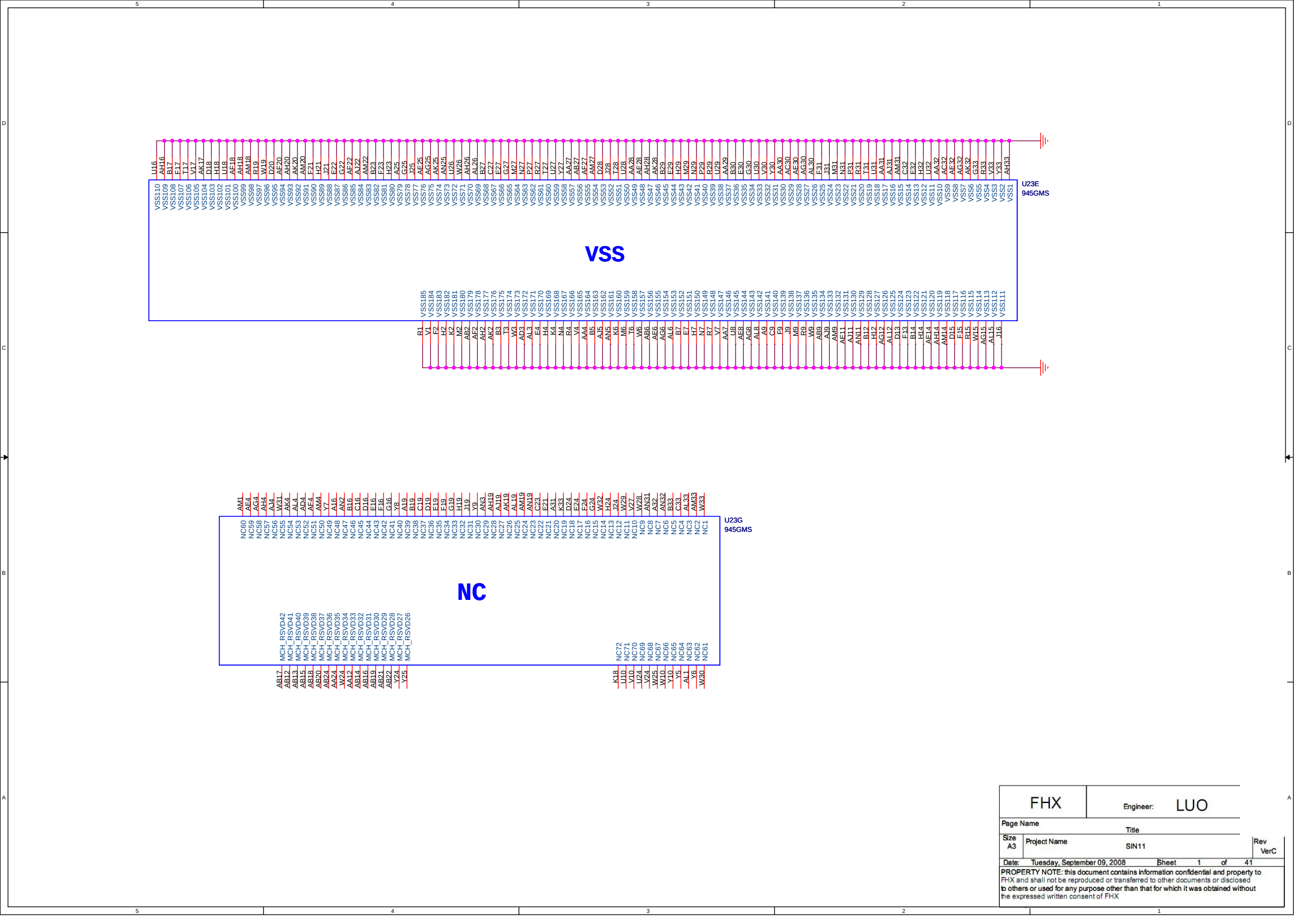
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- +V0.9S {33,36}
○ +V1.8 {12,13,33,35,36}
○ +V3.3S {6,7,10,12,13,16,17,18,19,20,21,23,24,25,26,27,28,29,34,35,36,37,38}

{11} MA_A[13:0] <<

MA A A0 102
MA A A1 101
MA A A2 100
MA A A3 99
MA A A4 98
MA A A5 97
MA A A6 94
MA A A7 92
MA A A8 93
MA A A9 91
MA A A10 105
MA A A11 90
MA A A12 89
MA A A13 116

{11} MA_BS#<<
{11} MA_BS#<<
{11} MA_BS#<<

{12} M_CS#0<<
{12} M_CS#1<<

{11} MA_DM[7:0] <<

MA DM0 10
MA DM1 26
MA DM2 52
MA DM3 67
MA DM4 130
MA DM5 147
MA DM6 170
MA DM7 185

{11} MA_A_WE#<<
{11} MA_A_CAS#<<
{11} MA_A_RAS#<<

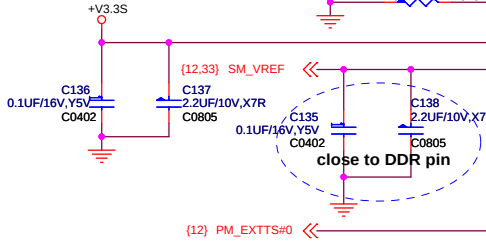
{12} M_CKE0<<
{12} M_CKE1<<

{12} M_CLK_DDR0<<
{12} M_CLK_DDR#0<<
{12} M_CLK_DDR1<<
{12} M_CLK_DDR#1<<

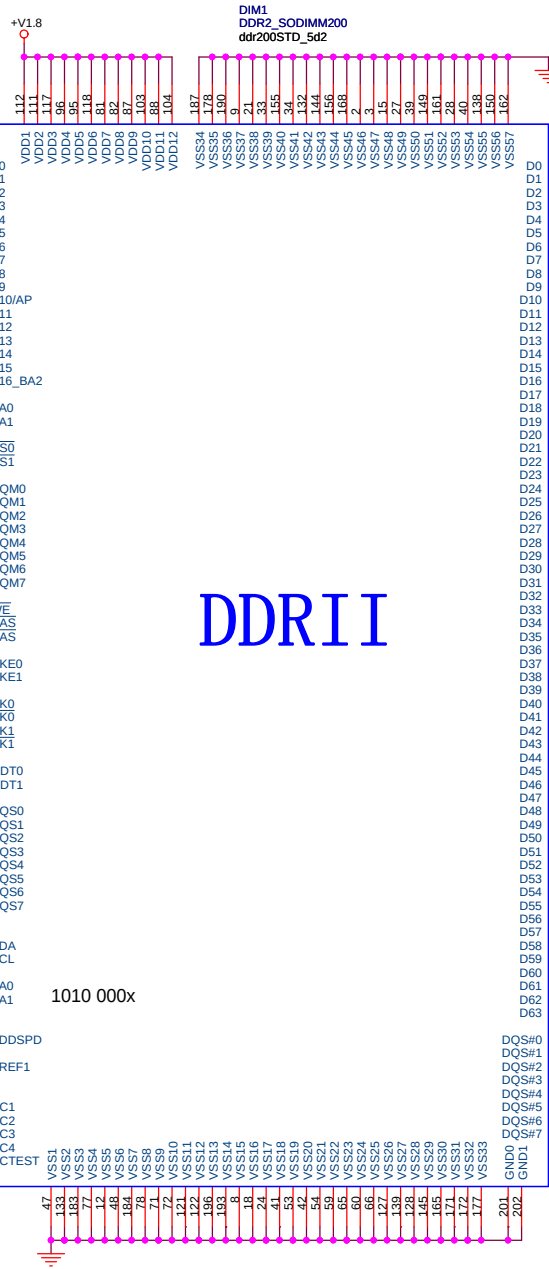
{12} M_ODT0<<
{12} M_ODT1<<

MA DQS0 13
MA DQS1 31
MA DQS2 51
MA DQS3 70
MA DQS4 131
MA DQS5 148
MA DQS6 169
MA DQS7 188

{6,20,23} SMB_DATA_S<<
{6,20,23} SMB_CLK_S<<



{12} PM_EXTTS#0<<

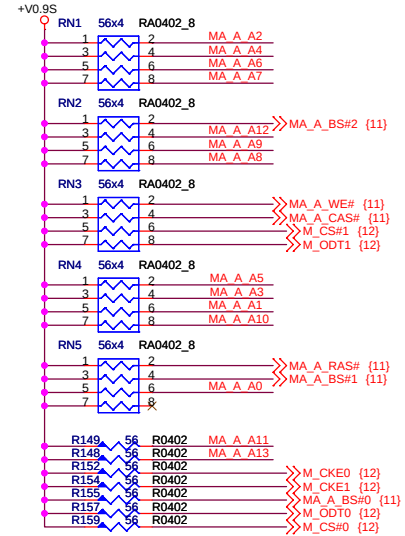
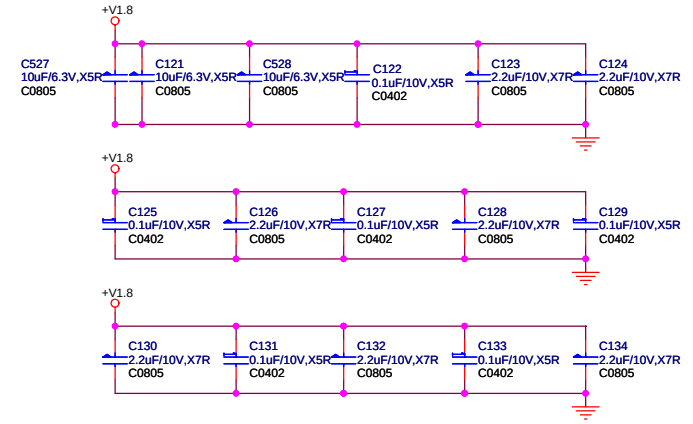


DDR I

SO-DIMM 0

<<MA_DATA[63:0] {11}

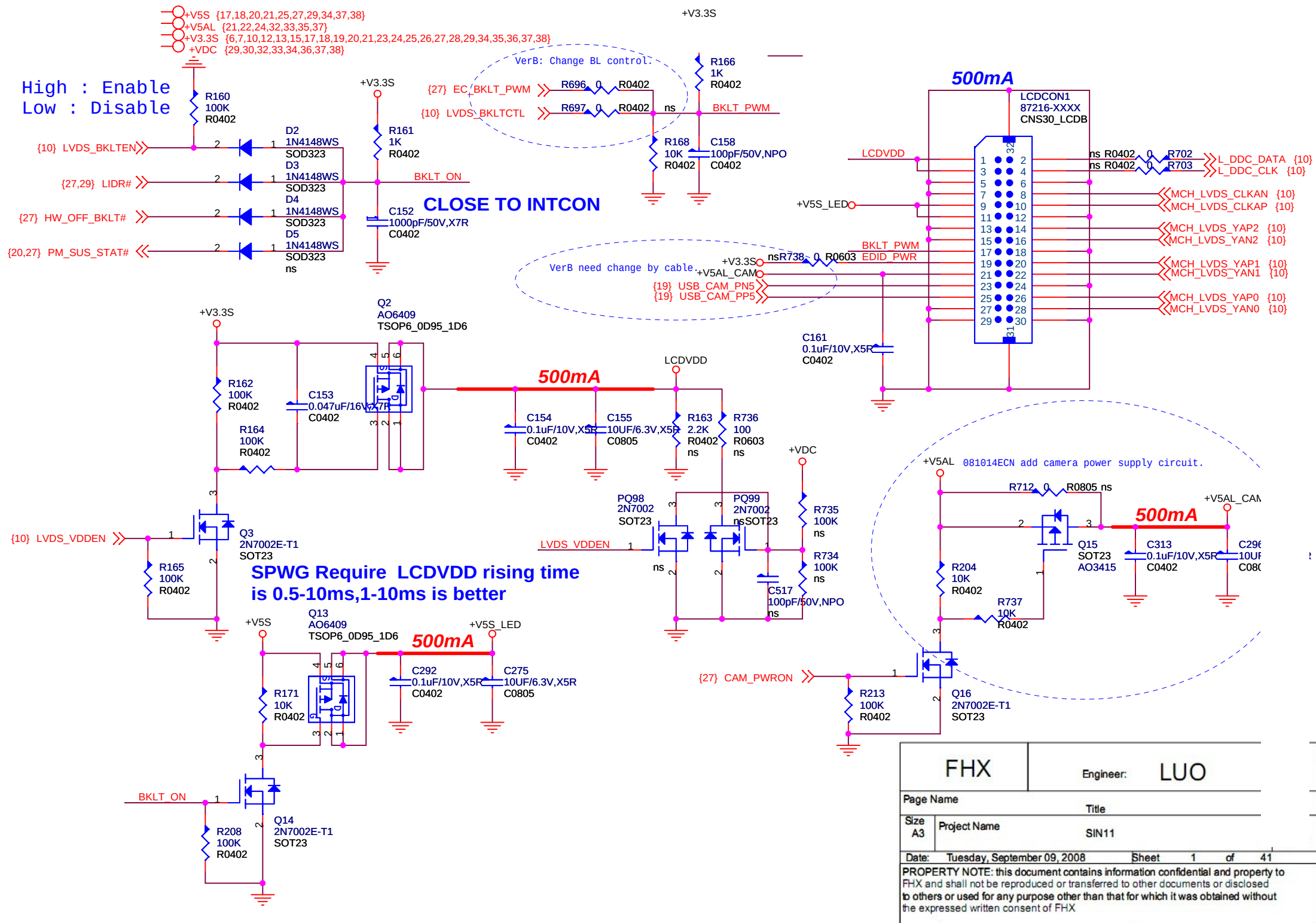
>>MA_DQS#7[7:0] {11}



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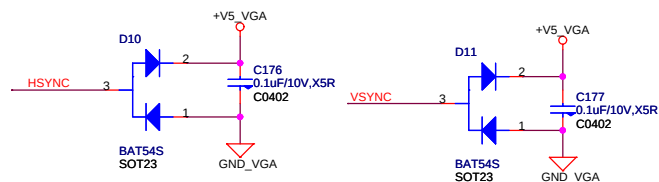
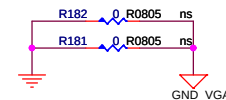
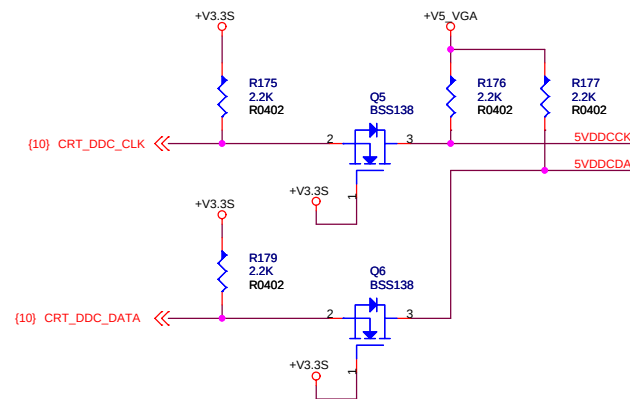
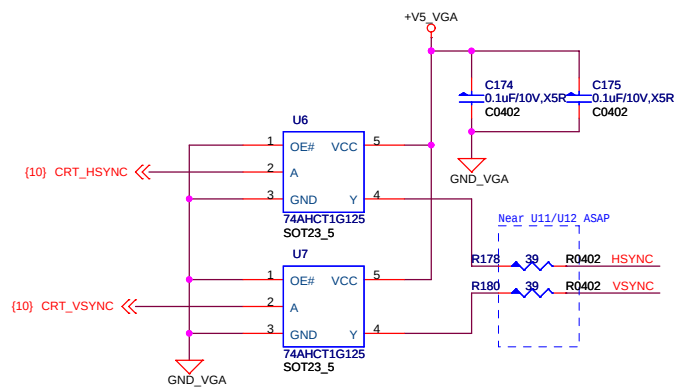
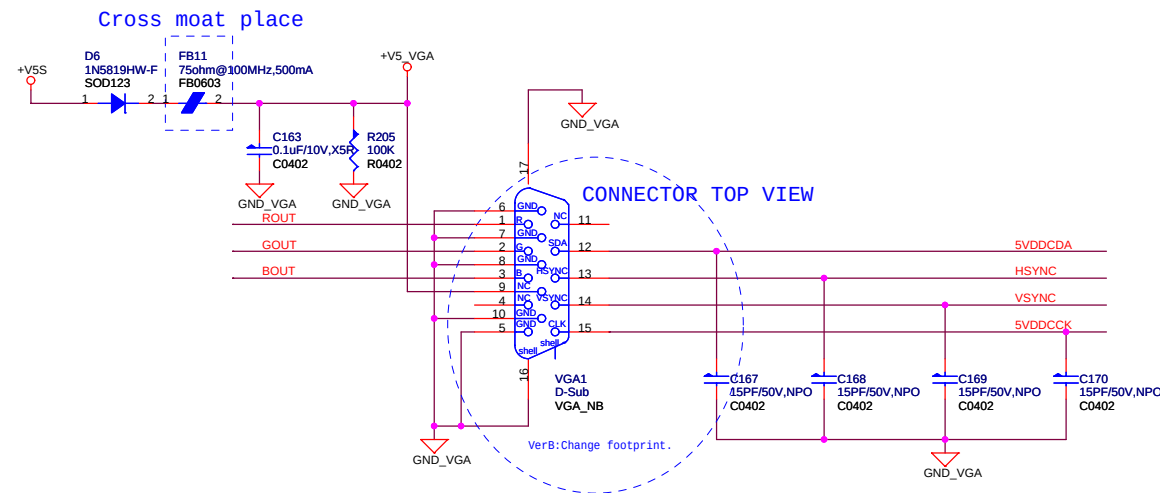
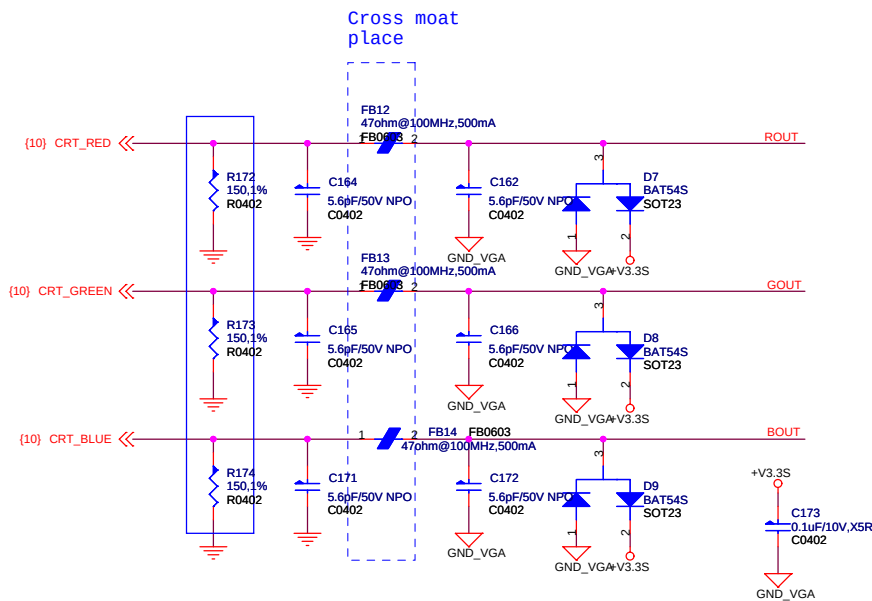
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 +V5AL {21,22,24,32,33,35,37}
 +V3.3S {6,7,10,12,13,15,17,18,19,20,21,23,24,25,26,27,28,29,34,35,36,37,38}
 +VDC {29,30,32,33,34,36,37,38}

High : Enable
 Low : Disable

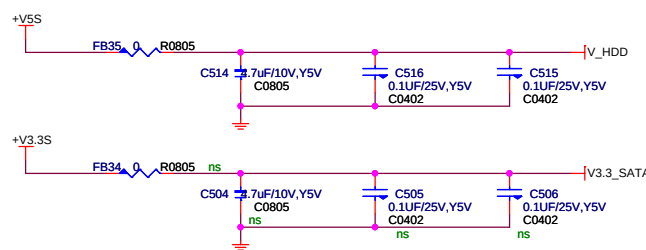
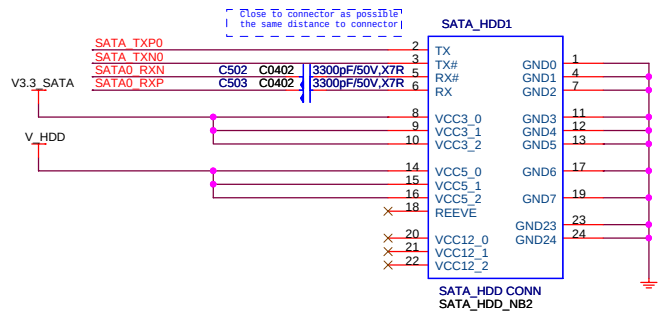
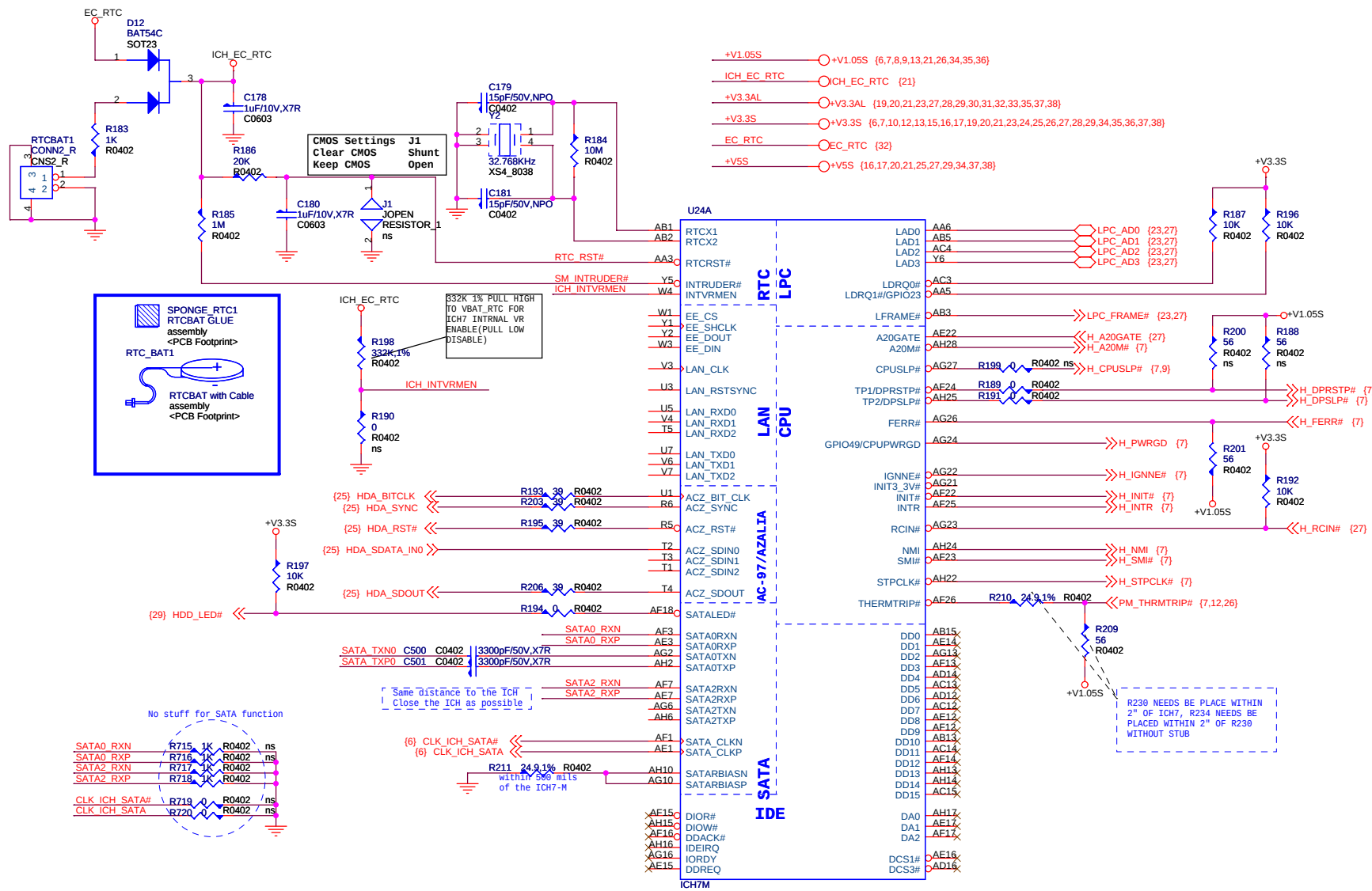


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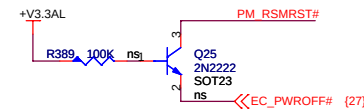
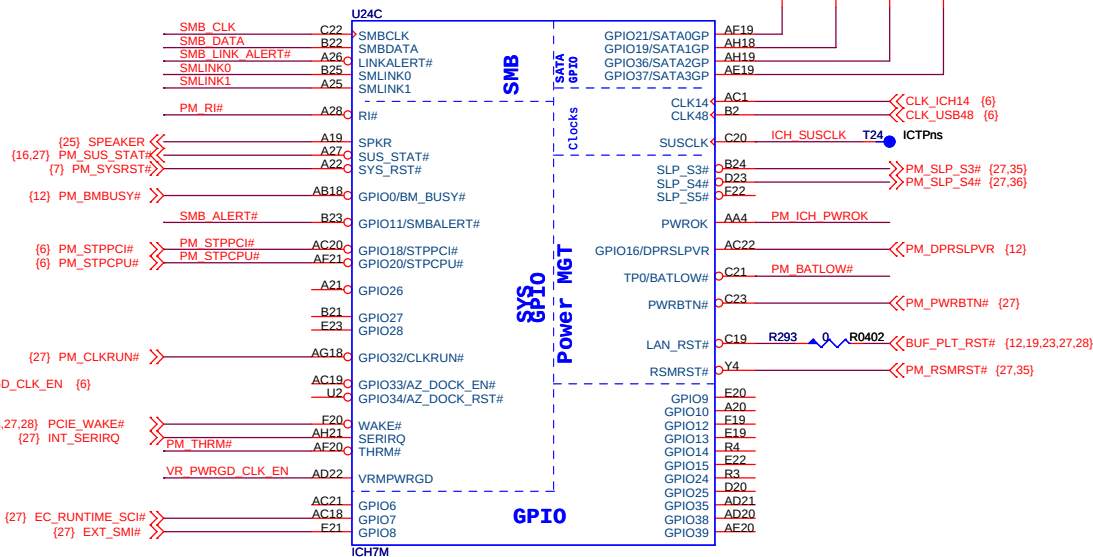
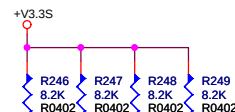
+V5S {16,18,20,21,25,27,29,34,37,38}
+V3.3S {6,7,10,12,13,15,16,18,19,20,21,23,24,25,26,27,28,29,34,35,36,37,38}



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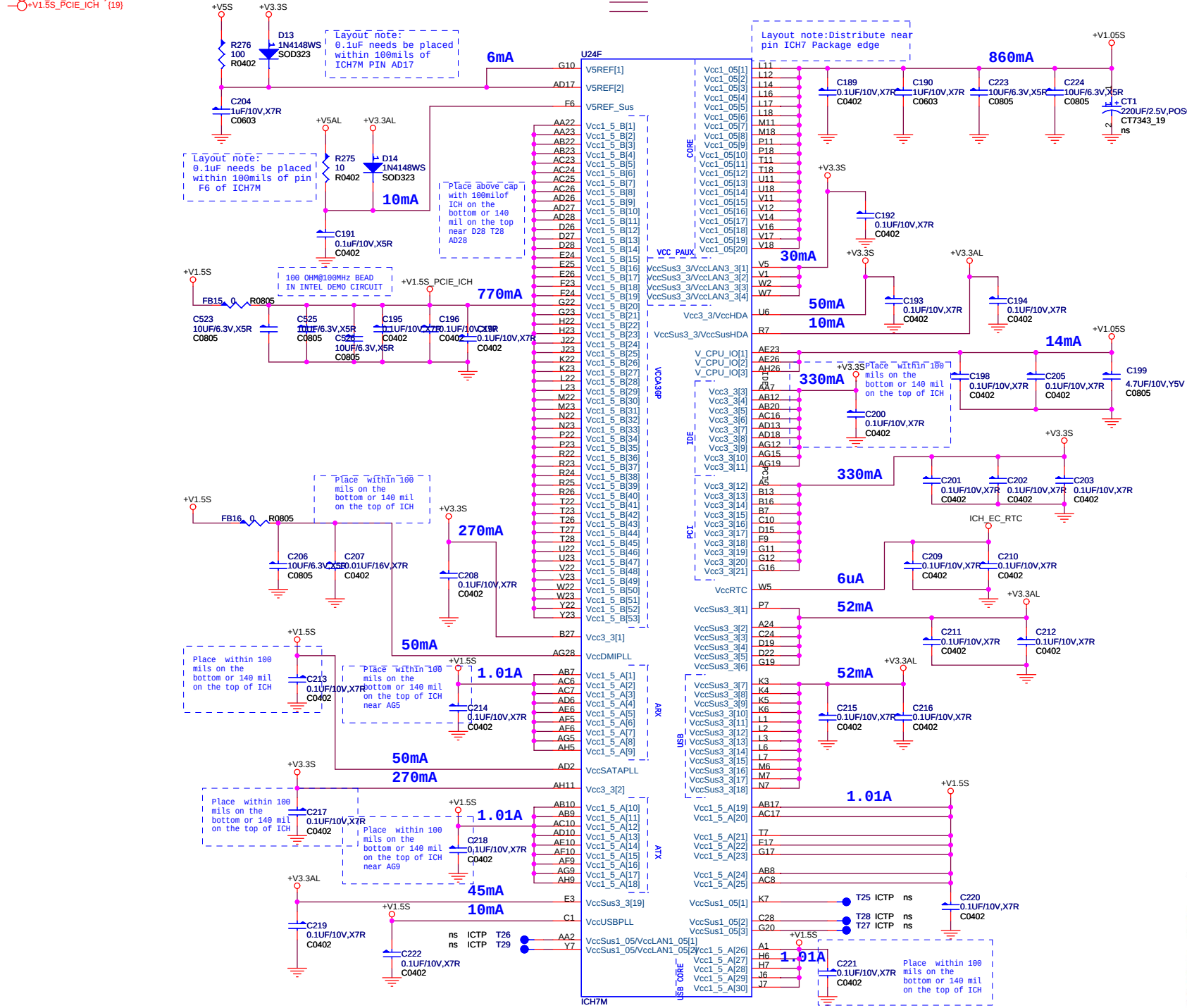
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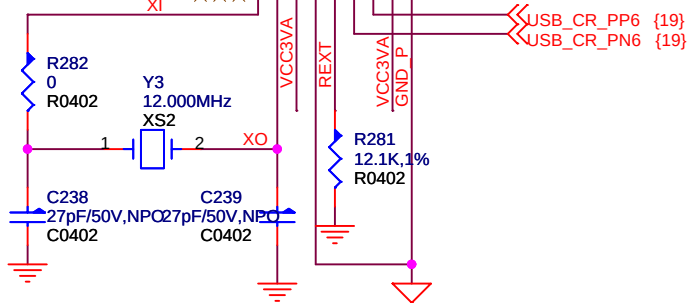
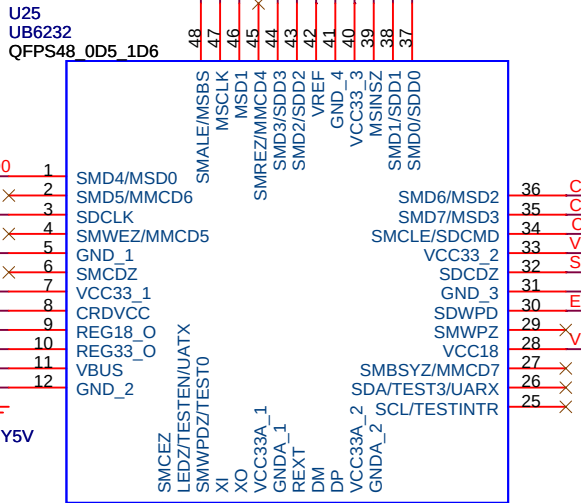
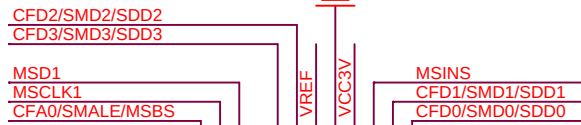
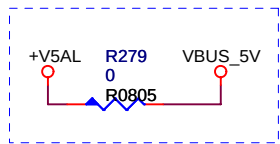
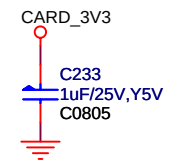
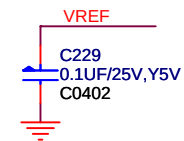
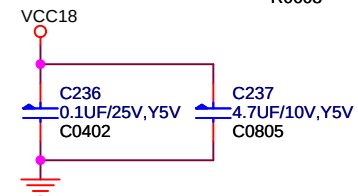
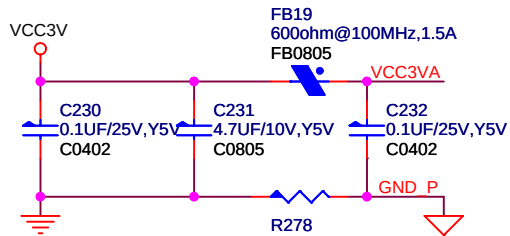
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- +V3.3A [19,20,23,27,28,29,30,31,32,33,35,37,38]
- +V3.3S [6,7,10,12,13,15,16,17,18,19,20,23,24,25,26,27,28,29,34,35,36,37,38]
- +V1.05S [6,7,8,9,13,18,26,34,35,36]
- +V5AL [16,22,24,32,33,35,37]
- +V5S [16,17,18,20,25,27,29,34,37,38]
- +V1.5S [8,10,13,23,34,35,36]
- ICH_EC_RTC [18]
- +V1.5S_PCIE_ICH [19]

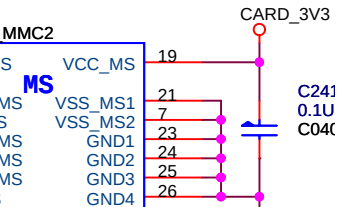
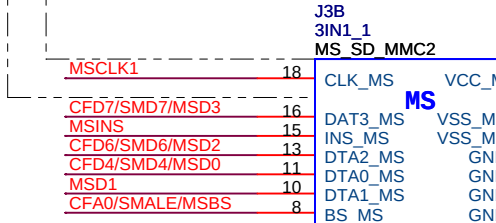
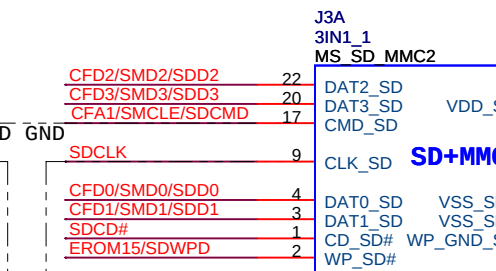
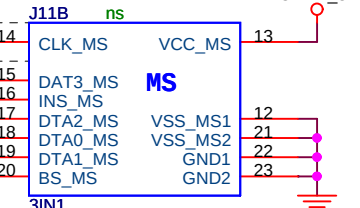
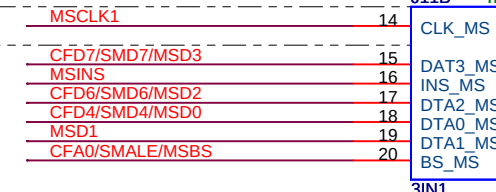
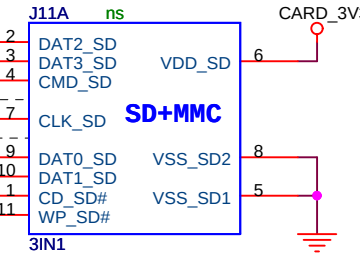


A4	VSS[1]	VSS[98]	P28
A23	VSS[2]	VSS[99]	R1
B1	VSS[3]	VSS[100]	R11
B8	VSS[4]	VSS[101]	R12
B11	VSS[5]	VSS[102]	R13
B14	VSS[6]	VSS[103]	R14
B17	VSS[7]	VSS[104]	R15
B20	VSS[8]	VSS[105]	R16
B26	VSS[9]	VSS[106]	R17
B28	VSS[10]	VSS[107]	R18
C2	VSS[11]	VSS[108]	T6
C6	VSS[12]	VSS[109]	T12
C27	VSS[13]	VSS[110]	T13
D10	VSS[14]	VSS[111]	T14
D13	VSS[15]	VSS[112]	T15
D18	VSS[16]	VSS[113]	T16
D21	VSS[17]	VSS[114]	T17
D24	VSS[18]	VSS[115]	U4
E1	VSS[19]	VSS[116]	U12
E2	VSS[20]	VSS[117]	U13
E4	VSS[21]	VSS[118]	U14
E8	VSS[22]	VSS[119]	U15
E15	VSS[23]	VSS[120]	U16
F3	VSS[24]	VSS[121]	U17
F4	VSS[25]	VSS[122]	U24
F5	VSS[26]	VSS[123]	U25
F12	VSS[27]	VSS[124]	U26
F27	VSS[28]	VSS[125]	V2
F28	VSS[29]	VSS[126]	V13
G1	VSS[30]	VSS[127]	V15
G2	VSS[31]	VSS[128]	V24
G5	VSS[32]	VSS[129]	V27
G6	VSS[33]	VSS[130]	V28
G9	VSS[34]	VSS[131]	W6
G14	VSS[35]	VSS[132]	W24
G18	VSS[36]	VSS[133]	W25
G21	VSS[37]	VSS[134]	W26
G24	VSS[38]	VSS[135]	Y3
G25	VSS[39]	VSS[136]	Y24
G26	VSS[40]	VSS[137]	Y27
H3	VSS[41]	VSS[138]	Y28
H4	VSS[42]	VSS[139]	AA24
H5	VSS[43]	VSS[140]	AA25
H24	VSS[44]	VSS[141]	AA26
H27	VSS[45]	VSS[142]	AB4
H28	VSS[46]	VSS[143]	AB6
J1	VSS[47]	VSS[144]	AB11
J2	VSS[48]	VSS[145]	AB14
J5	VSS[49]	VSS[146]	AB16
J24	VSS[50]	VSS[147]	AB19
J25	VSS[51]	VSS[148]	AB21
J26	VSS[52]	VSS[149]	AB24
K24	VSS[53]	VSS[150]	AB27
K27	VSS[54]	VSS[151]	AB28
K28	VSS[55]	VSS[152]	AC2
L13	VSS[56]	VSS[153]	AC5
L15	VSS[57]	VSS[154]	AC9
L24	VSS[58]	VSS[155]	AC11
L25	VSS[59]	VSS[156]	AD1
L26	VSS[60]	VSS[157]	AD3
M3	VSS[61]	VSS[158]	AD4
M4	VSS[62]	VSS[159]	AD7
M5	VSS[63]	VSS[160]	AD8
M12	VSS[64]	VSS[161]	AD11
M13	VSS[65]	VSS[162]	AD15
M14	VSS[66]	VSS[163]	AD19
M15	VSS[67]	VSS[164]	AD23
M16	VSS[68]	VSS[165]	AE2
M17	VSS[69]	VSS[166]	AE4
M24	VSS[70]	VSS[167]	AE8
M27	VSS[71]	VSS[168]	AE11
M28	VSS[72]	VSS[169]	AE13
N1	VSS[73]	VSS[170]	AE18
N2	VSS[74]	VSS[171]	AE21
N5	VSS[75]	VSS[172]	AE24
N11	VSS[76]	VSS[173]	AE25
N12	VSS[77]	VSS[174]	AF2
N13	VSS[78]	VSS[175]	AF4
N14	VSS[79]	VSS[176]	AF8
N15	VSS[80]	VSS[177]	AF11
N16	VSS[81]	VSS[178]	AF28
N17	VSS[82]	VSS[179]	AG1
N18	VSS[83]	VSS[180]	AG11
N24	VSS[84]	VSS[181]	AG14
N25	VSS[85]	VSS[182]	AG17
N26	VSS[86]	VSS[183]	AG25
P3	VSS[87]	VSS[184]	AG26
P4	VSS[88]	VSS[185]	AG27
P12	VSS[89]	VSS[186]	AG31
P13	VSS[90]	VSS[187]	AG34
P14	VSS[91]	VSS[188]	AG37
P15	VSS[92]	VSS[189]	AG41
P16	VSS[93]	VSS[190]	AG42
P17	VSS[94]	VSS[191]	AG43
P24	VSS[95]	VSS[192]	AG47
P27	VSS[96]	VSS[193]	AG48
U24E	VSS[97]	VSS[194]	AG49

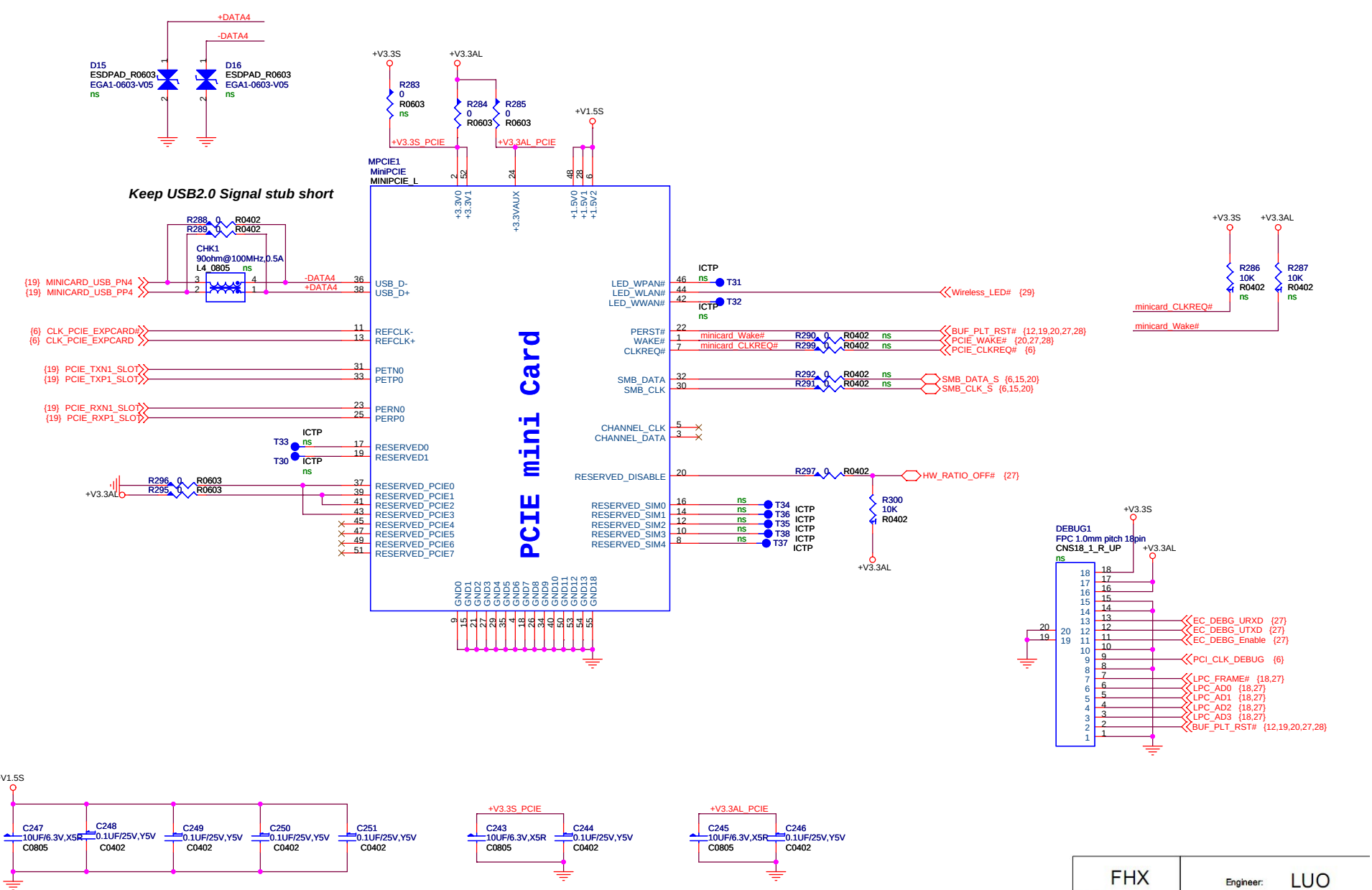


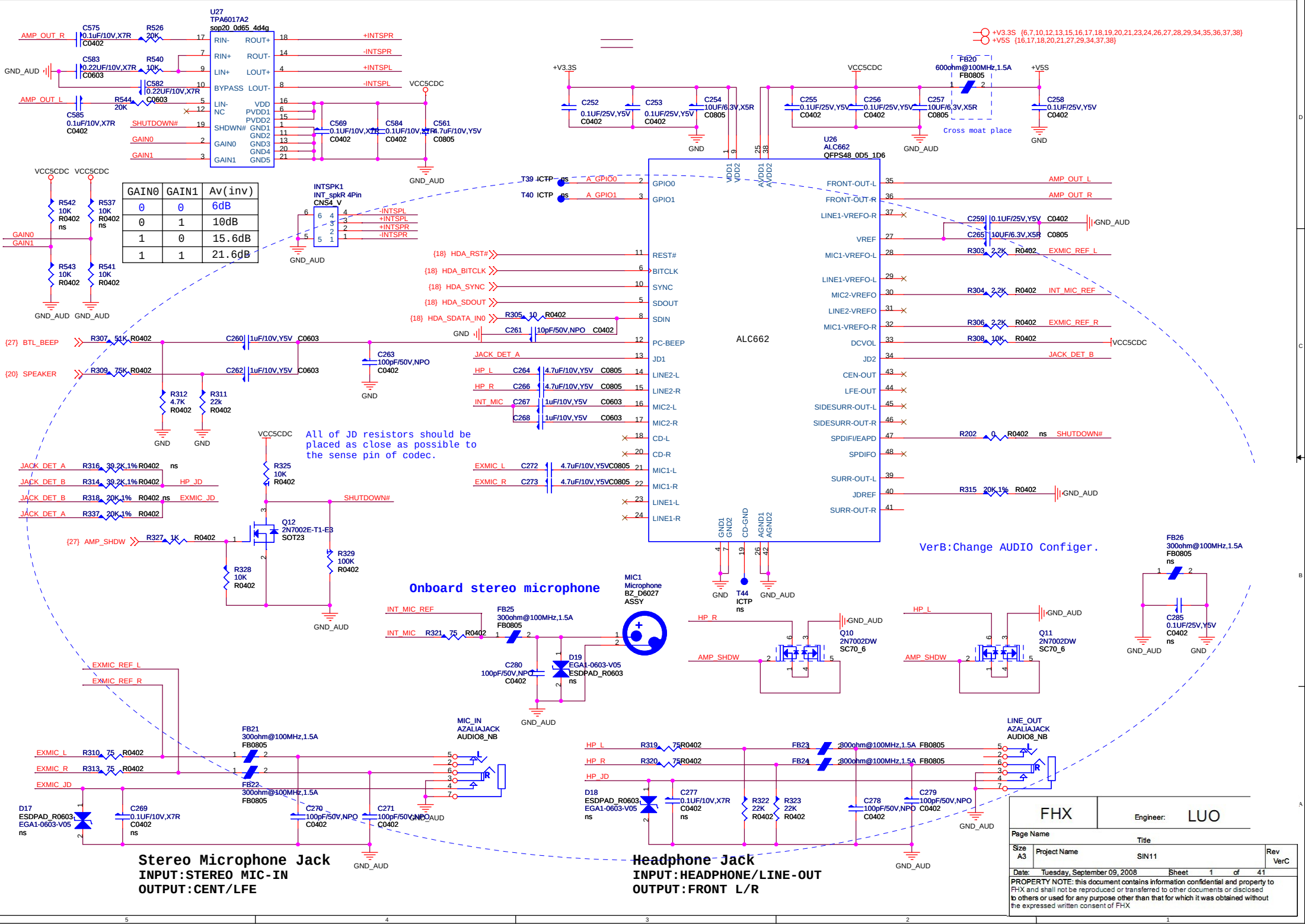
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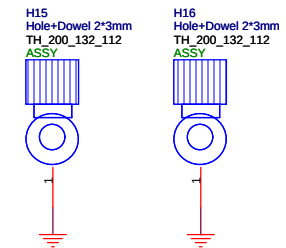
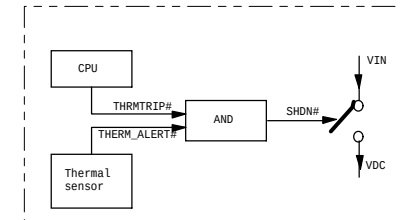
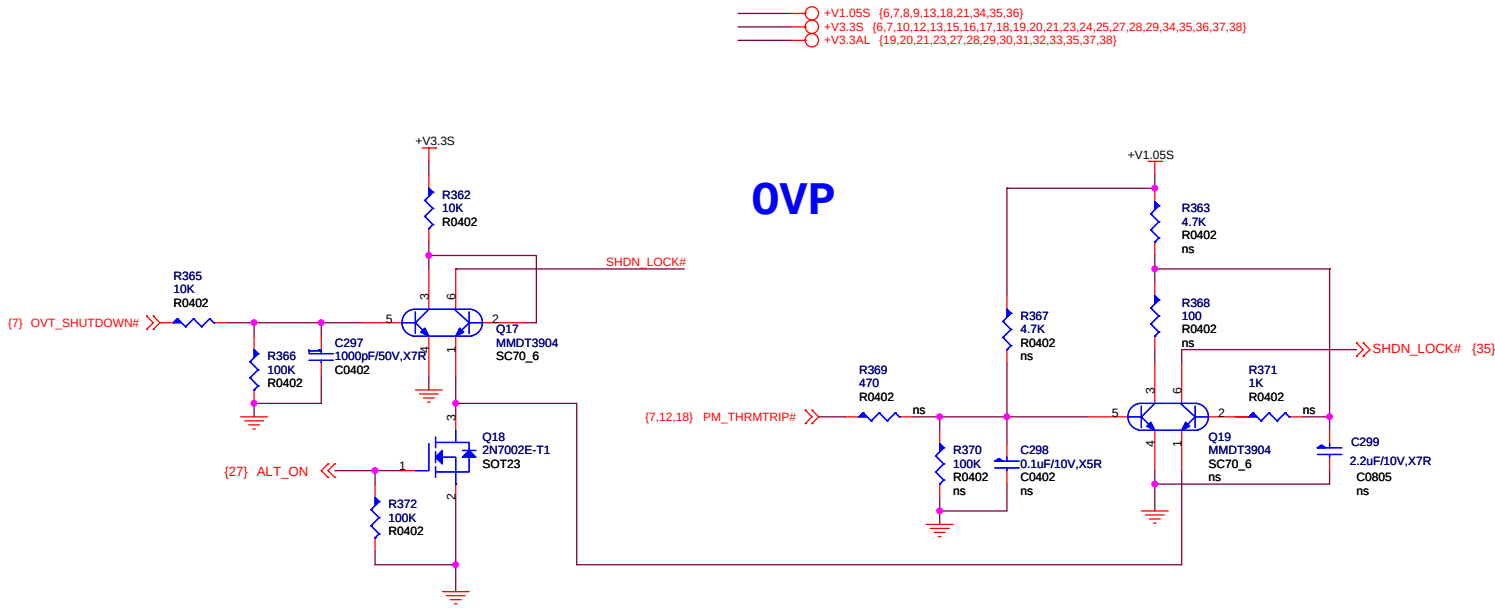
SHIELD GND



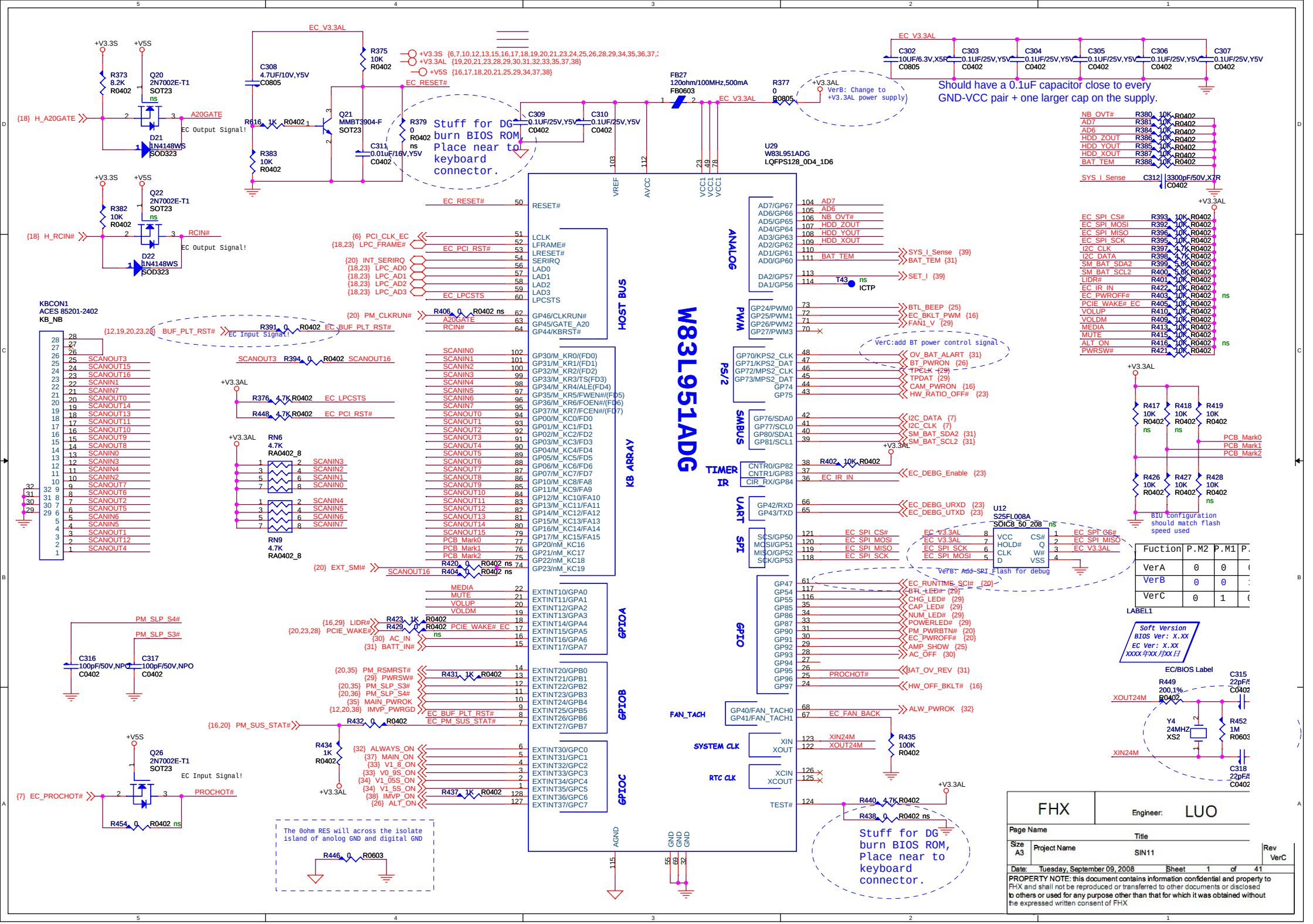
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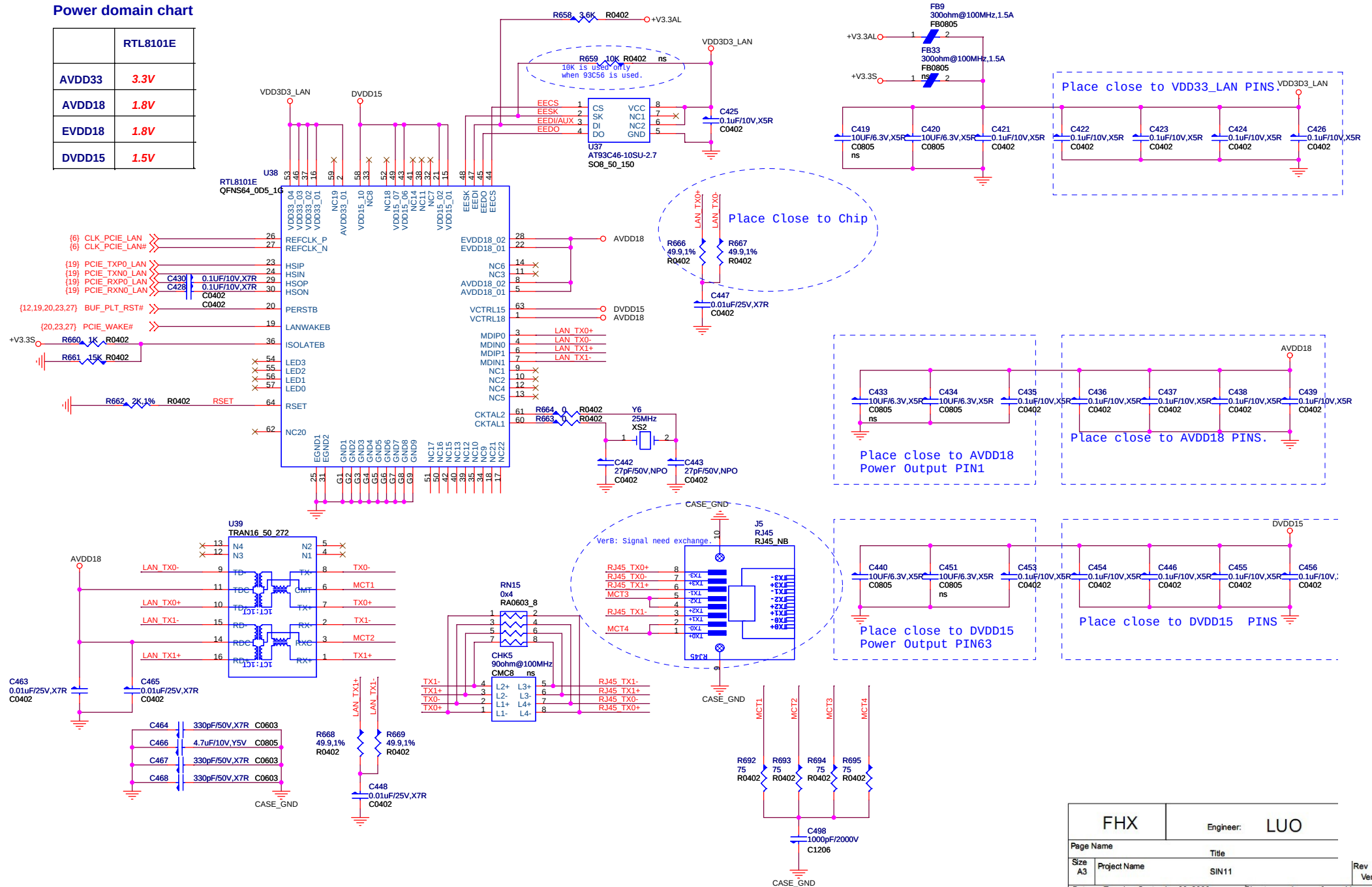


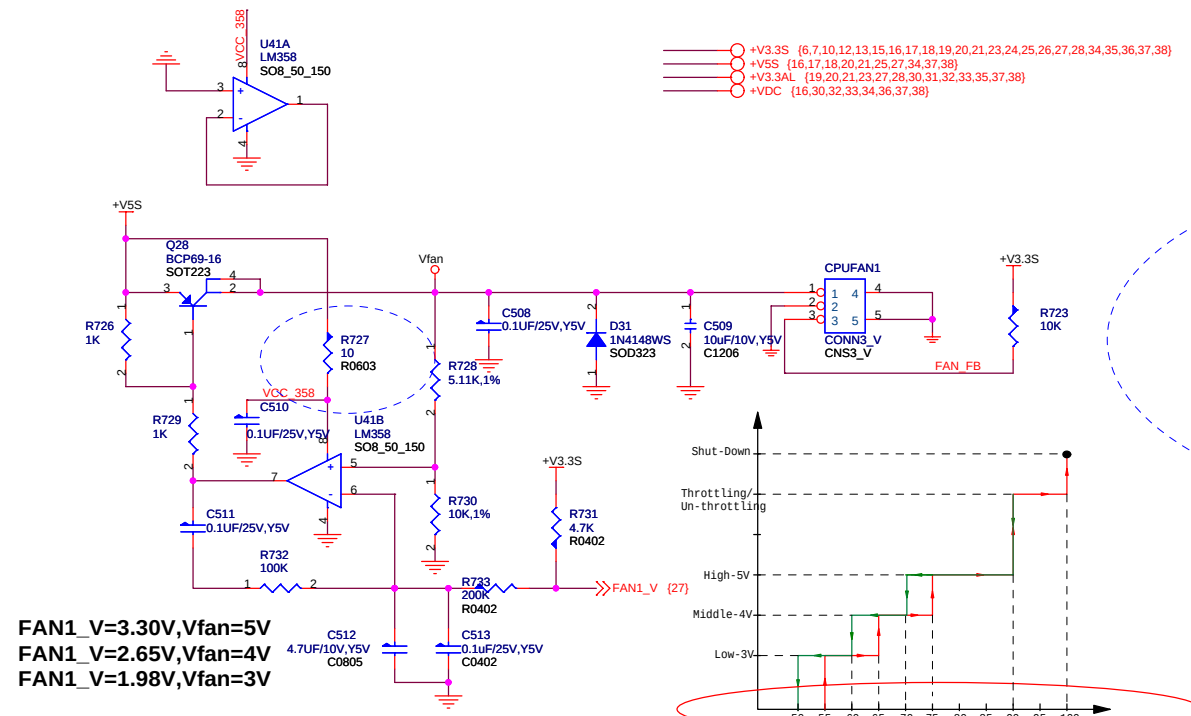
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—○+V3.3S {6,7,10,12,13,15,16,17,18,19,20,21,23,24,25,26,27,29,34,35,36,37,38}

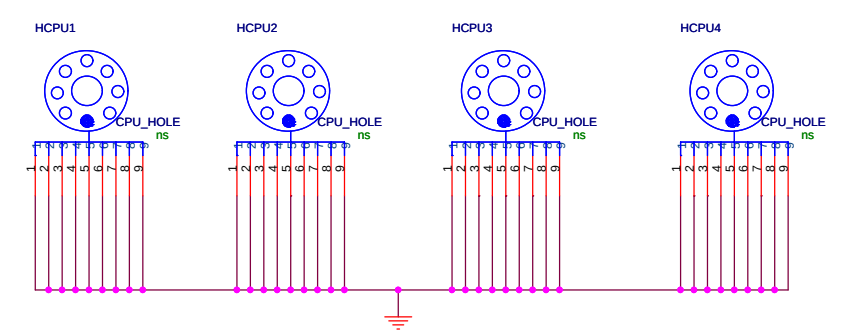
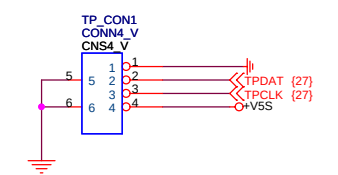
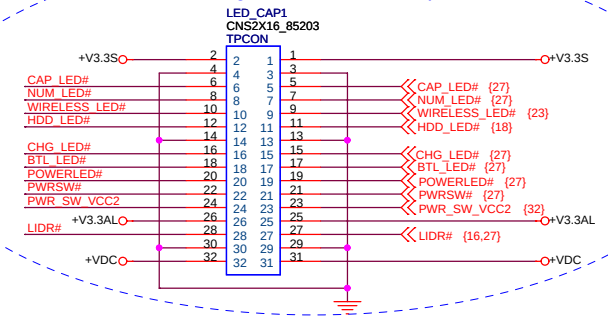
	RTL8101E
AVDD33	3.3V
AVDD18	1.8V
EVDD18	1.8V
DVDD15	1.5V



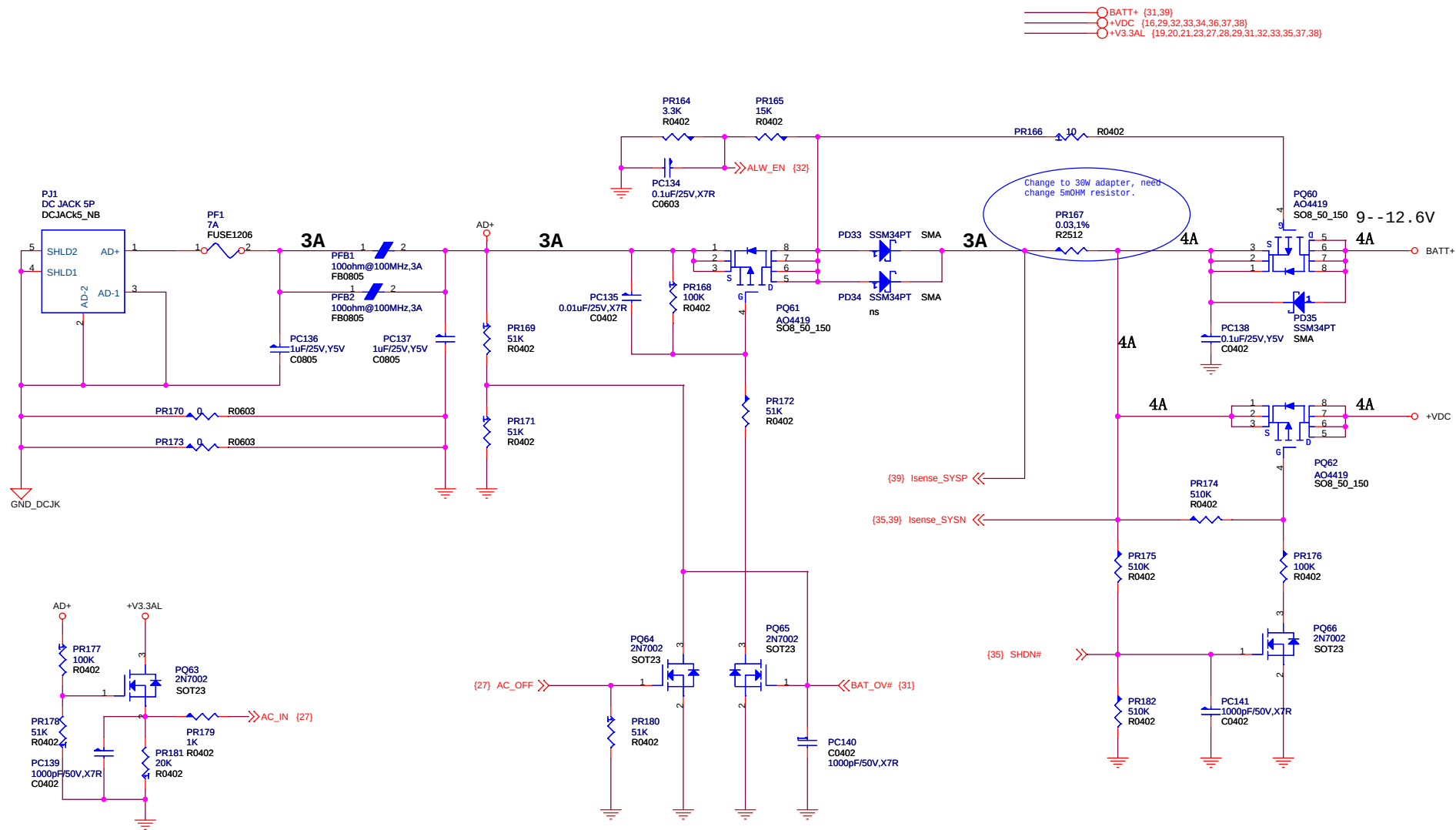


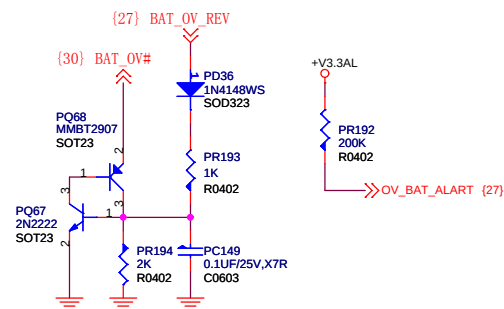
FAN1_V=3.30V,Vfan=5V
FAN1_V=2.65V,Vfan=4V
FAN1_V=1.98V,Vfan=3V

VerC: Change connect footprint.

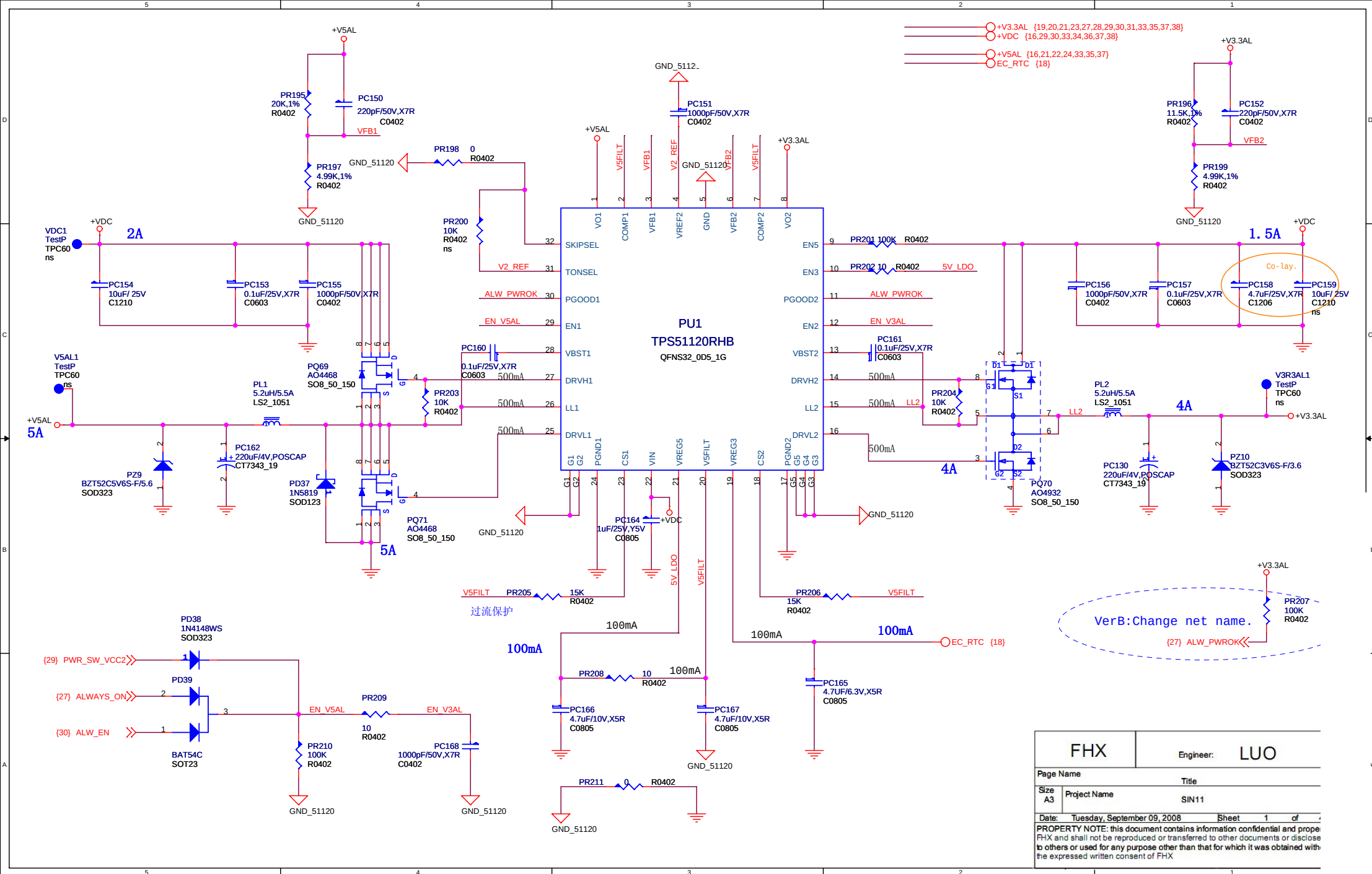


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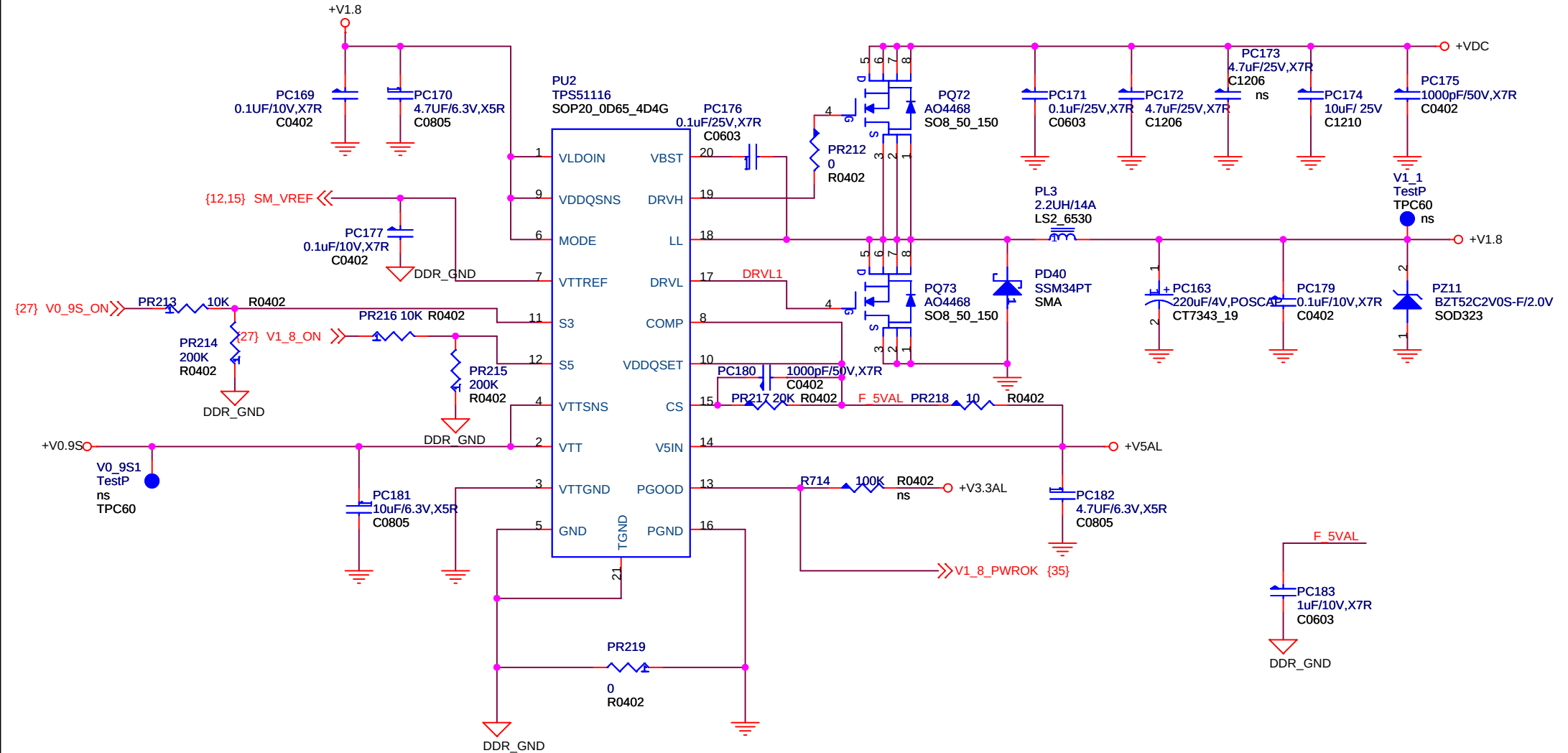




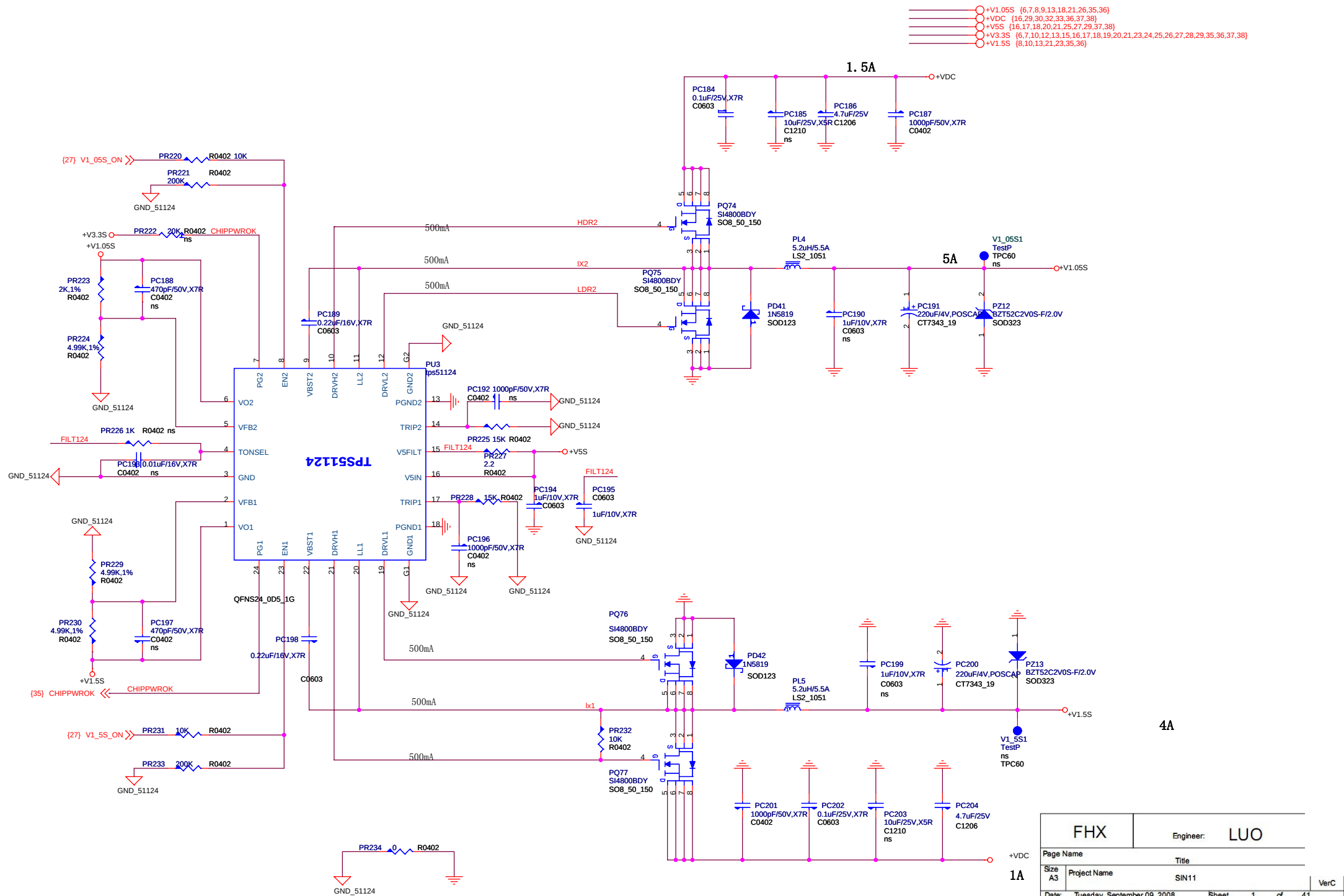
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- +V5AL {16,21,22,24,32,35,37}
- +V3.3AL {19,20,21,23,27,28,29,30,31,32,35,37,38}
- +VDC {16,29,30,32,34,36,37,38}
- +V1.8 {12,13,15,35,36}
- +V0.9S {15,36}

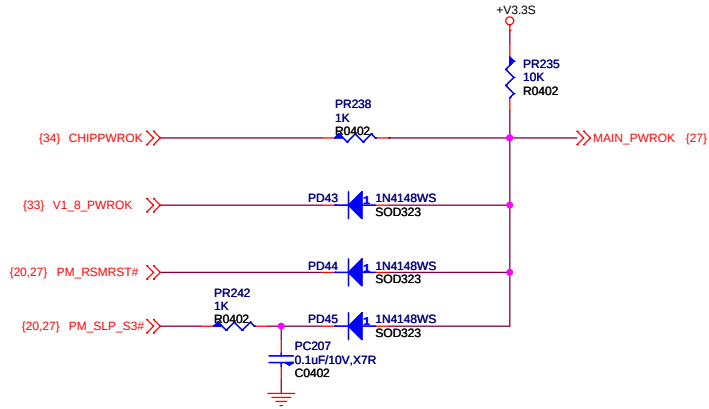


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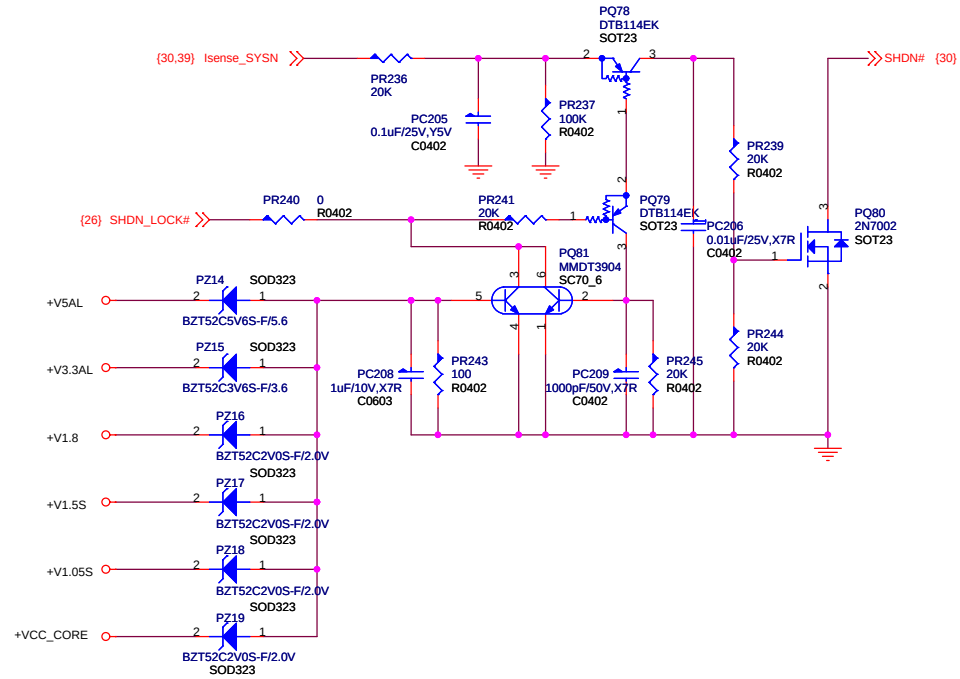


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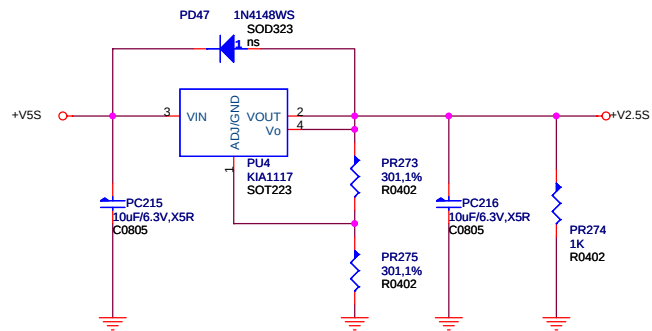
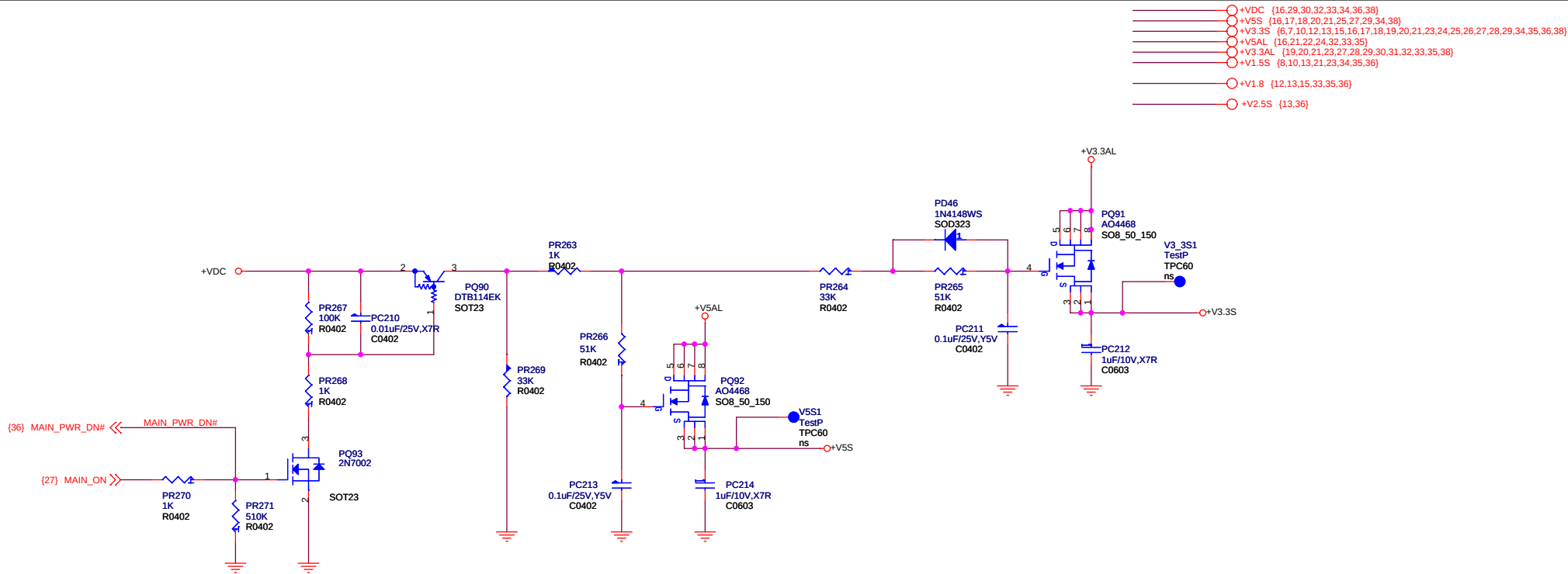
Power Good Logic CIRCUIT



OVP CIRCUIT

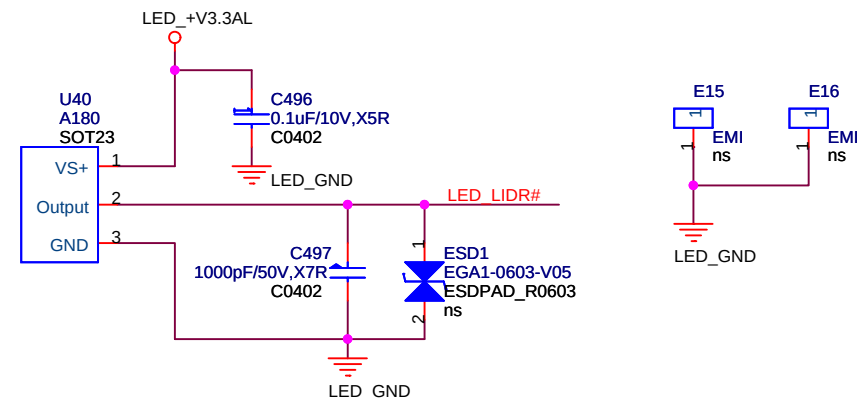
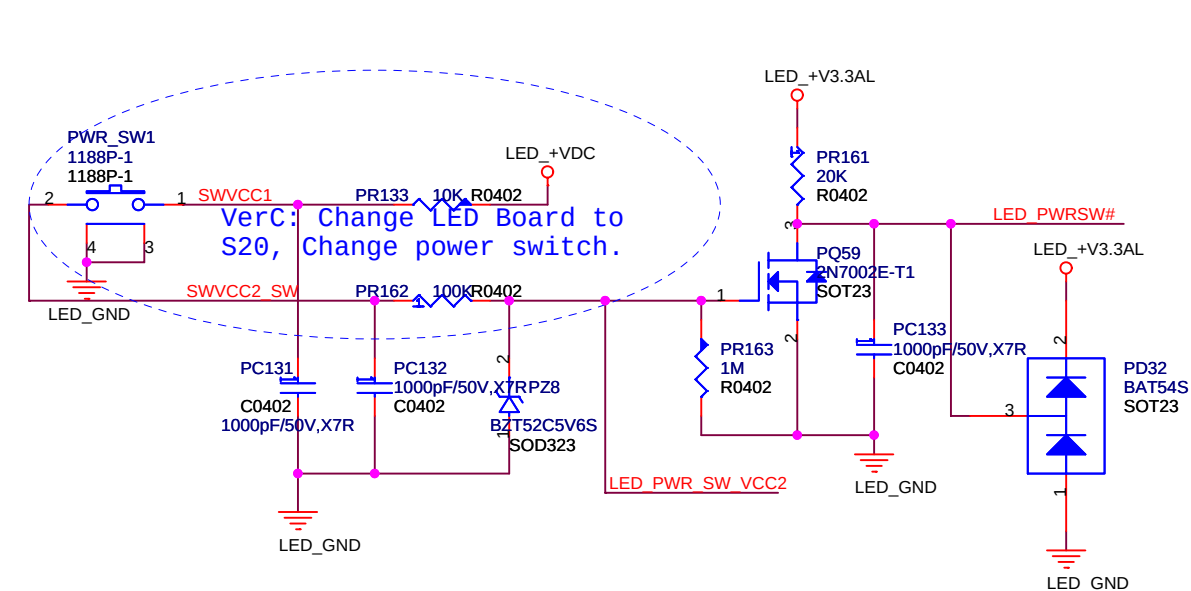
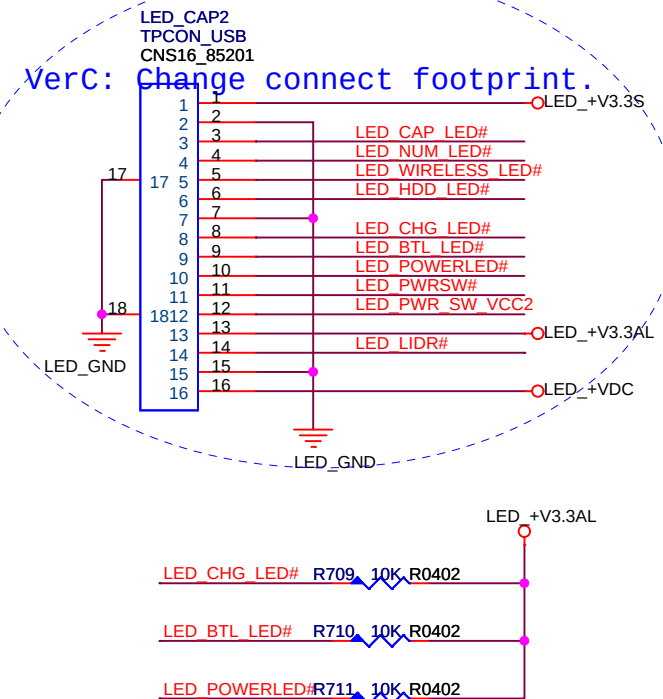
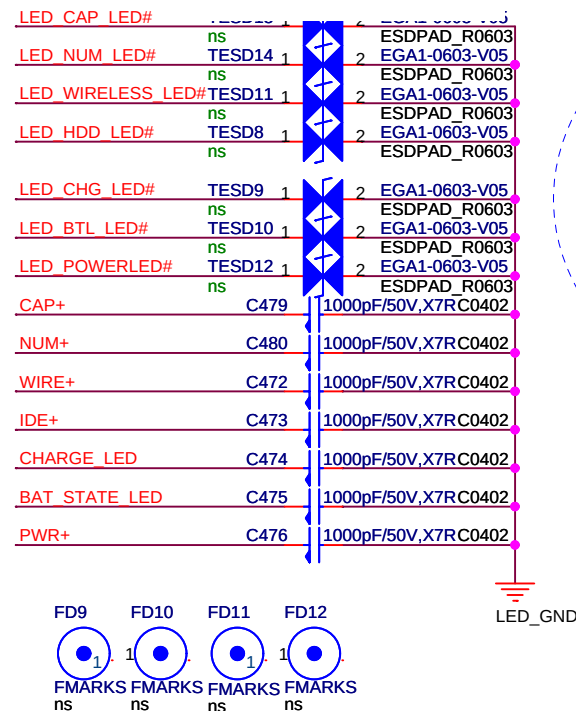
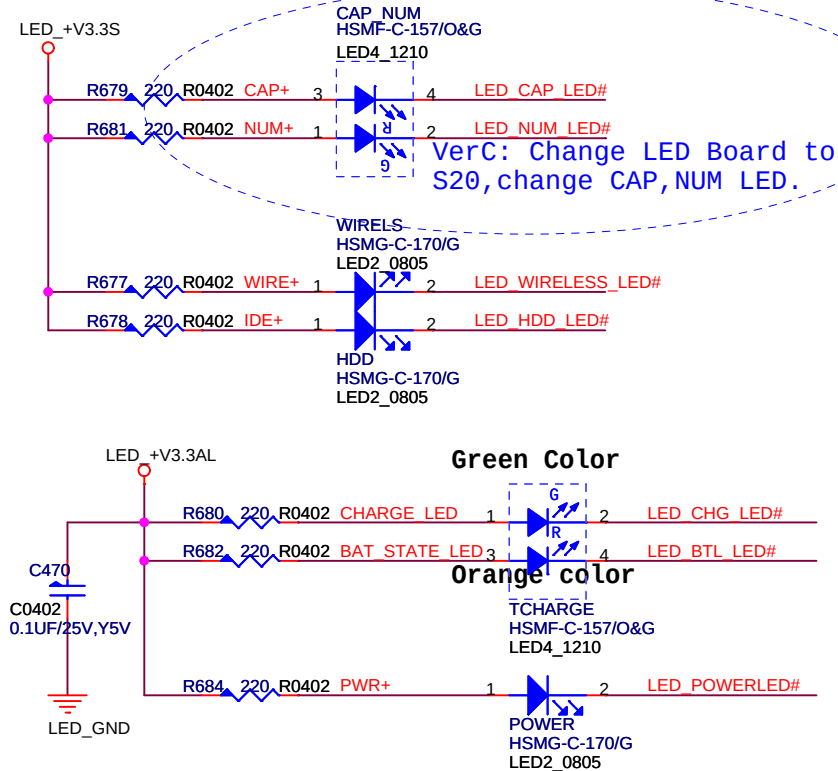


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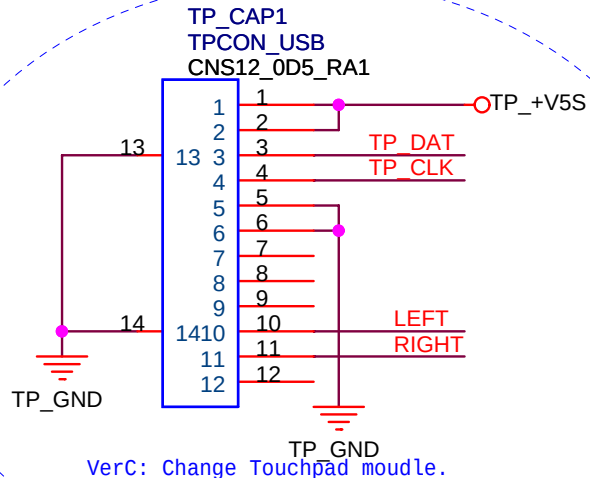
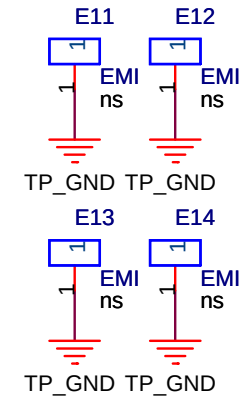
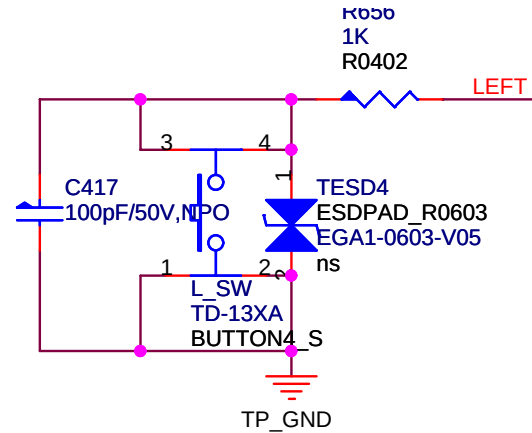
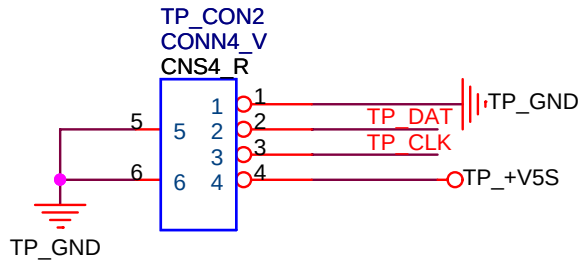


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LED

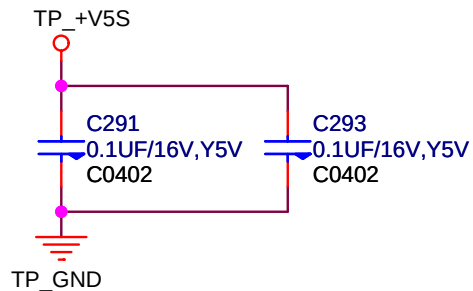
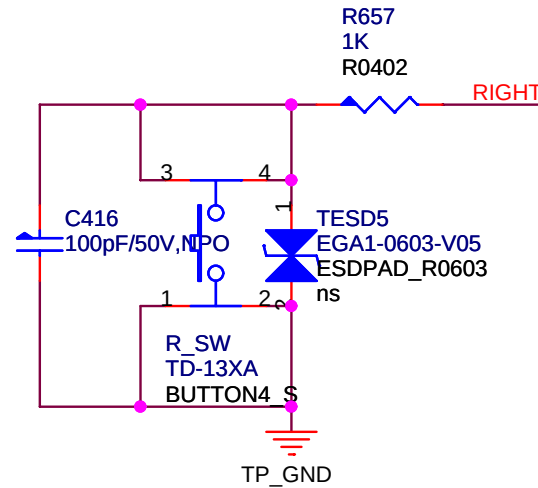


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VerC: Change Touchpad module.

Touchpad



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