1、HL9999 Radio Architecture

This section discusses the radio architecture for Class 2 designs. The first section covers the RF circuitry within the chip. Subsequent sections provide an overview of the external circuit design and Persistent Store (PS) Key configuration requirements.

1. 1 HL9999 Transceiver

1.1.1 Transmitter Architecture

The transmitter features a direct IQ modulator to minimize the frequency drift during a transmit timeslot, which results in a controlled modulation index. An additional frequency offset of up to ±1MHz can be added to the digital baseband signal. Digital baseband transmit circuitry provides the required spectral shaping.

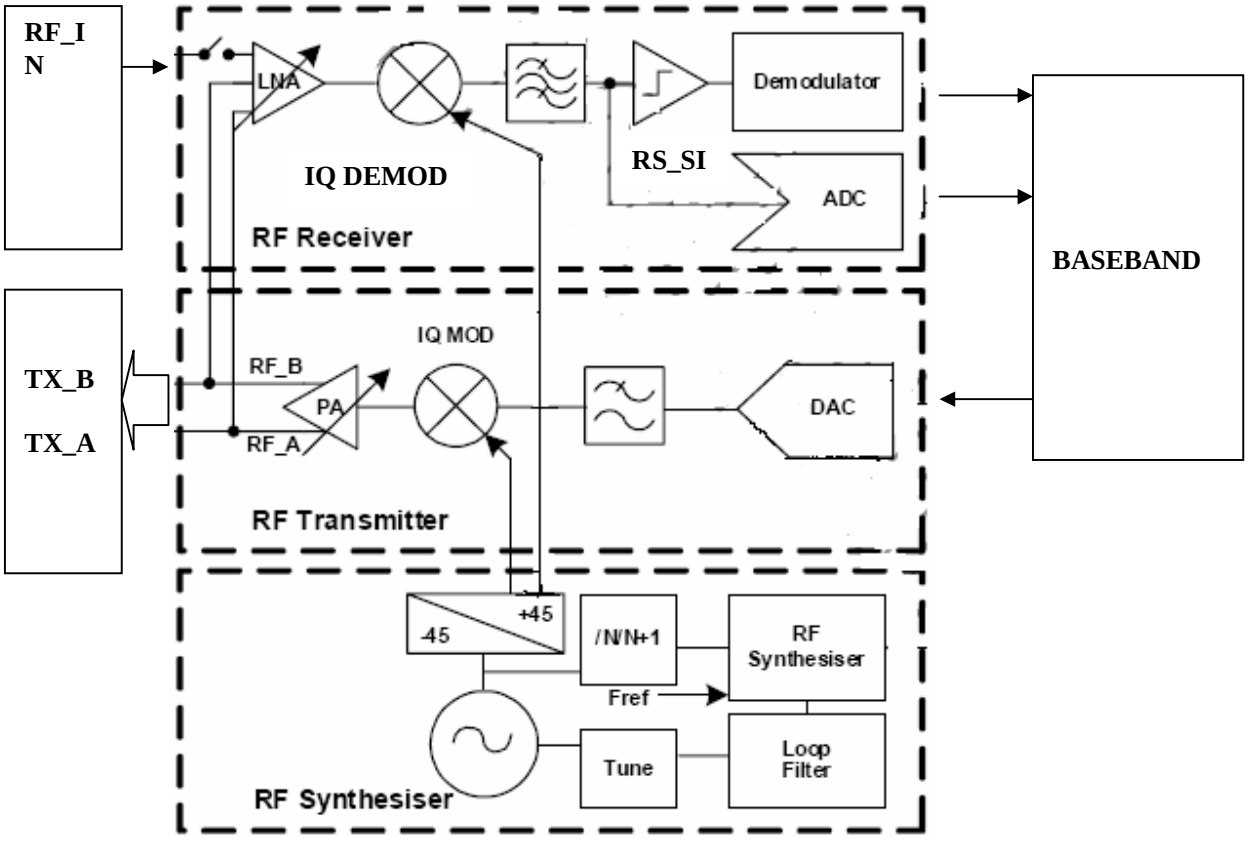
The internal power amplifier (PA) has a maximum output power of +6dBm allowing BlueCore3-Multimedia External to be used in Class 2 and Class 3 radios without an external RF PA. (Support for transmit power control allow a simple implementation for Class 1 with an external RF PA.)

1.1.2 Receiver Architecture

There is a receiver of a double conversion design, which uses the same synthesiser as the transmitter. But the TX_A and TX_ B ports utilized by the transmitter . Single-ended inputs use the RF_IN port.

The receiver features a near-zero intermediate frequency (IF) architecture that allows the channel filters to be integrated on to the die. Both differential and single-ended inputs are amplified by a low noise amplifier (LNA).

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RS SI) voltage on a slot-by-slot basis . The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input-signal within a limited range .This improves the dynamic range of the receiver, improving performance in interference limited environments.


RF_I
N
LNA
IQ DEMOD
RF Receiver
Demodulator
RS_SI
ADC
BASEBAND
TX_B
TX_A
IQ MOD
RF_B
PA
RF_A
DAC
RF Transmitter
-45
+45
/N/N+1
RF
Synthesiser
Fref
Tune
Loop
Filter
RF Synthesiser