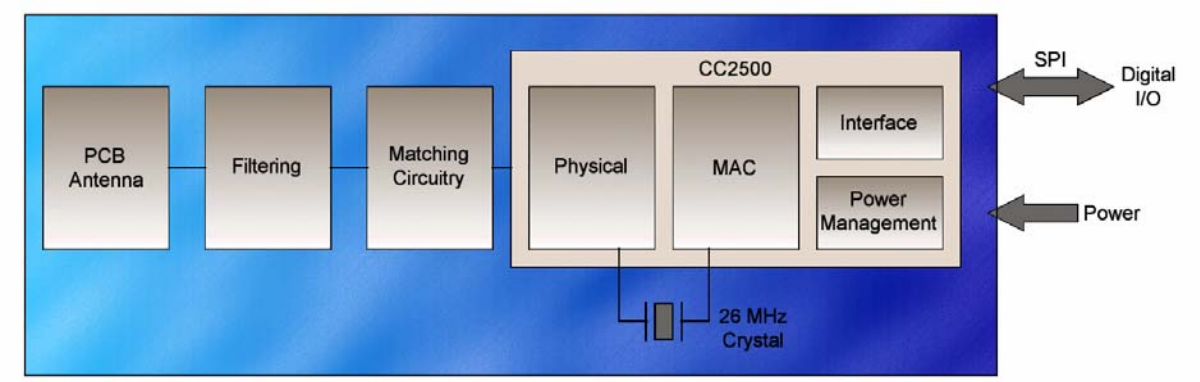

Figure 1 The functionality of the A2500R24A, using an integral antenna

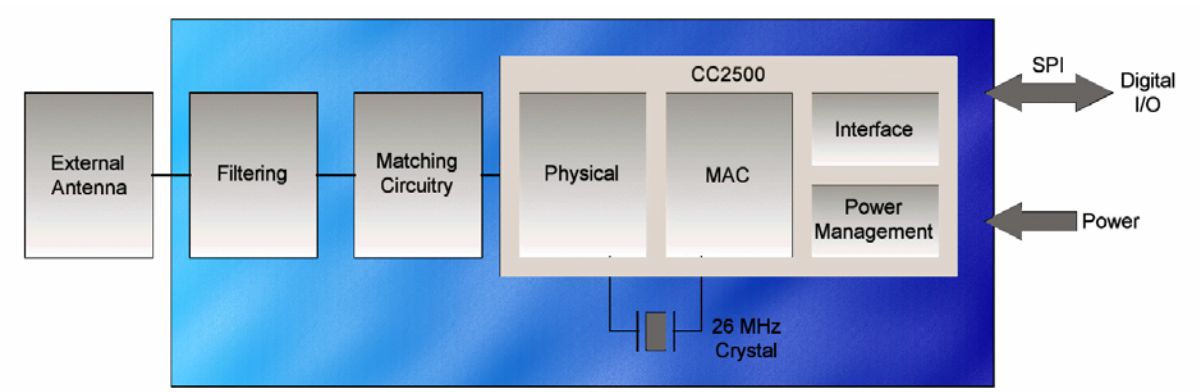

Figure 2 The functionality of the A2500R24C, using an external antenna.

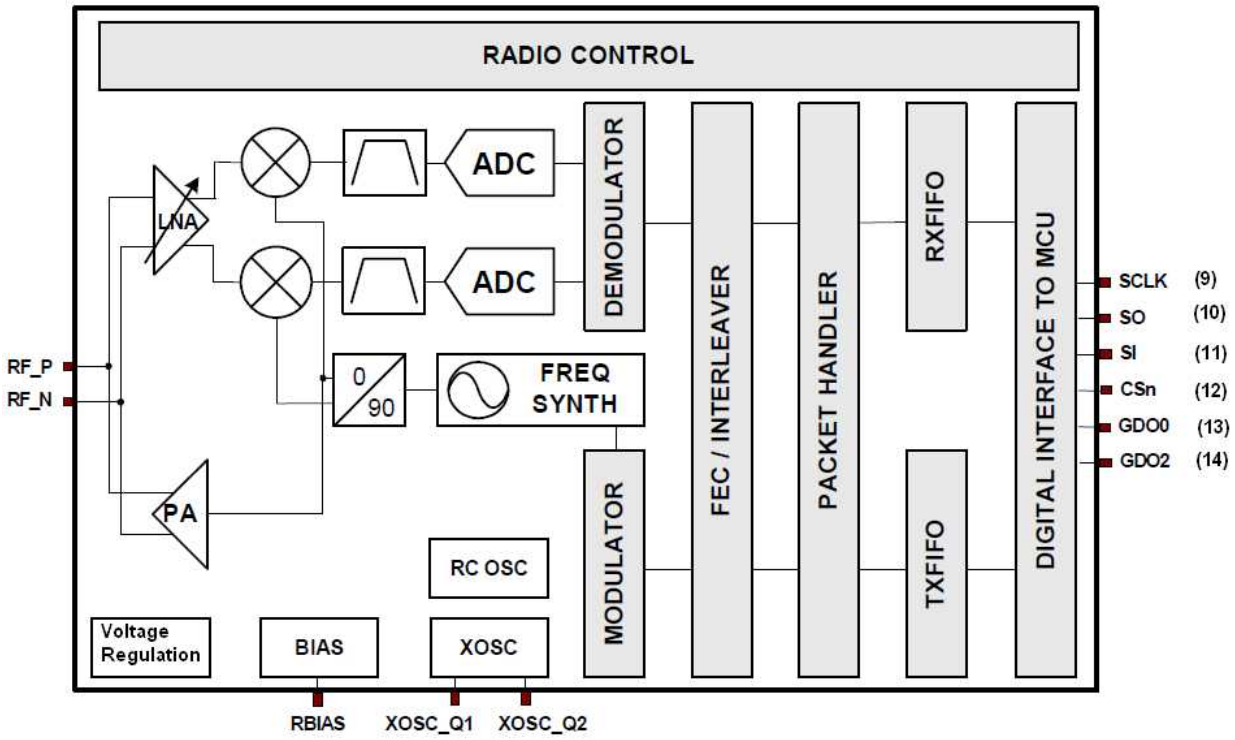

Figure 3 Transceiver IC block diagram.

1.4.1. Typical Flow

After initial setup of registers for desired behavior, the normal operation flow diagram is shown in Figure 4. In applications of infrequent data transmissions the transceiver would be in "sleep" mode to save power (400nA). From there it would be woken up and enter "idle" mode. As part of the wake up process the crystal oscillator is started (~250µs) and the digital microcontroller interface is powered up. Before transmit or receive the frequency synthesizer needs to be started ("FS_Wakeup") and having been powered off (or idle for a while) the control loop of the VCO/PLL needs to be calibrated ("calibrate").

A data frame is loaded into the transmit FIFO and the "TX" mode is entered. The transceiver will transmit the data and enter "idle" mode after completion. When transmit is complete "RX" mode is entered to wait for the acknowledge frame. Once a frame is received the transceiver will again enter "idle"mode. If no acknowledge frame is received within a given timeout the data frame would be re-transmitted. If the acknowledge frame indicated that the data was received the next data frame would be transmitted. After the last data frame have successfully been transmitted the transceiver would again be put in "sleep" mode.

Medium access

Figure 4 Transceiver state diagram

1.5. Applications

Ultra low-power wireless applications, operating in the 2400-2483.5 MHz ISM/SRD bands.

- Wireless alarm and security systems
- Industrial monitoring and control
- Wireless sensor networks